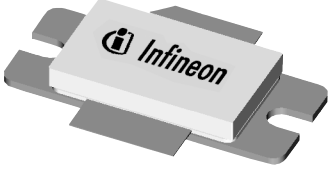
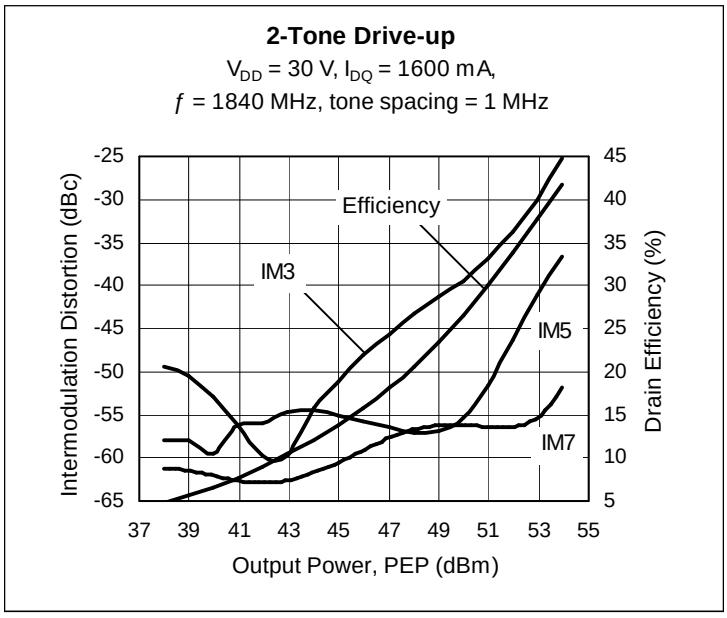
Thermally-Enhanced High Power RF LDMOS FET
200 W, 1805 – 1880 MHz

Description

The PTFA182001E is a 200-watt LDMOS FET intended for EDGE applications from 1805 to 1880 MHz. Features include input and output matching, and thermally-enhanced single-ended package with a slotted flange. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PTFA182001E
Package H-30260-2





Features

- Pb-free, RoHS-compliant and thermally-enhanced package
- Broadband internal matching
- Typical EDGE performance at 1836.6 MHz, 30 V
  - Average output power = 50 dBm
  - Linear gain = 16.3 dB
  - Efficiency = 37%
  - EVM = 3.1%
  - 400 kHz modulation = –61 dBc
  - 600 kHz modulation = –76 dBc
- Typical CW performance, 1880 MHz, 30 V
  - Output power at P–1dB = 220 W
  - Efficiency = 49%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 5:1 VSWR @ 30 V, 200 W (CW) output power

RF Characteristics

Two-tone Measurements (tested in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 200 W PEP, f = 1840 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.7	16.6	—	dB
Drain Efficiency	η_D	37	38	—	%
Intermodulation Distortion	IMD	—	–31.5	–30	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
Drain Leakage Current	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.05	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 1.8 A	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	625	W
Above 25°C derate by		3.57	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 200 W CW)	$R_{\theta JC}$	0.28	°C/W

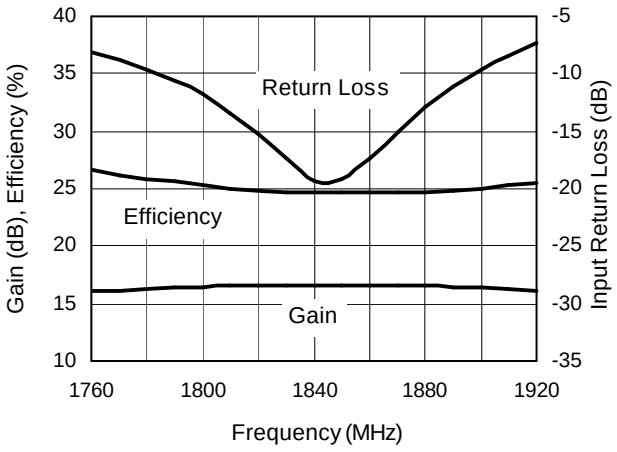
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA182001E V1	H-30260-2	Thermally-enhanced slotted flange, single-ended	PTFA182001E

Typical Performance (data taken in a production test fixture)

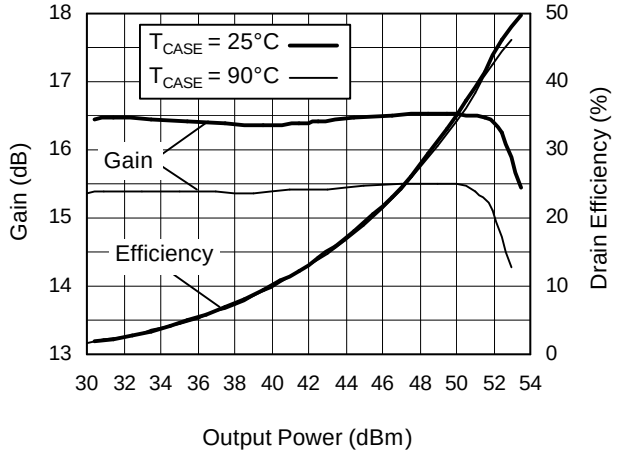
Broadband Performance

V_{DD} = 30 V, I_{DQ} = 1600 mA, P_{OUT} = 50 W



Power Sweep, CW Conditions

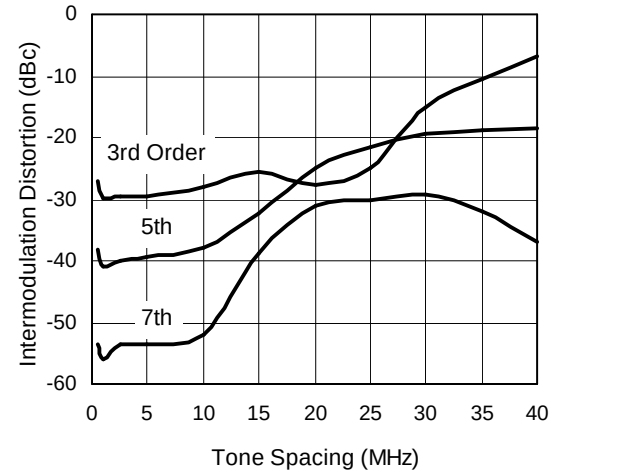
V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1880 MHz



Intermodulation Distortion Products vs. Tone Spacing

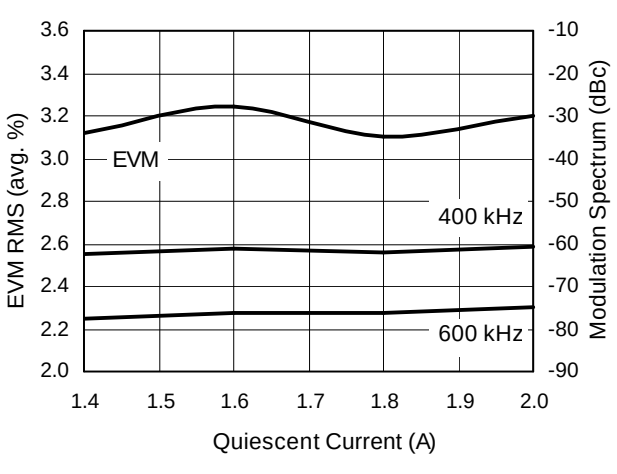
V_{DD} = 30 V I_{DQ} = 1600 mA , f = 1840 MHz,

P_{OUT} = 53 dBm PEP



Edge EVM and Modulation Spectrum vs. Quiescent Current

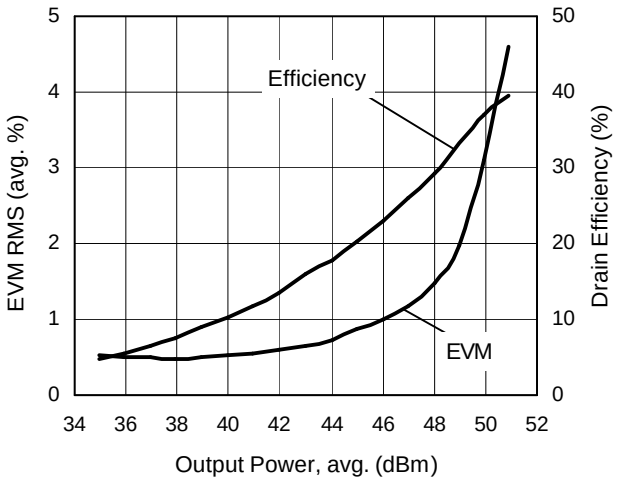
V_{DD} = 30 V, f = 1836.6 MHz, P_{OUT} = 50 dBm



Typical Performance (cont.)

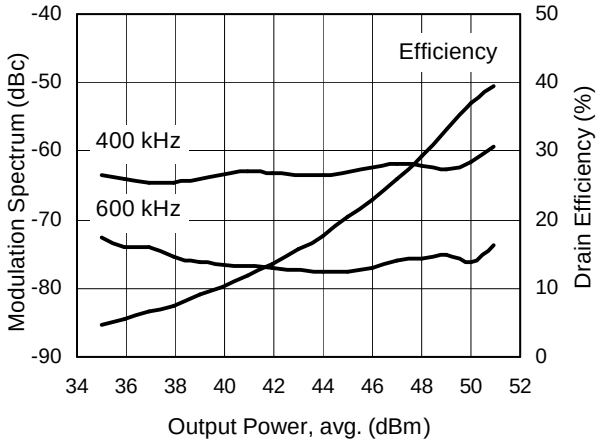
EDGE EVM Performance

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1836.6 MHz



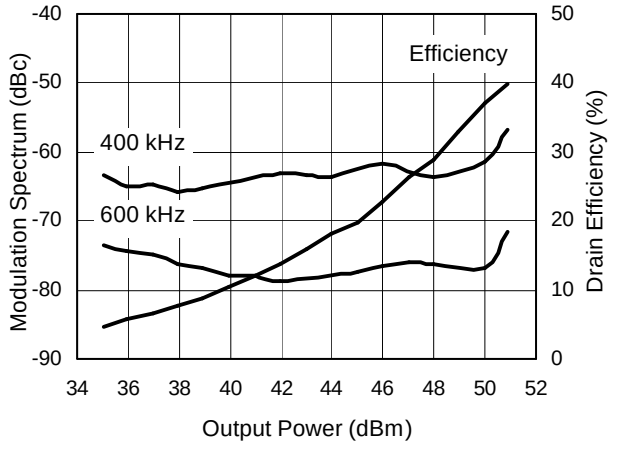
EDGE Modulation Spectrum Performance

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1836.6 MHz



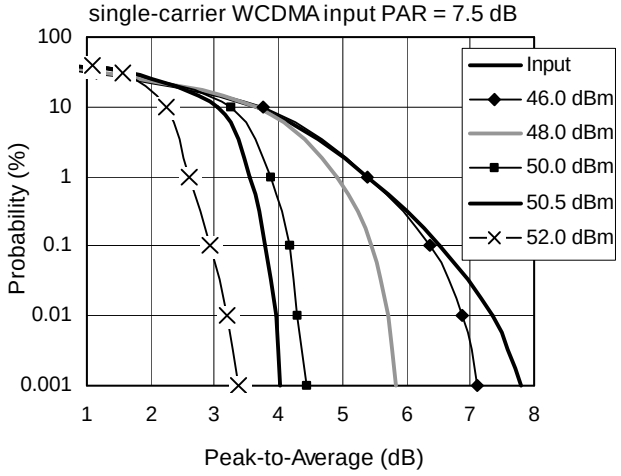
EDGE Modulation Spectrum Performance

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1879.8 MHz



Output Peak-to-Average Ratio Compression (PARC) at various Power levels

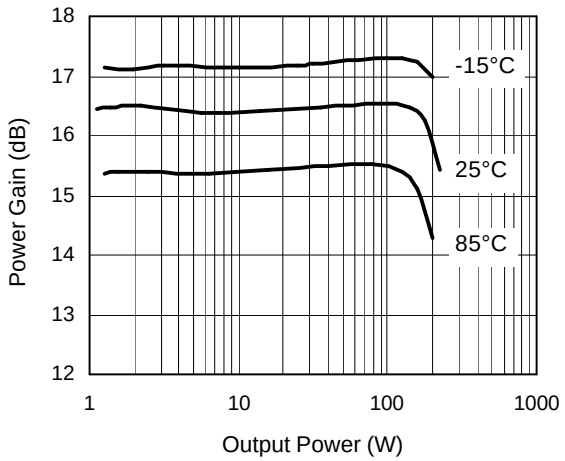
V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1880 MHz,
single-carrier WCDMA input PAR = 7.5 dB



Typical Performance (cont.)

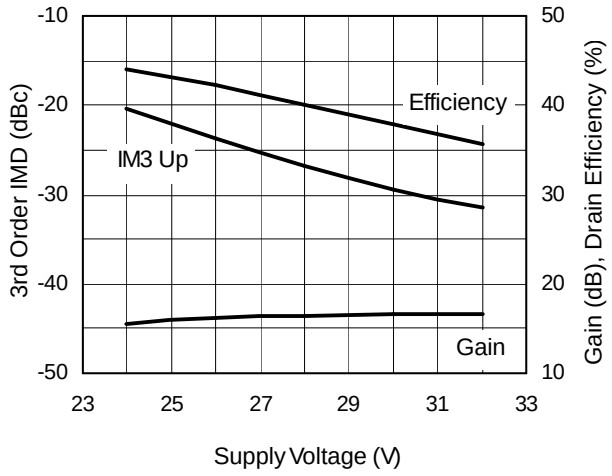
Power Sweep (CW) over Temperature

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1880 MHz



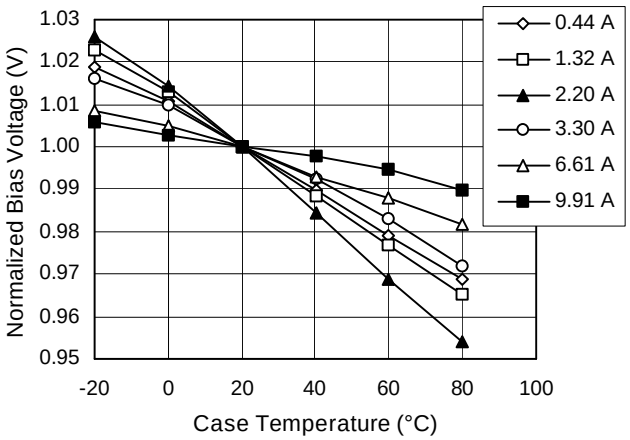
Voltage Sweep

I_{DQ} = 1600 mA, f = 1840 MHz, tone spacing = 1 MHz,
Output Power (PEP) = 53 dBm

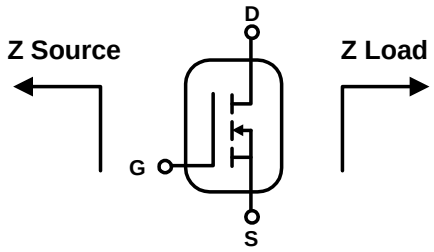


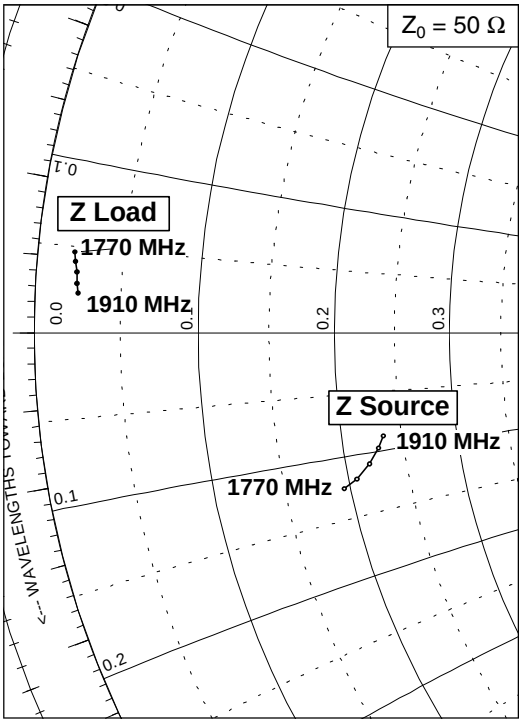
Bias Voltage vs. Temperature

Voltage normalized to typical gate voltage,
series show current



Broadband Circuit Impedance

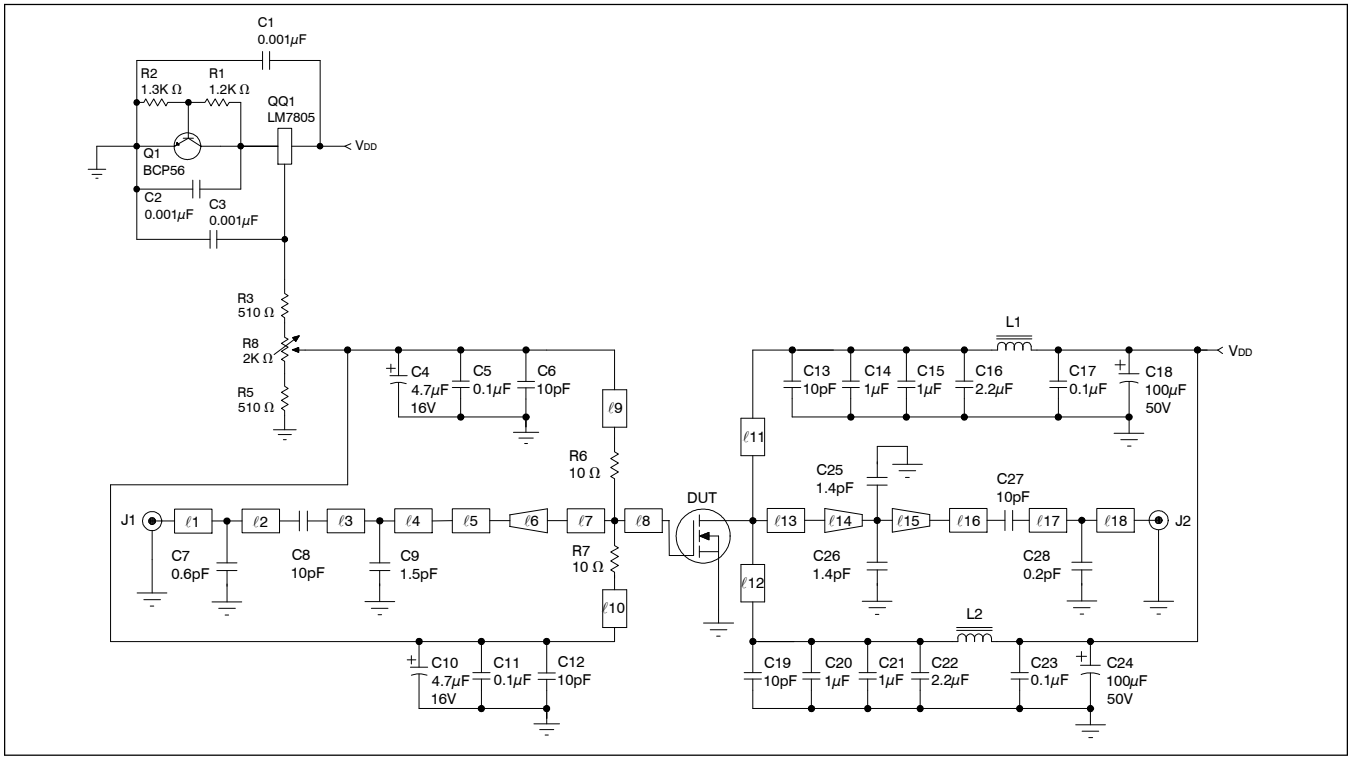




Frequency	Z Source W		Z Load W	
MHz	R	jX	R	jX
1770	11.72	–4.39	1.22	1.17
1800	11.45	–4.87	1.17	1.44
1840	10.97	–5.48	1.15	1.78
1880	10.33	–5.99	1.08	2.08
1910	9.76	–6.27	1.04	2.35

See next page for circuit information

Reference Circuit (cont.)

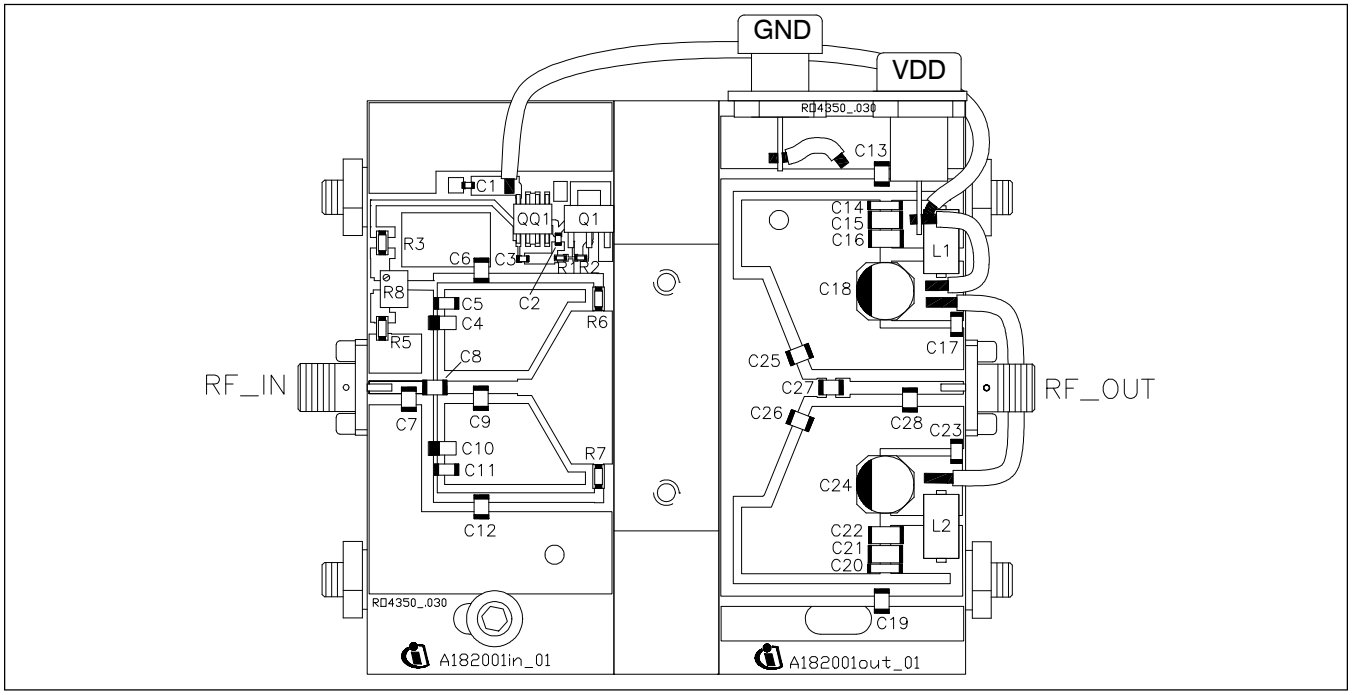


Reference circuit schematic for ƒ = 1840 MHz

Circuit Assembly Information			
DUT	PTFA182001E	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 3.48	Rogers RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 1840 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.056 λ, 50.2 Ω	5.54 x 1.68	0.218 x 0.066
ℓ2	0.024 λ, 50.2 Ω	2.39 x 1.68	0.094 x 0.066
ℓ3	0.051 λ, 50.2 Ω	5.00 x 1.68	0.197 x 0.066
ℓ4	0.050 λ, 50.2 Ω	4.93 x 1.68	0.194 x 0.066
ℓ5	0.019 λ, 42.8 Ω	1.88 x 2.16	0.074 x 0.085
ℓ6 (taper)	0.054 λ, 42.8 Ω./ 6.9 Ω	5.23 x 2.16 / 20.32	0.206 x 0.085 / 0.800
ℓ7	0.040 λ, 6.9 Ω	3.63 x 20.32	0.143 x 0.800
ℓ8	0.021 λ, 6.9 Ω	1.85 x 20.32	0.073 x 0.800
ℓ9, ℓ10	0.186 λ, 59.1 Ω	18.59 x 1.27	0.732 x 0.050
ℓ11, ℓ12	0.328 λ, 50.7 Ω	32.39 x 1.65	1.275 x 0.065
ℓ13	0.062 λ, 5.0 Ω	5.51 x 28.83	0.217 x 1.135
ℓ14 (taper)	0.043 λ, 5.0 Ω./ 15.1 Ω	3.84 x 28.83 / 8.43	0.151 x 1.135 / 0.332
ℓ15 (taper)	0.021 λ, 15.1 Ω./ 41.2 Ω	1.96 x 8.43 / 2.29	0.077 x 0.332 / 0.090
ℓ16	0.026 λ, 41.2 Ω	2.49 x 2.29	0.098 x 0.090
ℓ17	0.095 λ, 50.2 Ω	9.42 x 1.68	0.371 x 0.066
ℓ18	0.072 λ, 50.2 Ω	7.11 x 1.68	0.280 x 0.066

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4, C10	Capacitor, 4.7 µF, 16 V	Digi-Key	PCS3475CT-ND
C5, C11, C17, C23	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C12	Capacitor, 10 pF AVX	Garrett Electronics	08051J100GBTTR
C7	Ceramic capacitor, 0.6 pF	ATC	100B 0R6
C8, C13, C19, C27	Ceramic capacitor, 10 pF	ATC	100B 100
C9	Ceramic capacitor, 1.5 pF	ATC	100B 1R5
C14, C15, C20, C21	Ceramic capacitor, 1 µF	Digi-Key	445-1411-2-ND
C16, C22	Capacitor, 2.2 µF	Digi-Key	445-1447-2-ND
C18, C24	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	PCE3718CT-ND
C25, C26	Ceramic capacitor, 1.4 pF	ATC	100B 1R4
C28	Ceramic capacitor, 0.2 pF	ATC	100A 0R2
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infinion Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2k ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3k ohms	Digi-Key	P1.3KGCT-ND
R3, R5	Chip resistor 510 ohms	Digi-Key	P510ECT-ND
R4	Not used		
R6, R7	Chip resistor 10 ohms	Digi-Key	P10ECT-ND
R8	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND

**Gerber Files for this circuit available on request*

Package Outline Specifications

Package H-30260-2

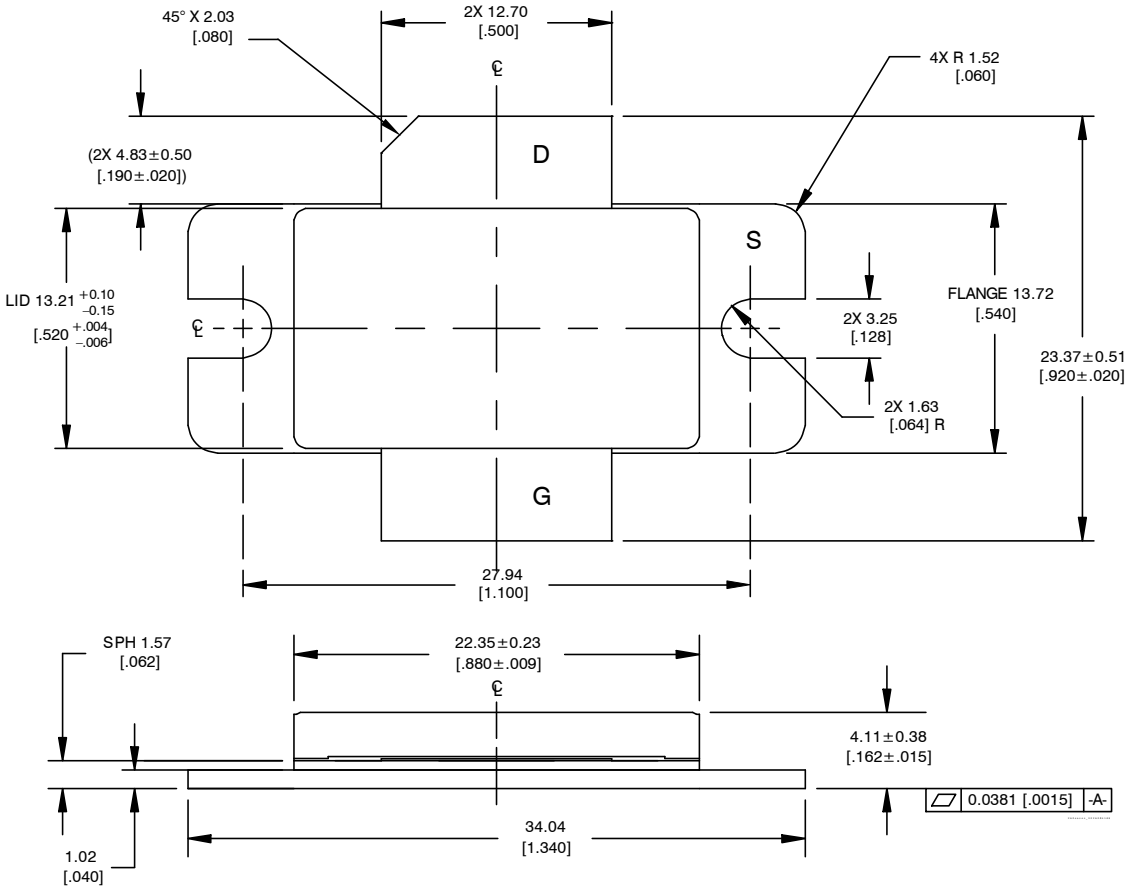


Diagram Notes—unless otherwise specified:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron [100 microinch] (min)
   D, G - leads: 1.14 ± 0.38 micron [45 ± 15 microinch]

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Revision History:	2008-03-12	Data Sheet
Previous Version:	none	

Page	Subjects (major changes since last revision)

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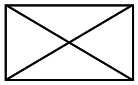

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