# DESCRIPTION

The PT5618 is a high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels for 3-phase gate driver. Built-in dead time protection and Shoot-through protection that prevent half-bridge against damage.

The UVLO circuits prevent malfunction when VCC and VBS are lower than the specified threshold voltage. Novel high-voltage BCD process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances and excellent negative transient voltage tolerance. PIN EN designed for standby mode can be used to enable chip into low quiescent current state and get long battery life time.

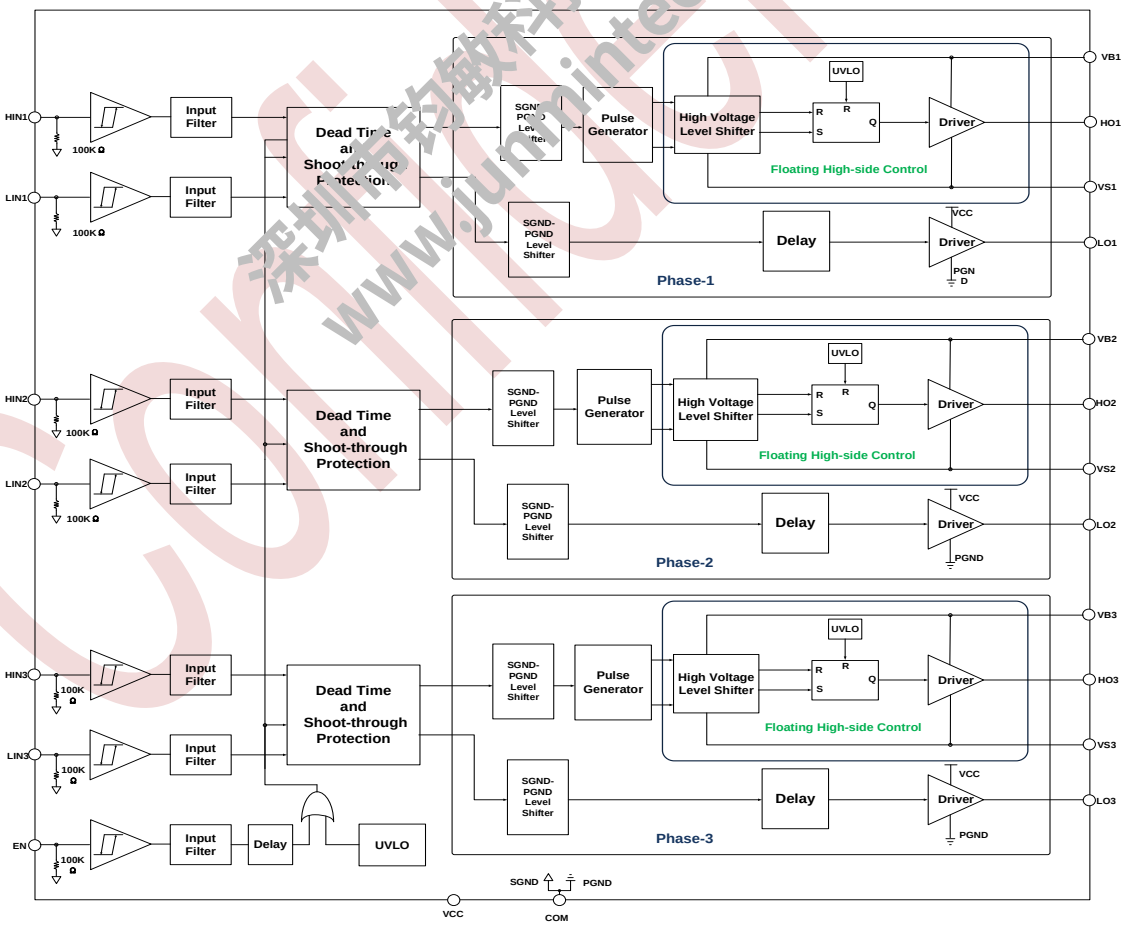
# FEATURES

- Integrated 200V half-bridge high side driver
- Driver up to 3-phase half-bridge gates
- Built-in dead time control
- Shoot-through protection
- Under voltage lockout for VCC and VBS
- 3.3V, 5V,15V input logic Compatible
- Built-in input filter
- Low standby current
- IO+/IO-: 320mA/620mA
- Built-in dead time：0.55us(typ.)
- Common-Mode dv/dt Noise Canceling Circuit
- Tolerant to negative transient voltage
- Low di/dt gate drive for better noised immunity
- -40°C - 125°C operating range
- Small footprint package：TSSOP 20P/24P,173mil

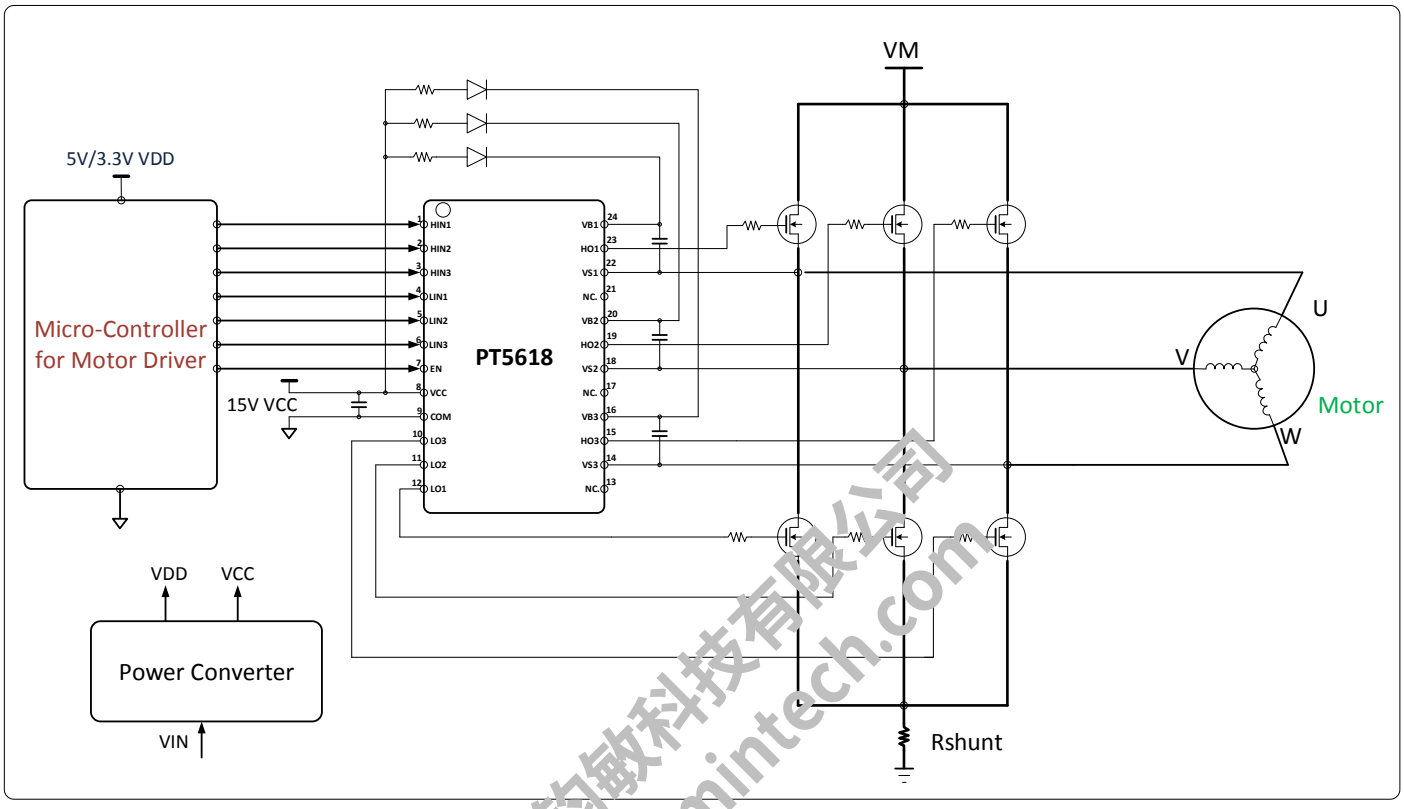
# APPLICATIONS

- 3-phase Motor Driver for E-BIKE, electric power tool
- Mini/micro motor control powered by battery
- Home appliance fed by 110V-AC grid
- General purpose inverter

# BLOCK DIAGRAM



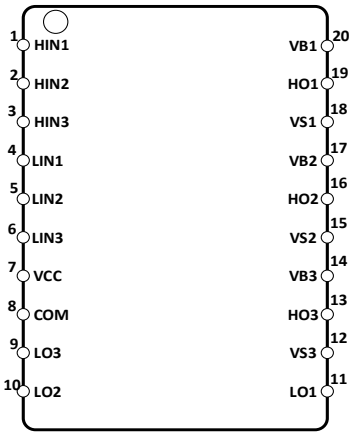
# APPLICATION CIRCUIT



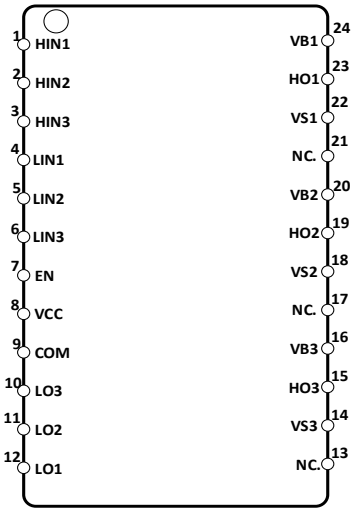



# PIN CONFIGURATION

## TSSOP20




## TSSOP24



# PIN DESCRIPTION

| Pin Name | Description | Pin No. | |
|---|---|---|---|
| | | TSSOP20 | TSSOP24 |
| HIN1 | Logic input for phase-1 high-side gate driver | 1 | 1 |
| HIN2 | Logic input for phase-2 high-side gate driver | 2 | 2 |
| HIN3 | Logic input for phase-3 high-side gate driver | 3 | 3 |
| LIN1 | Logic input for phase-1 low-side gate driver | 4 | 4 |
| LIN2 | Logic input for phase-2 low-side gate driver | 5 | 5 |
| LIN3 | Logic input for phase-3 low-side gate driver | 6 | 6 |
| EN | Logic input for standby mode control | - | 7 |
| VCC | Logic and low-side gate drivers power supply voltage | 7 | 8 |
| COM | Logic ground and low-side gate drivers ground | 8 | 9 |
| LO3 | Phase-3 Low-side gate driver output | 9 | 10 |
| LO2 | Phase-2 Low-side gate driver output | 10 | 11 |
| LO1 | Phase-1 Low-side gate driver output | 11 | 12 |
| NC. | Not Connected | - | 13 |
| VS3 | Phase-3 High-side driver floating supply offset voltage | 12 | 14 |
| HO3 | Phase-3 High-side driver output | 13 | 15 |
| VB3 | Phase-3 High-side driver floating supply | 14 | 16 |
| NC. | Not Connected | - | 17 |
| VS2 | Phase-2 High-side driver floating supply offset voltage | 15 | 18 |
| HO2 | Phase-2 High-side driver output | 16 | 19 |
| VB2 | Phase-2 High-side driver floating supply | 17 | 20 |
| NC. | Not Connected | - | 21 |
| VS1 | Phase-1 High-side driver floating supply offset voltage | 18 | 22 |
| HO1 | Phase-1High-side driver output | 19 | 23 |
| VB1 | Phase-1High-side driver floating supply | 20 | 24 |



# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT5618 | 20 Pins, TSSOP, 173mil | PT5618 |
| PT5618-T1 | 24 Pins, TSSOP, 173mil | PT5618-T1 |

# FUNCTION DESCRIPTION

## LOW SIDE POWER SUPPLY: VCC

VCC is the low side supply and it provides power to both input logic and low side output power stage. The built-in under-voltage lockout circuit enables the device to operate at sufficient power when a typical VCC supply voltage higher than $V_{CCUV+}$ =8.5V is present, shown as FIG1. The IC shuts down all the gate drivers outputs, when the VCC supply voltage is below $V_{CCUV-}$ =8.0 V, shown as FIG1. This prevents the external power devices against extremely low gate voltage levels during on-state and therefore against excessive power dissipation.

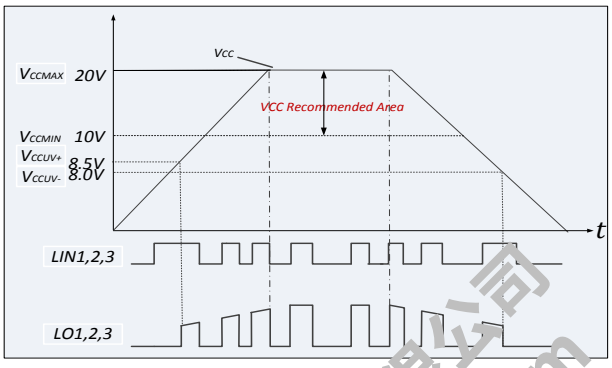



**Figure.1: VCC supply UVLO operating area**

## HIGH SIDE POWER SUPPLY: VBS (VB1-VS1, VB2-VS2, VB3-VS3)

VBS is the high side supply voltage. The totally high side circuitry can float with respect to COM following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to VCC, and it can be powered with small bootstrap capacitors.

The device operating area as a function of bias supply voltage is given in Figure2.

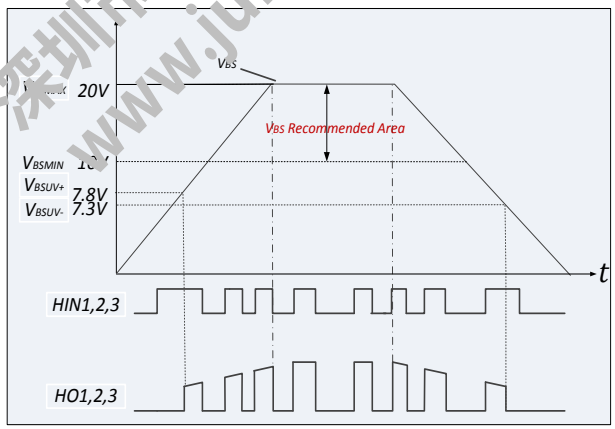



**Figure.2: VBS supply UVLO operating area**

## LOW SIDE AND HIGH CONTROL INPUT LOGIC: HIN&LIN (HIN1, 2, 3/LIN1, 2, 3)

The Schmitt trigger threshold of each input is designed enough low such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and advanced noise filter provide beneficial noise rejection to short input pulses. An internal pull-down resistor of about 100kΩ (positive logic) pre-biases each input during VCC supply start-up state. It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 500ns.

## SHOOT-THROUGH PREVENTION

The IC is equipped with shoot-through prevention circuitry (also known as cross conduction prevention circuitry). Figure 3 shows how this prevention circuitry prevents both the high- and low-side switches from conducting at the same time. During the inputs controlling high side driver and low side driver are both “high”, the both driver outputs are pulled down “low” to shutdown two power devices in the same bridge.

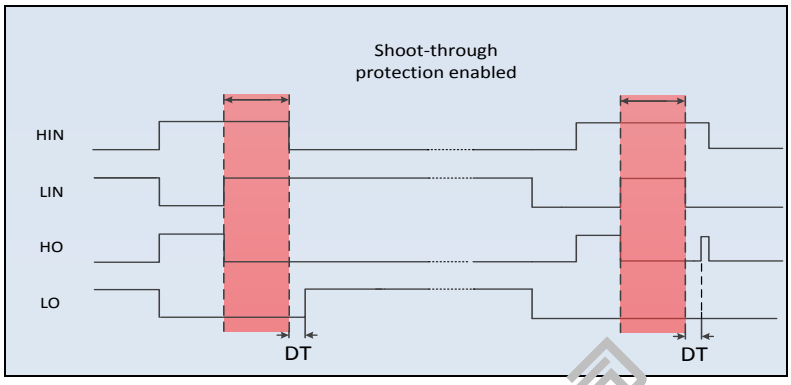



**Figure.3: Shoot-through prevention**

## DEAD TIME

The IC features integrated a fixed dead-time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver. Figure 4 illustrates the dead time period and the relationship between the output gate signals.

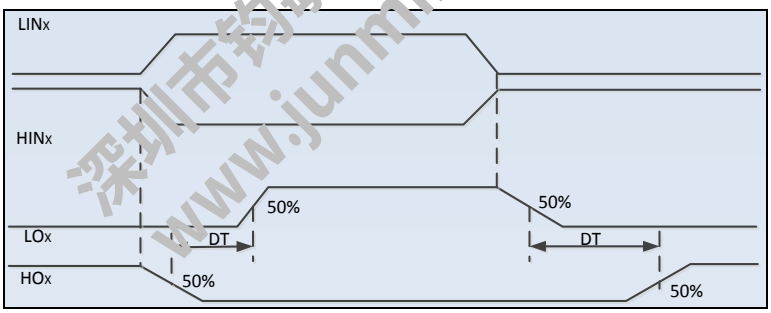



**Figure.4: Dead Time**

## GATE DRIVER (HO1, 2, 3/ LO1, 2, 3)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive the power devices such as IGBT and MOSFET. Low side outputs (i.e. LO1, 2, 3) are state triggered by the respective inputs, while high side outputs (i.e. HO1, 2, 3) are only changed at the edge of the respective inputs. In particular, after releasing from an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after releasing from a under voltage condition of the VCC supply, the low side outputs can directly switch to the state of their respective inputs and don’t suffer from the trouble as high side driver.

## STANDBY MODE

This device packed in TSSOP24 provides a featured pin, EN, to enable that it can work into low current dissipation state. EN can be compatible with 5V/3.3V logic level. If EN goes up to “high” level, this device is forced into standby mode, when all gate driver output is locked into “low” level and only 16uA (typ.)is dissipated. If EN goes from “high” level to “low” level, and waits a delay about 3us (typ.), this device can be released from standby mode, and all outputs are enabled. In order to lower the bias current, a 100kΩ, sufficiently large resistor is tied between EN and COM

# ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to IC COM unless otherwise stated in the table.

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| High-side floating supply voltage | $V_{B1,2,3}$ | -0.3 | 225 | V |
| High-side offset voltage | $V_{S1,2,3}$ | $V_{B1,2,3}$-25 | $V_{B1,2,3}$+0.3 | |
| High-side gate driver output voltage | $V_{HO1,2,3}$ | $V_{S1,2,3}$-0.3 | $V_{B1,2,3}$+0.3 | |
| Low-side gate driver output voltage | $V_{LO1,2,3}$ | COM-0.3 | $V_{CC}$+0.3 | |
| Logic input voltage | $V_{HIN1,2,3}$<br>$V_{LIN1,2,3}$<br>EN | -0.3 | 25 | |
| Low-side supply voltage | $V_{CC}$ | -0.3 | 25 | |
| Package power dissipation @ TA≤25°C [1] | $P_D$ | — | TSSOP20:1.2<br>TSSOP24:1.3 | W |
| Thermal resistance，junction to ambient [1] | $Rth_{JA}$ | — | TSSOP20:100<br>TSSOP24:94 | °C /W |
| Allowable Offset Voltage Slew Rate | dV/dt | — | 50 | V/ns |
| Junction temperature | $T_J$ | -40 | +150 | °C |
| Storage temperature | $T_S$ | -40 | +150 | |
| Soldering lead temperature (duration 10s) | TL | — | 260 | °C |

Note 1: $P_D$ and $Rth_{JA}$ are only guaranteed by design.

# RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Low-side supply voltage | $V_{CC}$ | 10 | — | 20 | V |
| High-side Floating Supply Offset Voltage[2, 3] | $V_{S1,2,3}$ | COM-6 | — | 200 | |
| High-side Floating Supply Voltage | $V_{B1,2,3}$ | $V_{S1,2,3}$+10 | — | $V_{B1,2,3}$+20 | |
| High-side gate driver output voltage | $V_{HO1,2,3}$ | $V_S$ | — | $V_B$ | |
| Low-side gate driver output voltage | $V_{LO1,2,3}$ | COM | — | $V_{CC}$ | |
| Logic input voltage | $V_{HIN1,2,3}$<br>$V_{LIN1,2,3}$<br>EN | 0 | — | 5 | |
| IC operating Junction temperature | $T_J$ | -40 | — | +125 | °C |

Note 2: For VBS=15V, normal Logic operation for VS of COM–6V to 200V. High-side circuitry will sustain current state if VS is of COM-6 to COM-$V_{BS}$. The parameter is only guaranteed by design.

Note 3 IC packed by TSSOP20L is recommended to operate at VS of -6 to 100V.

# STATIC ELECTRICAL CHARACTERISTICS

($V_{CC}$-COM)= ($V_B$-$V_S$) =15V. Ambient temperature TA=25°C unless otherwise specified. The $V_{IN,TH}$, $V_I$, and $I_{IN}$ Parameters are reference to COM and are applicable to all channels. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads. The VCCUV parameters are referenced to COM. The VBSUV parameters are referenced to VS.

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Low Side Power Supply Characteristics** | | | | | | |
| Quiescent VCC supply current | $I_{QVCC1}$ | $V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, $V_{EN}$=0 | 210 | 330 | 450 | μA |
| Quiescent VCC supply current in standby mode | $I_{QVCC2}$ | $V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, $V_{EN}$=5 | - | 16 | 40 | |
| operating VCC supply current | $I_{VCCOP}$ | f $_{LIN1,2,3}$=20KHz, f $_{HIN1,2,3}$=20KHz, | - | 1500 | - | |
| VCC supply under-voltage positive going threshold | $V_{CCUV+}$ | - | 7.7 | 8.5 | 9.5 | V |
| VCC supply under-voltage negative going threshold | $V_{CCUV-}$ | - | 7 | 8.0 | 9 | |
| VCC supply under-voltage lockout hysteresis | $V_{CCHYS}$ | - | - | 0.5 | - | |
| **High Side Floating Power Supply Characteristics** | | | | | | |
| High side VBS supply under-voltage positive going threshold | $V_{BSUV+}$ | - | 6.6 | 7.8 | 9 | V |
| High side VBS supply under-voltage negative going threshold | $V_{BSUV-}$ | - | 6.1 | 7.3 | 8.5 | |
| High side VBS supply under-voltage lockout hysteresis | $V_{BSUVHYS}$ | - | - | 0.5 | - | |
| High side quiescent VBS supply current | $I_{QBS}$ | $V_{BS}$=15V | 44 | 63 | 85 | μA |
| Offset supply leakage current | $I_{LK}$ | $V_B$=$V_S$=200V $V_{CC}$=0V | - | - | 10 | |
| **Logic Input Section** | | | | | | |
| Logic"1" Input voltage HIN1,2,3, LIN1,2,3 and EN | $V_{IH}$ | - | 2.5 | - | - | V |
| Logic"0" Input voltage HIN1,2,3, LIN1,2,3 and EN | $V_{IL}$ | - | - | - | 0.8 | |
| Input positive going threshold | $V_{IN,TH+}$ | - | - | 1.9 | - | |
| Input negative going threshold | $V_{IN,TH-}$ | - | - | 1.4 | - | |
| Logic "1" Input bias current | $I_{IN+}$ | $V_{IN}$=5V | - | 50 | - | μA |
| Logic "0" Input bias current | $I_{IN-}$ | $V_{IN}$=0 | - | 0 | - | |
| **Gate Driver Output Section** | | | | | | |
| High Side Output High Short-Circuit Pulse Current | $I_{HO+}$ | $V_{HO}$=$V_S$=0 | - | 320 | - | mA |
| High Side Output Low Short-Circuit Pulse Current | $I_{HO-}$ | $V_{HO}$=$V_B$=15V | - | 620 | - | |
| Low Side Output High Short-Circuit Pulse Current | $I_{LO+}$ | $V_{LO}$=0 | - | 320 | - | |
| Low Side Output Low Short-Circuit Pulse Current | $I_{LO-}$ | $V_{LO}$=$V_{CC}$=15V | - | 620 | - | |
| Allowable Negative VS Voltage for HIN1,2,3 Signal Propagation to HO1,2,3 | $V_{SN}$ | $V_{BS}$=15V | - | -8 | - | V |

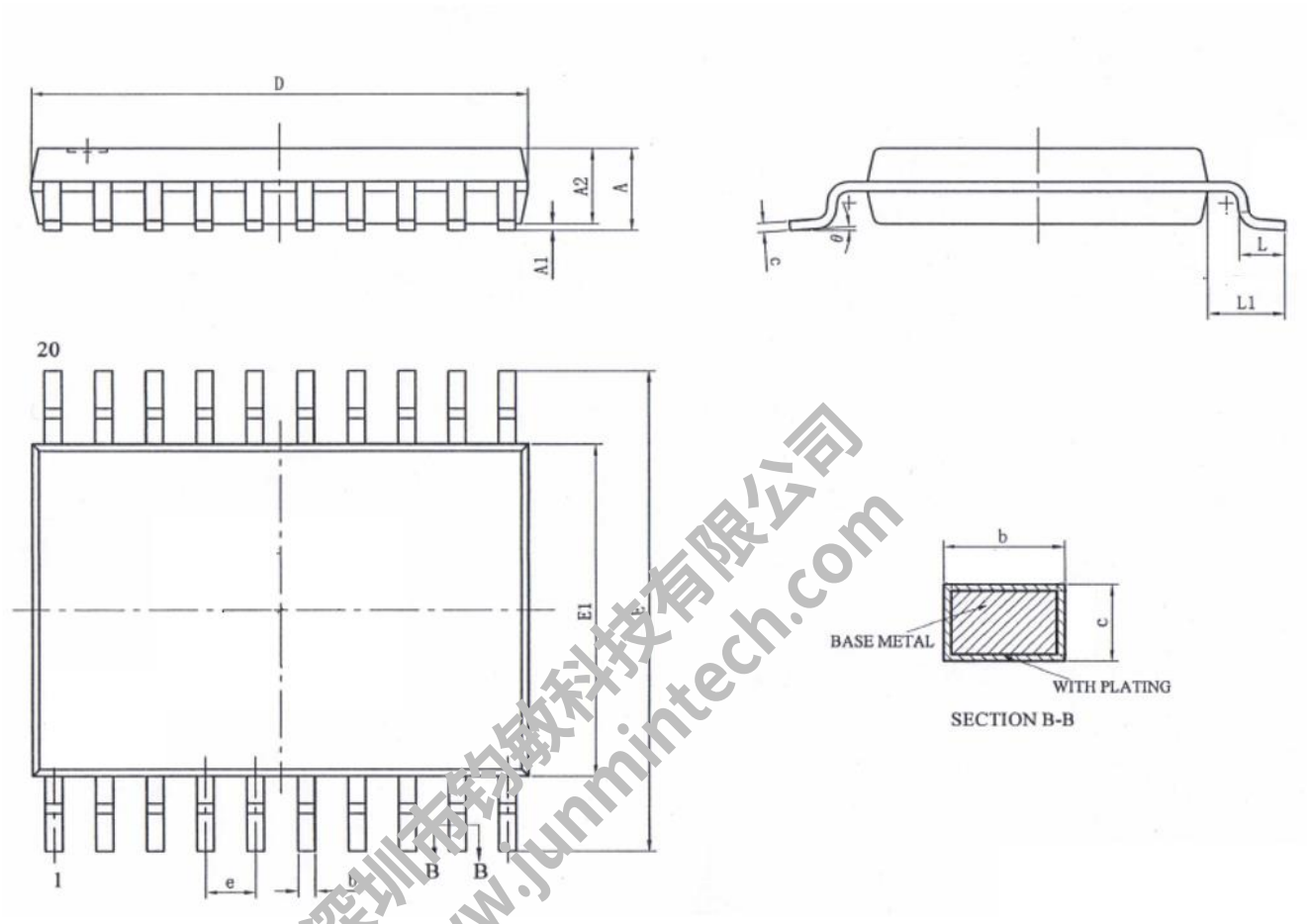
# DYNAMIC ELECTRICAL CHARACTERISTICS

(VCC-COM)= (VB-VS) =15V ,$V_{S1,2,3}$=COM, and $C_{load}$=1nF unless otherwise specified, ambient temperature $T_A$=25°C.

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Turn-On propagation delay | $t_{on}$ | $V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0 | 270 | 460 | 650 | ns |
| Turn-Off Propagation delay | $t_{off}$ | $V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=0 | 270 | 500 | 650 | |
| Turn-On Rise time | $t_r$ | $V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0 | - | 60 | - | |
| Turn-Off Fall time | $t_f$ | $V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=0 | - | 33 | - | |
| Input Filtering Time | $t_{FLT,IN}$ | $V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0 &5V | 100 | 300 | 500 | |
| Dead Time | DT | $V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0 &5V, Without External dead time | 400 | 600 | 800 | |
| Dead-Time Matching(All Six Channels) | MDT | Without External dead time | - | - | 100 | |
| Delay Matching(All Six Channels) | MT | External dead time >100ns | - | - | 100 | |
| Output Pulse-Width Matching | PM | External dead time > 100ns, $PW_{IN}$=1μs, PM=$PW_{OUT}$-$PW_{IN}$ | - | - | 100 | |
| EN input filter time | $t_{FLT,EN}$ | $V_{EN}$=0 &5V | - | 250 | - | |
| EN input “high” to HO/LO turn-off delay time | $t_{off,EN}$ | $V_{EN}$=5V | 0.5 | 0.9 | - | μs |
| EN input “low” to HO/LO turn-on delay time | $t_{on,EN}$ | $V_{EN}$=0V | 2 | 3 | - | |

# PACKAGE INFORMATION

## *20 PINS, TSSOP*

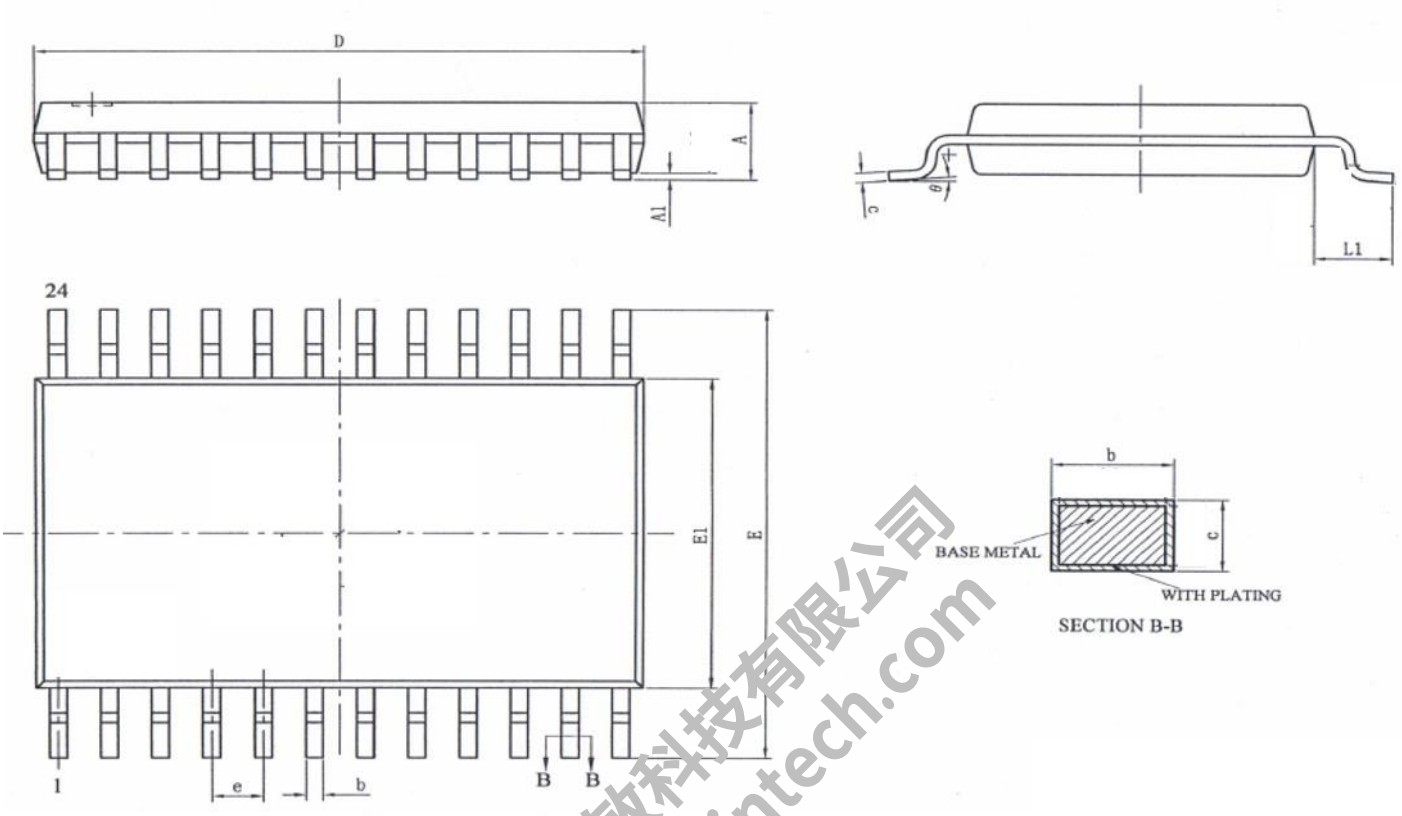





| Symbol | Dimensions | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | - | 0.30 |
| c | 0.09 | - | 0.20 |
| e | | 0.65 BSC. | |
| D | 6.40 | 6.50 | 6.60 |
| E | | 6.4 BSC. | |
| E1 | 4.30 | 4.40 | 4.50 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| θ | 0° | - | 8° |

Notes:
1. All dimensions refer to JEDEC MO-153 AC
2. All dimensions are in mm.

## *24 PINS, TSSOP*






| Symbol | Dimensions | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| b | 0.19 | 0.20 | 0.30 |
| c | 0.09 | - | 0.20 |
| e | 0.65 BSC. | | |
| D | 7.70 | 7.80 | 7.90 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| L1 | 1.00 REF | | |
| θ | 0° | - | 8° |

Notes:
3. All dimensions refer to JEDEC MO-153 ADT
4. All dimensions are in mm.