DESCRIPTION

The PT4302 is an ultra-low power OOK/ASK super heterodyne receiver for the 315/433.92 MHz frequency bands. It offers a high level of integration and requires only few external components. The PT4302 consists of a low-noise amplifier (LNA), a down-conversion mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, an OOK/ASK demodulator, a data filter, a data slicing comparator and an on-chip regulator. The PT4302 also implements a discrete one-step automatic gain control (AGC) that reduces the LNA gain when the RF input signal is greater than –68 dBm. The AGC circuitry can extend the dynamic range of received RF signal.

The PT4302 is available in a 16-pin SSOP package and is specified over the extended temperature range (–40 to +85°C).

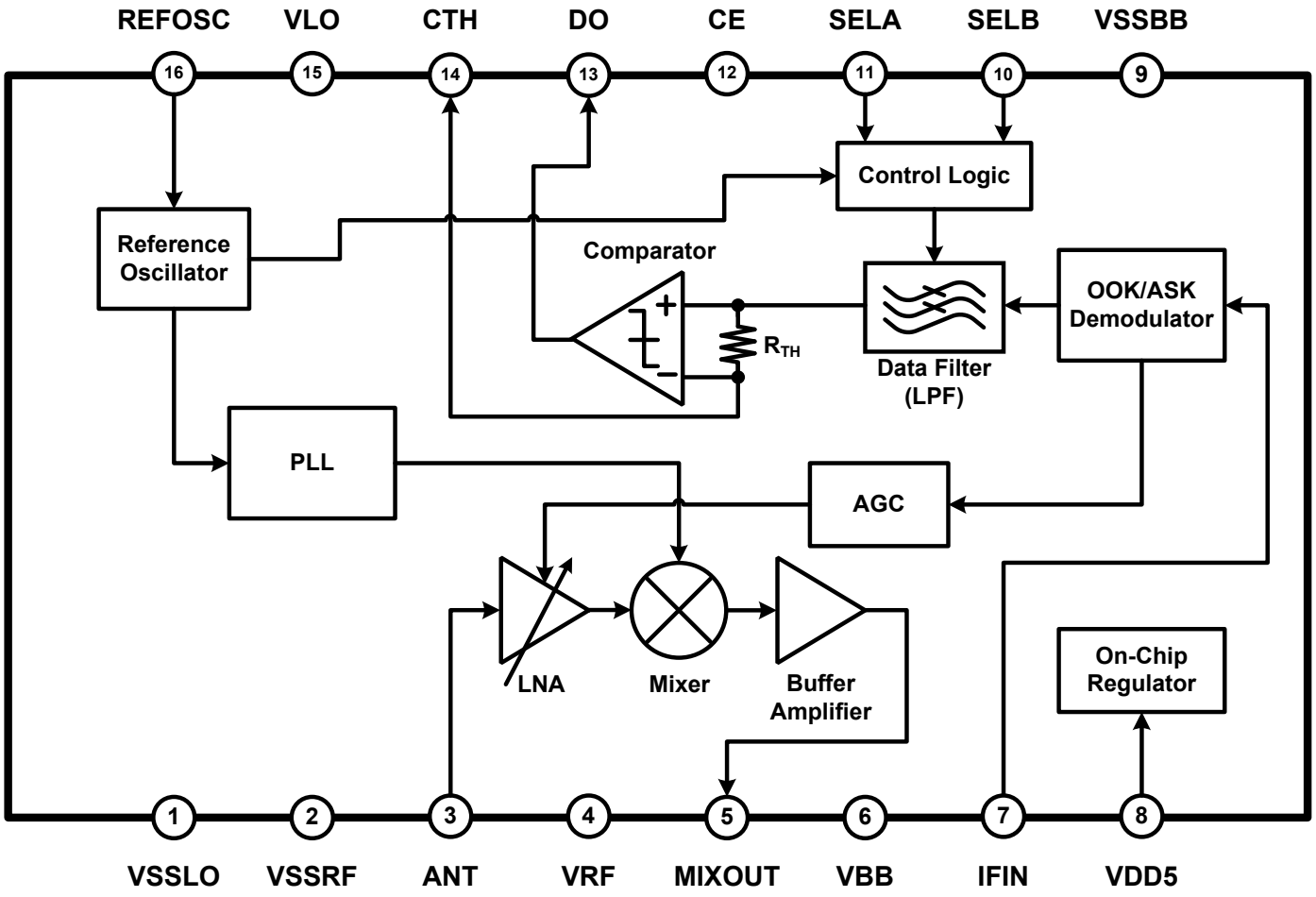
FEATURES

- Ultra-low power consumption: 2.7 mA for full operation (315 MHz)
- Few external components
- Excellent sensitivity of the order of –111 dBm (peak ASK signal level)
- 2.4 V to 5.5 V supply voltage range
- 250 MHz to 500 MHz frequency range
- Data rate up to 10 Kb/s

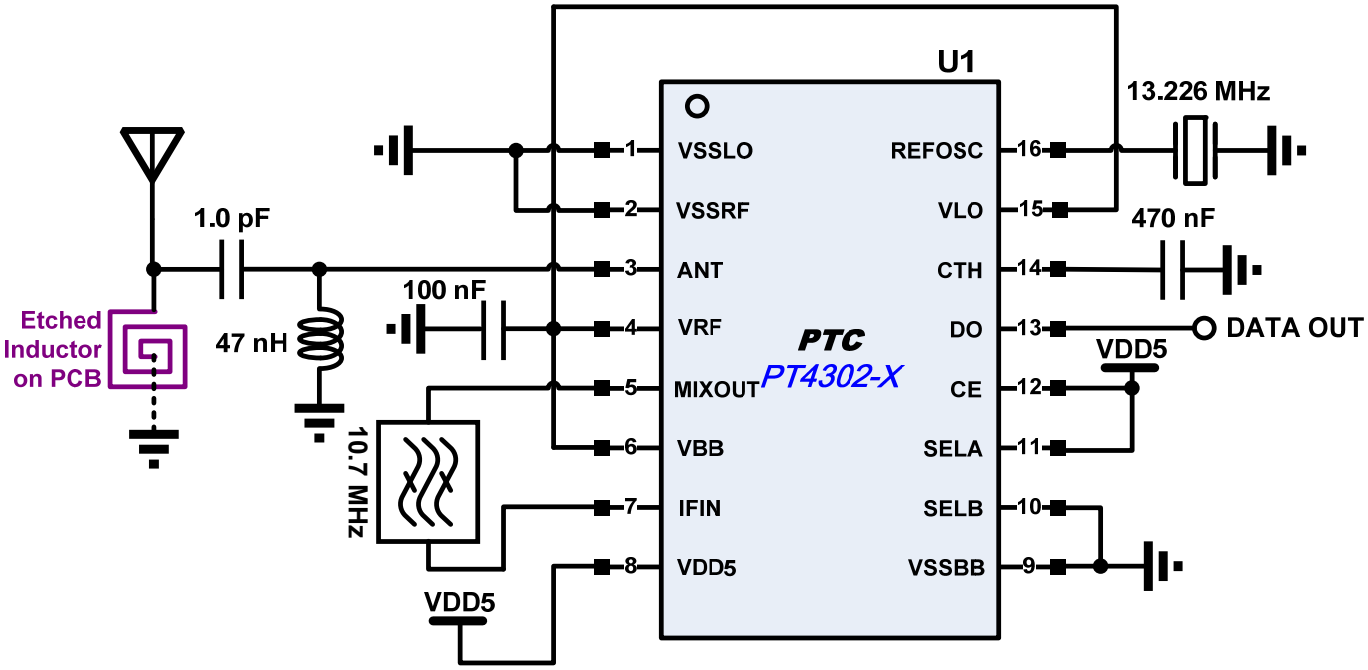
APPLICATIONS

- Automotive remote keyless entry (RKE)
- Remote control
- Garage door and gate openers
- Suitable for applications that meet either the European ETSI-300-220 or the North American FCC (Part 15) regulatory standards

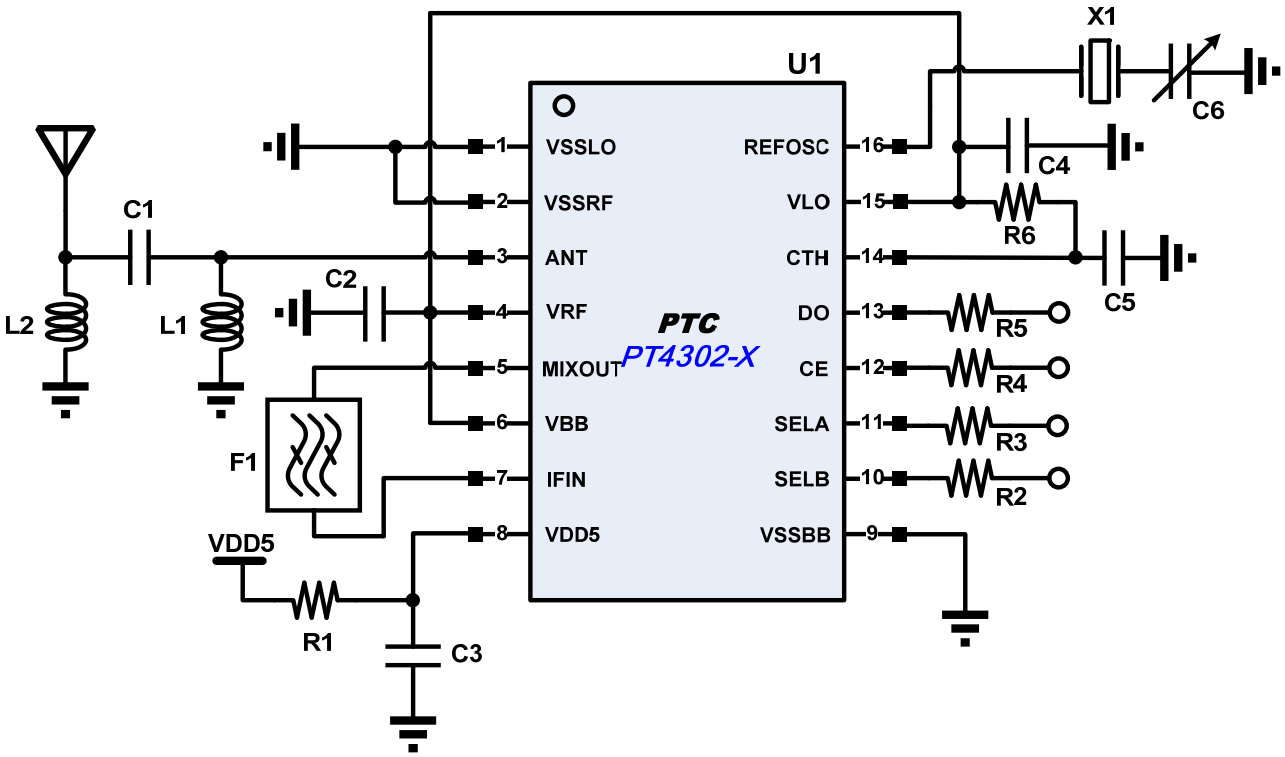
BLOCK DIAGRAM



433.92 MHZ RKE EXAMPLE



APPLICATION CIRCUIT



BILL OF MATERIALS

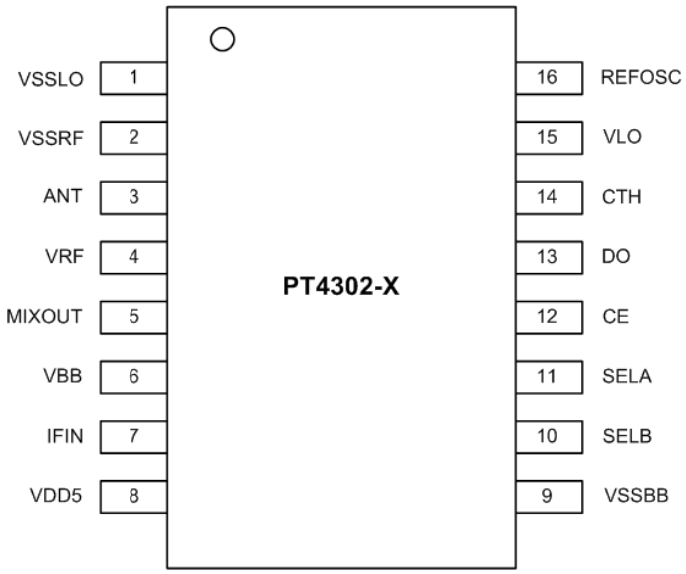
Part	Value		Unit	Description
	315 MHz	433.92 MHz		
L1	82 n	47 n	H	Antenna input matching, coil inductor
L2	39 n	27 n	H	Antenna ESD protection, coil inductor (optional)
C1	1.8 p	1.0 p	F	Antenna input matching
C2, C3, C4	100 n	100 n	F	Power supply de-coupling capacitor
C5	470 n	470 n	F	C_{TH} (affects coding type and start-up time)
C6	220 p	220 p	F	Depends on crystal oscillator vendor, for frequency fine tuning
R1	10	10	Ω	Power supply de-coupling resistor (optional)
R2, R3, R4, R5	10 K	10 K	Ω	MCU interface resistor (optional)
R6	8.2 M	8.2 M	Ω	For reducing data output noise (optional)
F1	10.7	10.7	MHz	Band-pass filter
X1	9.509	13.226	MHz	Reference crystal oscillator
U1	PT4302 IC	PT4302 IC	U1	Receiver chip

Notes:
1. L1 and C1 are the components for input matching network. They may have to be adjusted with different PCB layout and antenna requirement.
2. The value of C5 depends upon the data rate and coding pattern.
3. F1 is the 10.7 MHz ceramic filter. The recommended part number is Murata SFELA10M7HA00-B0.
4. The “optional” components are based on application requirements.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4302-X	16 Pins, SSOP, 150 mil	PT4302-X

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VSSLO	G	Ground for LO portion	1
VSSRF	G	Ground for RF portion	2
ANT	I	RF input connection to antenna by a matching network	3
VRF	P	Supply voltage for RF portion	4
MIXOUT	O	Mixer IF output	5
VBB	P	Supply voltage for baseband chain	6
IFIN	I	IF stage input	7
VDD5	P	5 V supply voltage input	8
VSSBB	G	Ground for baseband chain	9
SELB	I	Data filter bandwidth select (Pin B)	10
SELA	I	Data filter bandwidth select (Pin A)	11
CE	I	Chip enable pin (pull HIGH to enable the chip)	12
DO	O	Data output	13
CTH	I/O	Data slicing threshold capacitor connection	14
VLO	P	Supply voltage for LO portion	15
REFOSC	I	Reference oscillator input pin	16

FUNCTION DESCRIPTION

POWER SUPPLY

PT4302 provides an internal voltage regulator to supply power to the entire receiver. Hence, all supply voltage pins, except VDD5, should be connected together with sufficient bypass capacitance added as close to each pin as possible. Only the VDD5 pin (pin 8) should be connected to an external supply voltage, with series-R, shunt-C filtering included if necessary. The PT4302 chip can operate over the supply voltage range from 2.4 V to 5.5 V.

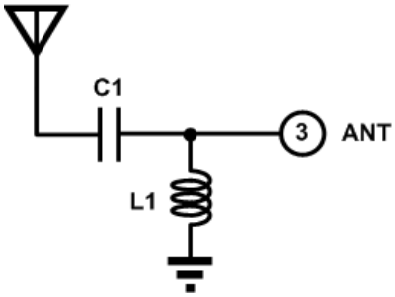
RF FRONT-END

The RF front-end of the receiver part is a superheterodyne configuration that converts the input radio frequency (RF) signal into an intermediate frequency (IF) signal. The IF for the PT4302 chip is 10.7 MHz. According to the block diagram, the RF front-end consists of a LNA and a down-conversion mixer, and the local oscillator (LO) signal for the mixer is generated by the PLL frequency synthesizer.

As the receiver constitutes a superheterodyne architecture, there is no inherent suppression of the image frequency. It depends upon the particular application and the system's environment conditions whether an RF front-end filter should be added or not. If image rejection or good blocking immunity is relevant system parameter, a band-pass filter must be placed in front of the LNA. This filter can be a SAW (surface acoustic wave) or LC-based filter (e.g. helix type).

The RF front-end provides the good low noise performance (NF less than 5 dB), high voltage conversion gain of over 40 dB, and excellent reversion isolation. The preferred LO side-band is low-side injection for reducing power consumption. The IF output impedance of the mixer is about 330 Ohm in order to match the IF channel selection filter.

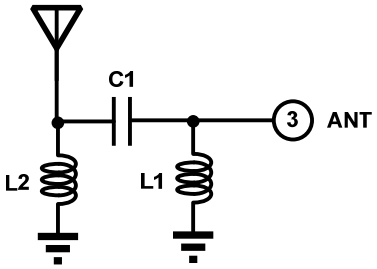
The ANT pin may be matched to 50 Ω with an L-type circuit (e.g. a shunt inductor from the RF input to ground and another in series from the RF input to the antenna pin). An example of the input matching network is shown in the following figure and the input impedance of the PT4302 for 315/433.92 MHz frequency bands are listed in the right-hand side table. The component values given in the BOM for the application circuit shown on page 2 are nominal values only. Inductor and capacitor values may be different from the values given in the table depending on PCB material, PCB thickness, ground configuration, and how long the traces are in the layout.



RF Frequency f_{RF}	ANT Input Impedance (Pin 3)
315 MHz	1.328 − j213.91
340 MHz	1.602 − j195.74
390 MHz	2.469 − j170.92
433.92 MHz	2.086 − j152.17

ANTENNA PART ESD PROTECTION

PT4302 IC provides better than 3 KV ESD immunity (human-body mode) at the ANT pin. However, higher ESD protection level may be required at the system level for some applications. For such cases, ESD enhancement may rely on external components. For example, changing L1 from SMD-type to coil-type can enhance ESD protection level by 1 KV, and adding a shunt coil inductor L2 in front of C1 can achieve additional ESD protection.



RF Frequency f_{RF}	Suggested value of L2
315 MHz	39 nH
340 MHz	39 nH
390 MHz	33 nH
433.92 MHz	27 nH

REFERENCE OSCILLATOR

All timing and tuning operations on the PT4302 are derived from the internal one-pin Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of two ways:

1. Connect a crystal,
2. Drive this pin with an external timing signal.

When a crystal is used, the minimum oscillation voltage swing is 300 mV_{PP}. For an externally applied signal, the source should be AC-coupled and limited to a voltage swing range from 0.3 V_{PP} to 1.5 V_{PP}.

As with any superheterodyne receiver, the mixing between the internal LO (local oscillator) frequency f_{LO} and the incoming carrier frequency f_{TX} must ideally equal the IF center frequency (10.7 MHz). The following equation may be used to compute the appropriate f_{LO} for a given f_{TX}:

$f_{LO} = f_{TX} \pm 10.7$.

Frequencies f_{TX} and f_{LO} are expressed in MHz. Note that two values of f_{LO} exist for any given f_{TX}, distinguished as "high-side" ($f_{LO} > f_{TX}$) and "low-side" ($f_{LO} < f_{TX}$) mixing. High-side mixing results in an image frequency above the frequency of interest and low-side mixing results in an image frequency below. We recommend low-side mixing for saving receiver power. After choosing one of the two acceptable values of f_{LO}, use the following equation to compute the reference oscillator frequency f_{REFOSC}:

$f_{REFOSC} = f_{LO} / 32 = (f_{TX} - 10.7) / 32$.

The following table identifies f_{REFOSC} for some common transmit frequencies when the PT4302 chip is operated with low-side mixing.

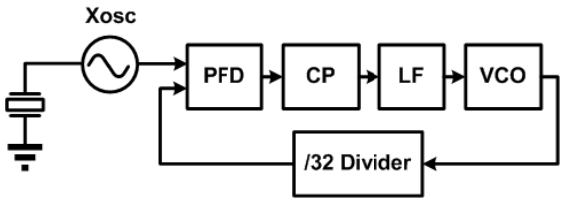
Transmit Frequency f_{TX}	Reference Oscillator Frequency f_{REFOSC}
315 MHz	9.509 MHz
340 MHz	10.29 MHz
390 MHz	11.853 MHz
433.92 MHz	13.226 MHz

The reference oscillator frequency is close to 10.7 MHz intermediate frequency. It is necessary to avoid signal trace coupling between the reference oscillator and intermediate frequency to prevent degradation of receiver performance.

PHASE-LOCKED LOOP (PLL)

The PT4302 utilizes a fixed divided-by-32 PLL to generate the receiver LO. The PLL consists of the voltage-controlled oscillator (VCO), crystal oscillator, asynchronous ÷32 divider, charge pump, loop filter and phase-frequency detector (PFD). All these components are integrated on-chip. The PFD compares two signals and produces an error signal which is proportional to the difference between the input phases. The error signal passes through a loop filter with an approximately 200 KHz bandwidth, and is used to control the VCO which generates an LO frequency. The VCO frequency is also fed through a frequency divider back to one input of the PFD, producing a feedback loop. Thus, the output is locked to the reference frequency at the other input, which is derived from a crystal oscillator (i.e. $f_{REFOSC} = (f_{RF} - f_{IF}) / 32$).

The block diagram below shows the basic elements of the PLL.



ASK DEMODULATOR

The OOK/ASK demodulation utilizes the RSSI signal level. The RSSI signal is decimated and filtered in the data filter and the data decision is then completed by the slicing comparator.

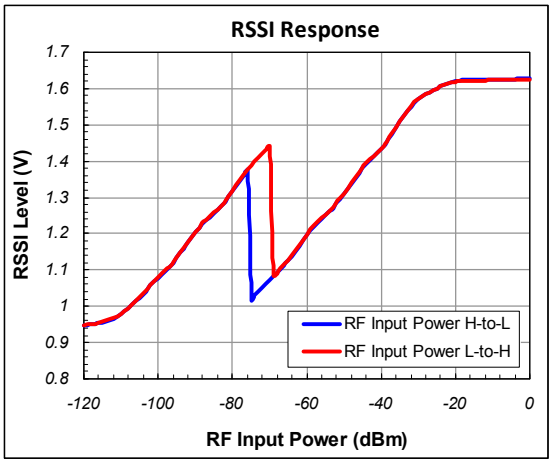
The RSSI is implemented as a successive-detection logarithmic amplifier which is followed by the external IF channel filtering. The logarithmic amplifier achieves ±3 dB logarithmic linearity, and the RSSI output level has a dynamic range of around 80 dB with a slope of approximately 11.5 mV /dB.

The IFIN pin presents a differential 330 Ohm load to provide good matching for the off-chip ceramic filter.

AUTOMATIC GAIN CONTROL (AGC)

The AGC circuitry monitors the RSSI voltage level. When the RSSI voltage exceeds a threshold reference value corresponding to an RF input level of approximately –68 dBm, the AGC switches on the LNA gain and then reduces the LNA gain by around 30 dB, thereby reducing the RSSI output by approximately 345 mV. The threshold reference voltage which is compared with the RSSI voltage to determine the gain state of the LNA is also reduced. The LNA resumes high-gain mode when the RSSI voltage drops below this lower threshold voltage corresponding to approximately –75 dBm RF input. The AGC incorporates an additional protection mechanism (delay timer of $2^{20} \times T_{REF}$ seconds) to prevent immediate resetting of the LNA back to the high-gain state during reception of a “space” for OOK/ASK modulation.

The figure below shows the change of RSSI voltage versus RF input power. When the RSSI level increases and then exceeds 1.47 V (RF input power rising), the AGC switches the LNA from high-gain mode to low-gain mode. As RSSI level decreases back to 1.06 V (RF input power falling), the AGC switches the LNA from low-gain mode back to high-gain mode.



The AGC hysteresis delay times for the different frequency bands are listed below.

Parameter	Condition	f_{RF} = 315 MHz	f_{RF} = 433.92MHz
AGC Hysteresis Delay Time	RF input power changes from High to Low	110 ms	79 ms

DATA FILTER

The data filter (post-demodulator filter) is utilized here to remove other unwanted spurious signals after the OOK/ASK demodulator, which is implemented as a 2nd-order low-pass Sallen-Key filter. The data filter bandwidth (BW_{DF}) must be selected according to the applications and should be set according to equation

BW_{DF} = 0.65 / Shortest pulse-width.

The input pins of SELA and SELB control the data filter bandwidth in four binary steps (see the table below). It should be noted that the values indicated in this table are nominal values. The filter bandwidth scales linearly with frequency, so the exact value will depend upon the operating frequency.

SELA	SELB	Data Filter Bandwidth BW_{DF}	
		f_{RF} = 315 MHz	f_{RF} = 433.92 MHz
1	1	900 Hz	1250 Hz
1	0	1800 Hz	2500 Hz
0	1	3600 Hz	5000 Hz
0	0	7200 Hz	10000 Hz

DATA SLICER

The purpose of the data slicer is to take the analog output of the data filter and convert it to a digital signal. Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip resistor R_{TH}, shown in the block diagram. Slicing level time constant (τ) values vary somewhat with decoder type, data pattern, and data rate, but typical values range from 2 ms to 20 ms. Optimization of the value of C_{TH} is required to maximize range.

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure. The effective resistance of R_{TH} is 25 KΩ and τ of 3x the period of longest “LOW” or “HIGH” bit stream is recommended. Assuming that a slicing level time constant τ has been established, capacitor C_{TH} may be computed using equation

$C_{TH} = \tau / R_{TH}$.

A standard ±20% X7R ceramic capacitor is generally sufficient.

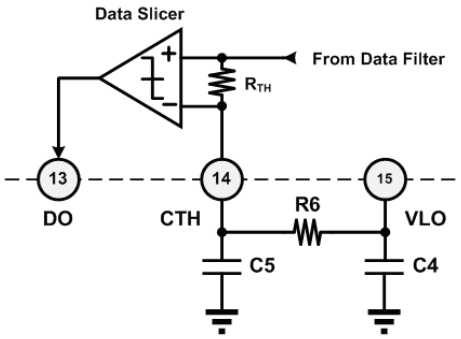
DATA SQUELCHING

During quiet periods (no signal) the data output (DO pin) transitions randomly with noise. Most decoders can discriminate between this random noise and actual data, but for some system the random transitions do present a problem. There are two possible approaches to reducing these output noise transitions:

1. Analog squelch to raise the demodulator threshold,
2. Output filter to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is add analog squelch by introducing a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal slicer. Usually 20 mV to 30 mV is sufficient and may be achieved by connecting a several mega-ohm resistor from the CTH pin to either VSS or internal supply voltage, depending on the desired offset polarity. The squelch offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce sensitivity and also reduce the receiving dynamic range. Only introduce an amount of offset sufficient to quiet the output. Typical squelch resistor values range from 5.1 MΩ to 8.2 MΩ.

The circuit below shows an application example of analog squelch, where R6 is the squelch resistor. The demodulated data then enters into a quasi-mute state as the RF input signal becomes very small (e.g. if there is no RF signal received or the RF signal is too small) and the DO output remains mostly at a logic "LOW" level. If the environment is very noisy, the R6 value may be reduced to achieve better immunity against noise, but at the cost of less sensitivity.



SENSITIVITY AND SELECTIVITY

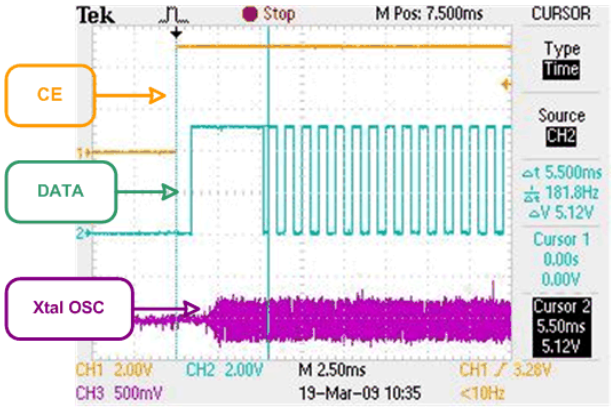
In digital radio systems, sensitivity is often defined as the lowest signal level at the receiver input that will achieve a specified bit error ratio (BER) at the output. The sensitivity of the PT4302 receiver, when used in the 315 MHz application, is typically –112 dBm (ASK modulated with 2 Kb/s, 50% duty cycle square wave) to achieve a 0.1% BER. The input was matched for a 50 Ω signal source. At 433.92 MHz, –111 dBm sensitivity is typically achievable.

The selectivity is governed by the response of the receiver front-end circuitry, the channel filter (off-chip 10.7 MHz IF filter), and the data filter. Note the IF filter provides not only channel selectivity but also interference rejection. Within the pass band of the receiver, no rejection for interfering signals is provided.

POWER-DOWN CONTROL

The chip enable (CE) pin controls the power on/off behavior of the PT4302. Connecting CE to "HIGH" sets the PT4302 to its normal operation mode; connecting CE to "LOW" sets the PT4302 to standby mode. The chip consumption current will be lower than 1 μA in standby mode. Once enabled, the PT4302 requires < 10 ms to recover received data with minimum received RF input level.

The following figure illustrates the system start-up time with T = 27 ºC, f_{RF} = 315 MHz, P_{RF} = –110 dBm, C_{TH} = 100 nF and D_{RATE} = 2 Kb/s. The CE pin is triggered every 200 mS.



ANTENNA DESIGN

For a $\lambda/4$ dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}.$$

For example, if the frequency is 315 MHz, then the length of a $\lambda/4$ antenna is 22.6 cm. If the calculated antenna length is too long for the application, then it may be reduced to $\lambda/8$, $\lambda/16$, etc. without degrading the input return loss. However, the RF input matching circuit may need to be re-optimized. Note that in general, the shorter the antenna, the worse the receiver sensitivity and the shorter the detection distance. Usually, when designing a $\lambda/4$ dipole antenna, it is better to use a single conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

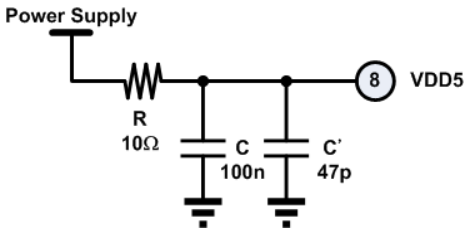
If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r = 4.7) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where "c" is the speed of light (3 x10^{10} cm/s)

PCB LAYOUT CONSIDERATION

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers. Note that if the PCB design incorporates a printed loop antenna, there should be no ground plane beneath the antenna.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. To reduce supply bus noise coupling, the power supply trace should be incorporate series-R, shunt-C filtering as shown below.

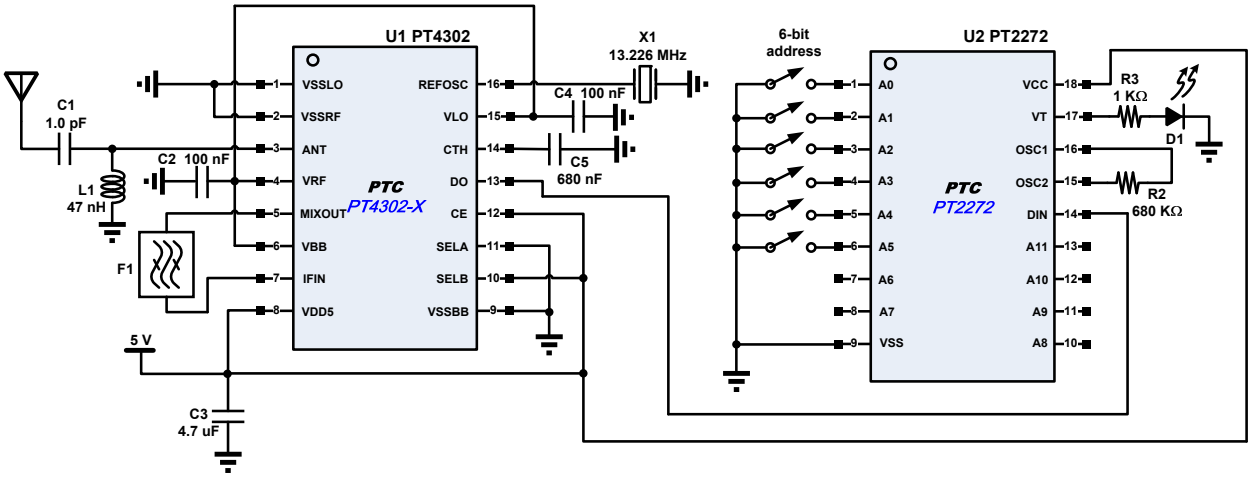


APPLICATION EXAMPLE

433.92 MHz Receiver / Decoder Application

The following schematic illustrates a typical application at 433.92 MHz frequency band for the PT4302 receiver IC. This receiver operates continuously (not duty cycled) in the enable (active) mode, and features 6-bit address decoding.

The value of C5 may need to be increased if the idle time is too long between each data frame. Changes from the 1 kb/s data rate may require a change in the value of R2. A bill of materials accompanies the schematic.



Part	Part Number	Manufacturer	Description
U1	PT4302-X	Princeton Technology Corp.	UHF OOK/ASK receiver
U2	PT2272	Princeton Technology Corp.	Remote control decoder
F1	SFELA10M7HA00-B0	Murata	10.7 MHz ceramic filter with 180 KHz BW
L1	-	-	47 nH SMD inductor
C1	-	-	1.0 pF SMD capacitor
C2	-	-	100 nF SMD capacitor
C3	-	-	4.7 F SMD capacitor
C4	-	-	100 nF SMD capacitor
C5	-	-	680 nF SMD capacitor
R1	-	-	1 K SMD resistor with 5% tolerance
R2	-	-	680 K SMD resistor with 5% tolerance
X1	-	-	13.226 MHz crystal with maximum 60 ESR
D1	-	-	Red LED

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD5}	–0.3	6	V
Analog I/O Voltage	–	–0.3	3	V
Digital I/O Voltage	–	–0.3	6	V
Operating Temperature Range	T_A	–40	+85	°C
Storage Temperature Range	T_{STG}	-40	+150	°C

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From Chip Conjunction Dissipation to External Environment	Rja	T_A = 27 °C	–	37.15	–	°C/W
From Chip Conjunction Dissipation to Package Surface	Rjc		–	1	1.8	

ELECTRICAL CHARACTERISTICS

Nominal conditions: V_{DD5} = 5.0 V, V_{SS} = 0 V, CE = "High", T_A = +27°C, f_{RF}= 315 / 433.92 MHz, f_{REFOSC} = 9.509 / 13.226 MHz.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD5}	Connect the supply voltage to VDD5 pin only	2.4	5.0	5.5	V
Current Consumption	I_{DD5}	f_{RF} = 315 MHz	–	2.7	3.0	mA
		f_{RF} = 433.92 MHz	–	2.9	3.2	
Standby Current	I_{STBY}	CE="Low"	–	–	1	μA
Operating Frequency Range	f_{RF}		250	–	500	MHz
Maximum Receiver Input Level	$P_{RF,MAX}$		–20	–15	–	dBm
Sensitivity[1]	S_{IN}	ASK[2], D_{Rate} = 2 Kb/s, peak power level @ 315 MHz	–	–112	–109	dBm
		OOK, D_{Rate} = 2 Kb/s, peak power level @ 315 MHz	–	–106	–103	
		ASK[2], D_{Rate} = 2 Kb/s, peak power level @ 433.92 MHz	–	–111	–108	dBm
		OOK, D_{Rate} = 2 Kb/s, peak power level @ 433.92 MHz	–	–105	–102	
Data Rate	D_{RATE}		–	2	10	Kb/s
LO Leakage	L_{LO}	Measured at antenna input	–	–	–80	dBm
System Start-Up Time	T_{STUP}	RF input power = –60 dBm	–	5	8	ms
RF Front-End						
Voltage Conversion Gain	GV_{RF}	Matched to 50Ω@ 315 MHz	40	43	46	dB
		Matched to 50Ω @ 433.92 MHz	39	42	45	
Noise Figure	NF_{RF}	Matched to 50Ω @ 315 MHz	–	5.7	6.3	dB
		Matched to 50Ω @ 433.92 MHz	–	6.1	6.7	
Mixer Output Impedance	$Z_{OUT,MIXER}$	Measured at MIXOUT pin	300	330	360	Ω
IF Section						
IF Frequency	f_{IF}		–	10.7	–	MHz
IF Bandwidth	BW_{IF}	Depends upon the external ceramic filter	–	180	–	KHz
IF Input Impedance	$Z_{IN,IF}$		300	330	360	Ω
RSSI Slope	SL_{RSSI}		9.5	11.5	13.5	mV/dB
Demodulator						
Post-Demodulator Filter Bandwidth	BW_{DF}	SELA = SELB = "HIGH"	–	0.9	–	KHz
		SELA = "HIGH"; SELB = "LOW"	–	1.8	–	
		SELA = "LOW"; SELB = "HIGH"	–	3.6	–	
		SELA = SELB = "LOW"	–	7.2	–	
CTH Leakage Current	I_{ZCTH}	T_A = +85°C	–	±100	–	nA
Automatic Gain Control (AGC)						
AGC Hysteresis Delay Time[3]	T_{HYS}	f_{RF} = 315 MHz	–	110	–	ms
		f_{RF} = 433.92 MHz	–	79	–	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Phase-Locked Loop						
Reference Frequency	f_{REFOSC}		7	–	16	MHz
Reference Signal Voltage Swing	V_{REF}	Peak-to-peak voltage (V_{PP})	0.3	–	1.5	V
VCO Frequency Range	f_{VCO}		220	–	550	MHz
Divider Ratio	DIV		–	32	–	–
Digital/Control Interface						
Input-High Voltage	$V_{IN,High}$	CE, SELA, SELB pins	0.8	–	–	V_{DD5}
Input-Low Voltage	$V_{IN,Low}$	CE, SELA, SELB pins	–	–	0.2	V_{DD5}
Output Current	I_{OUT}	DO pin, push-pull	–	20	–	μA
Output-High Voltage	$V_{OUT,High}$	DO pin, I_{OUT} = –1 μA	0.9	–	–	V_{DD5}
Output-Low Voltage	$V_{OUT,Low}$	DO pin, I_{OUT} = +1 μA	–	–	0.1	V_{DD5}
Output Rise/Fall Times	t_R/ t_F	DO pin, C_{LOAD} = 15 pF	–	10	–	μs

Notes:
1. BER = 1e–3
2. AM 99% with square-wave modulation
3. RF input power changes from high to low

Typical Operating Characteristics

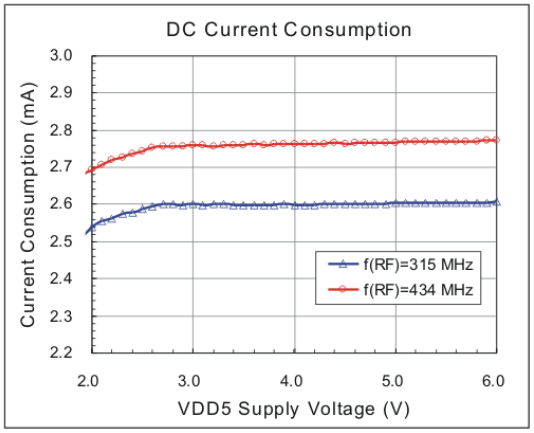


Figure 1. Supply Current vs. Supply Voltage

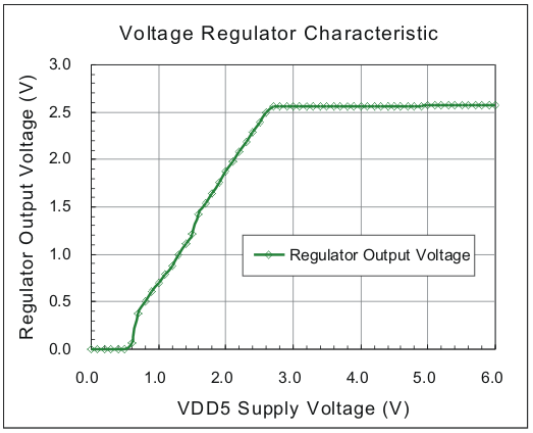


Figure 2. Voltage Regulator Characteristic

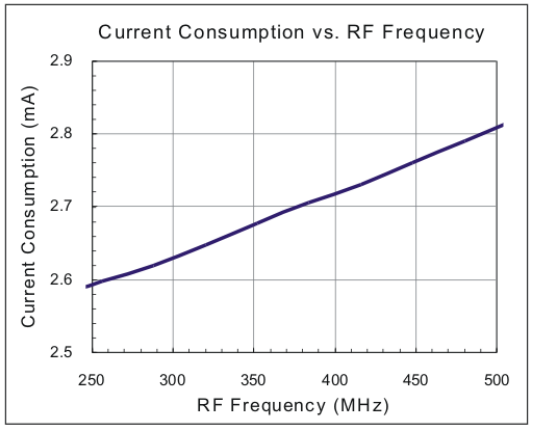


Figure 3. Current Consumption vs. RF Frequency

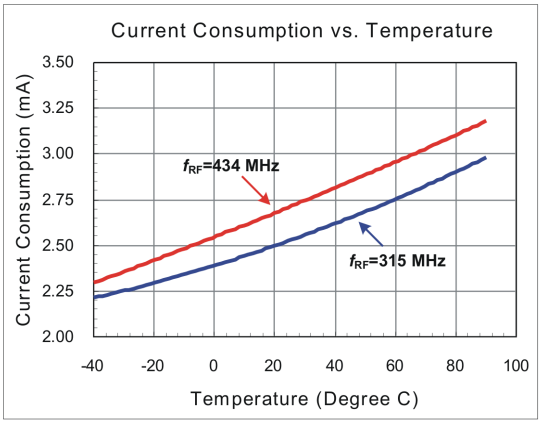


Figure 4. Current Consumption vs. Temperature

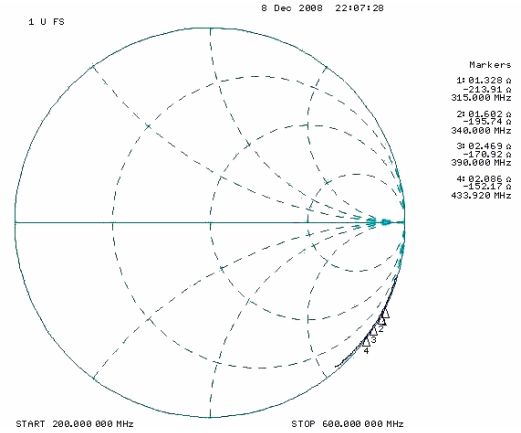


Figure 5. Smith Plot of ANT

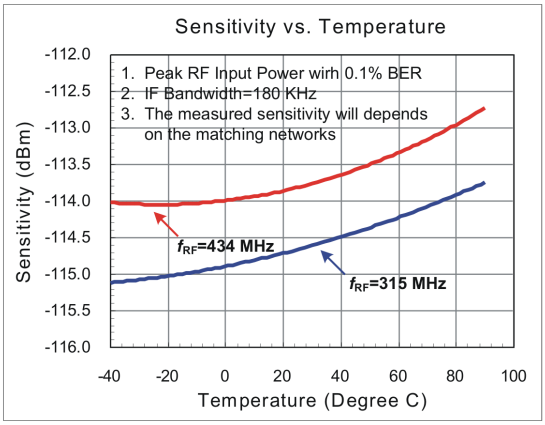


Figure 6. Sensitivity vs. Temperature

Typical Operating Characteristics (cont'd)

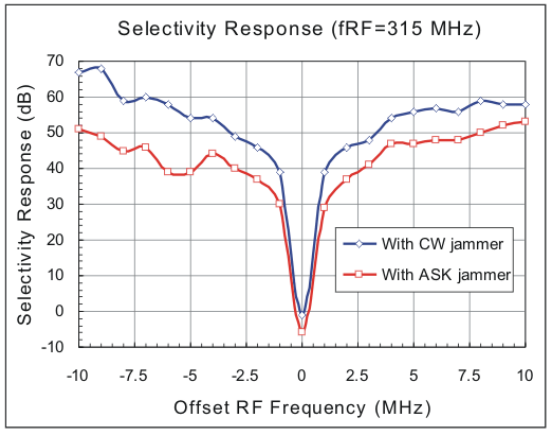


Figure 7. Selectivity Response for f_{RF} = 315 MHz

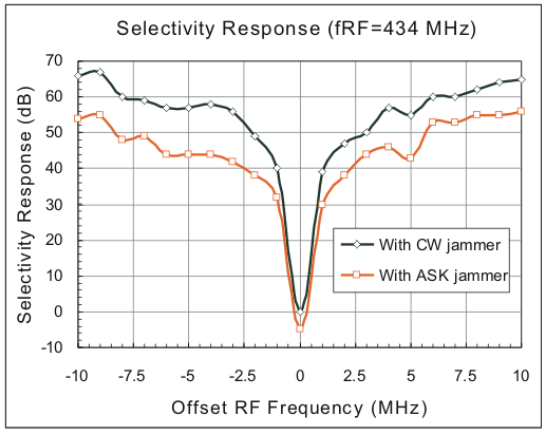
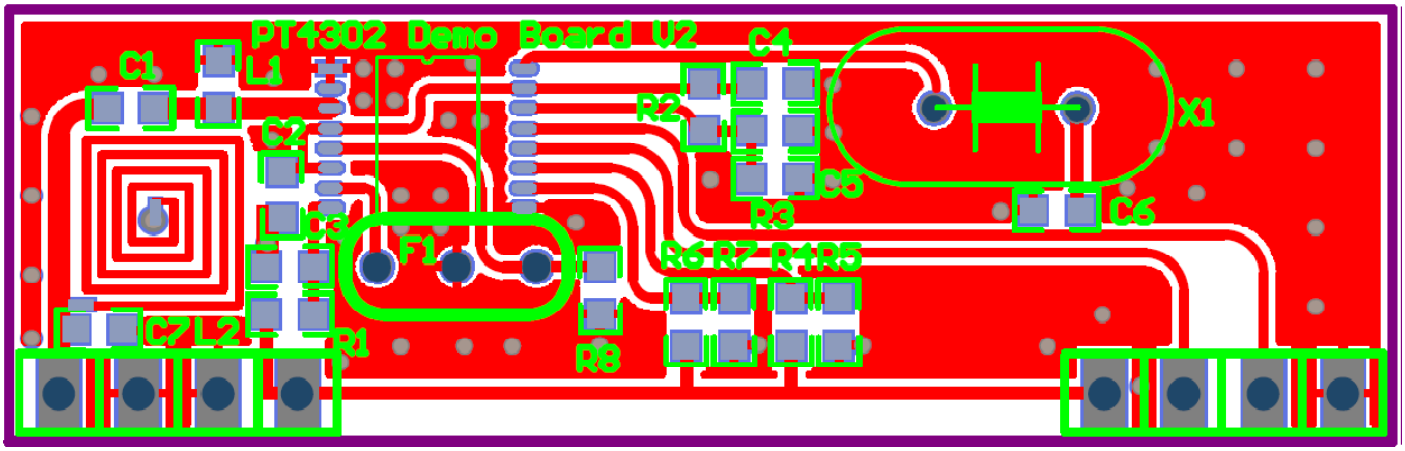
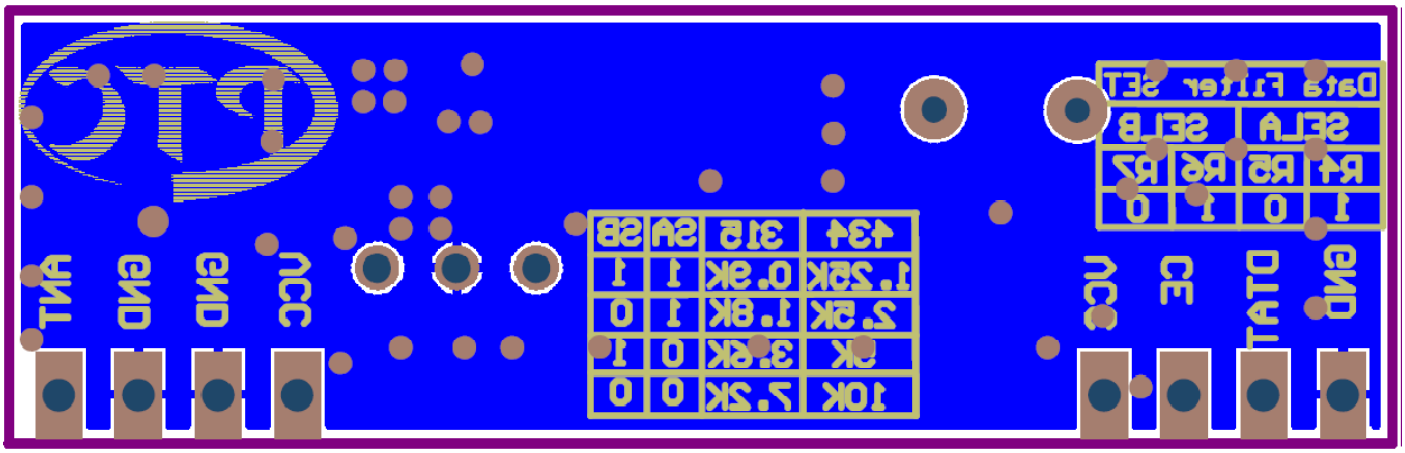


Figure 8. Selectivity Response for f_{RF} = 433.92 MHz

TEST BOARD LAYOUT



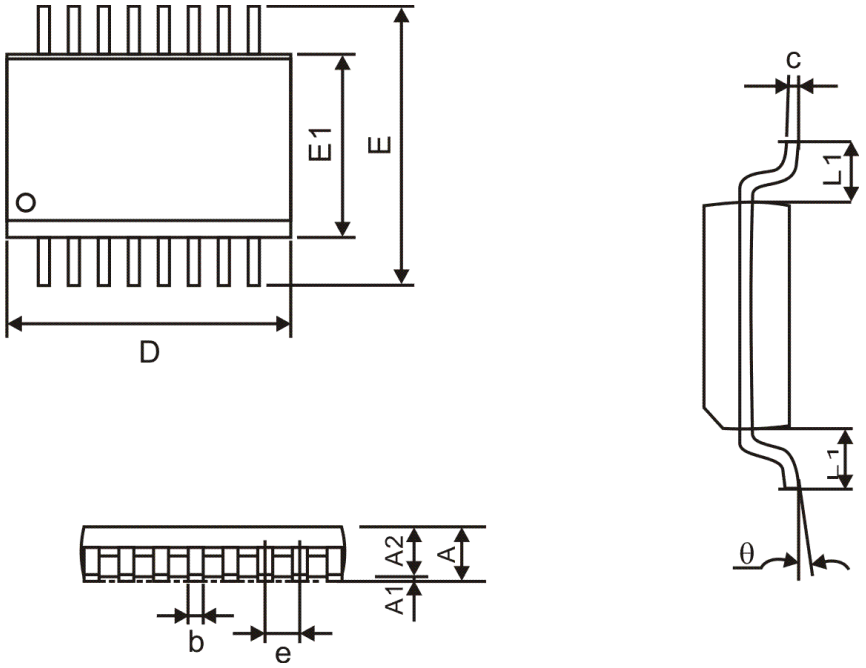
<Top Side>



<Bottom Side>

PACKAGE INFORMATION

16 Pins, SSOP (Shrink Small Outline Package with 3.9 × 4.9 mm Body Size, 0.64 mm Pitch Size and 1.6 mm Thick Body)



Symbol	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	-
A2	1.245	-	-
b	0.203	-	0.305
c	0.102	-	0.254
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L1	1.04 REF		
θ	0º	-	8º

Notes:
1. Refer to JEDEC MO-137AB
2. Unit: mm

IMPORTANT NOTICE

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Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw