Model name: PT320AT01-1

Ver. 1.0
Date: 29. Mar.2017

( ) Preliminary Specification

(v) Approval Specification

Any modification is not allowed without HKC's permission

Customer's Approval	**Chongqing HKC**
Signature Date	Approved By Product Director Date Name: York Signature: York
	Reviewed By PM Manager Date Name: LUCIUS Signature: Lucius 2017/3/31
	Reviewed By Project Leader Date Name: KK Signature: KK 2017/3/31
	Reviewed By PM Date Name: Pinky Signature: Pinky 2017/3/31

Contents

Revision History

Version	Date	Page (New)	Section	Description	Revision by
Ver 0.1	2017/03/07	-	All	Preliminary Specification was First Issued.	Pinky
Ver 1.0	2017/3/29	P7/P27	3.1.1/3.6	Update Power Supply Current / Driver IC ESD spec	Pinky

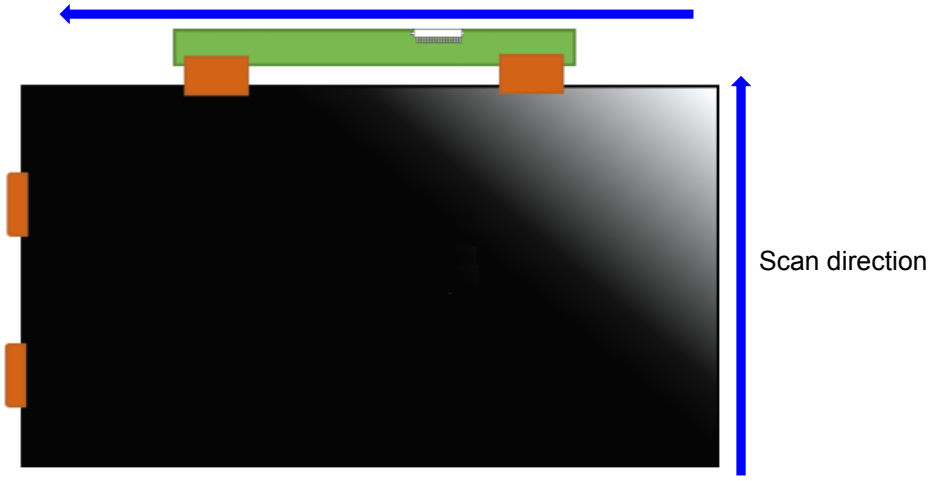
1. GENERAL DESCRIPTION

The specification is applied to 31.5” model (PT320AT01-1) TFT Liquid Crystal Display open cell and it supports 1366 x 768 HD mode with 16.7M colors. This product is with driver ICs and a 30-pins-1ch-LVDS circuit board and built in without backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	31.5 inch Diagonal	inch	-
Outline Dimension	715(H) x 411(V) x 1.4(D)	mm	D: cell thickness
Active area	697.6845(H) x 392.256(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Cell transmittance	6.50	%	C light，center point
Pixel Number	1366 x 768	pixel	-
Sub Pixel Pitch	0.17025 (H) x 0.51075 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Mode	Normally Black	-	-
Display Orientation	Signal input as below	-	-
Surface Treatment	Type=AG	-	-
	Haze=3%		
	Top Surface Hardness ≧ 3H	-	
Weight	937.5	g	

Note:



2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Input Signal Voltage	V_{in}	-0.3	3.6	V	(1)

Note:

(1) Within Ta=25±2°C

2.2 Absolute Ratings of Environment

Temperature and relative humidity range is shown in the figure below.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	°C	(1)
Operating Temperature	TOP	0	50	°C	(1), (2), (3)

Note:

(1) a. 90 % RH Max. (Ta ≤ 40 °C).

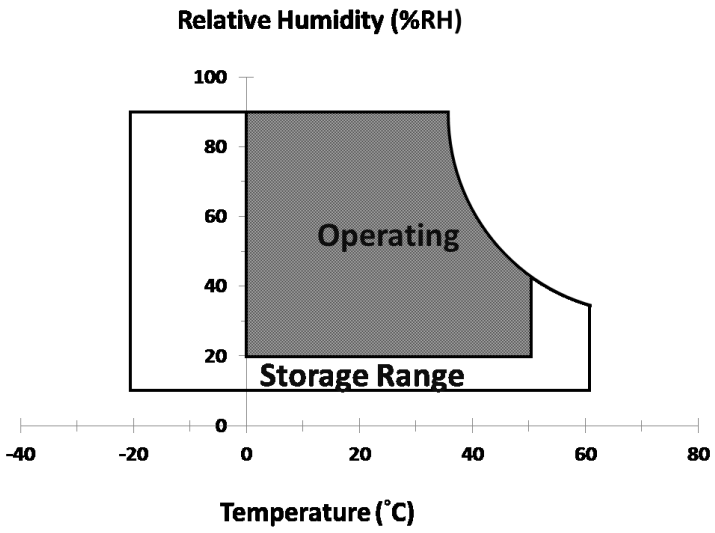
b. Web-bulb temperature should be 39℃ Max.(Ta>40℃)

c. No condensation

d. Operating condition with a assemble module

(2) The temperature of panel surface should be 0 ºC min. and 50 ºC max.

(3) Any point on the Driver surface must be less than 105 ºC under any condition ,If the surface temperature is out of the spec, thermal solutions should be applied to avoid be damaged.



3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power consumption

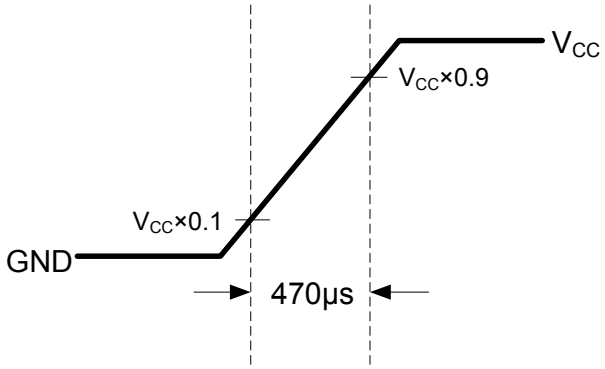
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(2)
Rush Current		I_{RUSH}	-	-	2.0	A	(3)
Power Supply Current	White Pattern	-	-	0.37	0.50	A	(4)
	Horizontal Stripe	-	-	0.35	0.45	A	
	Black Pattern	-	-	0.25	0.31	A	

Note:

(1) Ambient temperature: 25 ± 2ºC

(2) The ripple voltage should be controlled under 10% of V_{CC}.

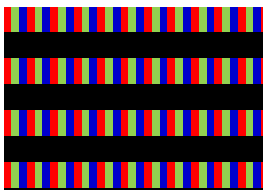
(3) Measurement Conditions: V_{CC} rising time=470μs. ds



(4) Measurement Conditions: V_{cc} =12V, Ta = 25 ± 2 ºC, F_v = 60 Hz, whereas the test pattern is shown as below.

A. White Pattern

B. Horizontal Strip



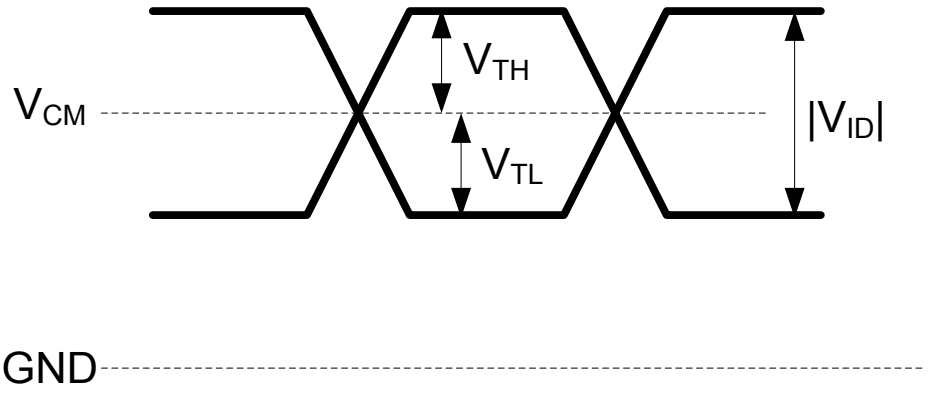
C. Black Pattern

3.1.2 LVDS characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	100	-	600	mV	
	Terminating Resistor	R_T	90	100	110	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.6	V	

Note:

(1) The LVDS input signal has been defined as follows:

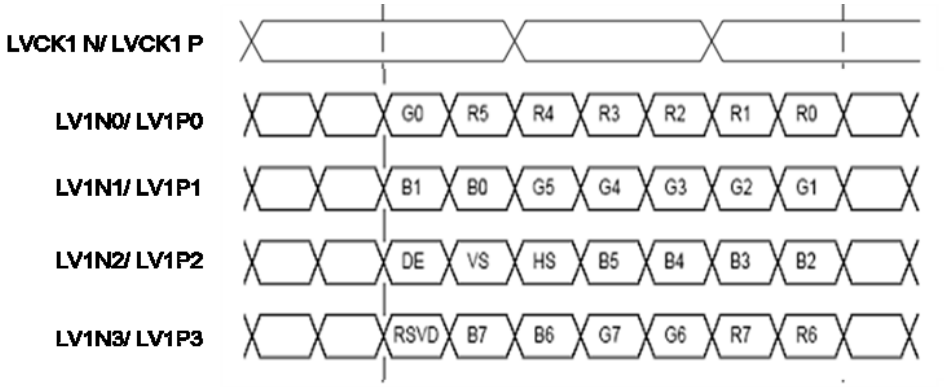


3.1.3 LVDS characteristics

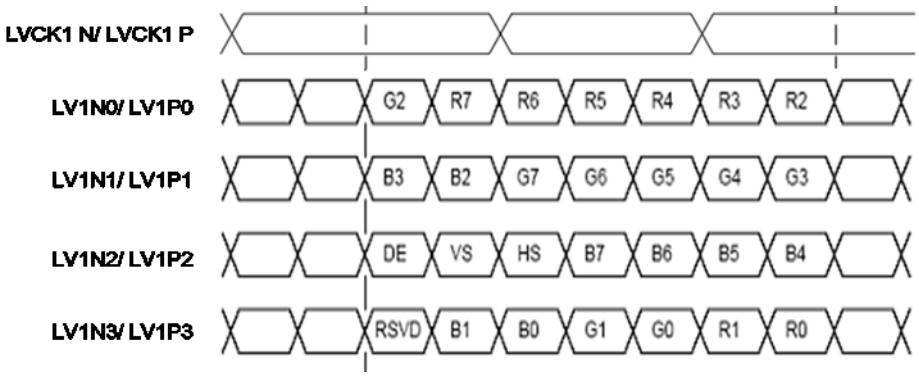
VESA Format: SELLVDS = L or Open

JEIDA Format: SELLVDS = H

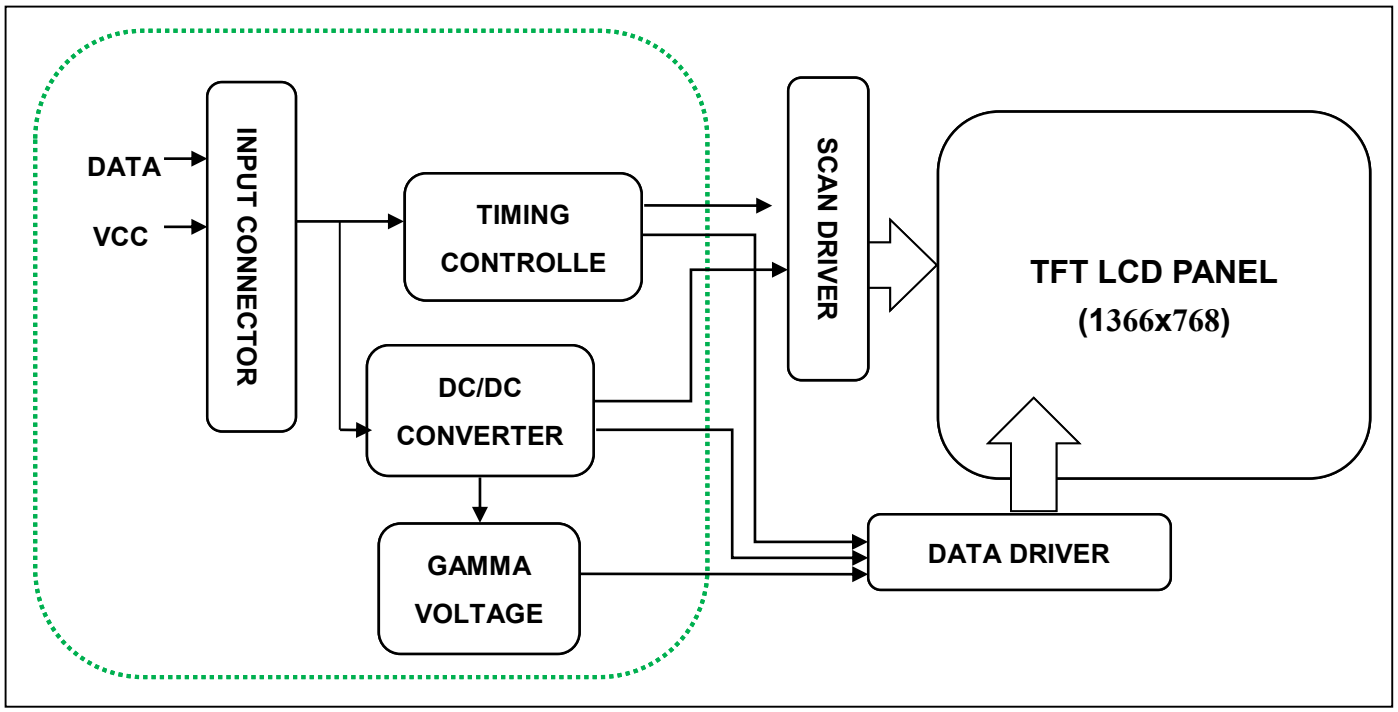
VESA Format



JEIDA Format



3.1.4 Block diagram



3.2 Interface Connections

Interface Pin Assignment

Connector part No. : CN1 03-187053-30091(P-TWO) or equivalent 1mm pitch 30 pin (1)

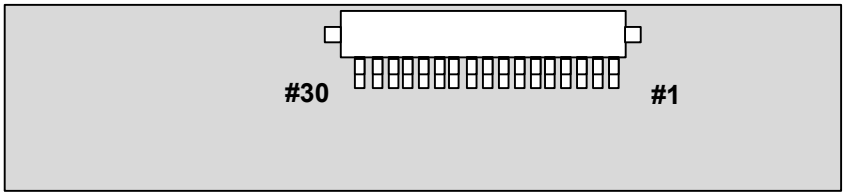
Pin No.	Symbol	Description	Note
1	VCC	Power supply	
2	VCC	Power supply	
3	VCC	Power supply	
4	VCC	Power supply	
5	GND	Power Ground	
6	GND	Power Ground	
7	GND	Power Ground	
8	GND	Power Ground	
9	SELLVDS	LVDS Data Format Selection	(3)
10	NC	No Connection	
11	GND	Power Ground	
12	RX0N	LVDS Data(0) -	
13	RX0P	LVDS Data(0) +	
14	GND	Power Ground	
15	RX1N	LVDS Data(1) -	
16	RX1P	LVDS Data(1) +	
17	GND	Power Ground	
18	RX2N	LVDS Data(2) -	
19	RX2P	LVDS Data(2) +	
20	GND	Power Ground	
21	RXCN	LVDS clock -	
22	RXCP	LVDS clock +	
23	GND	Power Ground	
24	RX3N	LVDS Data(3) -	
25	RX3P	LVDS Data(3) +	
26	GND	Power Ground	
27	NC	No Connection	(2)
28	NC	No Connection	(2)
29	NC	No Connection	(2)
30	GND	Power Ground	

Note:

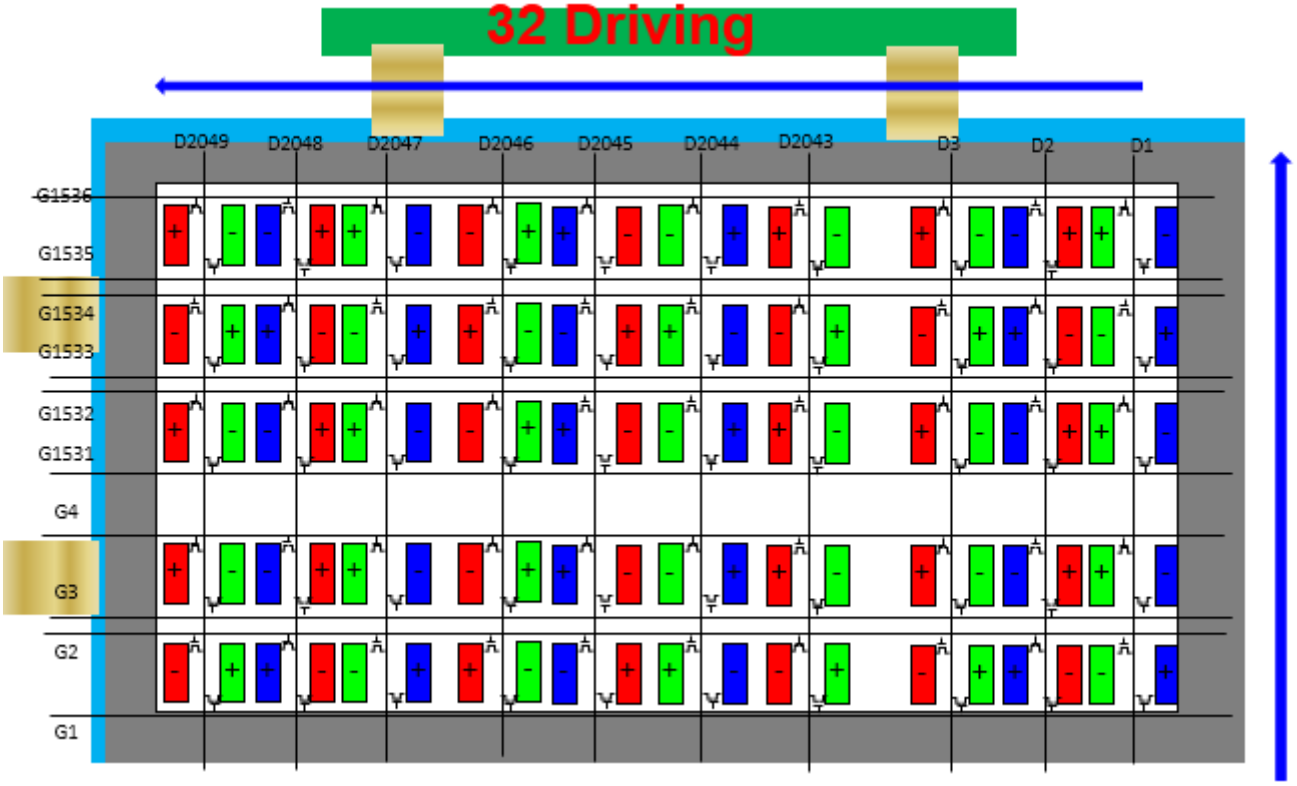
(1) Following finger shows the LVDS pin1 diagram.

(2) For HKC used only, please leave it open.

(3) High: connect to +3.3V→JEIDA Format；Low: connect to GND or Open→VESA Format.



(4) The first pixel is odd. Base on gate driver on left side, source driver on upside.



3.3 Timing Spec.

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	**F_{clkin}**	50	75.4	85	MHz	（1）
	Input cycle to cycle jitter	Trcl	—	—	200	ps	（2）
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	（3）
	Spread spectrum modulation frequency	FSSM	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSM	-400	—	400	ps	(4)
Vertical Term	Frame Rate	**F**	48	60	62.5	Hz	
	Total	**T_V**	784	806	1015	T_H	$T_V = T_{VD} + T_{VB}$
	Active Display	**T_{VD}**	768			T_H	
	Blank	**T_{VB}**	16	38	247	T_H	
Horizontal Term	Total	**T_H**	1460	1560	2000	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Active Display	**T_{HD}**	1366			T_{CLK}	
	Blank	**T_{HB}**	94	194	634	T_{CLK}	

Attention:

The module is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

Note:

（1）Please make sure the range of pixel clock follows the following equations:

$F_{CLK}(max) \geq F_{max} \times T_V \times T_H$ $F_{CLK}(min) \leq F_{min} \times T_V \times T_H$

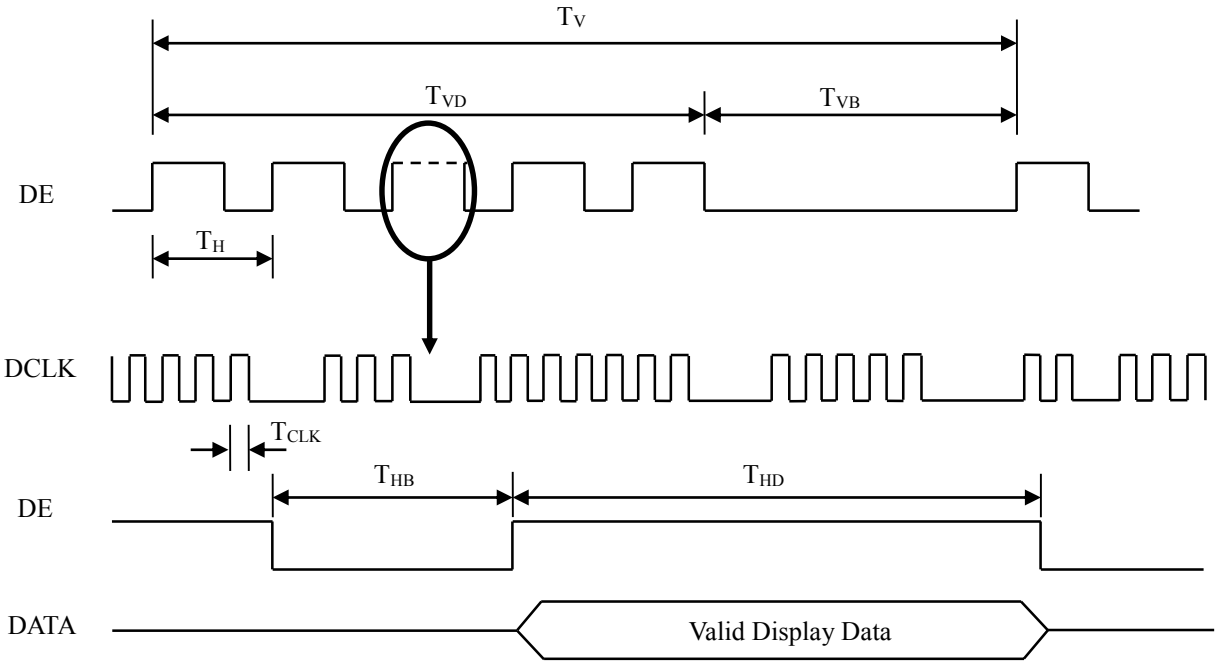


Fig 3.1 Signal timing diagram

（2）The input clock cycle-to-cycle is defined as below figures.

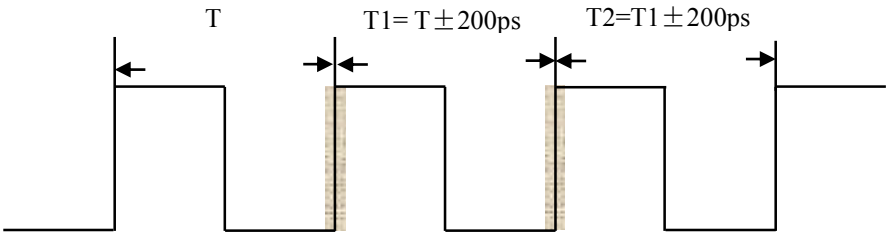
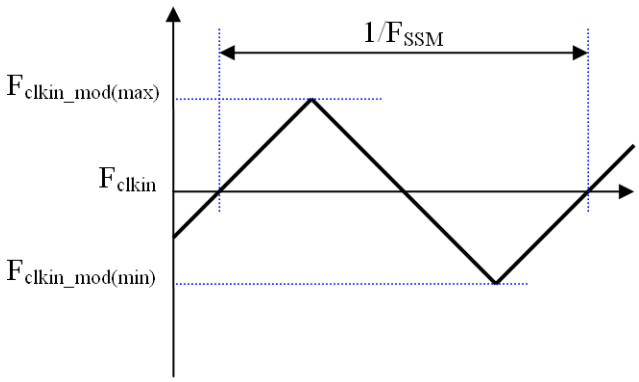


Fig 3.2 Jitter

(3) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.



(4) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

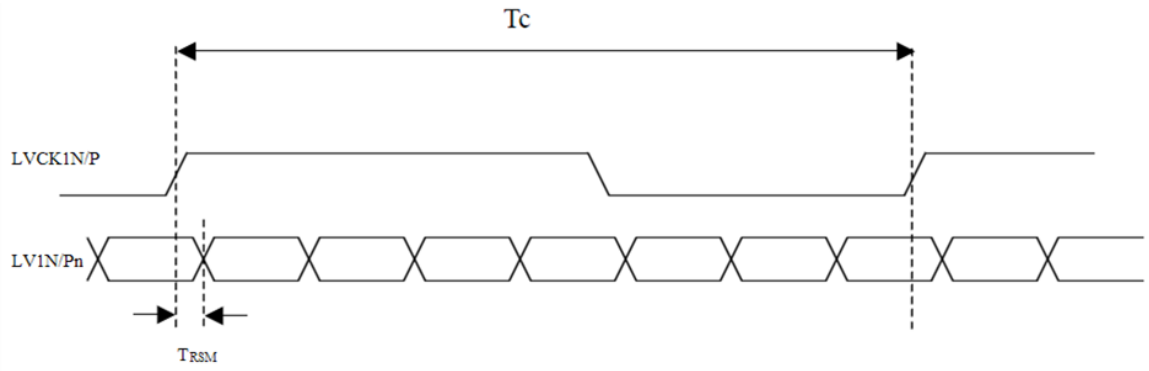


Fig 3.3 LVDS receive interface timing diagram

3.4 Power On/Off Sequence

The power sequence specifications are shown as the following table and diagram

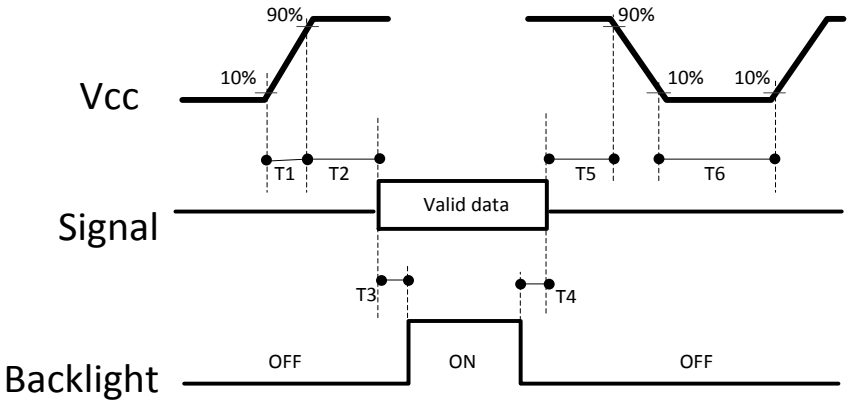


Fig 3.4 Power on/off signal sequence

Parameters	Values			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	500	-	-	ms
T4	100	-	-	ms
T5	0	-	50	ms
T6	1000	-	-	ms

Attention:

(1)The supply voltage of the external system for the module input should be the same as the definition.

(2) To avoid some abnormal display noise, we suggest " V_{CC} falling time" to follow "T6" definition.

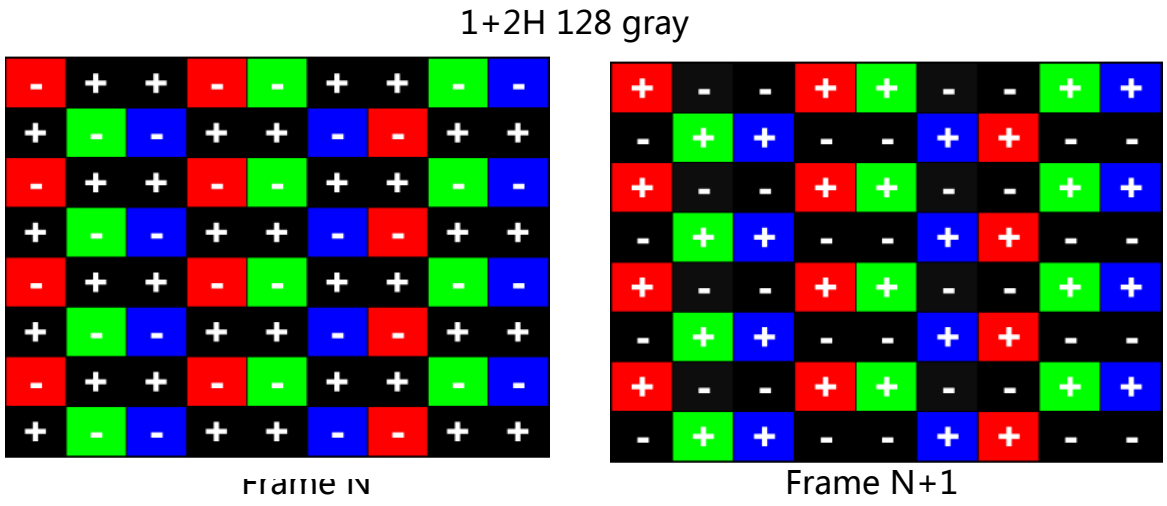
(3) The product should be always operated within above ranges.

(4) In case of V_{CC} is off level, please keep the level of input signals on the low or keep high impedance.

3.5 Flicker Adjustment

Flicker must be optimized after module assembly and aging. Its patterns are as follow:

1+2 line sub pixel checker under 50% gray level.



3.6 Driver IC ESD spec

If the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig.3.5 and Fig.3.6.

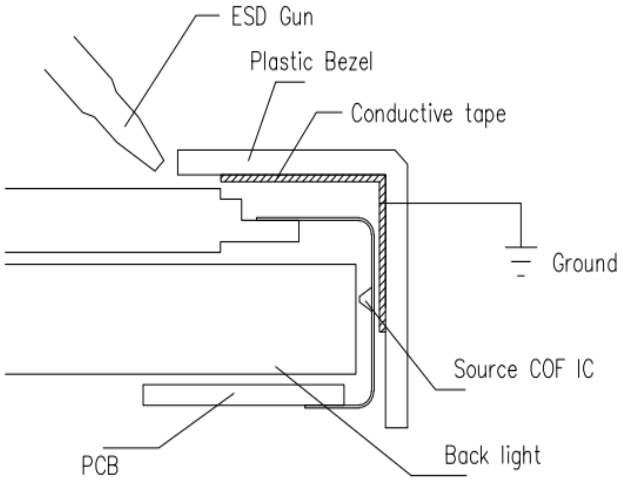


Fig. 3.5 Source COF IC ESD protection

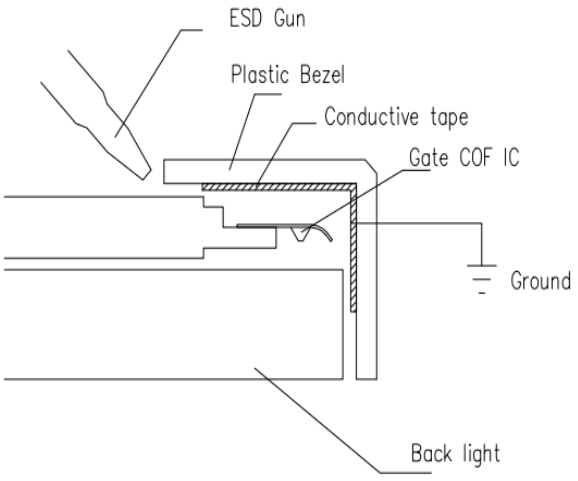


Fig. 3.6 Gate COF IC ESD protection

4. OPTICAL CHARACTERISTICS

4.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	ºC
Ambient Humidity	H_A	50±10	% RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_v	60	Hz
Light source	HKC 31.5" WXGA module White LED Backlight Module/ Film structure		
Warm up time	Twarm	>30 min	min
Dark room	ED	1lux>	lux

To avoid abrupt temperature change during optical measurement, the measurement should be executed in a stable, windless, in dark room after lighting the light source.

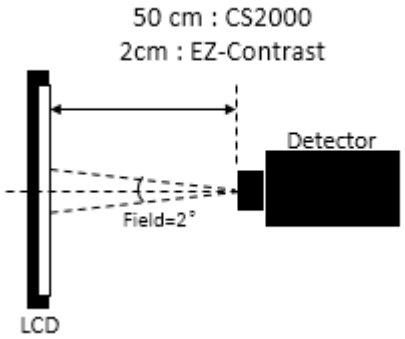


Fig 4.1 Measurement equipment.

4. 2 Optical Specifications

The relative measurement methods of optical characteristics are shown in 4.2. The following items should be measured under the test conditions described in 4.1 and stable environment shown in 4.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE1931)	Red	Rx	θ_x=0°,θ_y=0° Viewing Angle at Normal Direction at center point of panel, Light source is C light	Typ - 0.03	0.654	Typ + 0.03	--	(1)
		Ry			0.327			
	Green	Gx			0.278			
		Gy			0.578			
	Blue	Bx			0.136			
		By			0.105			
	White	Wx			0.307			
		Wy			0.347			
Color Gamut		CG			68		%	(2)
Transmittance		T%			6.5		%	(3)
Contrast Ratio		CR	θ_x=0°,θ_y=0°		3000		-	(4)
Response Time		T_g		-	8.5	17	ms	(5)
Viewing Angle	Horizontal	θ_x+	CR≧10	-	89	-	Deg.	(6)
		θ_x -		-	89	-		
	Vertical	θ_y+		-	89	-		
		θ_y-		-	89	-		

Note:

(1) Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying (Red, Green, Blue, White) and light source is defined by C-light, Measurements shall be made at the center of the panel, and setup of measurement is shown in Fig 4.1.

(2) The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig 4.1.

(3) Definition of Transmittance (T%):

The transmittance is measured with full white pattern (L_{max}) at the center of the LCD panel.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

Contrast Ratio (CR): $\boldsymbol{CR} = \frac{\boldsymbol{CR_W}}{\boldsymbol{CR_D}}$

CR_W : Luminance of LCD module with full screen white pattern (255,255, 255) at center point.

CR_D : Luminance of LCD module with full screen Dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel

(5) Definition of Response time (T_g):

Average of gray to gray response time (T_g) means the average switching time of luminance ratios among 0%,25%,50%,75%,and 100% to each other and is optimized on frame rate =60Hz.

Measured Response time		To				
		0%	25%	50%	75%	100%
From	0%		$T_{0\%to25\%}$	$T_{0\% to 50\%}$	$T_{0\% to 75\%}$	$T_{0\% to 100\%}$
	25%	$T_{25\% to 0\%}$		$T_{25\% to 50\%}$	$T_{25\% to 75\%}$	$T_{25\% to 100\%}$
	50%	$T_{50\% to 0\%}$	$T_{50\% to 25\%}$		$T_{50\% to 75\%}$	$T_{50\% to 100\%}$
	75%	$T_{75\% to 0\%}$	$T_{75\% to 25\%}$	$T_{75\% to 50\%}$		$T_{75\% to 100\%}$
	100%	$T_{100\% to 0\%}$	$T_{100\% to 0\%}$	$T_{100\% to 50\%}$	$T_{100\% to 75\%}$	

Table 4.2 switching time of luminance ratios matrix

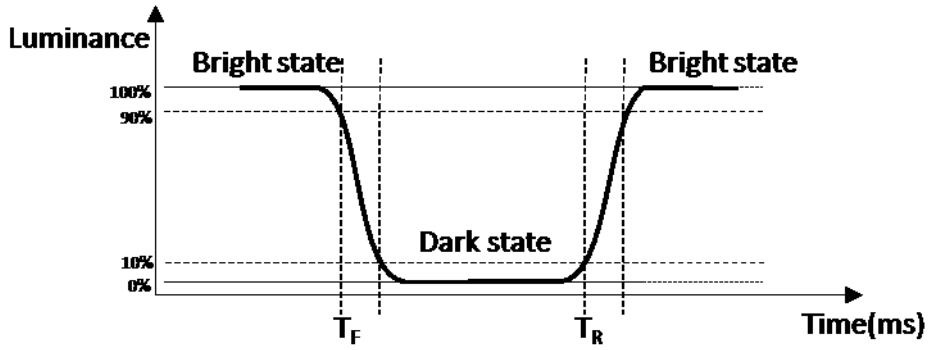


Fig 4.3 The definition of TR and TF

Measured response time is determined by 10% to 90% brightness difference of rising (T_R) or falling (T_F) time,

(6) Definition of Viewing angle:

As Note (4) the static contrast ratio definition, the viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the HKC's module (two vertical angles: up θ_y+ and down θ_y-; and two horizontal angles: right θ_x+ and left θ_x-). The contrast ratio is measured by ELDIM EZ-Contrast and the standard setup of measurement is shown in Fig 4.1 & 4.4

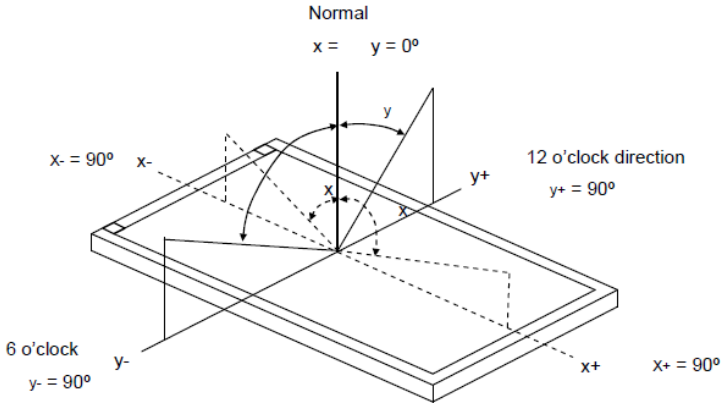
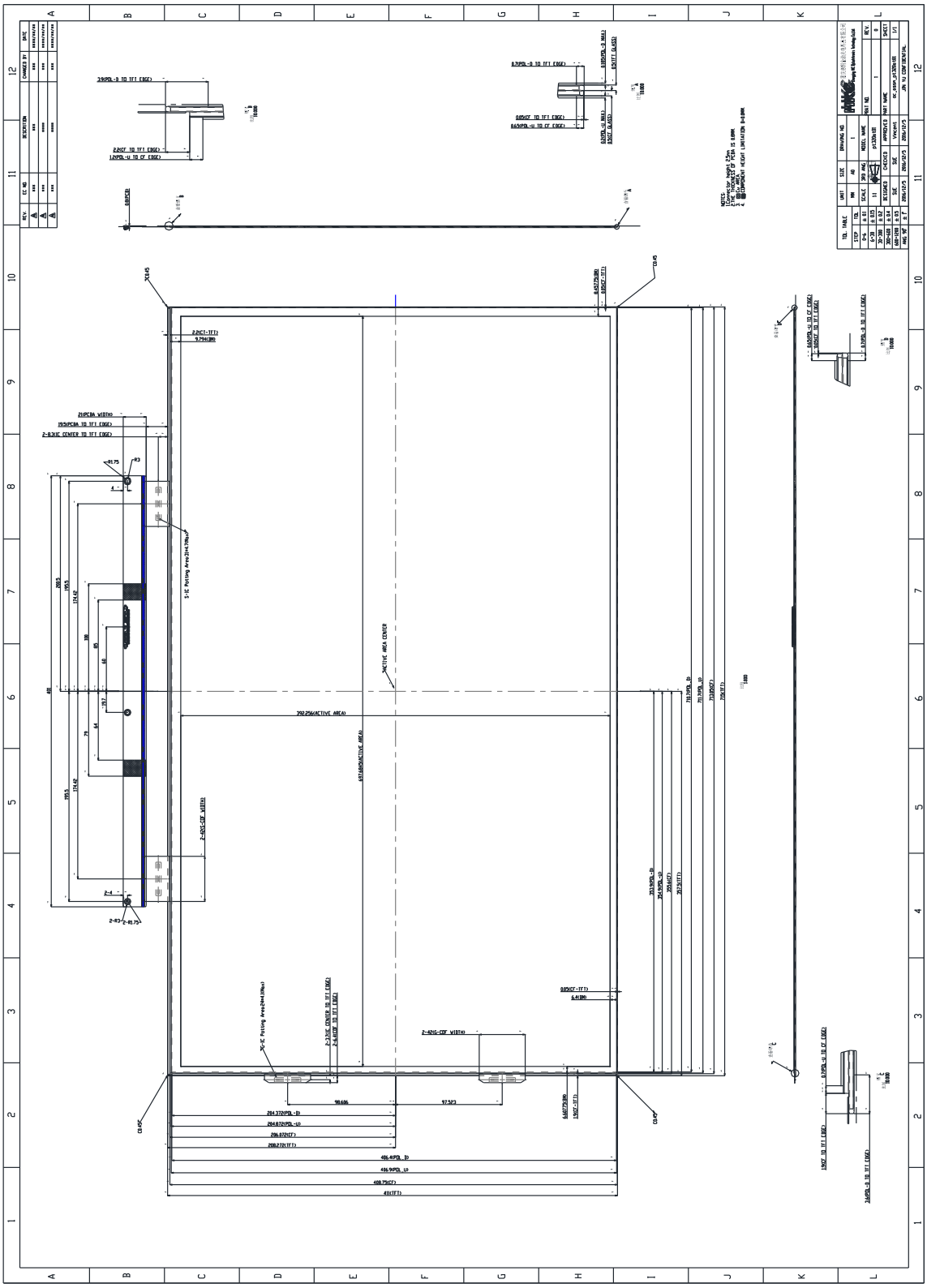


Fig 4.4

5. MECHANICAL CHARACTERISTICS

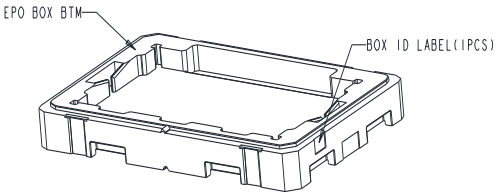
5.1 Mechanical Specification

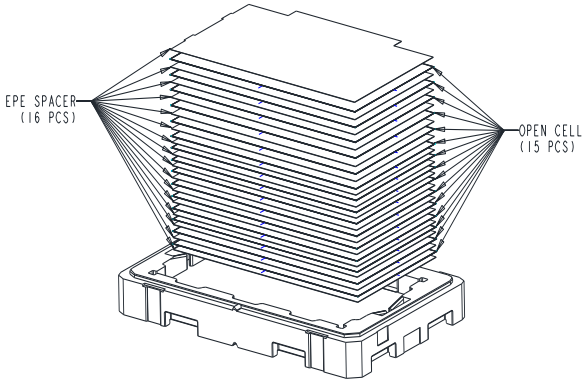


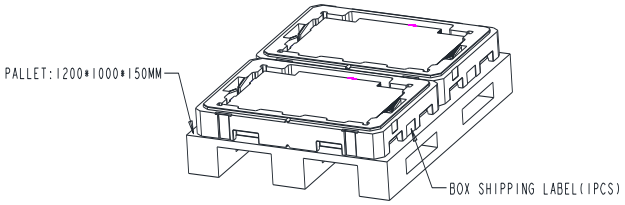
5.2 Packing

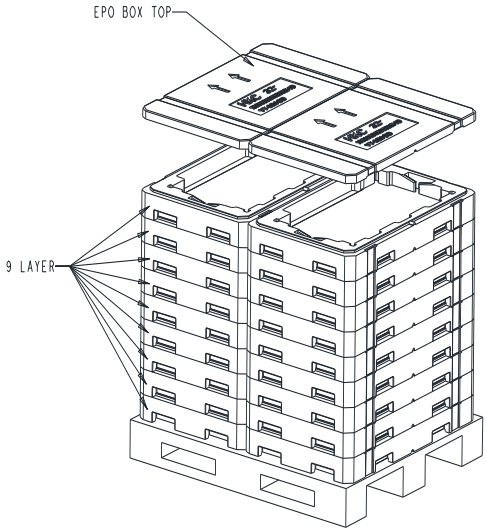
5.2.1 Packing specifications

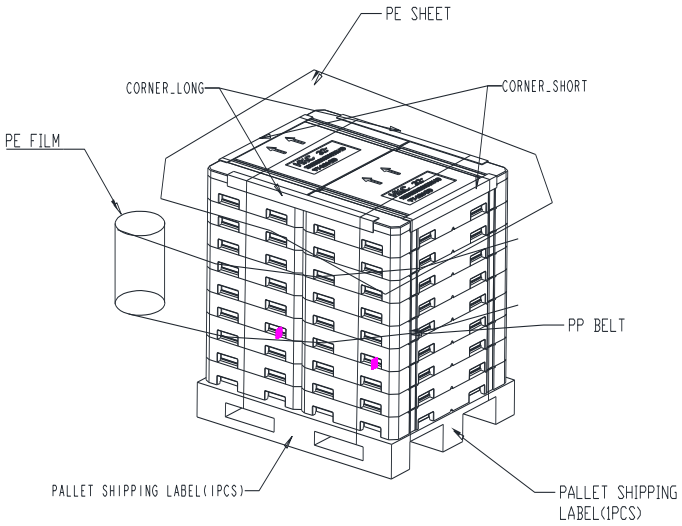
Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	15pcs/box	930 (L) x 590 (W) x 108.5 (H)	Net Weight:14.1 Gross Weight:15.82
Pallet	1	1200(L) x 1000 (W) x 150 (H)	Net Weight:12
Stack Layer	9		
Boxes per Pallet	18		
Pallet after Packing	270pcs/pallet	1200(L) x 1000 (W) x 1074.5 (H)	Gross Weight:304.17

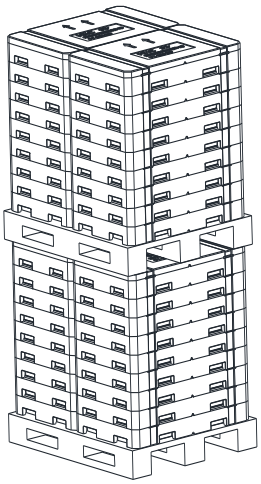












6. DEFINITION OF LABELS

6.1 Open Cell Label

XXXXXXXXXXXXXXXXXXXXX YMDD PT320AT01-1 Ver.X.X

- Ver.X.X → Model Version Code
- PT320AT01-1 → Model Name
- YMDD → Manufactured Date
- XXXXXXXXXXXXXXXXXXXXX → Serial Number

Serial Number: XXXXXXXXXXXX XXXXXXXXX

- XXXXXXXXXXXX → Panel ID
- XXXXXXXXX → HKC Internal Use

Manufactured Date: Y M DD

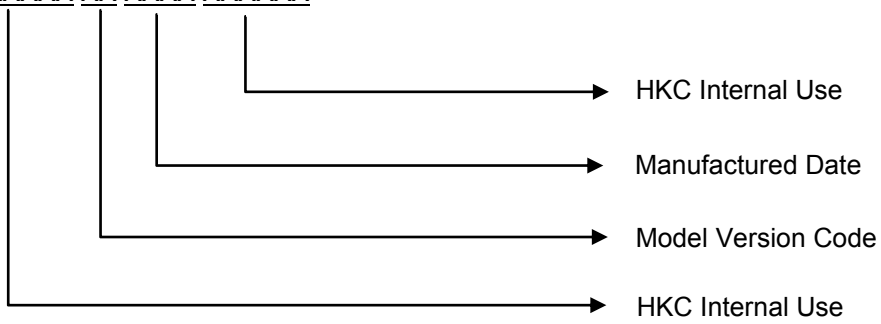
- DD → Date: 01~31
- M → Month: 1~9, A~C, for Jan.~Dec
- Y → Year: 2017=7, 2018=8, 2020=0……

Model Name: PT320AT01-1

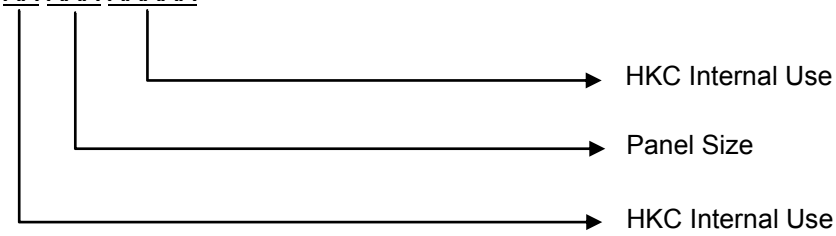
Model Version Code: Ver.X.X, for example: 0.0,0.1…,1.0,1.1….,2.0,2.1……

6.2 Carton Label

Serial Number: XXXXXXXX XX XXXX XXXXXX



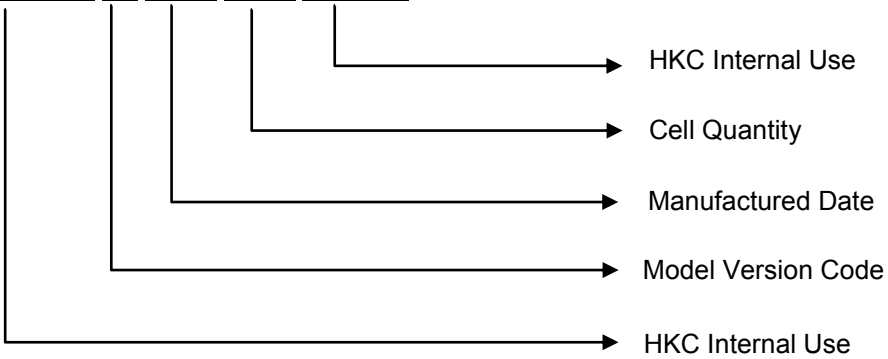
Box ID: XX XXX XXXXX



Model Version Code: Ver.X.X, for example: 0.0,0.1…,1.0,1.1….,2.0,2.1……

6.3 Pallet Label

Serial Number: XXXXXXXX XX XXXX XXXX XXXXXX



Pallet ID: XXXXXXXX

7. PRECAUTION

Please pay attention to the followings when a TFT-LCD cell is used, handled and mounted.

7.1 Unpacking

Should use immediately after unpacking TFT -LCD cell to prevent the terminal corrosion.

Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

Source PCB should be connected to the ground when peel off the protection film.

The protection film should not be contacted to the driver during peeling off.