GENERAL DESCRIPTION

The PT2209 is a highly integrated current mode PWM controller， providing low standby power and cost effective system solution for the flyback converter applications.

The PT2209 operates at fixed 65kHz frequency. Under no load or light load conditions, PWM frequency is reduced to minimize switching loss, low standby power and high efficiency is thus achieved. The PT2209 also features low VDD startup current which also contributes to low standby power. The built in LEB on the current sense input removes the signal glitches due to snubber circuit diode reverse recovery and thus reduces the external component count and the system cost in the design.

A complete set protection is implemented in the PT2209 including cycle-by-cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). The PT2209 also features latched shut down including programmable OTP and programmable OVP protection. By limiting the minimum frequency above 22 kHz, the PT2209 based system eliminates the potential audible noise when the system works under light or no load conditions.

Excellent EMI performance is achieved with PowTech proprietary frequency Jittering technique together with soft driving control at totem pole gate drive output.

The PT2209 is available in an SOT23-6 package.

FEATURES

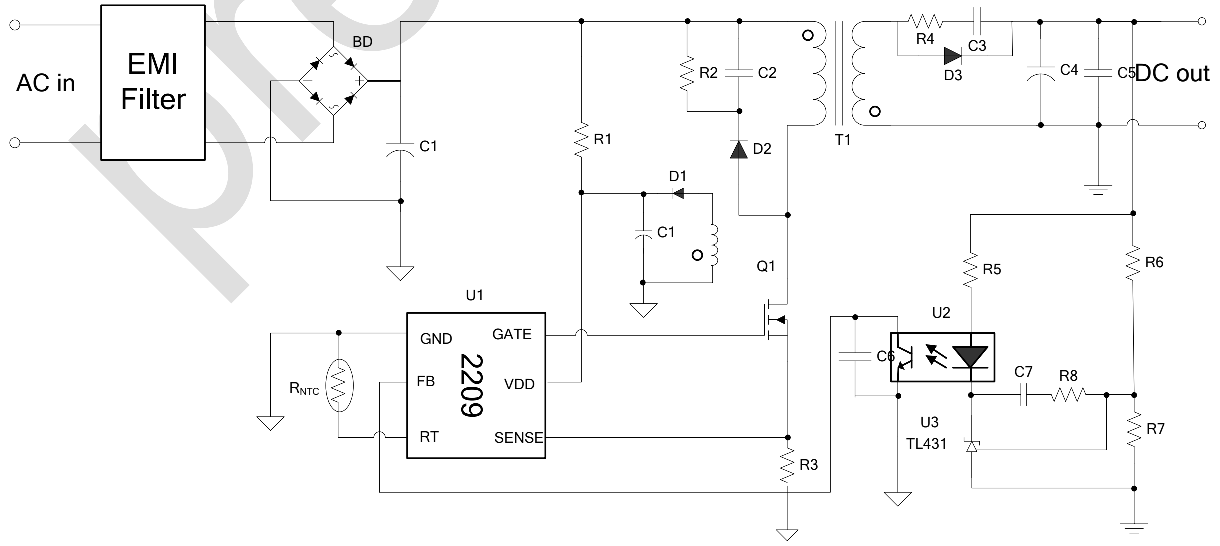
- Frequency jittering for improved EMI
- Green-Mode PWM for improved efficiency and minimum standby power design
- Fixed 65kHz PWM frequency
- Built in 4mS soft start
- Low start up current 20uA (Typ. 3μA) and low operation current (Typ. 1.8mA)
- Current mode operation
- Leading-edge blanking on current sense input
- Constant output power limit for universal AC input
- Built-in power limit control (OLP)
- Cycle-by-cycle current limiting (OCP)
- Under voltage lockout (UVLO)
- Latched programmable OTP
- Latched programmable OVP

APPLICATIONS

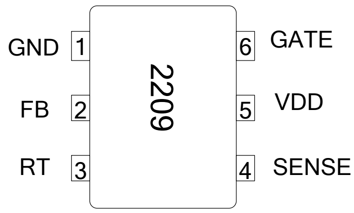
Offline AC/DC flyback converters for

- Power Adapter
- Open-frame SMPS
- Battery Charger Adapter
- HB LED lighting.

TYPICAL APPLICATIONS



PIN ASSIGNMENT



SOT23-6

PIN DESCRIPTIONS

NAMES	PIN No.	DESCRIPTION
GND	1	Ground
FB	2	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and SENSE pin voltage level.
RT	3	Multi-function pin. Connects a NTC resistor between RT and GND for ambient temperature OTP or connect a Zener diode to VDD for over voltage protection.
SENSE	4	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	5	DC power supply pin.
GATE	6	Totem-pole gate drive output for power MOSFET.

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
SOT23-6, Pb free	-40°C to 85°C	PT2209E23F	3000/Tape and Reel	2209

ABSOLUTE MAXIMUM RATINGS(note1)

SYM	PARAMETER	VALUE	UNIT
V_{DD}	V_{DD} DC Supply Voltage	35	V
$I_{DD\ -Clamp}$	V_{DD} DC Clamp Current	10	mA
$V_{I/O}$	Other I/O PIN Input Voltage	-0.3~7	V
T_J	Min/Max Operating Junction Temperature T_J	-40~150	℃
T_{STG}	Storage Temperature Range	-55~160	℃
HBM	ESD Capability, HBM model(note 2)	2.0	kV

PACKAGE DISSIPATION RATING

SYM	PARAMETER	VALUE	UNIT
$R_{\Theta JA}$	SOT23-6	250	℃/W

OPERATING RANGE

SYM	PARAMETER	VALUE	UNIT
V_{DD}	V_{DD} Supply Voltage	10~23.5	V
T_A	Operating Ambient Temperature	-20~85	℃

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS

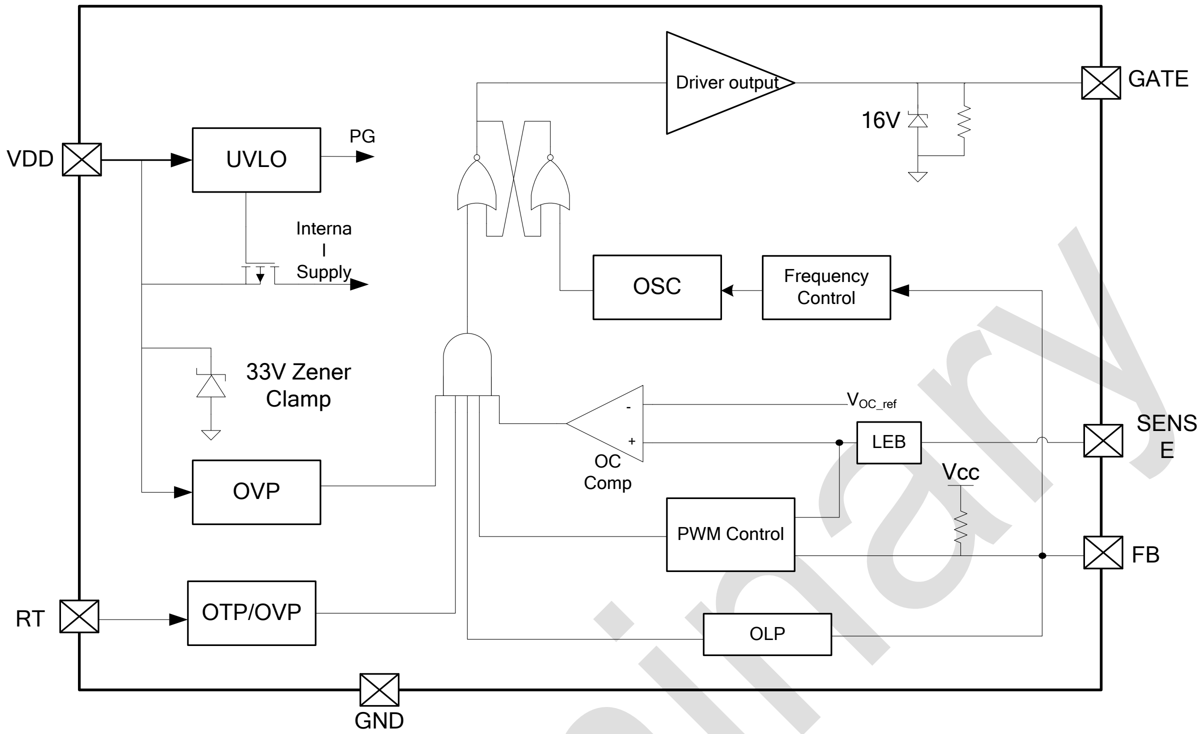
(T_{OPT}=25℃, VDD=16V，unless specified otherwise)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VDD)						
V_{DD_ON}	V_{DD} Start-up voltage	V_{DD} rising	13.5	15	16.5	V
V_{DD_MIN}	V_{DD} minimum operating level	V_{DD} falling	7.5	8.5	9.5	V
V_{DD_LATCH}	V_{DD} Latch release voltage			5		V
V_{DD_OVP}	V_{DD} Over Voltage Protection Level	V_{DD} rising	24.0	26.0	28.0	V
V_{ZENER}	V_{DD} Pin Zener Diode Clamp Voltage	$I(V_{DD})$=10mA		33		V
Current Into VDD						
I_{VDD_START}	V_{DD} Start-up Current	V_{DD}=12.0V Measuring Current into V_{DD}		3	20	μA
I_{VDD_OPER}	V_{DD} Operating Current	V_{FB}=3V, CS=0V, C_{GATE}=1nF		1.8		mA
FEED BACK PIN (FB)						
V_{OFB}	V_{FB} Open Loop Voltage	V_{DD}=16V,		4.8		V
V_{PL}	FB Over Load Protection level			3.7		V
V_{GM}	Green Mode FB Threshold			2.0		V
V_{BM}	Burst Mode Entering Threshold			0.80		V
V_{ZD}	Zero Duty Cycle FB Threshold			0.70		V
T_{PL_DELAY}	Over Load Protection Delay Time			88		ms
Z_{FB}	FB Pin Input Impendence			12.0		kΩ
I_{FB}	FB Pin Supply Current	FB Short To GND, Measuring Current Flowing From FB Pin		0.4		mA
OSCILLATOR (OSC)						
F_{osc}	Oscillator Frequency		60	65	70	kHz
$\triangle F_{JIT}$	△Fosc/Fosc		-3		3	%
F_{MIN}	Minimum PWM Frequency			22		kHz
F_{DT}	Oscillator Frequency Stability At Different Temperature	-20°C ~100°C		2		%
F_{DV}	Oscillator Frequency Stability At Different VDD Input Level	V_{DD}=12~23V		2		%

ELECTRICAL CHARACTERISTICS (CONTINUE)

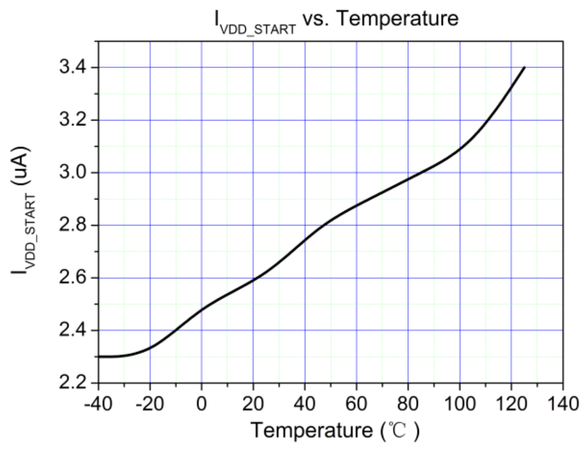
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PWM SECTION						
A_V	PWM Input GAIN	$\triangle V_{FB}/\triangle V_{CS}$		2.0		V/V
T_{BLK}	Leading Edge Blanking Time			300		ns
D_{MAX}	PWM Maximum Duty Cycle			75		%
D_{MIN}	PWM Minimum Duty Cycle				0	%
CURRENT SENSE INPUT (SENSE)						
Z_{CS}	SENSE Input Impendence			40		kΩ
V_{TH_OC}	OCP Threshold at Duty=0	FB=3V, V_{GATE}<0.3V	0.65	0.70	0.75	V
T_{OC_DELAY}	Delay Time From OCP to Gate Output OFF	V_{DD}=16V, CS>V_{TH}_OC , C_{GATE}=1000pF		120		nS
T_{SST}	Soft start time			4		mS
GATE OUTPUT						
V_{OL}	GATE Output Low Level	V_{DD}=14V, Io=-5mA			1	V
V_{OH}	GATE Output High Level	V_{DD}=14V, Io=20mA	6			V
I_{SOURCE}	GATE Source Current	V_{GS}=12V		250		mA
I_{SINK}	GATE Sink Current	V_{GS}=12V		500		mA
V_{GMAX}	GATE Output Clamp Voltage			16		V
PROTECTION						
I_{RT}	RT pin pull up current		95	100	105	μA
V_{OTP}	RT pin OTP threshold		0.95	1	1.05	V
T_{D_OTP}	OTP debounce time			32		cycles
$V_{\_RT}$	RT pin floating voltage			2.3		V
V_{OV}	RT pin OVP threshold			4		V

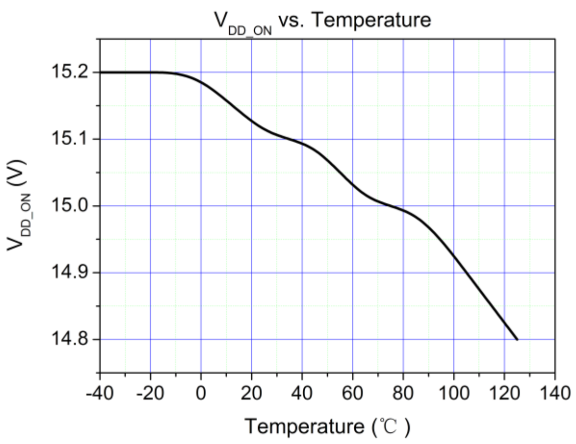
SIMPLIFIED BLOCK DIAGRAM

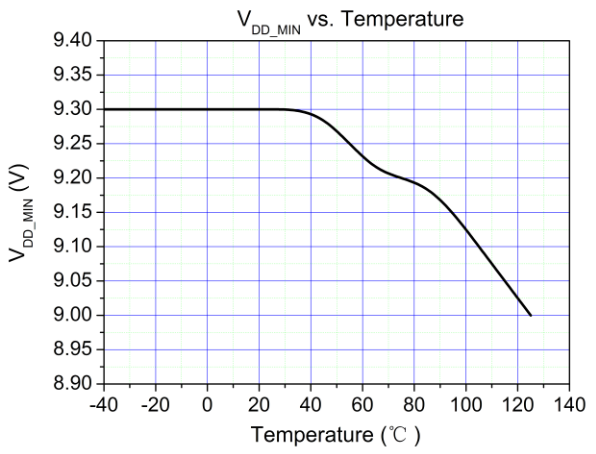


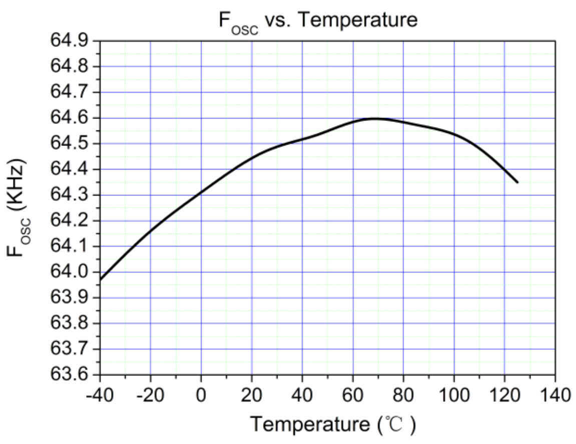
TYPICAL PERFORMANCE CHARACTERISTICS

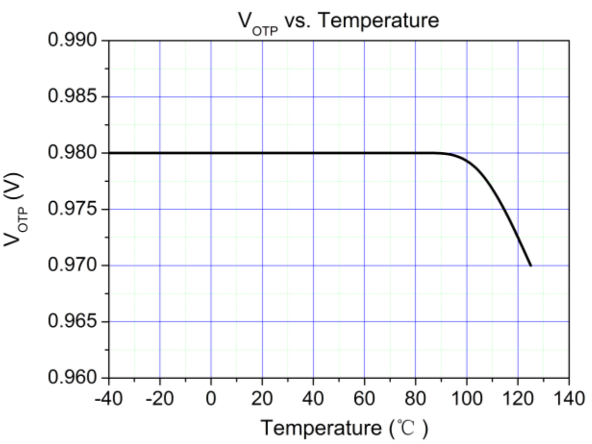
（VDD=16V unless specified otherwise）

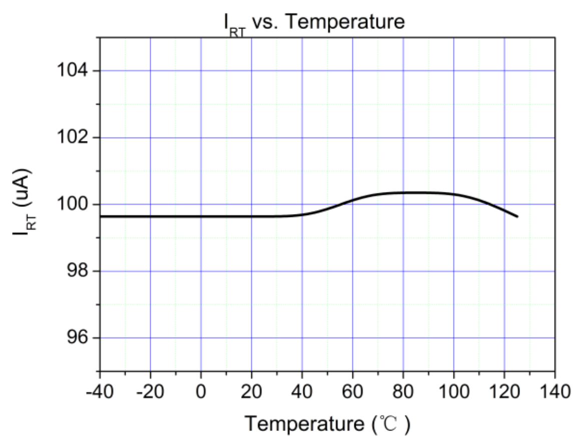












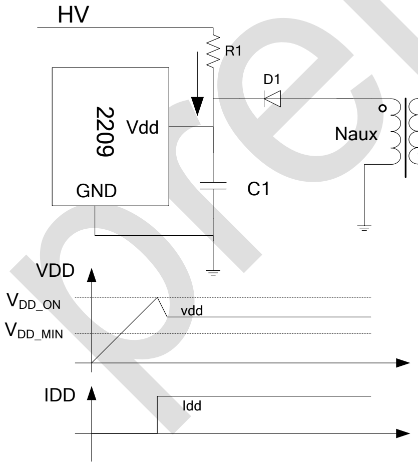
OPERATION DESCRIPTION

With enhanced functions and extremely low start up current and low operating current together with optimized controlling mode, the PT2209 is easy to meet the high performance as well as low standby power requirement in the SMPS application. Its detail features are described as below:

STARTUP AND UVLO:

The start up of the PT2209 is realized through the current provided by a resistor connecting to HV line, which charges the capacitor connecting to VDD pin to the start up threshold voltage. As shown below, initially the voltage on C_1 is below the start up threshold and the PT2209 stays in the UVLO state. As the current supplied by R_1 charges up the C_1 to V_{DD_ON}, the PT2209 starts to deliver drive signal at the GATE pin and the operating current is supplied by the auxiliary winding of the transformer.

Since the PT2209 sinks a few macro amperes of current before start up, a large start up resistor could be used in the start up circuit to minimize standby power. As for the applications with general AC input range a 2 Mohm 1/8W resistor and a 10uF/50V capacitor compose a simple and reliable start up circuit.

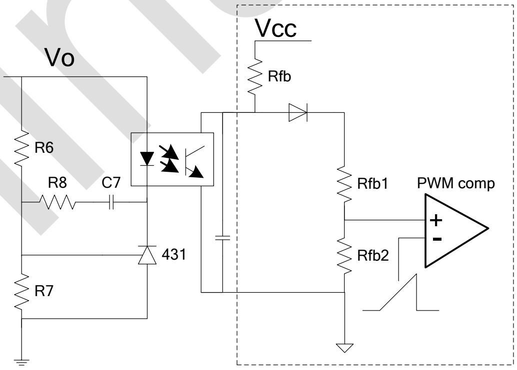


OPERATING CURRENT:

The PT2209 is fabricated with HVCMOS process. The operating current has been reduced to less than 1mA when GATE is floating, thus the system efficiency is improved and in the mean time, a smaller hold up capacitor can be used to speed up start up progress.

FEEDBACK AND PWM ：

The PT2209 adopts a current mode control scheme. The voltage feedback loop is closed by the TL431 and an opto-coupler connected between the output node and FB pin, as shown below: A 2.5V reference is implemented in the TL431. If the divided voltage of R6 and R6 is less than 2.5V, the TL431 sinks current from Vo and the current is transferred to the FB pin through the opto-coupler. The transferred current flows into a resistor connected to the internal regulator output, which forms the FB voltage. The the PWM signal is generated through the PWM comparator.



ENERGY SAVING OPERATION AT LIGHT LOAD:

Typically the SMPS switching loss is proportional to the switching frequency of the power MOSFET. In order to achieve high conversion efficiency when the load decreases, the PT2209 automatically decrease the PWM frequency to reduce the switching loss. The reduction of the load current results in decrease of the voltage on the FB pin. When the voltage on the FB pin is lower than 2.0V, the PWM frequency linearly decreases with V_{FB} until it reaches the 1/3 normal operating frequency. Once the FB pin voltage drops below the preset level, the PT2209 enters the burst mode operation where some PWM cycles are skipped to minimize the switching loss.

OSCILLATOR AND FREQUENCY JITTERING:

The PT2209 integrates a 65 kHz oscillator to generate PWM pulses. A jitter of +/-3% is added to the oscillation frequency so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and helps to ease the system EMI design.

CURRENT SENSE AND LEB:

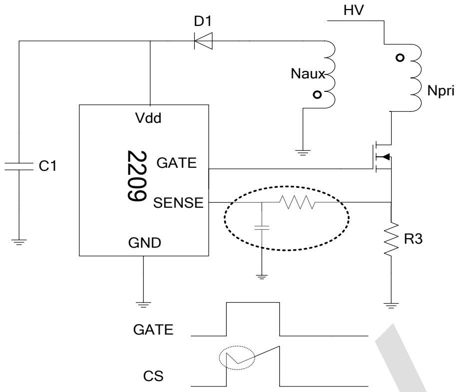
One function of the SENSE pin is sensing the current of the power MOSFET to generate a current slope and the other function is providing cycle by cycle current limit. The current of the power MOSFET is transferred to a voltage signal through a resistor connected between the source terminal and GND, which is then fed into the SENSE input. The voltage on SENSE and FB determines the duty cycle of the PWM signal.

The cycle by cycle current limit works in the following way: At each PWM cycle, when the voltage of the SENSE input excesses the internal threshold, the PWM signal is terminated after a short delay to protect the power MOSFET. The relationship between the OCP threshold and the power MOSFET current follows following expression:

$$I_{OC} = V_{OC} / R_{CS}$$

Where Ioc stands for the power MOSFET current, Voc for the OCP threshold and Rcs for the sensing resistor. The internal OCP threshold varies with the PWM duty cycle, being 0.70V at zero PWM duty cycle.

A spike is inevitable on the sensed signal on Rcs at the instance when the power MOSFET is turned on due to recovery time of the secondary rectifier and the snubber circuit. The LEB is implemented in the PT2209 eliminate the effect of this spike. During the LEB time, the OCP comparator is disabled. So the PWM signal will not be falsely terminated by the spikes on the sensed signal and therefore the external RC filter can be removed.



INTERNAL SLOPE COMPENSATION:

To eliminate the potential sub-harmonic oscillation problem when the duty cycle excesses 0.5, the slope compensation is implemented in the PT2209. At each PWM duty cycle a constant slope is added to the sensed current ramp so that the system stability is guaranteed.

UNIVERSAL INPUT OCP COMPENSATION:

Because there is always a constant delay time Td from OCP is triggered to the power MOSFET is turned off, the actual current when the MOSFET is turned off is different from the preset OCP value. Taking the delay time of Td into consideration, the actual current can be derived as:

$$I_{PEAK} = I_{PEAK1} + I_{SLOP1} \times Td$$

$$I_{SLOP1} = V_{INDC} / Lpri$$

With a higher input level the actual OCP current is:

$$I_{PEAK} = I_{PEAK2} + I_{SLOP2} \times Td$$

$$I_{SLOP2} = V_{INDC} / Lpri$$

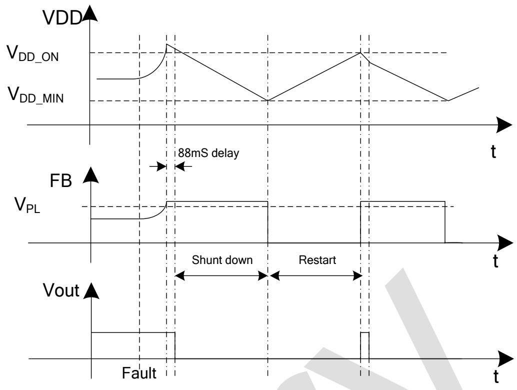
Where Lpri represents the primary winding inductance of the transformer; Td is a constant delay time that does not vary with Vin. From above equations it can be derived that the actual OCP threshold of the power MOSFET is always greater than the preset value due to the OCP delay time. Also this difference increases with Vin going higher. In order to compensate the difference, the OCP threshold in the PT2209 is designed to vary with the duty cycle. It works in a way that a smaller duty cycle results in a smaller OCP threshold. When the input AC voltage increases, the duty cycle gets small and the OCP point decreases. Thus the actual OCP threshold of the power MOSFET maintains unchanged in the universal input range.

VDD OVER VOLTAGE PROTECTION:

When open loop occurs, the opto-coupler does not sink current, which causes the voltage at the FB pin to rise and the current limit will be triggered. If the load is not large enough, the output voltage will increase because power keeps being delivered to the load. Under this condition, if the OLP is not triggered, the output voltage will keep going up and the load is in danger of over voltage damage. Because the voltage on the auxiliary winding is proportional to the output voltage, the VDD rises with the output. When the voltage on VDD reaches the OVP threshold the PT2209 stops delivering PWM signal to the power MOSFET.

OVER LOAD PROTECTION:

The Over Load Protection function (OLP) provides another protection to the system from short load and over load damages. If a short load or over load occurs, the voltage at the FB pin rises. When V_{FB} reaches 3.7V, an internal timer is started to provide a delay time T_{PL_DELAY}. If the fault condition still exists after the delay, the PWM signal is blocked. VDD will then drops due to internal power consumption. When VDD drops below the V_{DD_MIN} threshold, the PT2209 will be completely shut down. When this happens, the start up sequence will kick in and VDD is charging up again.



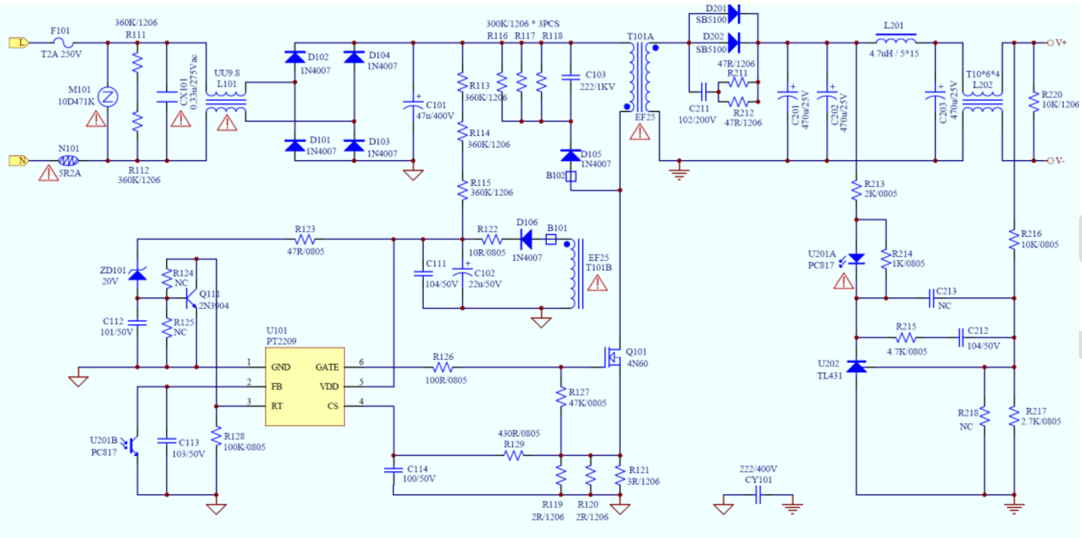
OTP&OVP PROTECTION:

Once OTP or OVP is triggered, the PT2209 enters the latched shut down mode. The control circuit keeps the power MOSFET shut down until VDD drops below the VDD latch release threshold and then the PT2209 will be restarted.

GATE OUTPUT:

The output drives the GATE of the power MOSFET. The optimized totem-pole type driver offers a good tradeoff between the driving capability and EMI. Additionally the output high level is clamped to 16V by an internal clamp to protect the power MOSFET from undesired gate over voltage. A resistor between GATE and GND pulls down the gate voltage to zero at the off state.

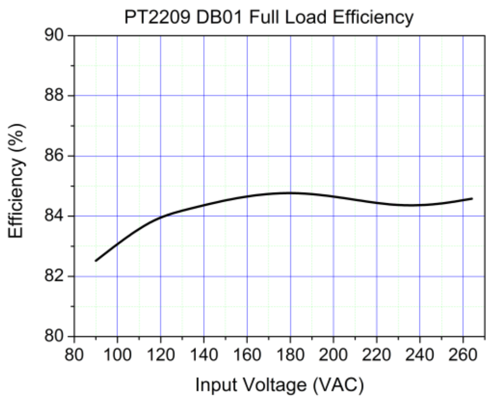
TYPICAL 12V/2A APPLICATIONS CIRCUIT:



Full Load Efficiency

Vin=230Vac,Vout=12V,Iout=2A(CC load)

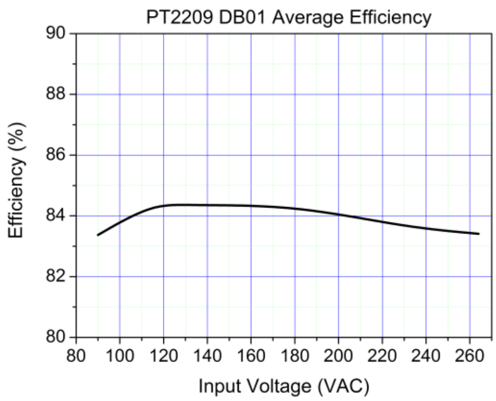
Test at PCB Side



Full Load Efficiency

Vin=230Vac,Vout=12V

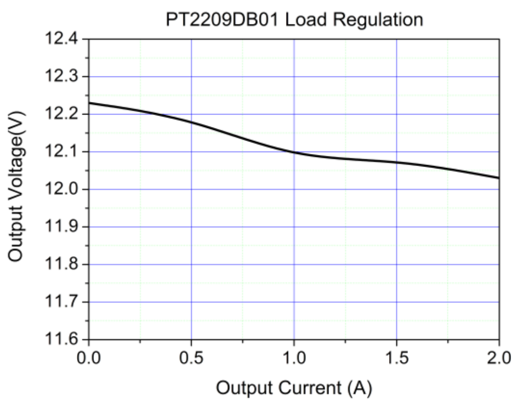
Test at PCB Side



Load regulation

Vin=230Vac,Vout=12V,

Output cord=20#AWG(1.5m)



Startup Waveform

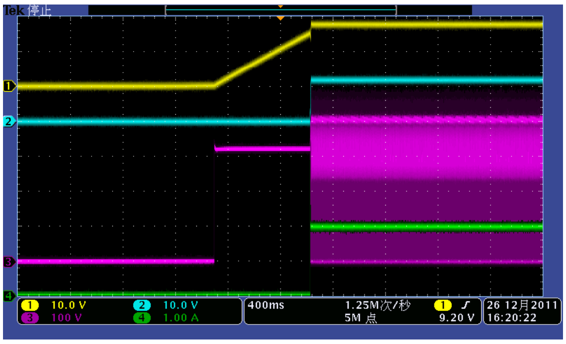
Vin=230Vac,Vout=12V,Iout=2A(CC load)

Probe 1. VCC voltage(Yellow)

Probe 2. Output voltage(Blue)

Probe 3. MOSFET Drain voltage(Pink)

Probe 4. Output current(Green)



Light Load Operation Waveform

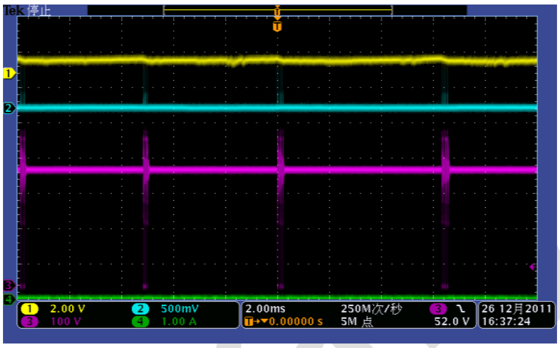
Vin=230Vac,Vout=12V,Iout=0A(CC load)

Probe 1. FB voltage(Yellow)

Probe 2. CS voltage(Blue)

Probe 3. MOSFET Drain voltage(Pink)

Probe 4. Output current(Green)



Heavy Load Operation Waveform

Vin=230Vac,Vout=12V,Iout=0A(CC load)

Probe 1. FB voltage(Yellow)

Probe 2. CS voltage(Blue)

Probe 3. MOSFET Drain voltage(Pink)

Probe 4. Output current(Green)

Shutdown Waveform

Vin=230Vac,Vout=12V,Iout=2A(CC load)

Probe 1. VCC voltage(Yellow)

Probe 2. Output voltage(Blue)

Probe 3. MOSFET Drain voltage(Pink)

Probe 4. Output current(Green)

Medium Load Operation Waveform

Vin=230Vac,Vout=12V,Iout=1A(CC load)

Probe 1. FB voltage(Yellow)

Probe 2. CS voltage(Blue)

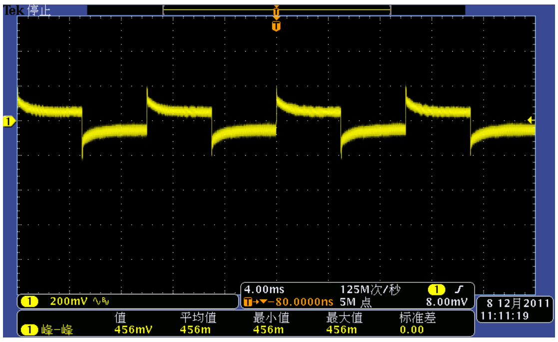
Probe 3. MOSFET Drain voltage(Pink)

Probe 4. Output current(Green)

Load Transient Waveform

Vin=230Vac,Vout=12V,Iout=0.5A to 1.5A(CC load)

Probe 1. Output voltage(Yellow)

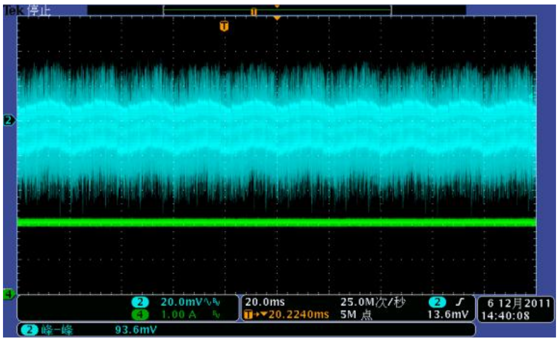


Ripple and Noise Waveform

Vin=230Vac,Vout=12V,Iout=2A(CC load)

Probe 2. Ripple and Noise (Blue)

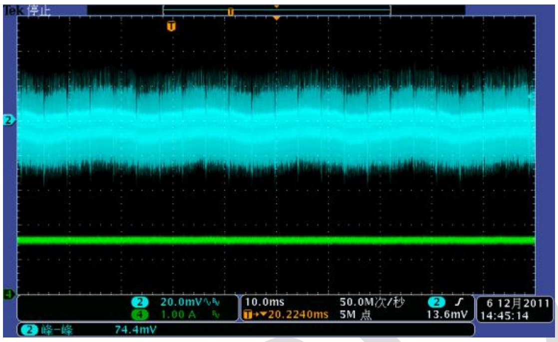
Probe 4. Output current(Green)



Vin=230Vac,Vout=12V,Iout=1.5A(CC load)

Probe 2. Ripple and Noise (Blue)

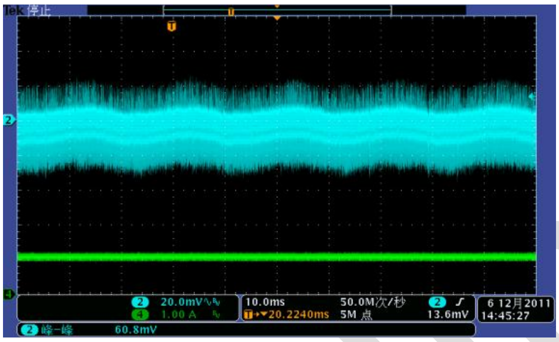
Probe 4. Output current(Green)



Vin=230Vac,Vout=12V,Iout=1A(CC load)

Probe 2. Ripple and Noise (Blue)

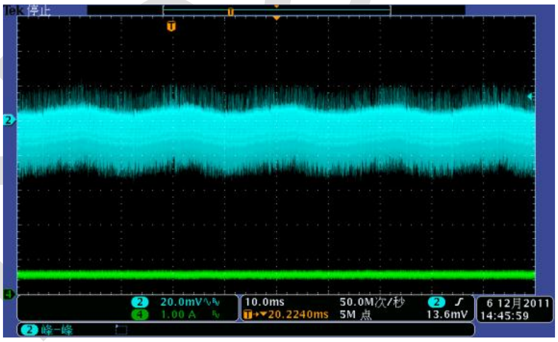
Probe 4. Output current(Green)



Vin=230Vac,Vout=12V,Iout=0.5A(CC load)

Probe 2. Ripple and Noise (Blue)

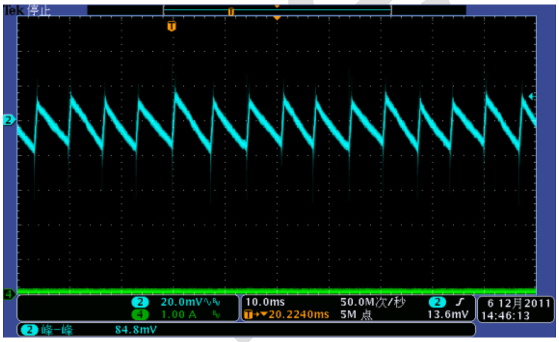
Probe 4. Output current(Green)



Vin=230Vac,Vout=12V,Iout=0A(CC load)

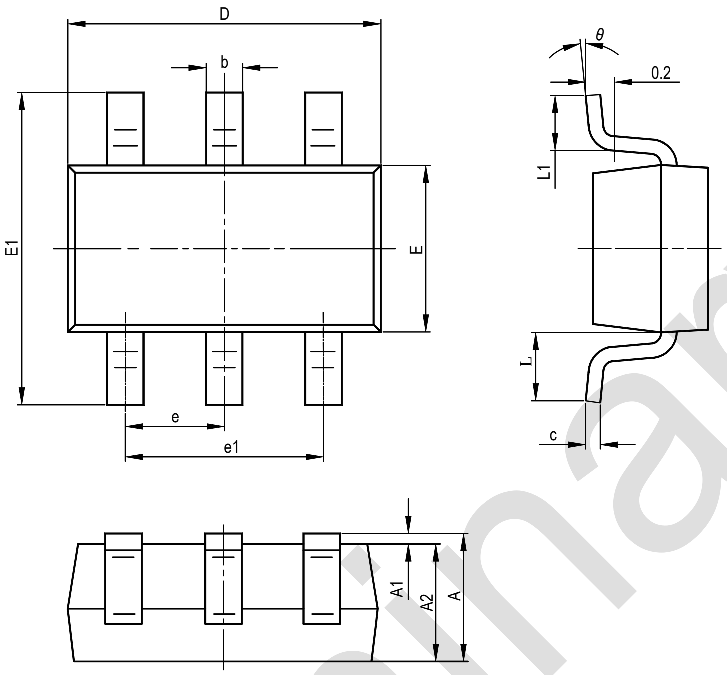
Probe 2. Ripple and Noise (Blue)

Probe 4. Output current(Green)



PACKAGE INFORMATION

SOT23-6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°