

N-channel 30 V 9.8 m Ω logic level MOSFET in LFPAK using NextPower technology

Rev. 2 — 1 September 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, and QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching

Synchronous buck regulator

1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-------------------|----------------------------------|--|-----|------|------|------|
| V _{DS} | drain-source voltage | 25 °C ≤ T _j ≤ 175 °C | - | - | 30 | V |
| I_D | drain current | T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u> | - | - | 44 | Α |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; see <u>Figure 2</u> | - | - | 34 | W |
| T _j | junction temperature | | -55 | - | 175 | °C |
| Static char | acteristics | | | | | |
| R _{DSon} | drain-source on-state resistance | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 12}}{\text{ or } 12}$ | - | 10.3 | 12.1 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_i = 25 \text{ °C}; \text{ see Figure 12}$ | - | 8.3 | 9.8 | mΩ |



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Table 1. Quick reference data ...continued

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|-------------------|--|-----|-----|-----|------|
| Dynamic c | haracteristics | | | | | |
| Q_{GD} | gate-drain charge | V_{GS} = 4.5 V; I_D = 15 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u> | - | 1.6 | - | nC |
| Q _{G(tot)} | total gate charge | V_{GS} = 4.5 V; I_D = 15 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u> | - | 5 | - | nC |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--------------------|----------------|
| 1 | S | source | | _ |
| 2 | S | source | mb | D |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | 1 2 3 4 | mbb076 S |

SOT669 (LFPAK; Power-SO8)

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|------------------|---|---------|
| | Name | Description | Version |
| PSMN9R5-30YLC | LFPAK; Power-SO8 | plastic single-ended surface-mounted package; 4 leads | SOT669 |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|--|--|-----|-----|------|
| V_{DS} | drain-source voltage | 25 °C ≤ T _j ≤ 175 °C | - | 30 | V |
| V_{DGR} | drain-gate voltage | 25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ | - | 30 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I _D | drain current | $V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$ | - | 44 | Α |
| | | V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u> | - | 31 | Α |
| I _{DM} | peak drain current | pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 4 | - | 177 | Α |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; see <u>Figure 2</u> | - | 34 | W |
| T _{stg} | storage temperature | | -55 | 175 | °C |
| Tj | junction temperature | | -55 | 175 | °C |
| T _{sld(M)} | peak soldering temperature | | - | 260 | °C |
| V _{ESD} | electrostatic discharge voltage | MM (JEDEC JESD22-A115) | 150 | - | V |
| Source-drai | n diode | | | | |
| Is | source current | $T_{mb} = 25 ^{\circ}C$ | - | 31 | Α |
| I _{SM} | peak source current | pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$ | - | 177 | Α |
| Avalanche r | ruggedness | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 44 A; $V_{sup} \le 30$ V; R_{GS} = 50 Ω; unclamped; see Figure 3 | - | 9 | mJ |

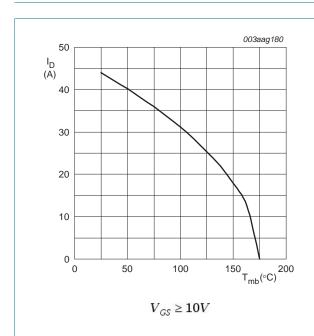
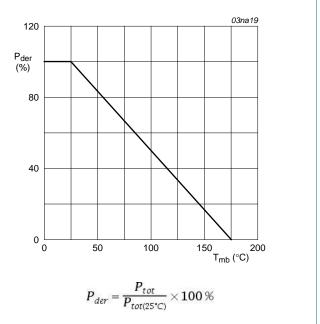


Fig 1. Continuous drain current as a function of mounting base temperature



g 2. Normalized total power dissipation as a function of mounting base temperature

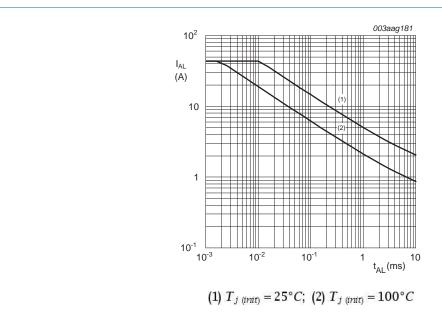
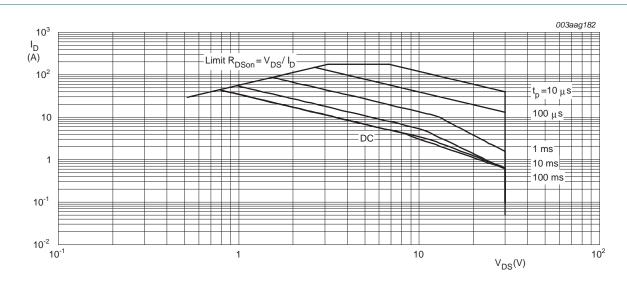


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



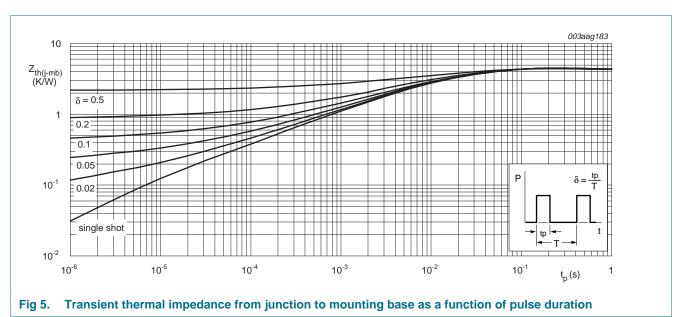
 $T_{mb} = 25$ °C; I_{DM} is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-----------------------|---|--------------|-----|------|------|------|
| R _{th(j-mb)} | thermal resistance from junction to mounting base | see Figure 5 | - | 4.14 | 4.36 | K/W |



6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|------------------------|-----------------------------------|--|------|------|------|------|
| _ | racteristics | | | 7 F | | |
| V _{(BR)DSS} | drain-source breakdown | I _D = 250 μA; V _{GS} = 0 V; T _i = 25 °C | 30 | - | - | V |
| (511)500 | voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 V; T_i = -55 ^{\circ}\text{C}$ | 27 | - | - | V |
| V _{GS(th)} | gate-source threshold voltage | , , , , , , , , , , , , , , , , , , , | 1.05 | 1.66 | 1.95 | V |
| | | $I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_i = 150 \text{ °C}$ | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$ | - | - | 2.25 | V |
| I _{DSS} | drain leakage current | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$ | - | - | 1 | μΑ |
| | | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$ | - | - | 100 | μA |
| I _{GSS} | gate leakage current | V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C | - | - | 100 | nA |
| | | $V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$ | - | - | 100 | nA |
| D0011 | drain-source on-state resistance | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12 | - | 10.3 | 12.1 | mΩ |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 150 ^{\circ}\text{C};$ see Figure 12; see Figure 13 | - | - | 20.3 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12 | - | 8.3 | 9.8 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ °C};$ see Figure 12; see Figure 13 | - | - | 16.5 | mΩ |
| R _G | gate resistance | f = 1 MHz | - | 2.35 | 4.7 | Ω |
| Dynamic o | characteristics | | | | | |
| $Q_{G(tot)}$ | total gate charge | I_D = 15 A; V_{DS} = 15 V; V_{GS} = 10 V; see Figure 14; see Figure 15 | - | 10.4 | - | nC |
| | | I _D = 15 A; V _{DS} = 15 V; V _{GS} = 4.5 V; see <u>Figure 14</u> ; see <u>Figure 15</u> | - | 5 | - | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 10.1 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ | - | 1.6 | - | nC |
| Q _{GS(th)} | pre-threshold gate-source charge | see <u>Figure 14</u> ; see <u>Figure 15</u> | - | 1.1 | - | nC |
| Q _{GS(th-pl)} | post-threshold gate-source charge | | - | 0.5 | - | nC |
| Q_{GD} | gate-drain charge | | - | 1.6 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 15 \text{ A}$; $V_{DS} = 15 \text{ V}$; see <u>Figure 14</u> ; see <u>Figure 15</u> | - | 2.77 | - | V |
| C _{iss} | input capacitance | V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz; | - | 681 | - | рF |
| C _{oss} | output capacitance | T _j = 25 °C; see <u>Figure 16</u> | - | 169 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 50 | - | pF |
| t _{d(on)} | turn-on delay time | $V_{DS} = 15 \text{ V}; R_L = 1 \Omega; V_{GS} = 4.5 \text{ V};$ | - | 13 | - | ns |
| t _r | rise time | $R_{G(ext)} = 4.7 \Omega$ | - | 8.8 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 15 | - | ns |
| t _f | fall time | | - | 4.7 | - | ns |
| | | | | | | |

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 Table 6.
 Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|--------------------|----------------------------|--|-----|------|-----|------|
| Q _{oss} | output charge | $V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$ | - | 4.4 | - | nC |
| Source-drain diode | | | | | | |
| V _{SD} | source-drain voltage | $I_S = 15 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 17 | - | 0.86 | 1.1 | V |
| t _{rr} | reverse recovery time | $I_S = 15 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; | - | 10 | - | ns |
| Q _r | recovered charge | $V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$ | - | 18 | - | nC |
| t _a | reverse recovery rise time | $V_{GS} = 0 \text{ V}; I_S = 15 \text{ A};$ | - | 11 | - | ns |
| t _b | reverse recovery fall time | $dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{DS} = 15 \text{ V};$ see Figure 18 | - | 7 | - | ns |

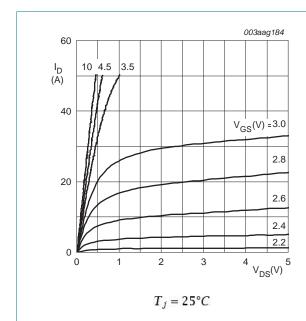
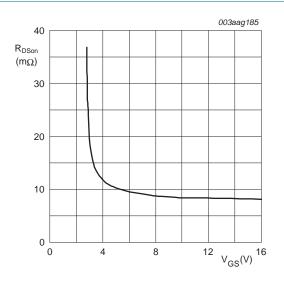


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



 $T_j = 25^{\circ}C; \ I_D = 15A$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

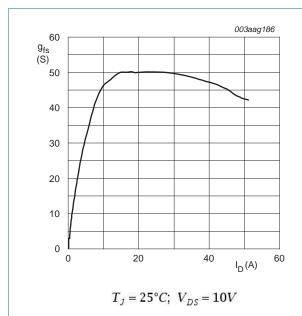
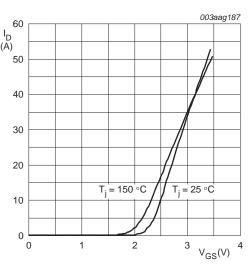


Fig 8. Forward transconductance as a function of drain current; typical values



 $V_{DS} = 10V$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

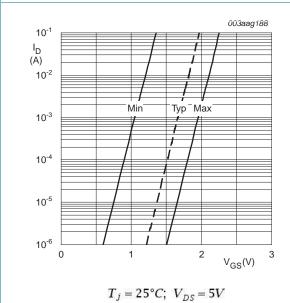


Fig 10. Sub-threshold drain current as a function of gate-source voltage

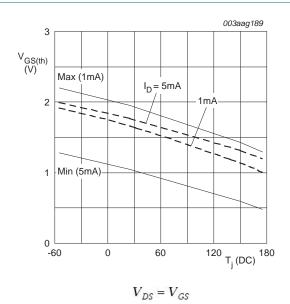


Fig 11. Gate-source threshold voltage as a function of junction temperature

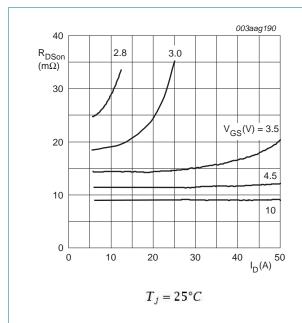


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

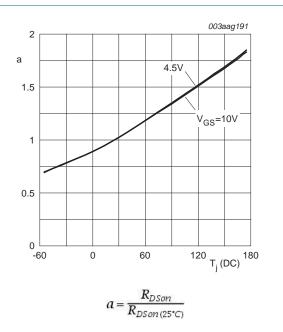


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

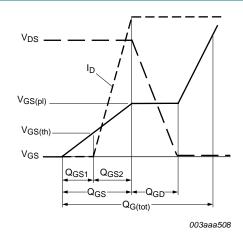
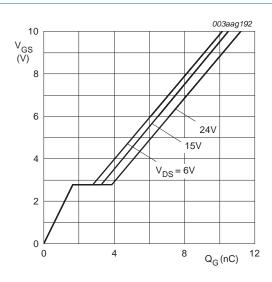
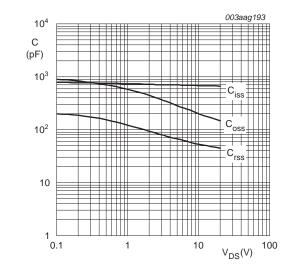


Fig 14. Gate charge waveform definitions



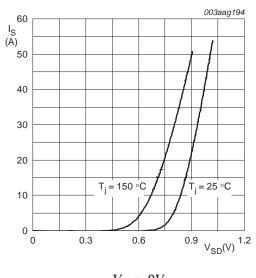
 $T_j = 25^{\circ}C; I_D = 15A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = 0V$

Fig 17. Source current as a function of source-drain voltage; typical values

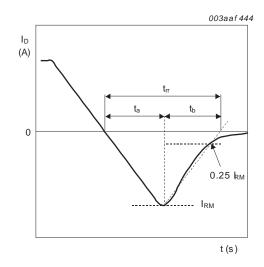
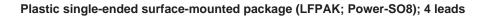


Fig 18. Reverse recovery timing definition

7. Package outline



SOT669

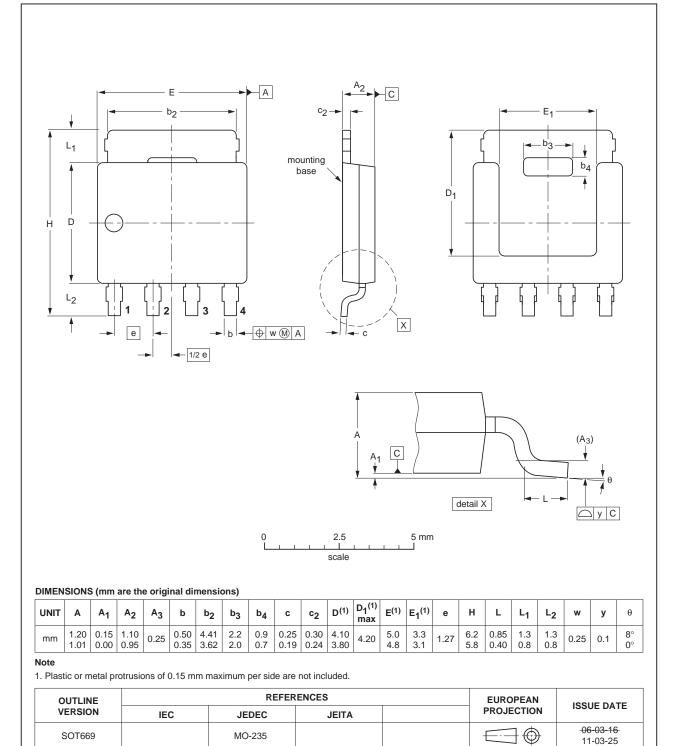


Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

PSMN9R5-30YLC

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8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|--|------------------------|---------------|-------------------|
| PSMN9R5-30YLC v.2 | 20110901 | Product data sheet | - | PSMN9R5-30YLC v.1 |
| Modifications: • Status changed from preliminary to product. | | | | |
| | Various changes to | content. | | |
| PSMN9R5-30YLC v.1 | 20110711 | Preliminary data sheet | - | - |

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9.1 Data sheet status

| Document status [1] [2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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