



# PSMN2R7-30BL

N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

Rev. 1 — 21 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

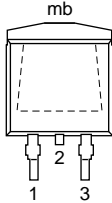
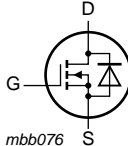
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	30	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	[1]	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	170	W
T <sub>j</sub>	junction temperature		-55	-	175	°C
Static characteristics						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 100 °C; see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	3.6	4.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	2.57	3	mΩ
Dynamic characteristics						
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V	-	8	-	nC
Q <sub>G(tot)</sub>	total gate charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	32	-	nC
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped	-	-	300	mJ

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R7-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R7-30BL	PSMN2R7-30BL

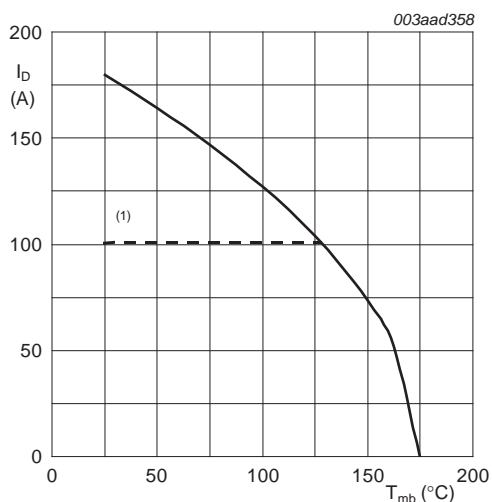
## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

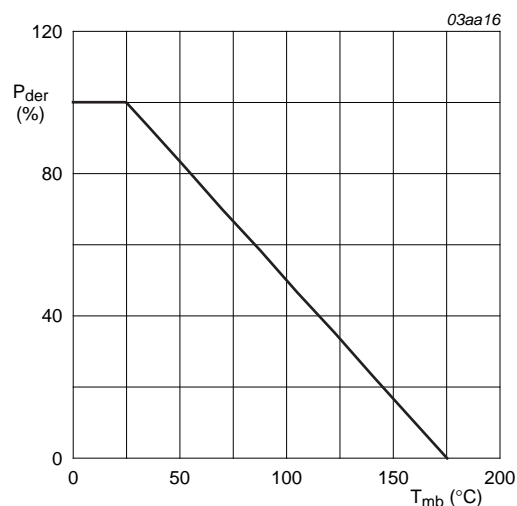
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	30	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	30	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	<a href="#">[1]</a> -	100	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a>	<a href="#">[1]</a> -	100	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	730	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	170	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature		-	260	°C
Source-drain diode					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	<a href="#">[1]</a> -	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	730	A
Avalanche ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped	-	300	mJ

[1] Continuous current is limited by package.



$V_{GS} \geq 10\text{ V}$   
(1) Capped at 100 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

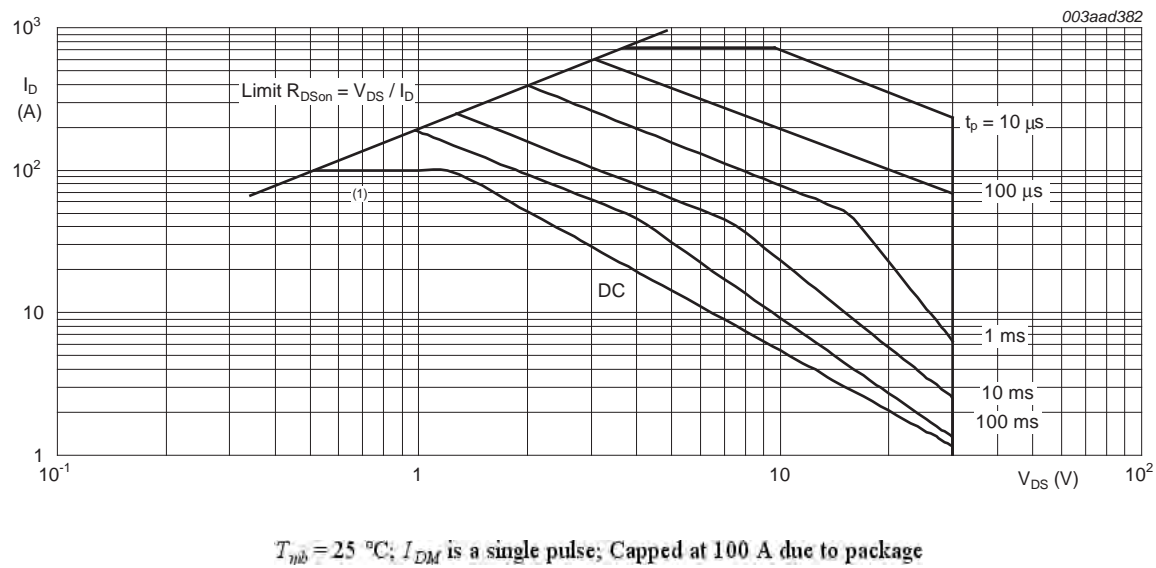
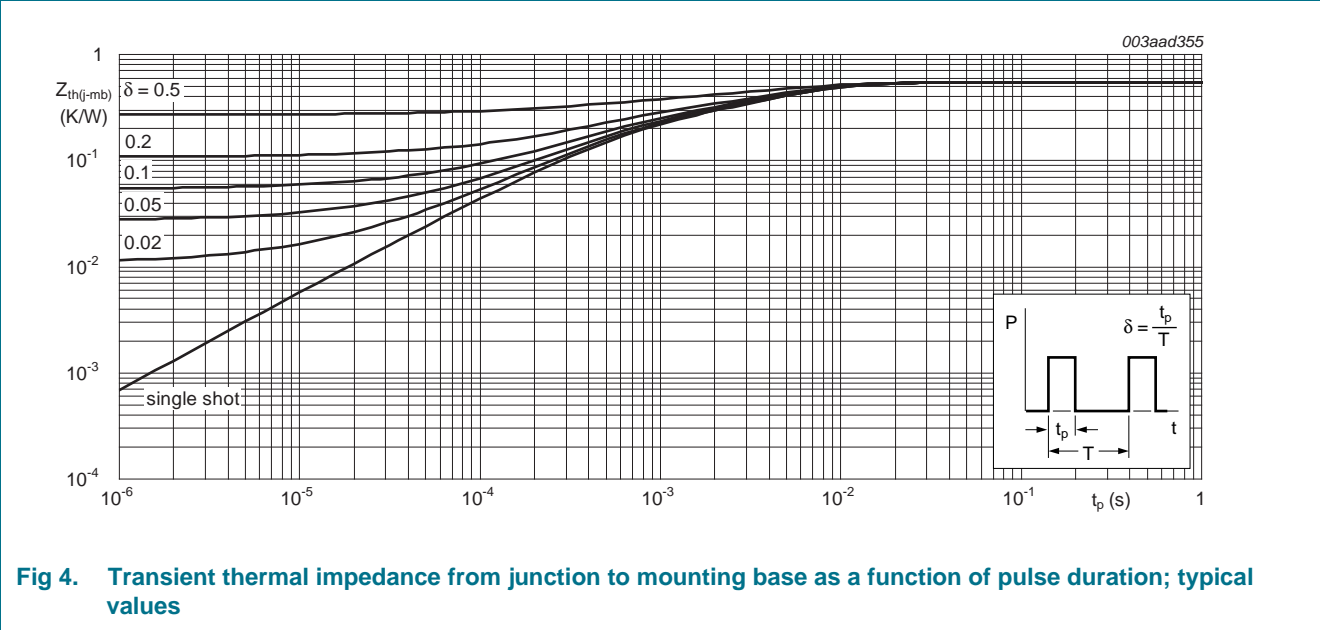


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.54	0.88	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



## 7. Characteristics

**Table 7. Characteristics**

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_j = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_j = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	1.3	1.7	2.15	V
		$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 175\ ^\circ C$ ; see <a href="#">Figure 11</a>	0.5	-	-	V
		$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\ ^\circ C$ ; see <a href="#">Figure 11</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30\ V$ ; $V_{GS} = 0\ V$ ; $T_j = 25\ ^\circ C$	-	0.3	5	$\mu A$
		$V_{DS} = 30\ V$ ; $V_{GS} = 0\ V$ ; $T_j = 125\ ^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16\ V$ ; $V_{DS} = 0\ V$ ; $T_j = 25\ ^\circ C$	-	10	100	nA
		$V_{GS} = -16\ V$ ; $V_{DS} = 0\ V$ ; $T_j = 25\ ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$ ; $I_D = 25\ A$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 12</a>	-	3.16	3.7	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 25\ A$ ; $T_j = 175\ ^\circ C$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	4.88	5.7	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 25\ A$ ; $T_j = 100\ ^\circ C$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	3.6	4.2	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 25\ A$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 12</a>	-	2.57	3	mΩ
$R_G$	gate resistance	$f = 1\ MHz$	-	1	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 10\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	66	-	nC
		$I_D = 0\ A$ ; $V_{DS} = 0\ V$ ; $V_{GS} = 10\ V$	-	60	-	nC
		$I_D = 25\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 4.5\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	32	-	nC
$Q_{GS}$	gate-source charge		-	12	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5.6	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 4.5\ V$	-	8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ A$ ; $V_{DS} = 15\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	2.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15\ V$ ; $V_{GS} = 0\ V$ ; $f = 1\ MHz$ ;	-	3954	-	pF
$C_{oss}$	output capacitance	$T_j = 25\ ^\circ C$ ; see <a href="#">Figure 16</a>	-	822	-	pF
$C_{rss}$	reverse transfer capacitance		-	356	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ V$ ; $R_L = 0.5\ \Omega$ ; $V_{GS} = 4.5\ V$ ; $R_{G(ext)} = 4.7\ \Omega$	-	46	-	ns

Table 7. Characteristics ...continued  
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>r</sub>	rise time	V <sub>DS</sub> = 15 V; R <sub>L</sub> = 0.5 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 4.7 Ω	-	82	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	74	-	ns
t <sub>f</sub>	fall time		-	35	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 17</a>	-	0.7	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;	-	40	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 15 V	-	33	-	nC

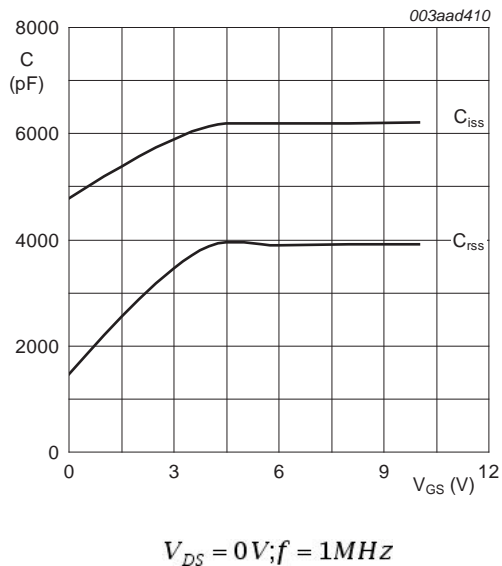


Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

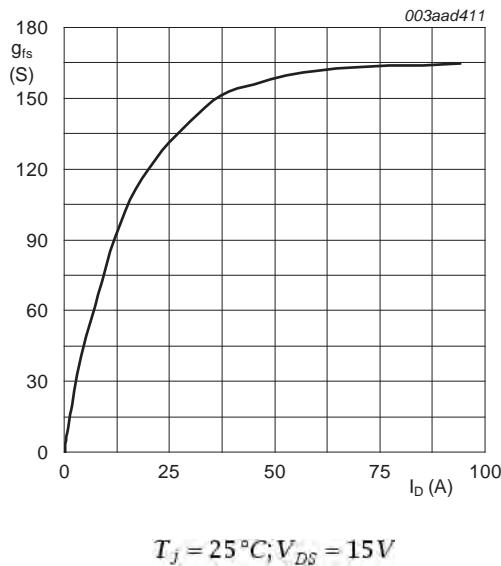
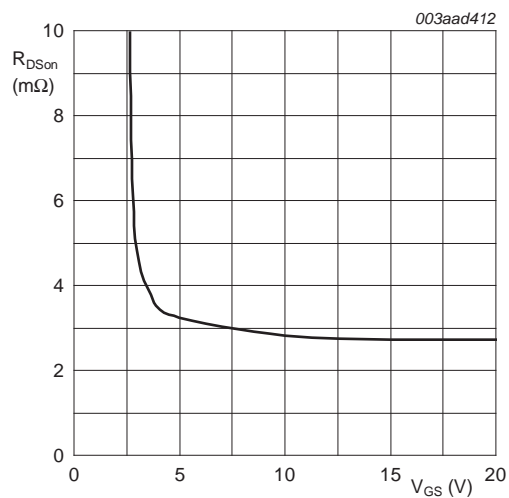
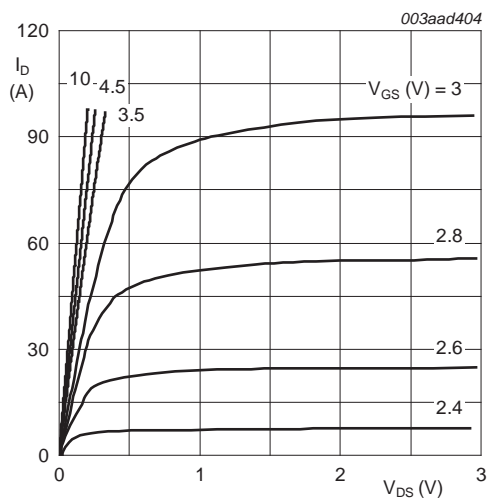


Fig 6. Forward transconductance as a function of drain current; typical values



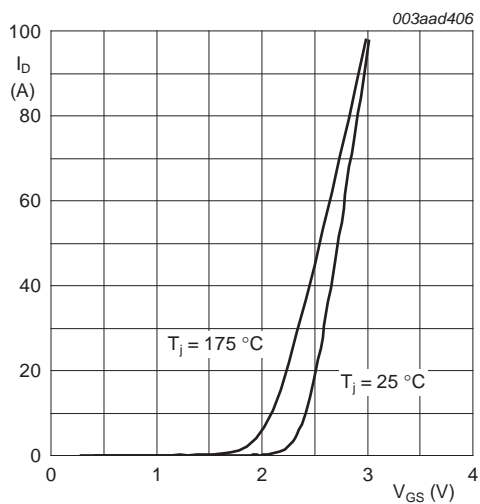
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



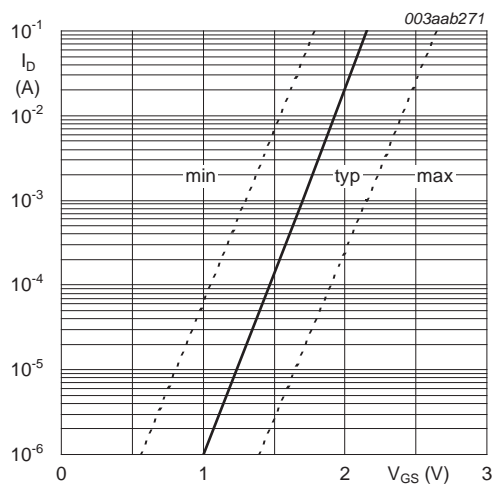
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} > I_D \times R_{DS(on)}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

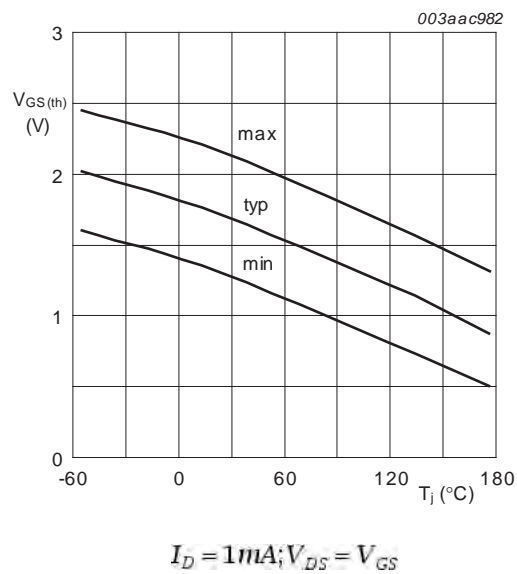


Fig 11. Gate-source threshold voltage as a function of junction temperature

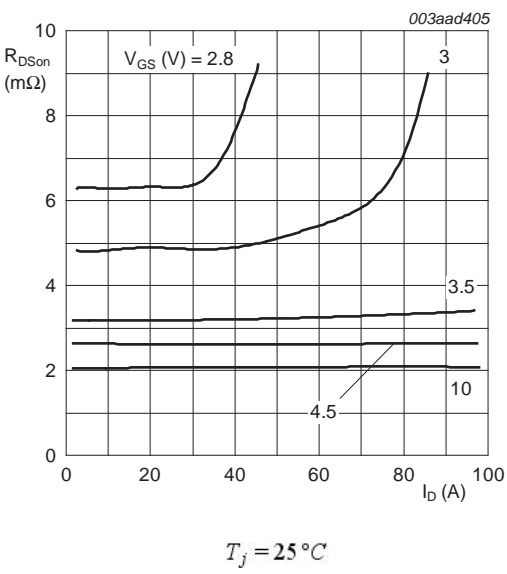


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

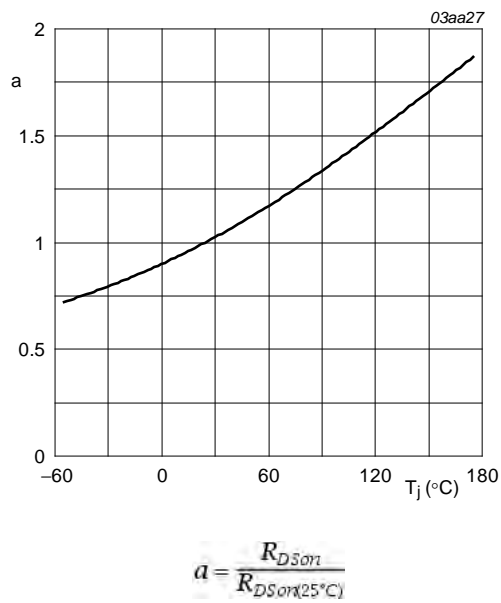


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

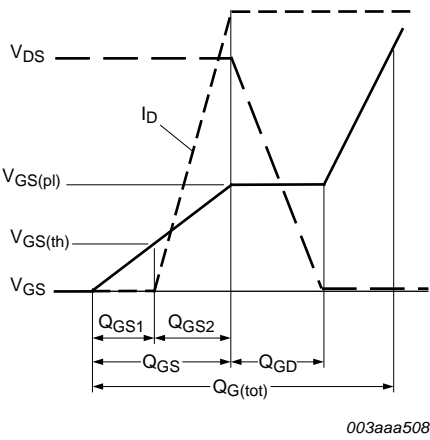
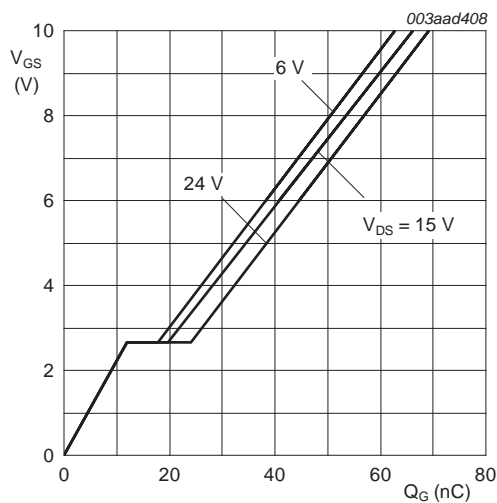
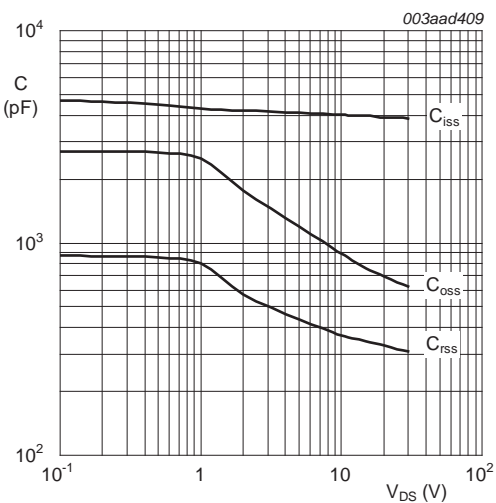


Fig 14. Gate charge waveform definitions



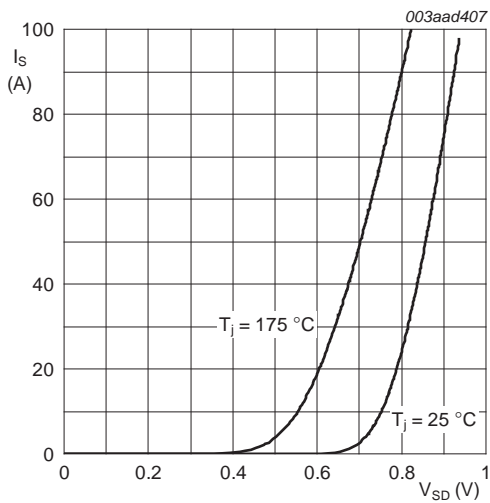
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



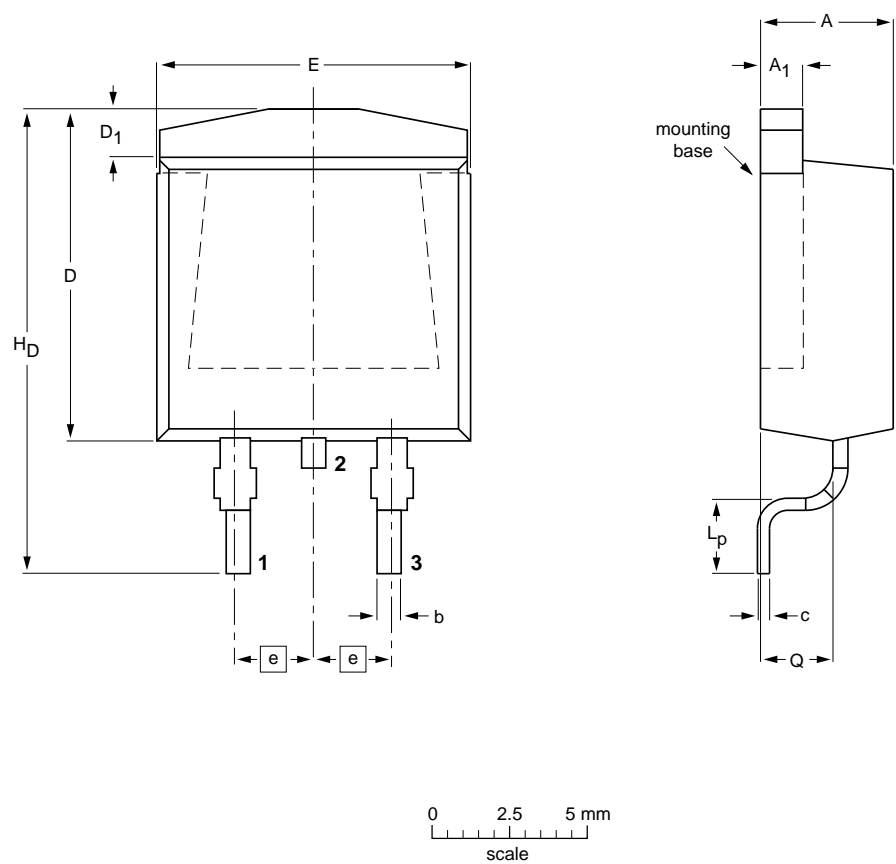
$V_{GS} = 0\text{ V}$

Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>max.</sub>	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

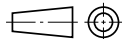
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R7-30BL v.1	20120321	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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## 11. Contact information

For more information, please visit: <http://www.nxp.com>

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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