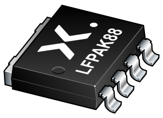


PSMN2R3-100SSJ

N-channel 100 V, 2.3 mOhm ASFET with enhanced dynamic current sharing in LFPAK88

13 January 2025 — Preliminary data sheet

1. General description

In high-power applications, it is common practice to connect two or more MOSFETs in parallel to provide high current capability. Even when the gates are driven from the same gate driver, it can be challenging to ensure that MOSFETs share the load current equally.

Small differences in $V_{GS(th)}$ for individual devices cause the MOSFET with the lowest $V_{GS(th)}$ to turn-on first, taking a larger share of the load current during the dynamic switching phase.

The difference in load current between individual MOSFETs (ΔI_D) can be significant often leading to differential heating and potential accelerated failure.

One method to reduce the ΔI between MOSFETs is to select devices with matched $V_{GS(th)}$, but testing & sorting MOSFETs with matched $V_{GS(th)}$ can be a difficult process. $V_{GS(th)}$ is typically measured at $I_D \leq 1$ mA and is influenced by temperature also.

ASFETs with enhanced dynamic current sharing are designed to show significantly improved current sharing with low ΔI_D when connected in parallel applications.

2. Features and benefits

- Removes the need for $V_{GS(th)}$ matching
- Low ΔI_D enhances current sharing in parallel applications
- Reduced $V_{GS(th)}$ spread
- Low R_{DSon}
- 255 A continuous I_D Max
- Avalanche rated, 100% tested
- Compact and Reliable 8x8 LFPAK88 package, qualified to 175 °C

3. Applications

- Applications using MOSFETs in parallel
- Applications utilizing MOSFETs with matched $V_{GS(th)}$
- High-power motor control

4. Quick reference data

Table 1. Quick reference data

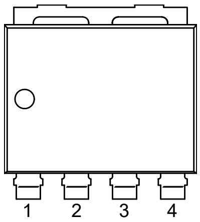
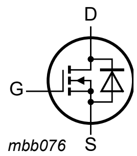
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	255	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	500	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 15		-	1.85	2.3	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 17; Fig. 18		2	8	18	nC
$Q_{G(tot)}$	total gate charge			140	280	420	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 81.7 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 142 µs; Fig. 4	[1]	-	-	753	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 21		-	147	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R3-100SSJ	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R3-100SSJ	`X2J3S10S`

8. Limiting values

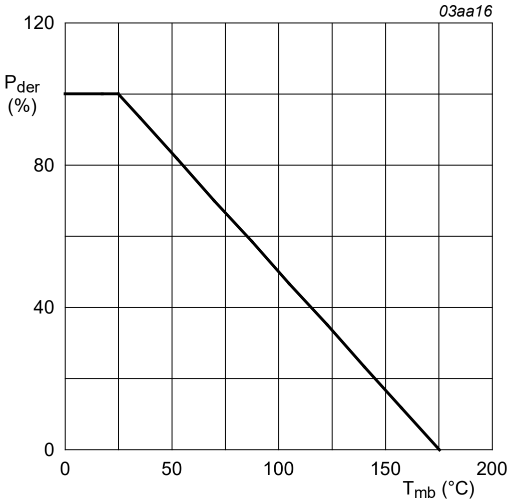
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V

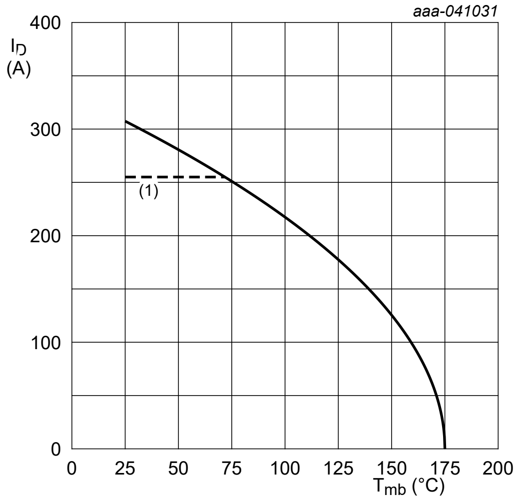
Symbol	Parameter	Conditions		Min	Max	Unit
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	500	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	255	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	217	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1230	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	255	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1230	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 81.7 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 142 µs; Fig. 4	[1]	-	753	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[1]	-	81.7	A

[1] Protected by 100% test



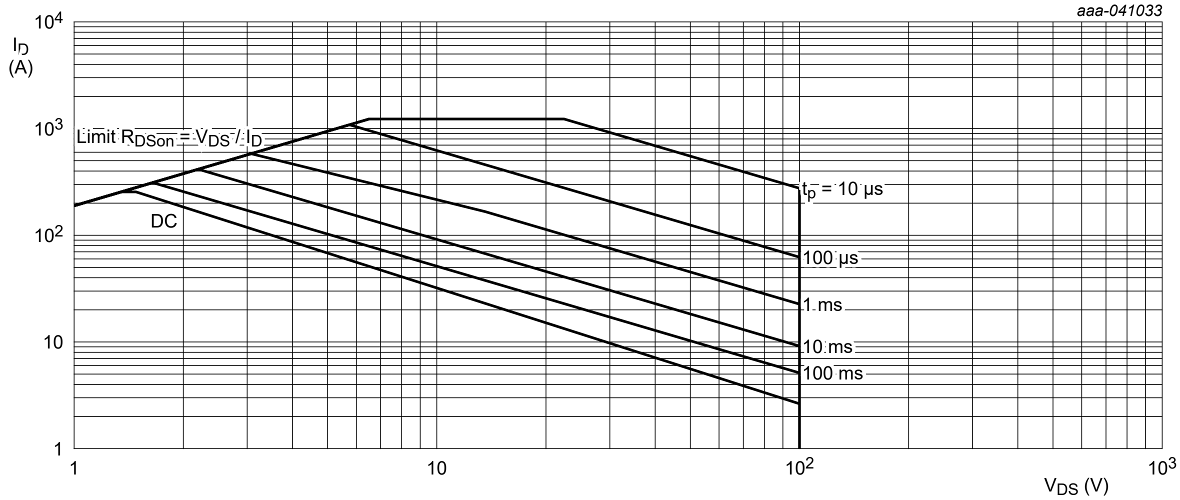
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



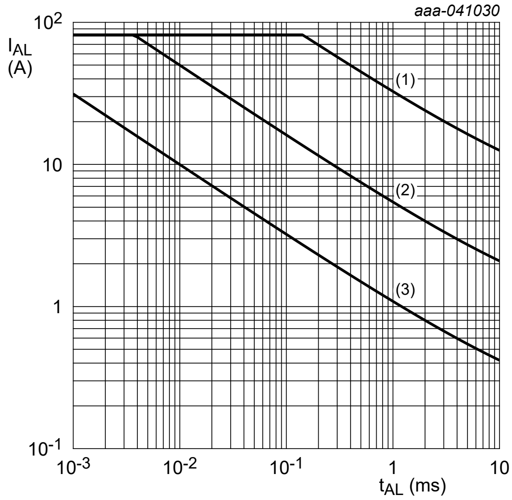
V_{GS} ≥ 10 V
(1) 255 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.23	0.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	35	-	K/W
		Fig. 7		-	70	-	K/W

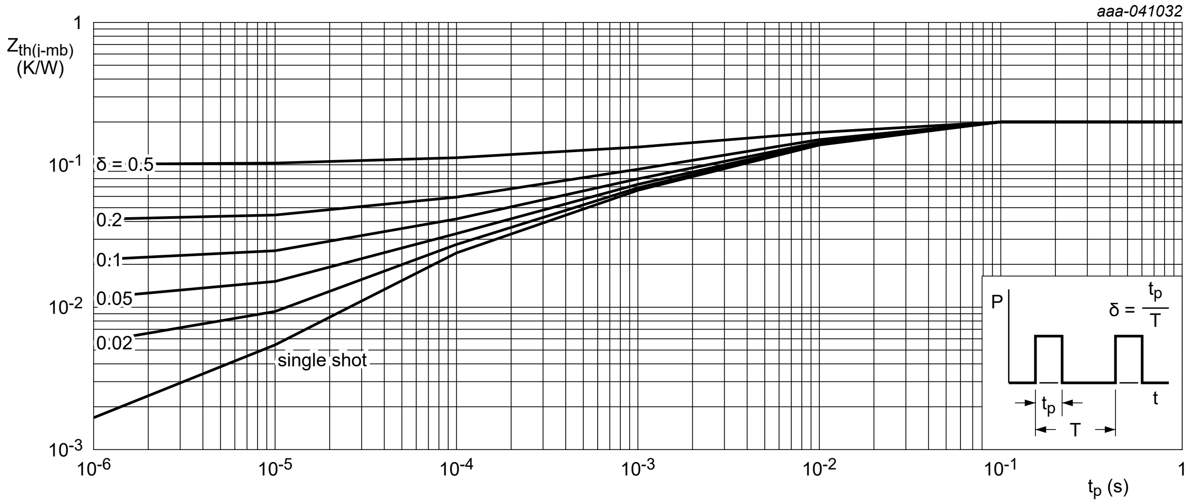
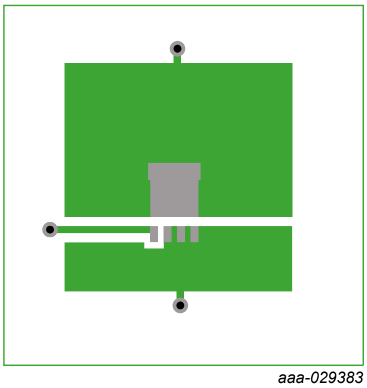
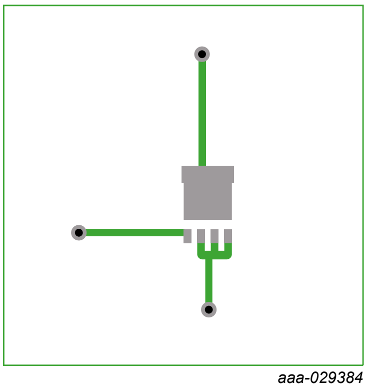


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



Copper square 25.4 mm square; 70 μm thick on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

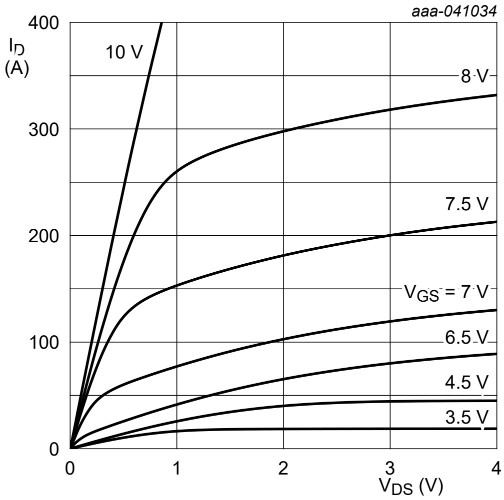
Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

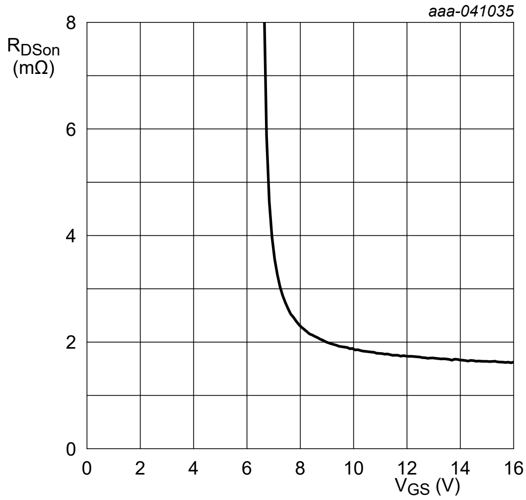
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 14		1.6	1.85	2.2	V
		I_D = 100 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 14		-	2.2	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.2	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	2.1	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-4.2	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.06	1	μA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	20	100	μA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 15		-	1.85	2.3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 16		-	2.8	3.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 16		-	3.9	5.2	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.68	1.35	2.7	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 17; Fig. 18		140	280	420	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	274	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 17; Fig. 18		52	88	123	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	38	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	50	-	nC
Q_{GD}	gate-drain charge			2	8	18	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; T_j = 25 °C; Fig. 17; Fig. 18		-	3.8	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 19		14904	24840	34776	pF
C_{oss}	output capacitance			1610	2683	4293	pF
C_{rss}	reverse transfer capacitance			5	47	122	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	57	-	ns
t_r	rise time			-	57	-	ns
$t_{d(off)}$	turn-off delay time			-	200	-	ns
t_f	fall time			-	89	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	V_{GS} = 0 V; T_j = 25 °C; Fig. 20		-	0.81	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 21		-	72	-	ns
Q_r	recovered charge			-	147	-	nC



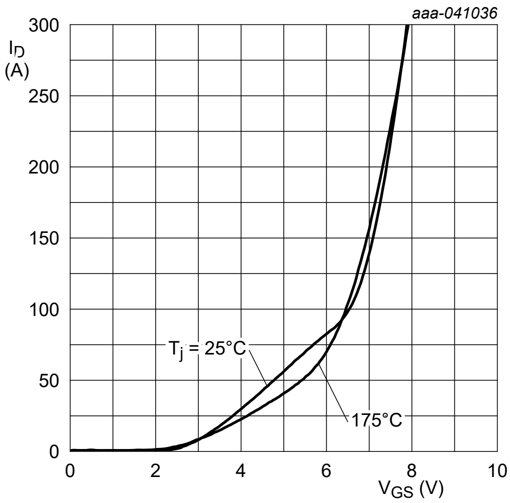
T_j = 25 °C

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values



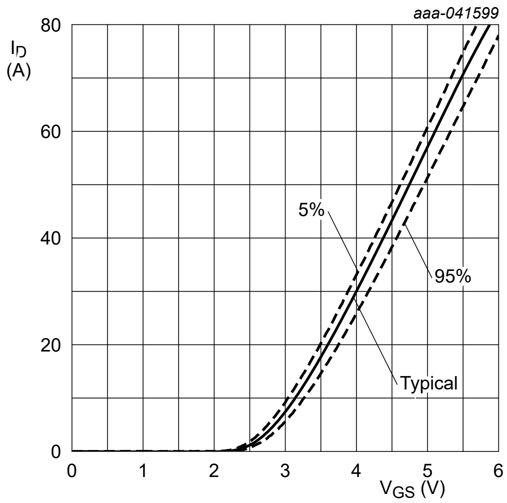
T_j = 25 °C; I_D = 25 A

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



V_{DS} = 8 V

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



T_j = 25 °C; V_{DS} = 8 V

Fig. 11. Transfer characteristics; drain current as a function of gate-source voltage; typical, 5% and 95% percentile values

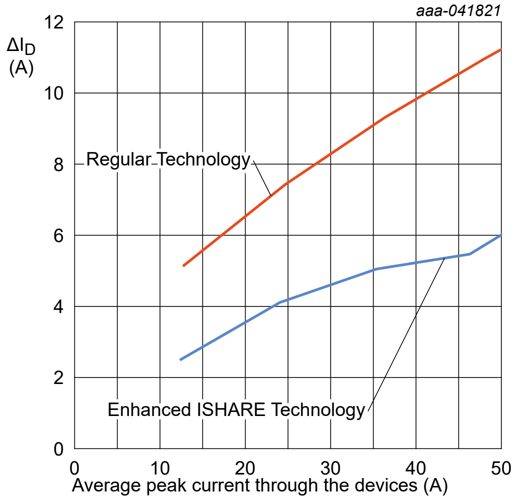


Fig. 12. Typical response of regular and enhanced technology MOSFETs showing delta current for two MOSFETs in parallel having delta VGSth of 0.45V@20A

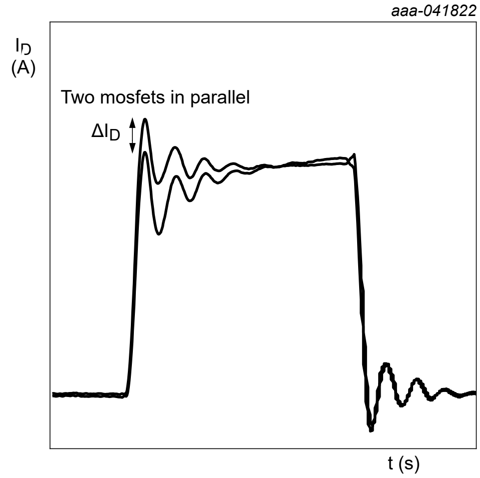
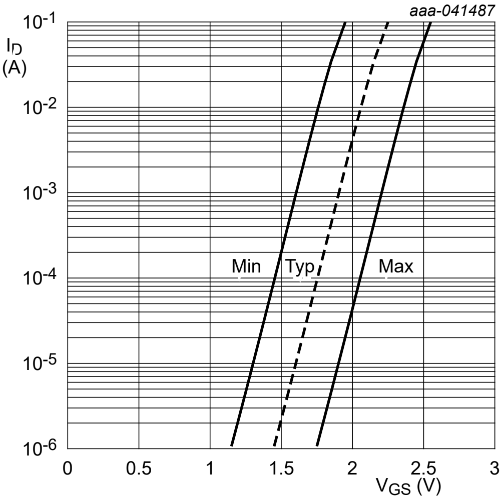
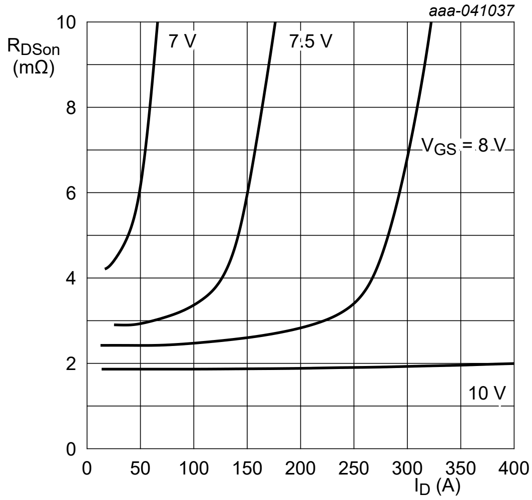


Fig. 13. Dynamic current imbalance between two MOSFETs in parallel.



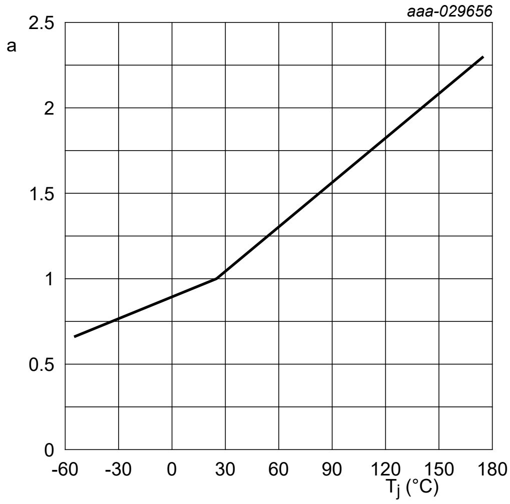
T_j = 25 °C; V_{DS} = 5 V

Fig. 14. Sub-threshold drain current as a function of gate-source voltage



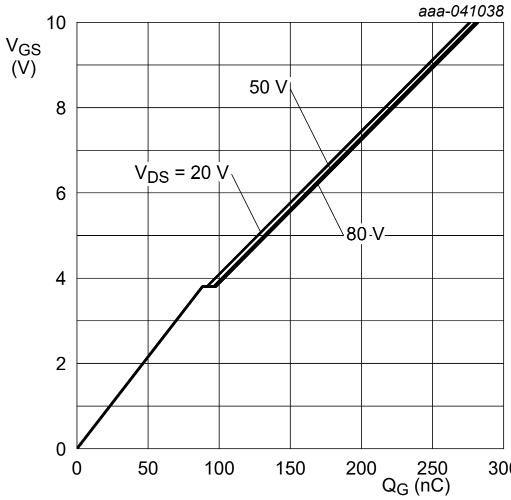
T_j = 25 °C

Fig. 15. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 16. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 17. Gate-source voltage as a function of gate charge; typical values

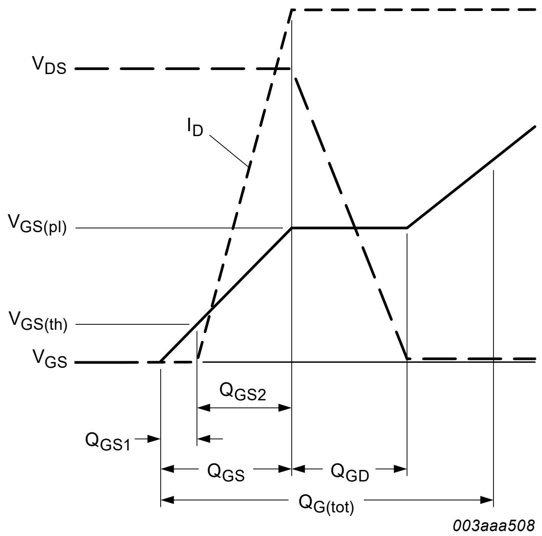
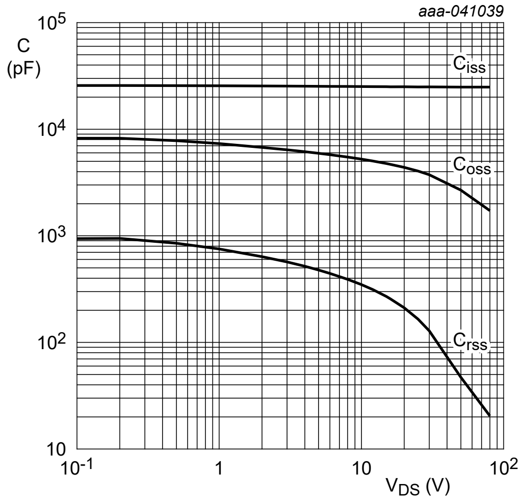
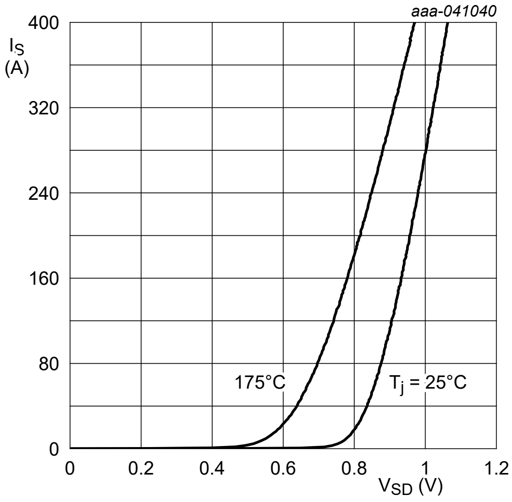


Fig. 18. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 19. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 20. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

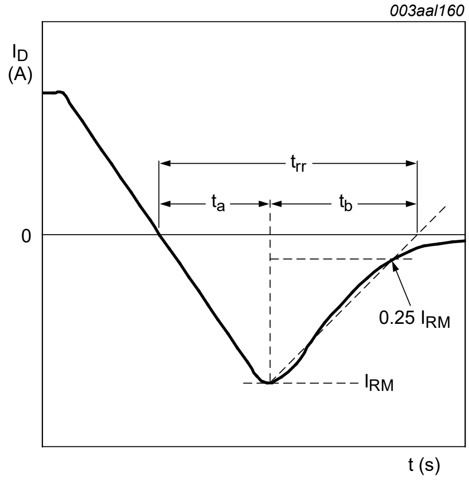
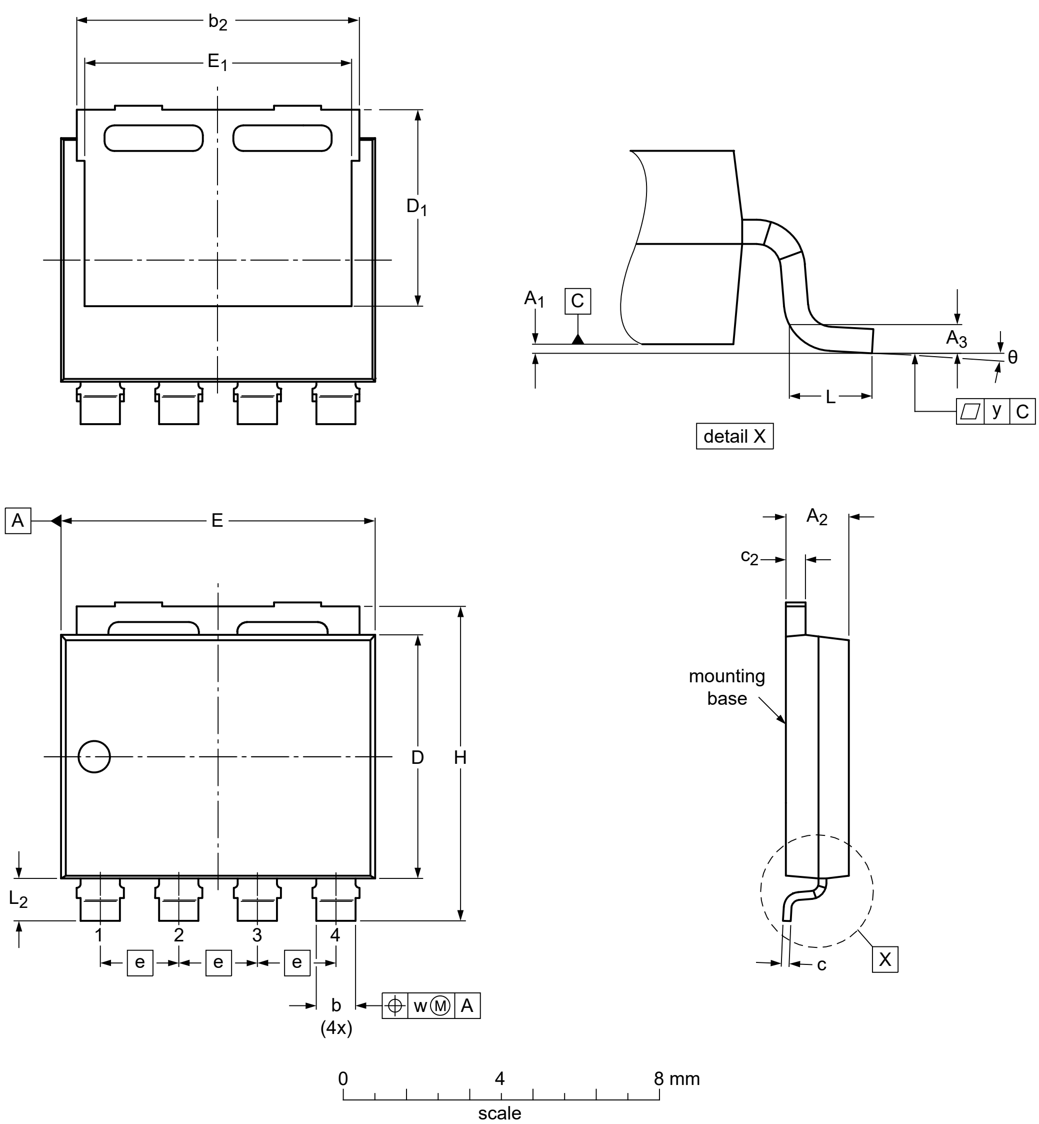


Fig. 21. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads **SOT1235**



Dimensions (mm are the original dimensions)

Unit		A_1	A_2	A_3	b	b_2	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H(1)	L	L_2	w	y	θ
mm	max	0.15	1.7		1.1	7.3	0.24	0.55	6.3	5.1	8.1	6.9		8.1	0.8	1.3			8°
	nom			0.25									2.0				0.25	0.10	
	min	0.00	1.5		0.9	7.1	0.18	0.45	6.1	4.9	7.9	6.7		7.8	0.6	0.9			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1235_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1235						~~17-08-02~~ 17-08-07

Fig. 22. Package outline LFPAK88 (SOT1235)

12. Soldering

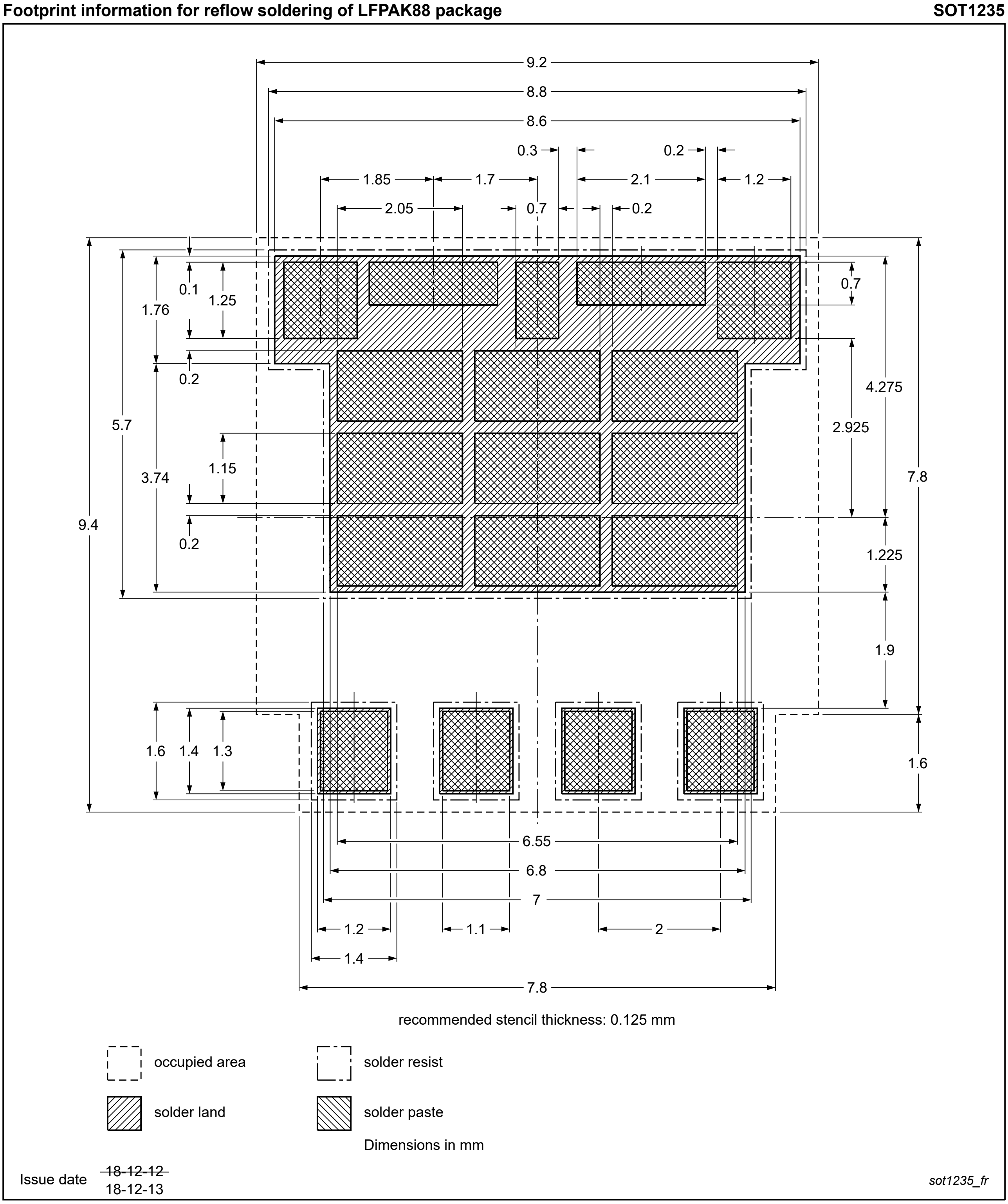


Fig. 23. Reflow soldering footprint for LFPAK88 (SOT1235)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 13 January 2025