



PSMN2R0-40YLD

40 V logic level MOSFET

8 July 2019

Preliminary data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET.

2. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	120	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	166	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 8		-	1.8	2.1	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 8		-	2.3	2.7	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; Fig. 10 ; Fig. 11		-	7.3	15	nC
Q _{G(tot)}	total gate charge			-	30	42	nC

[1] 120A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

3. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	<p>LFPAK56; Power-SO8 (SOT669)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

4. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-40YLD	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

5. Limiting values

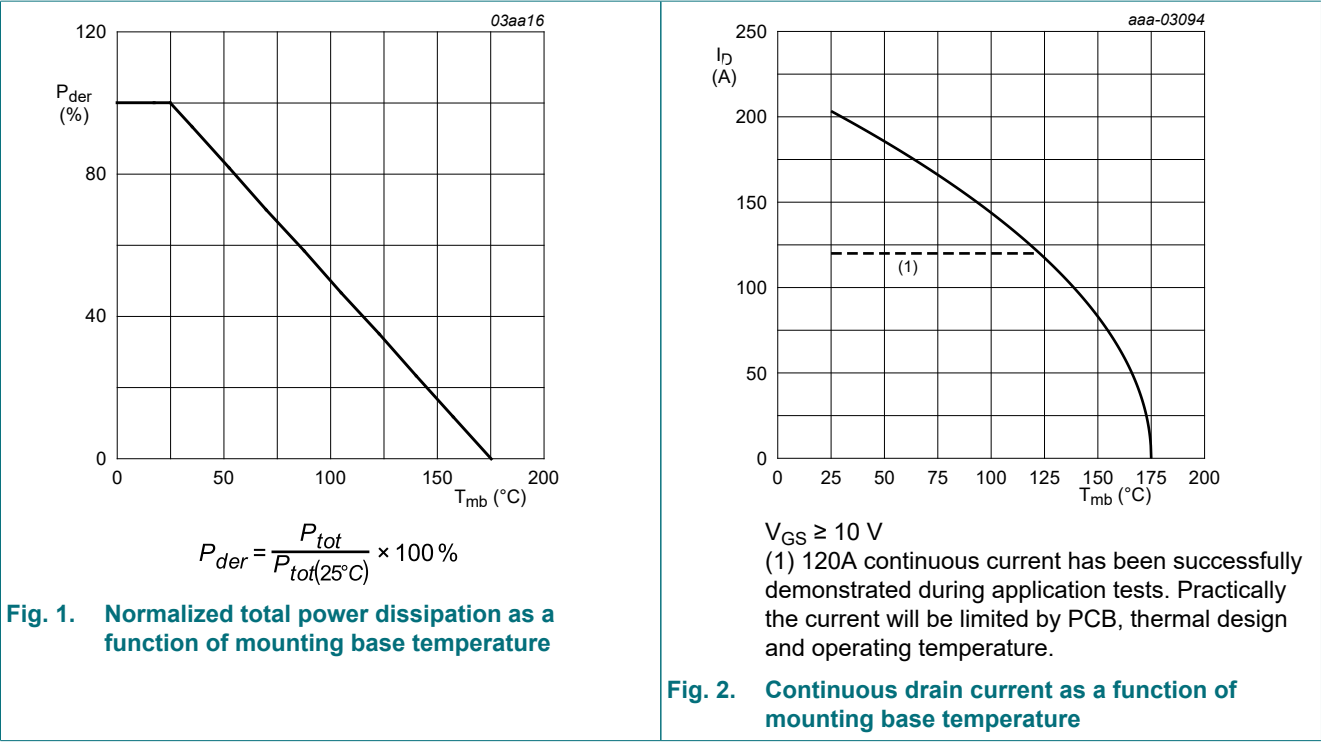
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed		-	45	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	166	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	120	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	813	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	813	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 53.5\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 182\text{ }\mu\text{s}$	[2]	-	253	mJ
		$I_D = 25\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 937\text{ }\mu\text{s}$	[2]	-	609	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	120	A

[1] 120A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

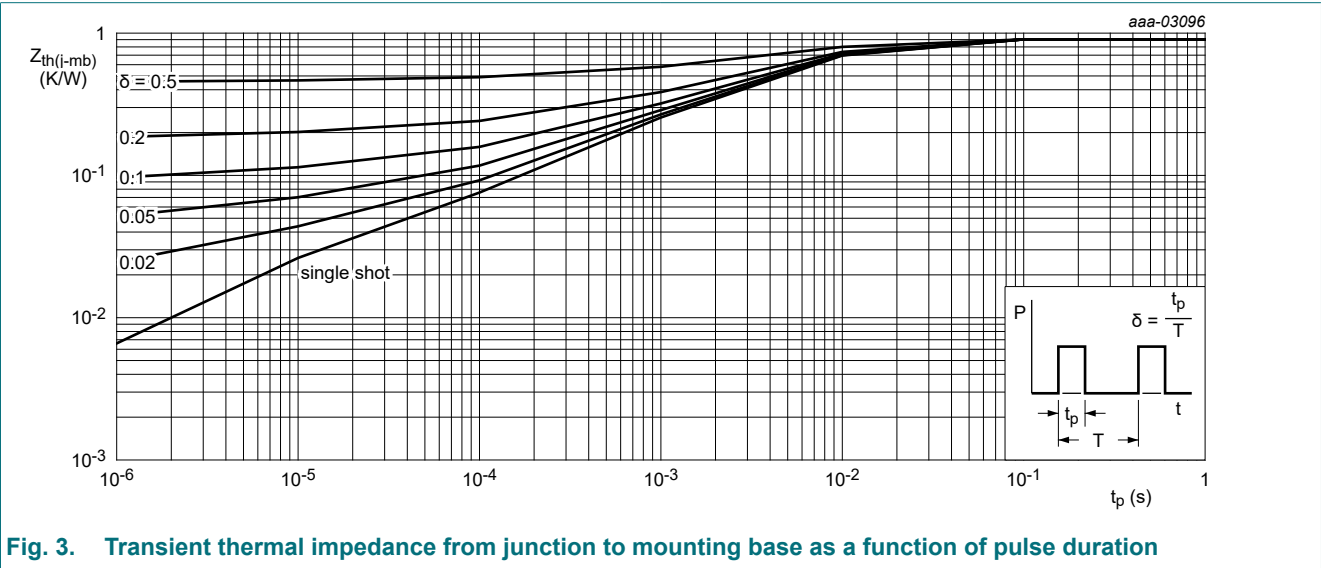
[2] Protected by 100% test

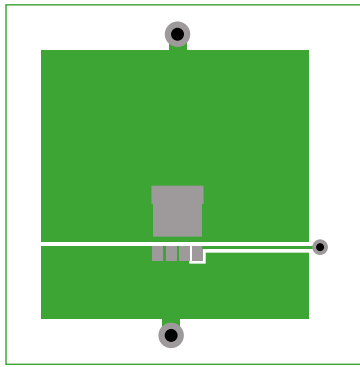


6. Thermal characteristics

Table 5. Thermal characteristics

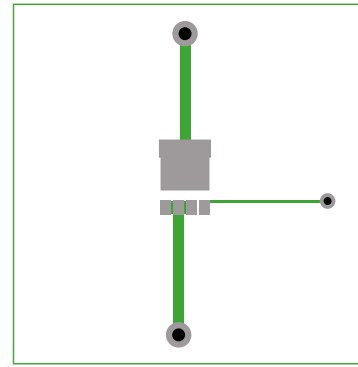
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3	-	0.8	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 4	-	42	-	K/W
		Fig. 5	-	85	-	K/W





Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 4. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 5. PCB layout with minimum footprint for thermal resistance from junction to ambient

7. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 ^\circ C$	1.35	1.7	2.05	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_j \leq 150 ^\circ C$	-	-4.3	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 ^\circ C$	-	0.01	1	μA
		$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125 ^\circ C$	-	[tbd]	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 ^\circ C; \text{Fig. 8}$	-	1.8	2.1	m Ω
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175 ^\circ C; \text{Fig. 9}$	-	-	4.1	m Ω
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 ^\circ C; \text{Fig. 8}$	-	2.3	2.7	m Ω
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 175 ^\circ C; \text{Fig. 9}$	-	-	5.2	m Ω
R_G	gate resistance	$f = 1 MHz; T_j = 25 ^\circ C$	0.3	0.8	2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; \text{Fig. 10; Fig. 11}$	-	30	42	nC
		$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; \text{Fig. 10; Fig. 11}$	-	66	92	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	35	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 10 ; Fig. 11		-	11	17	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	7	11	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	4.1	6	nC
Q_{GD}	gate-drain charge			-	7.3	15	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; Fig. 10 ; Fig. 11		-	2.7	-	V
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12		-	4701	6581	pF
C_{oss}	output capacitance			-	1047	1466	pF
C_{rss}	reverse transfer capacitance			-	181	398	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}$; $R_L = 0.8\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$		-	10	-	ns
t_r	rise time			-	8	-	ns
$t_{d(off)}$	turn-off delay time			-	57	-	ns
t_f	fall time			-	18	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$		-	33	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 14		-	32	-	ns
Q_r	recovered charge		[1]	-	27	-	nC
t_a	reverse recovery rise time			-	17	-	ns
t_b	reverse recovery fall time			-	15	-	ns

[1] includes capacitive recovery

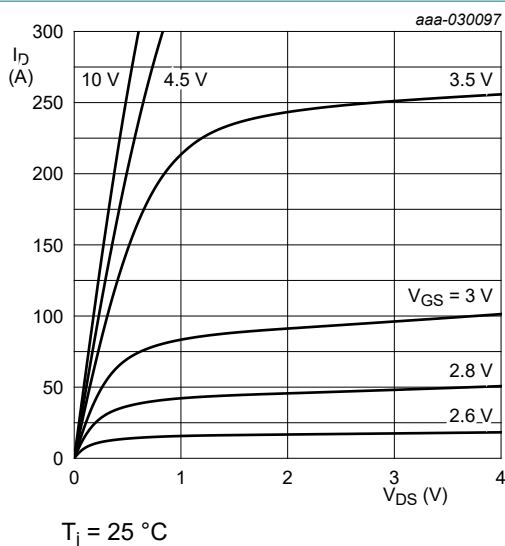


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

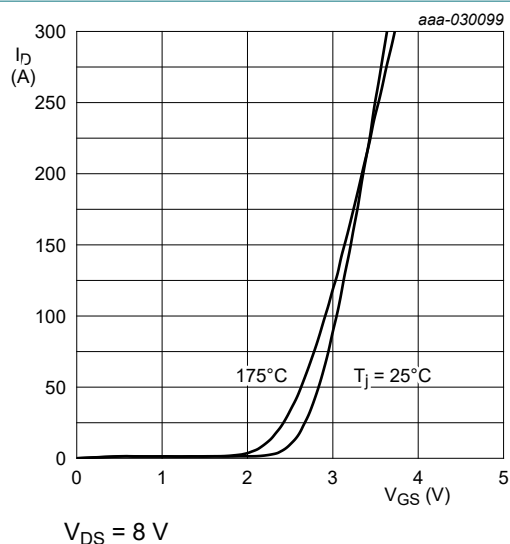


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

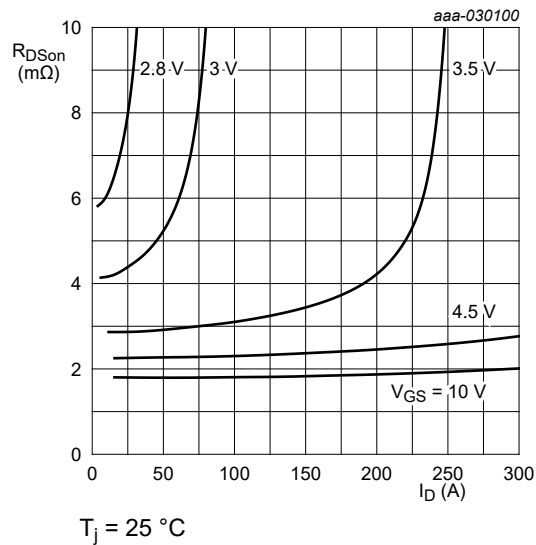


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

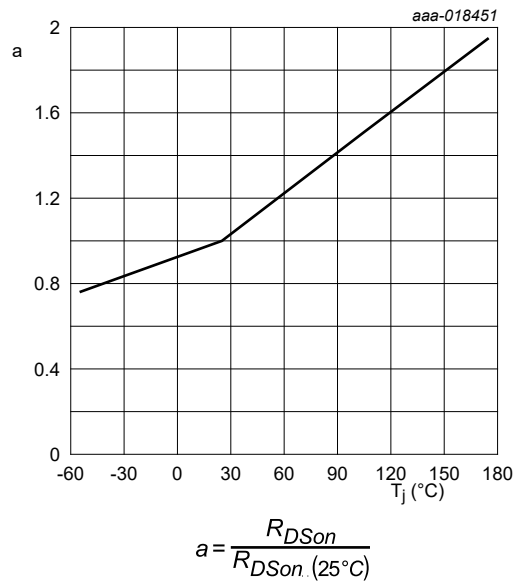


Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

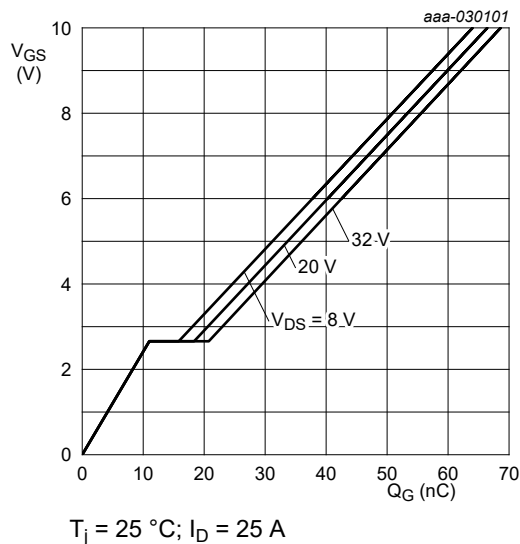


Fig. 10. Gate-source voltage as a function of gate charge; typical values

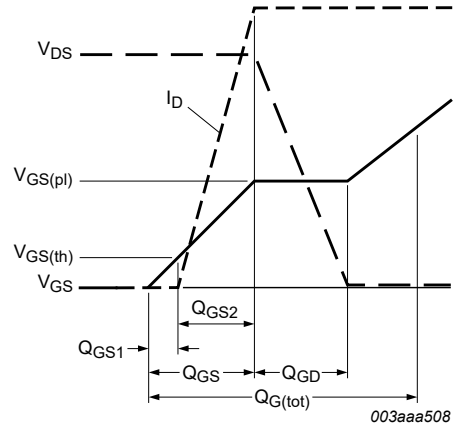
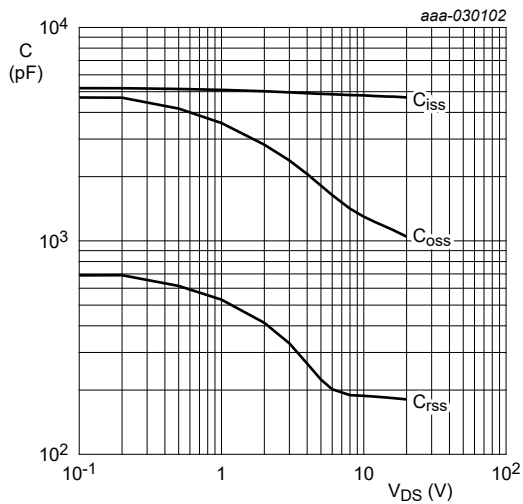
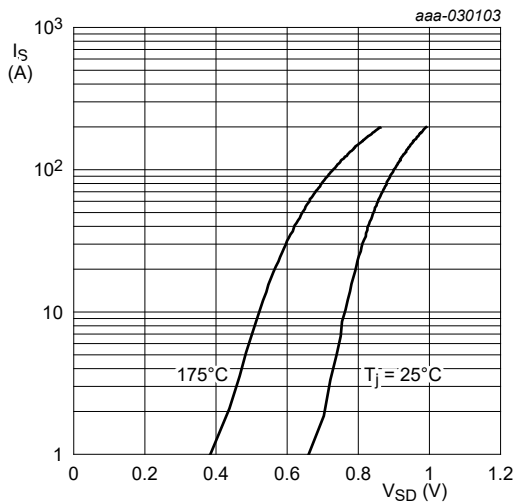


Fig. 11. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 13. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

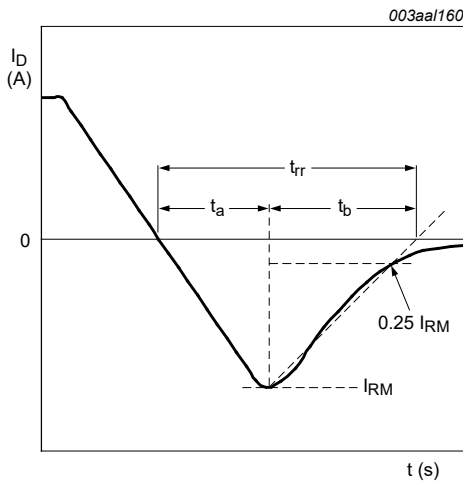


Fig. 14. Reverse recovery timing definition

8. Package outline

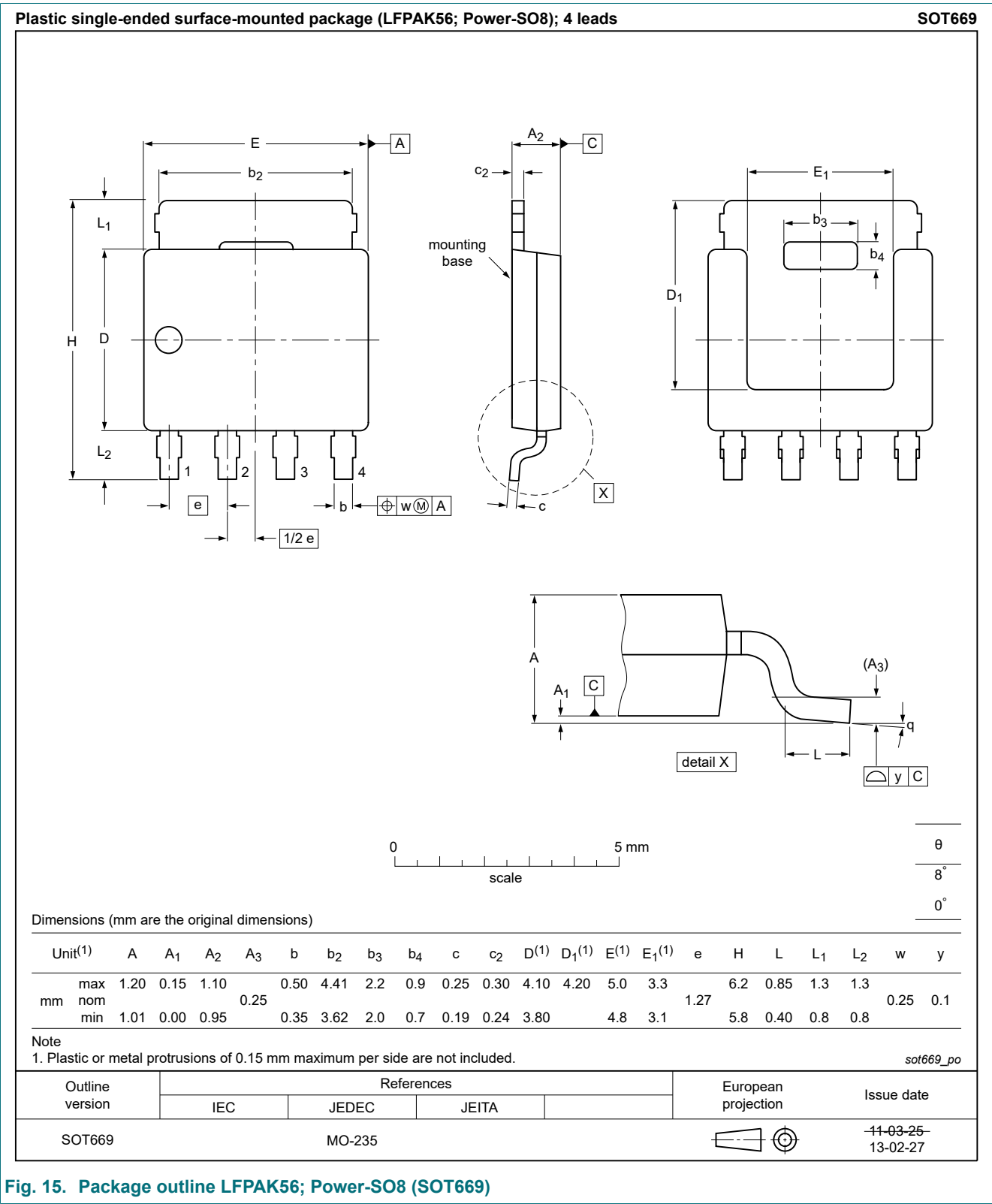


Fig. 15. Package outline LPAK56; Power-SO8 (SOT669)

9. Soldering

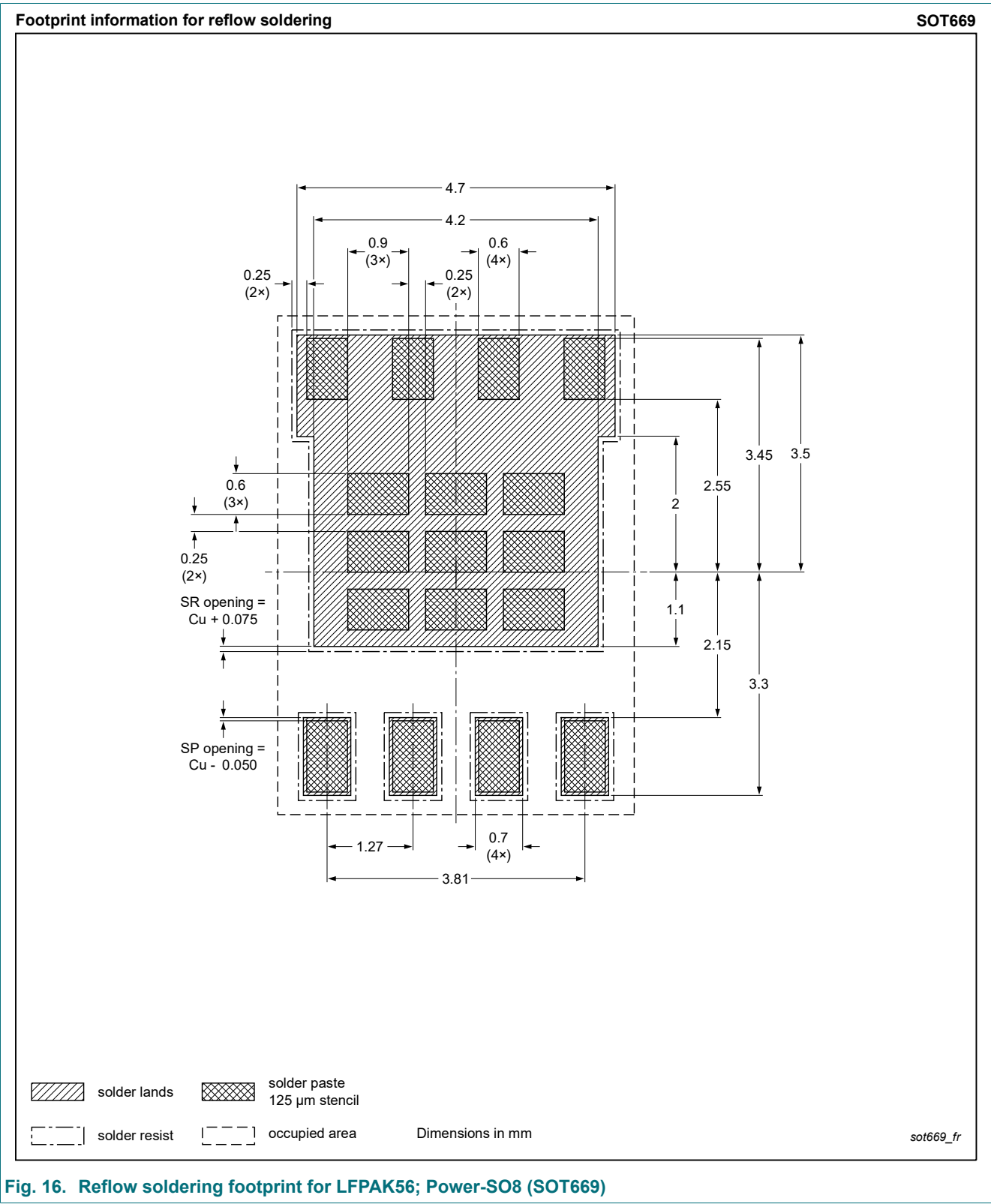


Fig. 16. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package

SOT669

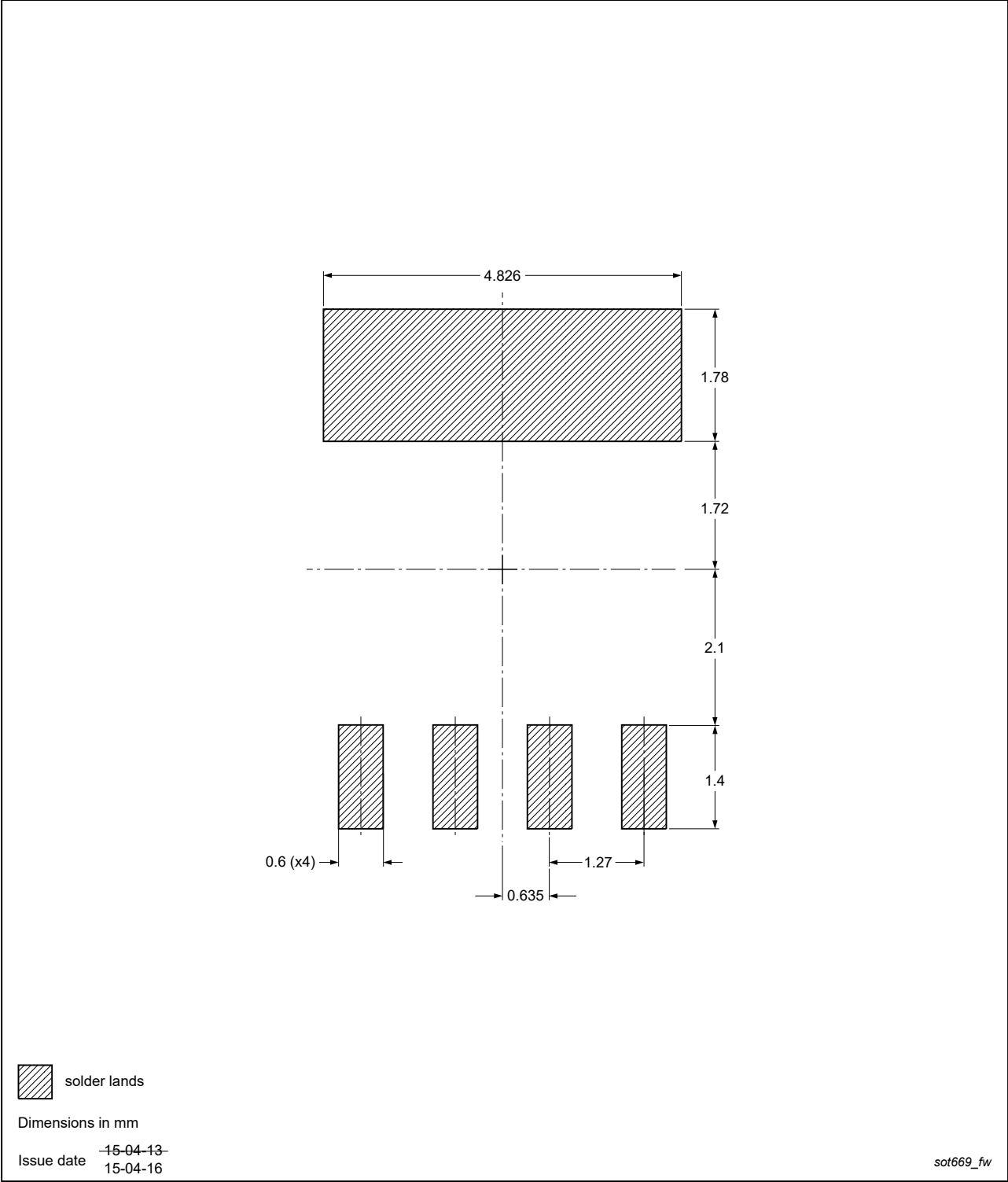


Fig. 17. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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