



PSMN1R9-80SSJ

N-channel 80 V, 1.9 mOhm ASFET with enhanced dynamic current sharing in LFPK88

13 January 2025

Preliminary data sheet

1. General description

In high-power applications, it is common practice to connect two or more MOSFETs in parallel to provide high current capability. Even when the gates are driven from the same gate driver, it can be challenging to ensure that MOSFETs share the load current equally.

Small differences in $V_{GS(th)}$ for individual devices cause the MOSFET with the lowest $V_{GS(th)}$ to turn-on first, taking a larger share of the load current during the dynamic switching phase.

The difference in load current between individual MOSFETs (ΔI_D) can be significant often leading to differential heating and potential accelerated failure.

One method to reduce the ΔI between MOSFETs is to select devices with matched $V_{GS(th)}$, but testing & sorting MOSFETs with matched $V_{GS(th)}$ can be a difficult process. $V_{GS(th)}$ is typically measured at $I_D \leq 1$ mA and is influenced by temperature also.

ASFETs with enhanced dynamic current sharing are designed to show significantly improved current sharing with low ΔI_D when connected in parallel applications.

2. Features and benefits

- Removes the need for $V_{GS(th)}$ matching
- Low ΔI_D enhances current sharing in parallel applications
- Reduced $V_{GS(th)}$ spread
- Low R_{DSon}
- 286 A continuous I_D Max
- Avalanche rated, 100% tested
- Compact and Reliable 8x8 LFPK88 package, qualified to 175 °C

3. Applications

- Applications using MOSFETs in parallel
- Applications utilizing MOSFETs with matched $V_{GS(th)}$
- High-power motor control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	286	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	500	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 15	-	1.6	1.9	mΩ

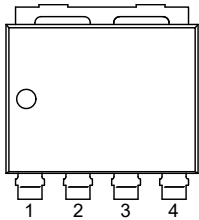
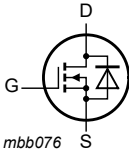
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V;		1.8	6	14	nC
Q _{G(tot)}	total gate charge	T _j = 25 °C; Fig. 17 ; Fig. 18		136	272	408	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 89.6 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 186 μs; Fig. 4	[1]	-	-	867	mJ
Source-drain diode							
Q _r	recovered charge	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 21		-	103	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	 mbb076
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R9-80SSJ	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R9-80SSJ	X1J9S80S

8. Limiting values

Table 5. Limiting values

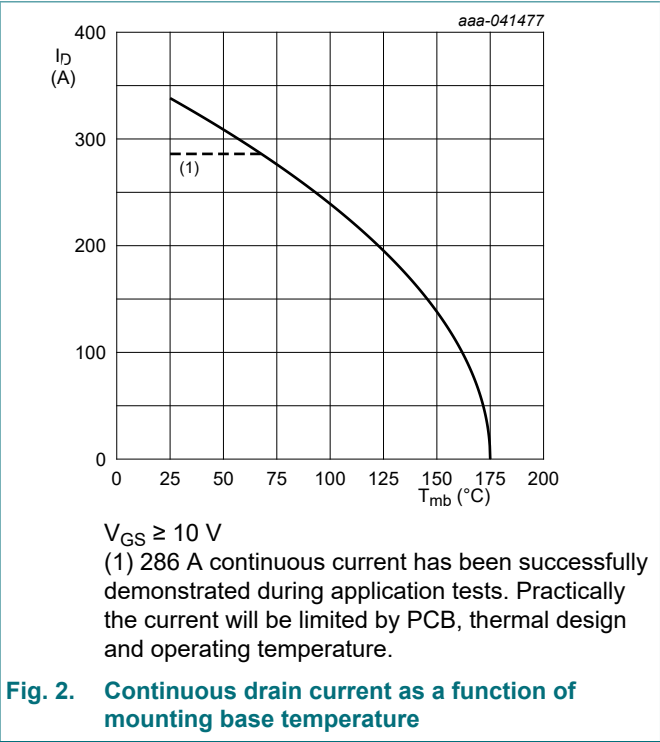
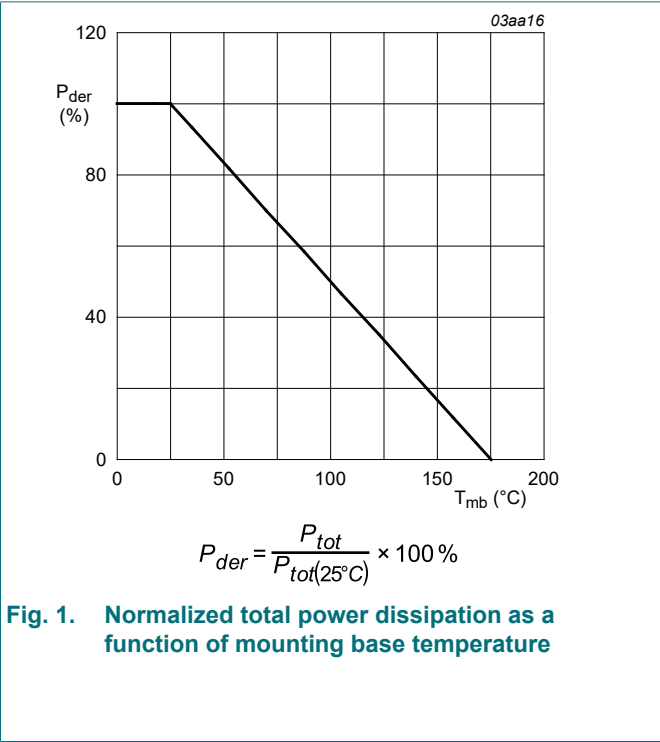
In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	80	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	80	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	500	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	286	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	239	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1353	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	286	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1353	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 89.6 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 186 μs; Fig. 4	[1]	-	867	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 80 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	89.6	A

[1] Protected by 100% test



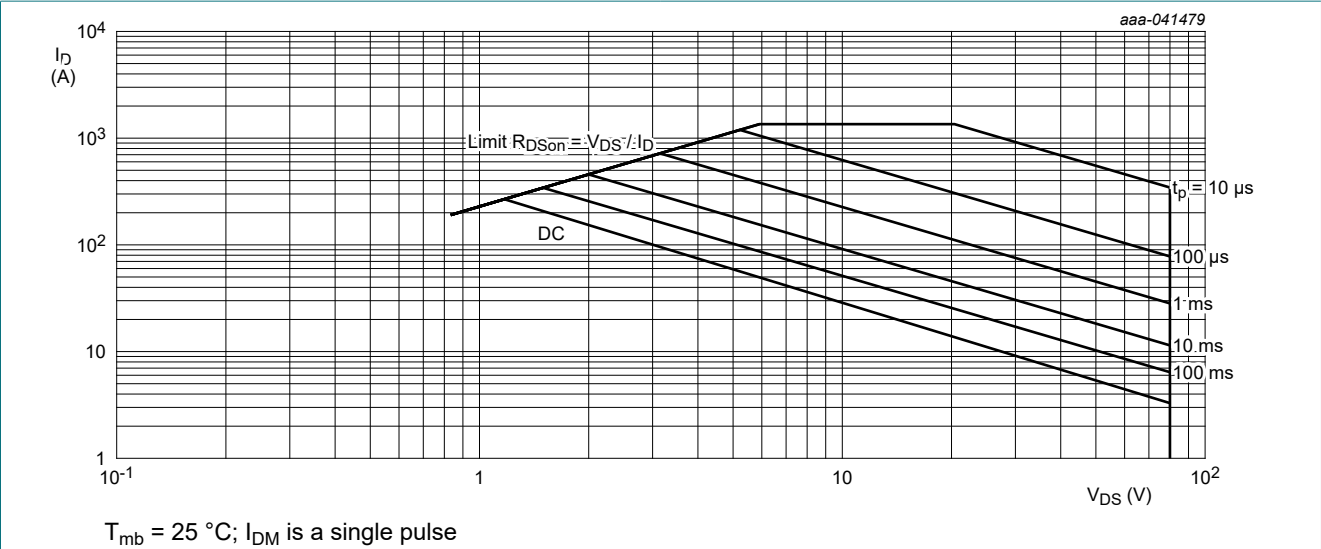


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

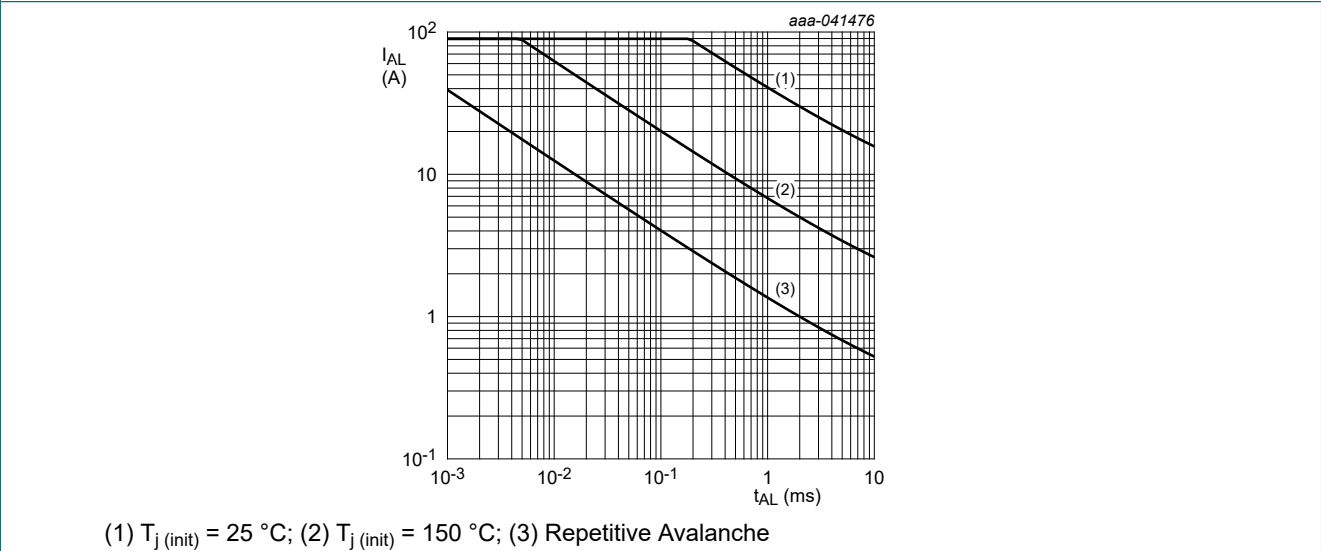


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.23	0.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	35	-	K/W
		Fig. 7	-	70	-	K/W

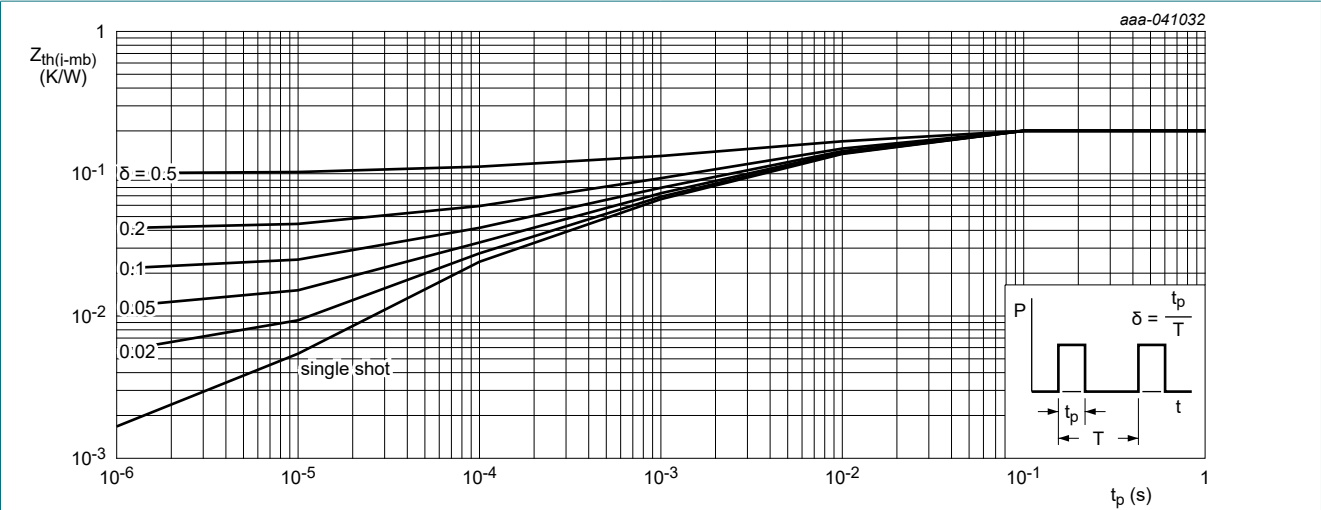


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-029383

Copper square 25.4 mm square; 70 μm thick on FR4 board

aaa-029384

70 μm thick copper on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		80	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		72	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 14		1.6	1.9	2.2	V
		I _D = 100 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 14		-	2.25	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C		-	1.2	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C		-	2.1	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 150 °C		-	-4.22	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _J = 25 °C		-	0.15	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _J = 125 °C		-	38	100	μA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 15		-	1.6	1.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 16		-	2.4	2.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 16		-	3.4	4.4	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.65	1.3	2.6	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 17 ; Fig. 18		136	272	408	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	265	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 17 ; Fig. 18		53	89	125	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	45	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	44	-	nC
Q _{GD}	gate-drain charge			1.8	6	14	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 40 V; T _j = 25 °C; Fig. 17 ; Fig. 18		-	3.8	-	V
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 19		14884	24807	34730	pF
C _{oss}	output capacitance			1694	2823	4517	pF
C _{rss}	reverse transfer capacitance			4	43	129	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	60	-	ns
t _r	rise time			-	55	-	ns
t _{d(off)}	turn-off delay time			-	197	-	ns
t _f	fall time			-	78	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 20		-	0.81	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 21		-	63	-	ns
Q _r	recovered charge			-	103	-	nC

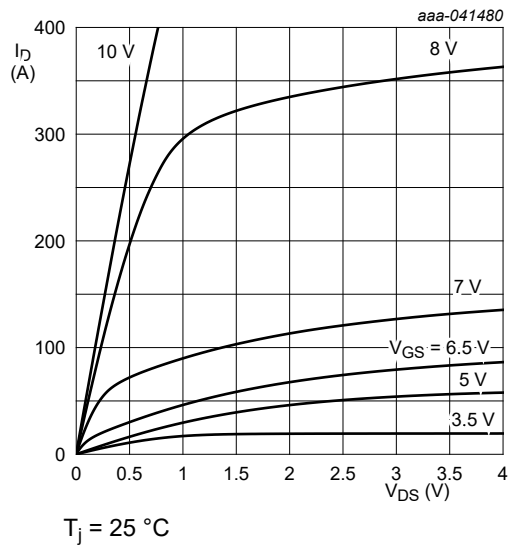


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

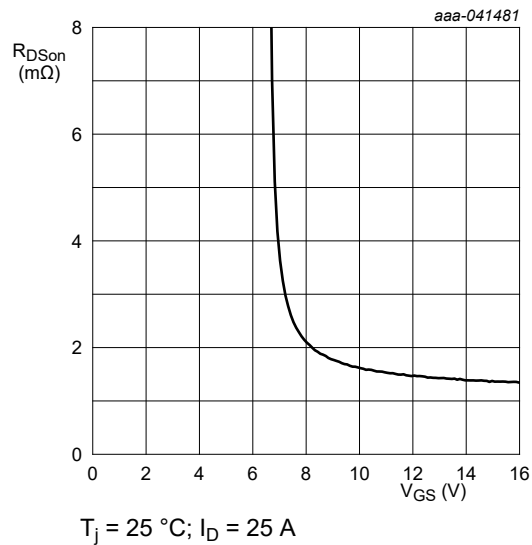


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

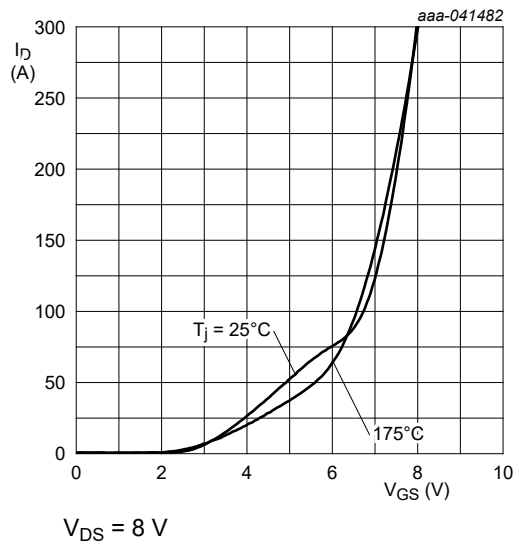


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

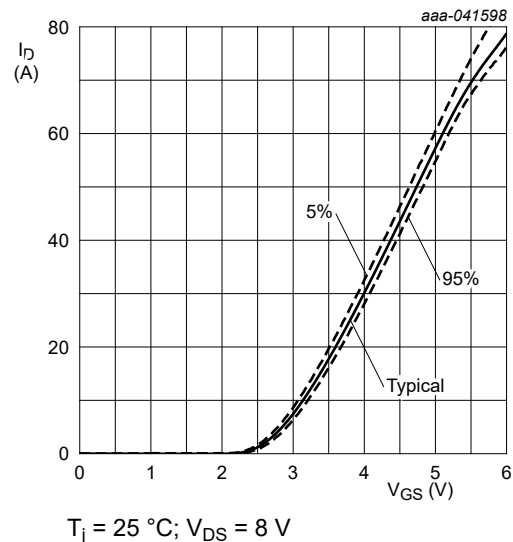


Fig. 11. Transfer characteristics; drain current as a function of gate-source voltage; typical, 5% and 95% percentile values

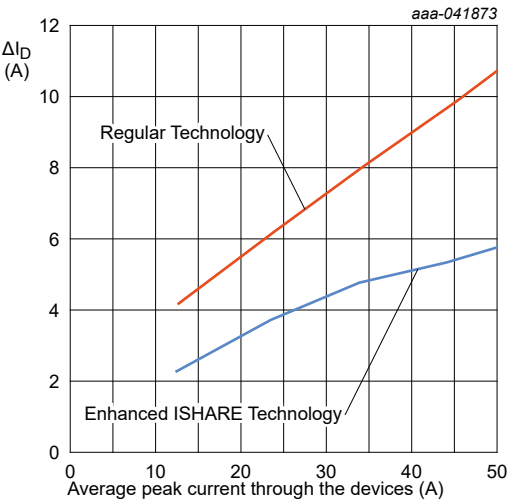


Fig. 12. Typical response of regular and enhanced technology MOSFETs showing delta current for two MOSFETs in parallel having delta VGSth of 0.35V@20A

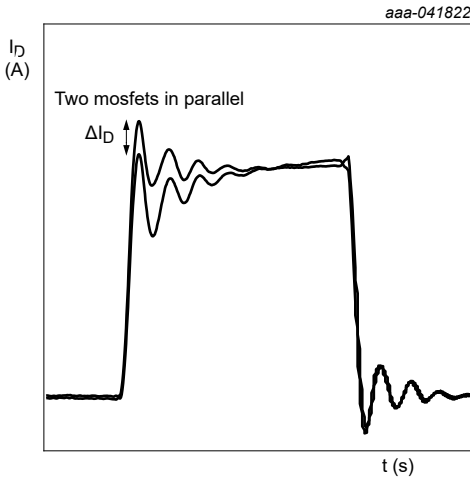


Fig. 13. Dynamic current imbalance between two MOSFETs in parallel.

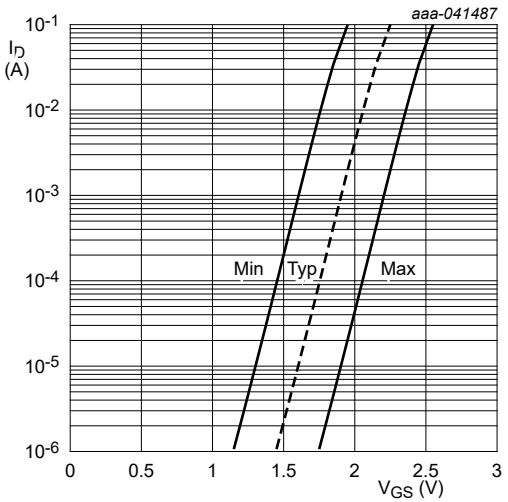


Fig. 14. Sub-threshold drain current as a function of gate-source voltage

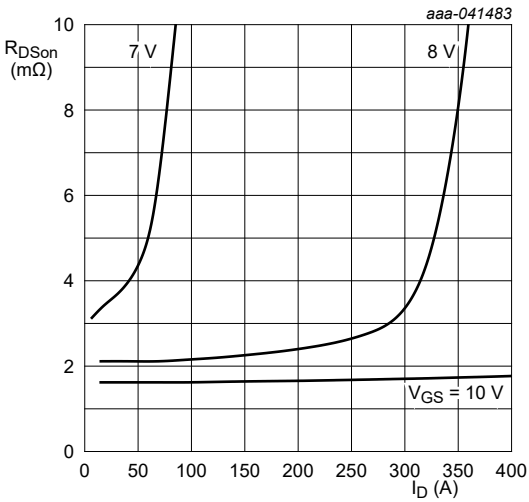


Fig. 15. Drain-source on-state resistance as a function of drain current; typical values

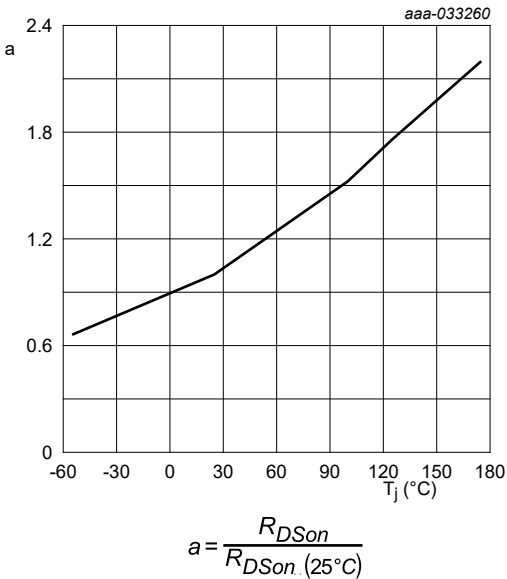


Fig. 16. Normalized drain-source on-state resistance factor as a function of junction temperature

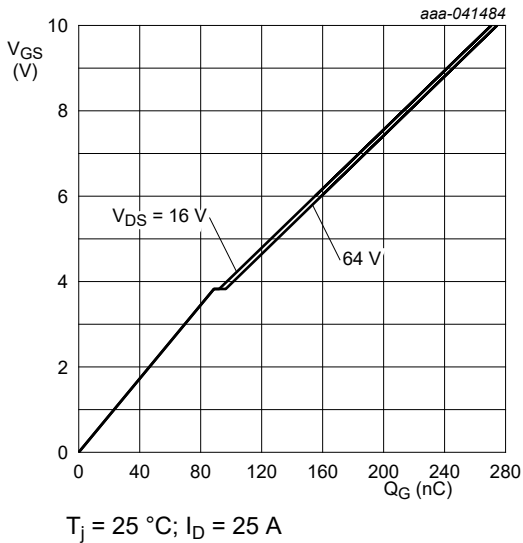


Fig. 17. Gate-source voltage as a function of gate charge; typical values

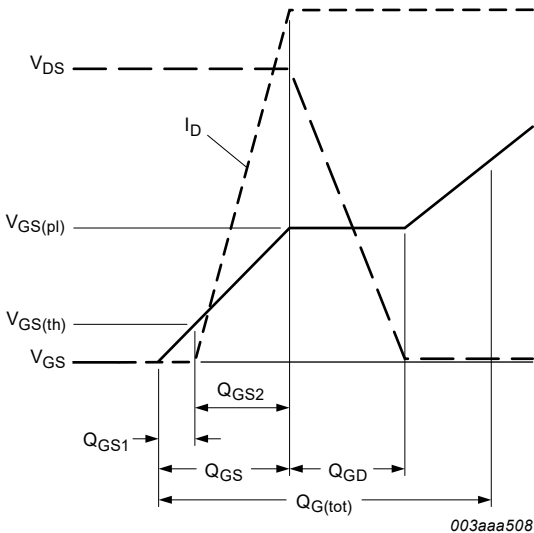


Fig. 18. Gate charge waveform definitions

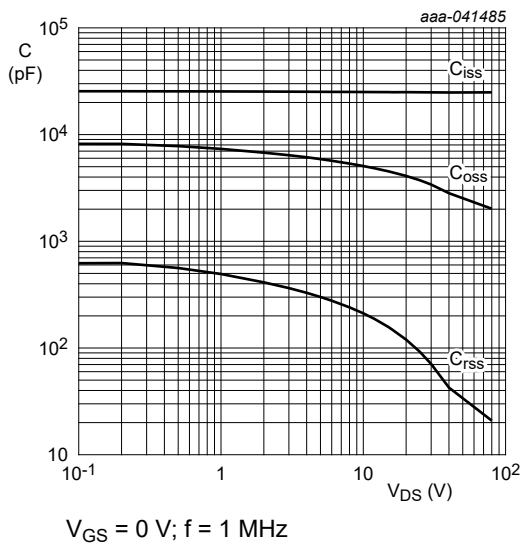
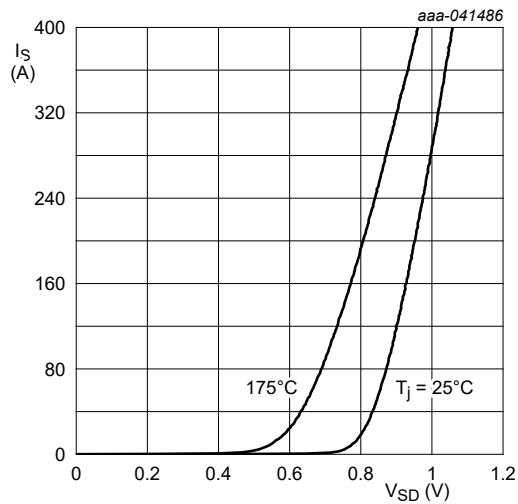


Fig. 19. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 20. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

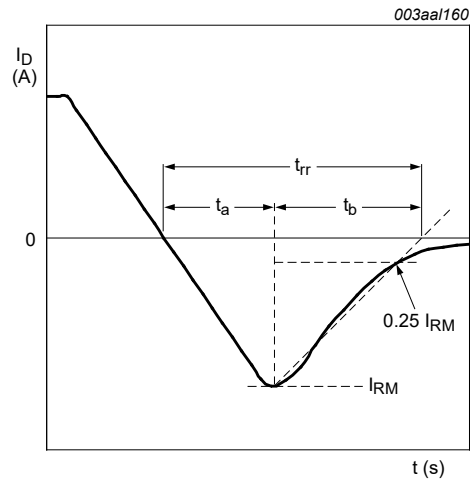
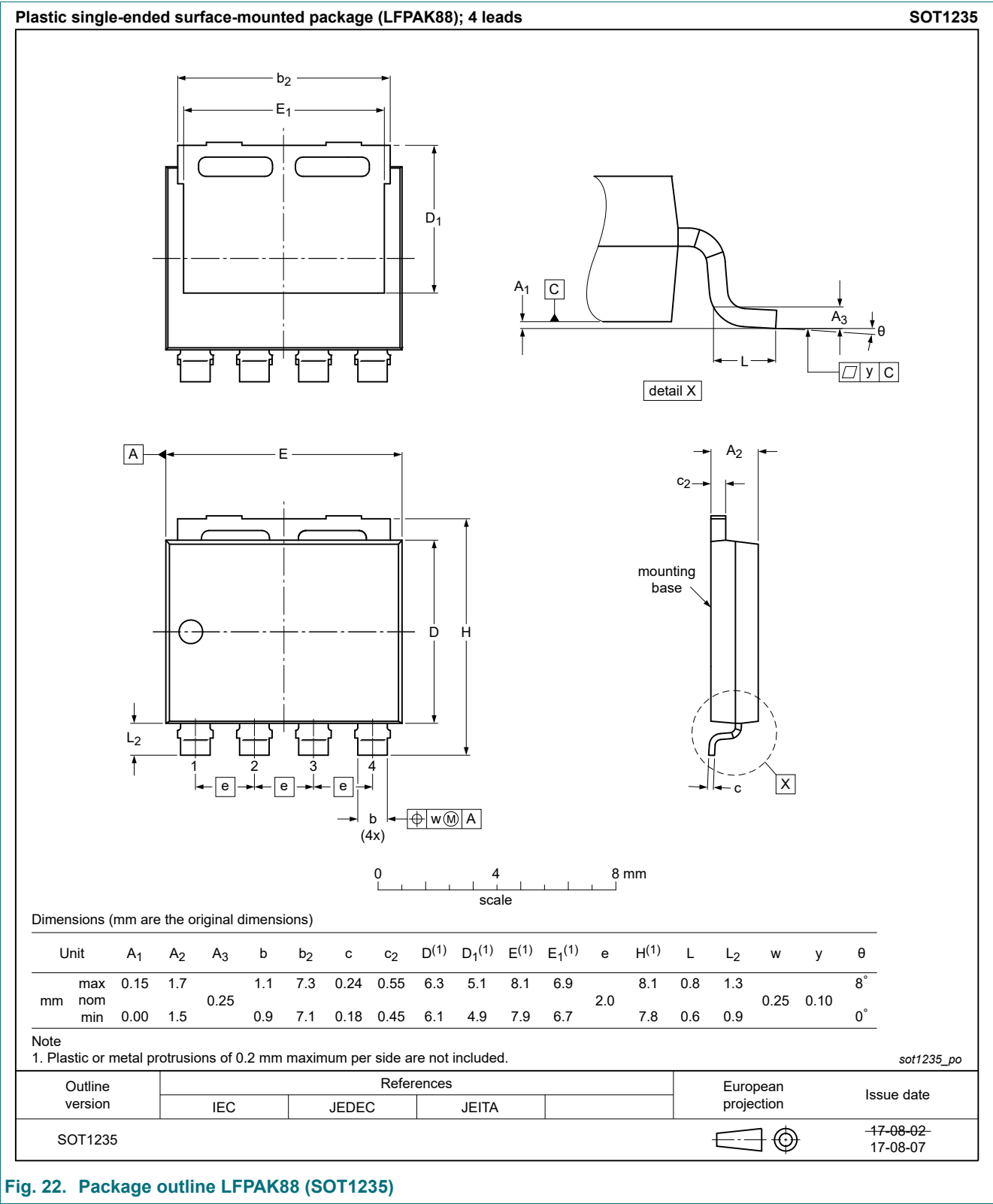


Fig. 21. Reverse recovery timing definition

11. Package outline



12. Soldering

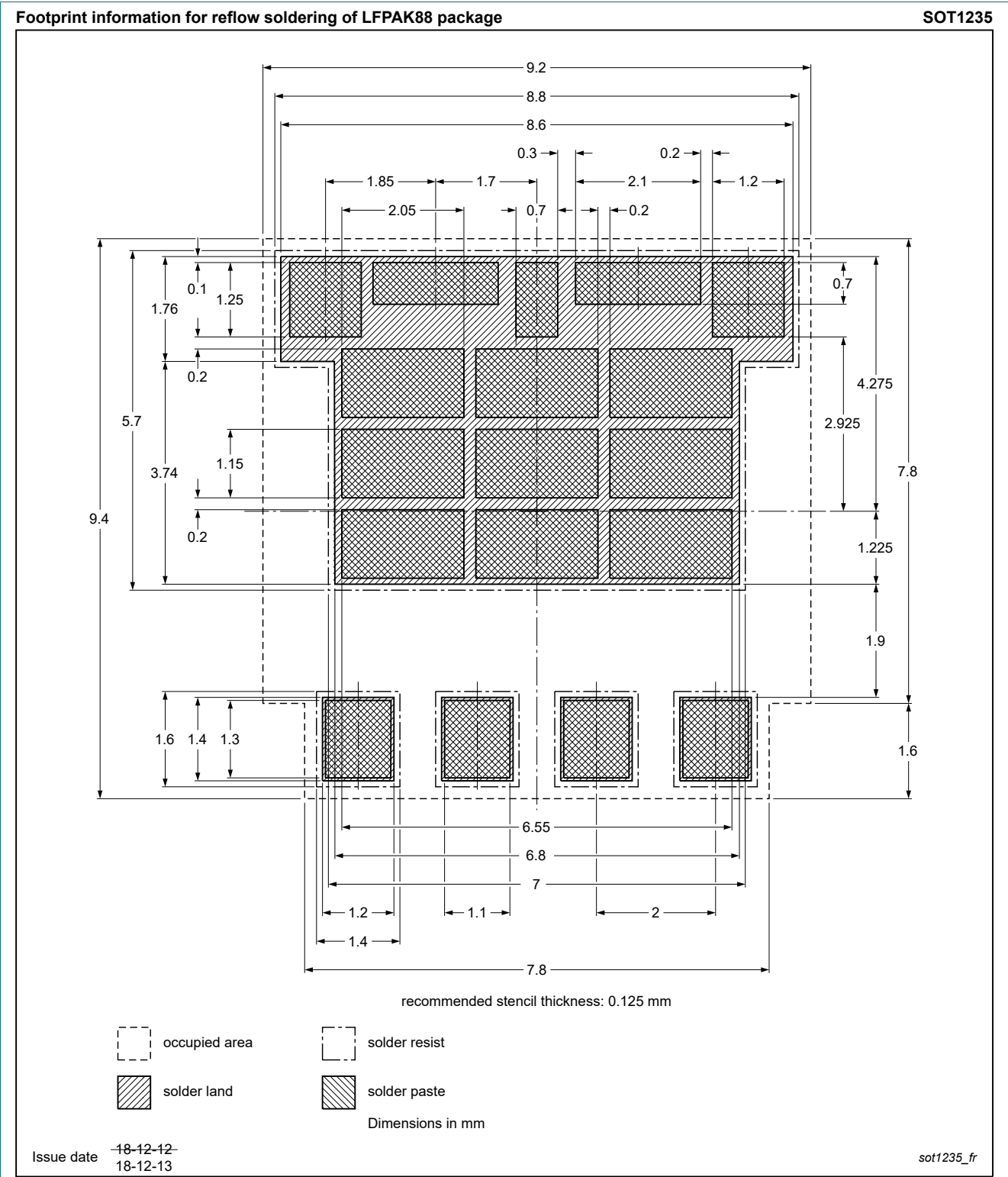


Fig. 23. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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