



PSMN1R9-80SSE

N-channel 80 V, 1.9 mOhm MOSFET with enhanced SOA in LFAK88

11 June 2024

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a LFAK88 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN1R9-80SSE delivers very low $R_{DS(on)}$ and enhanced safe operating area performance in a high-reliability copper-clip LFAK88 package.

PSMN1R9-80SSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low $R_{DS(on)}$ to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DS(on)}$ for low I^2R conduction losses
- LFAK88 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication and computing systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	80	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	286	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	340	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	1.6	1.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13		-	2.6	3	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		7	23	53	nC
Q _{G(tot)}	total gate charge			77	155	232	nC

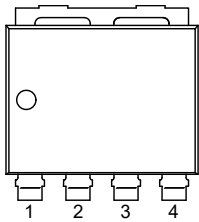
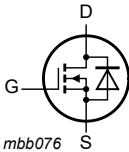
N-channel 80 V, 1.9 mOhm MOSFET with enhanced SOA in LFPAK88

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 90\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 179\text{ }\mu\text{s}$; Fig. 4	[1]	-	-	840	mJ
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 18	[2]	-	60	-	nC

[1] Protected by 100% test
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	 mbb076
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R9-80SSE	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R9-80SSE	X1E9S80S

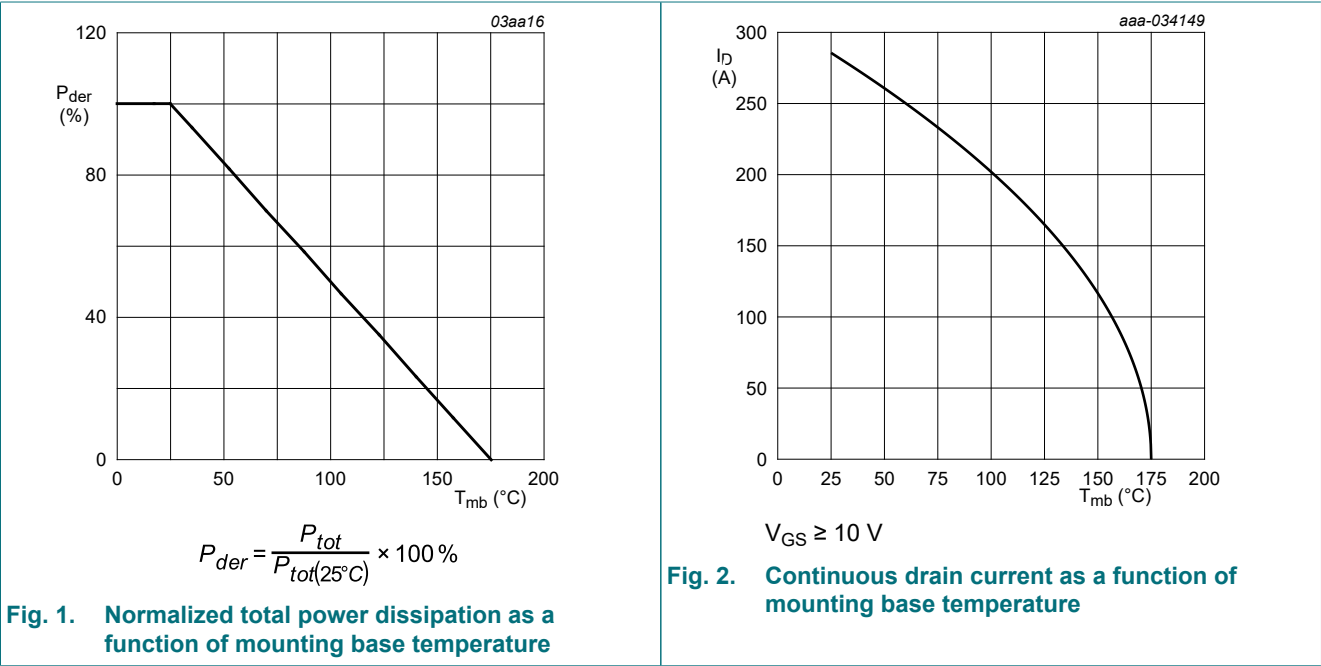
8. Limiting values

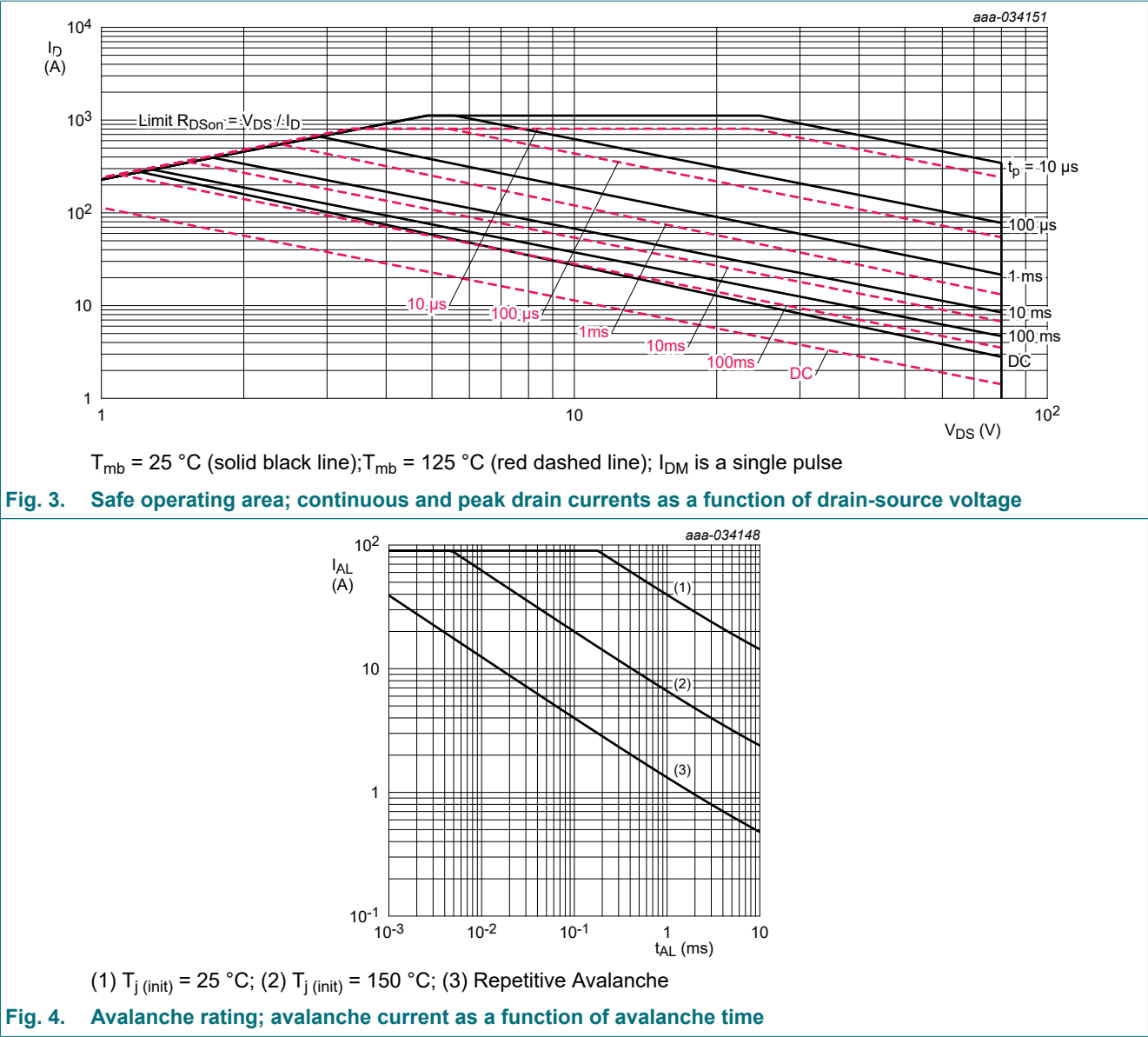
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	80	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	80	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	340	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	286	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	202	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1142	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	286	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1142	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 90 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 179 μs; Fig. 4	[1]	-	840	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 80 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	90	A

[1] Protected by 100% test





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.2	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	35	-	K/W
		Fig. 7	-	70	-	K/W

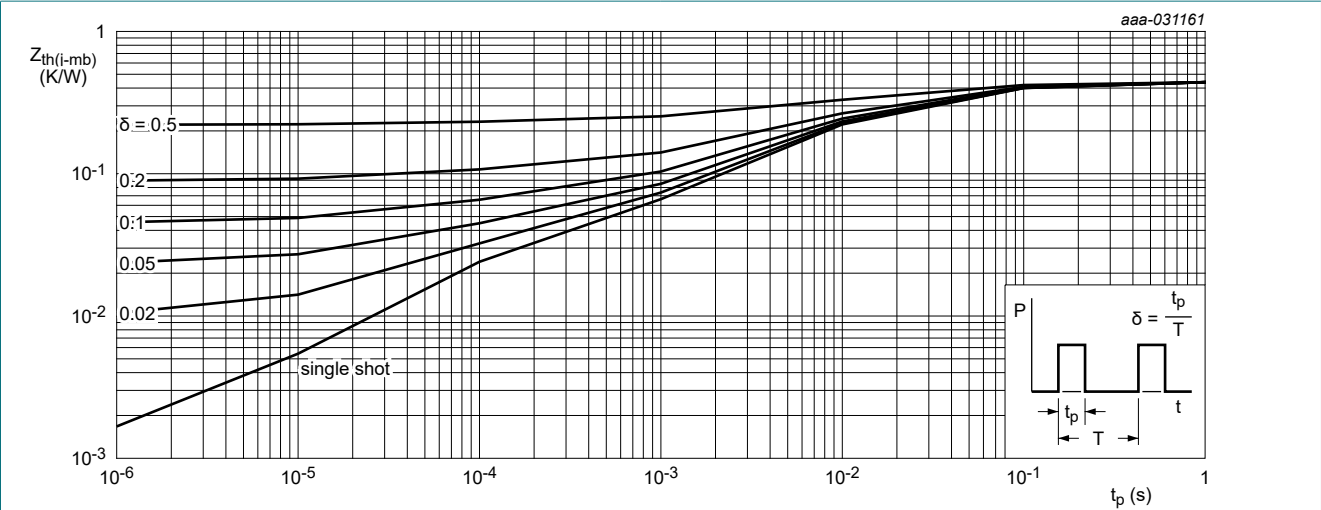
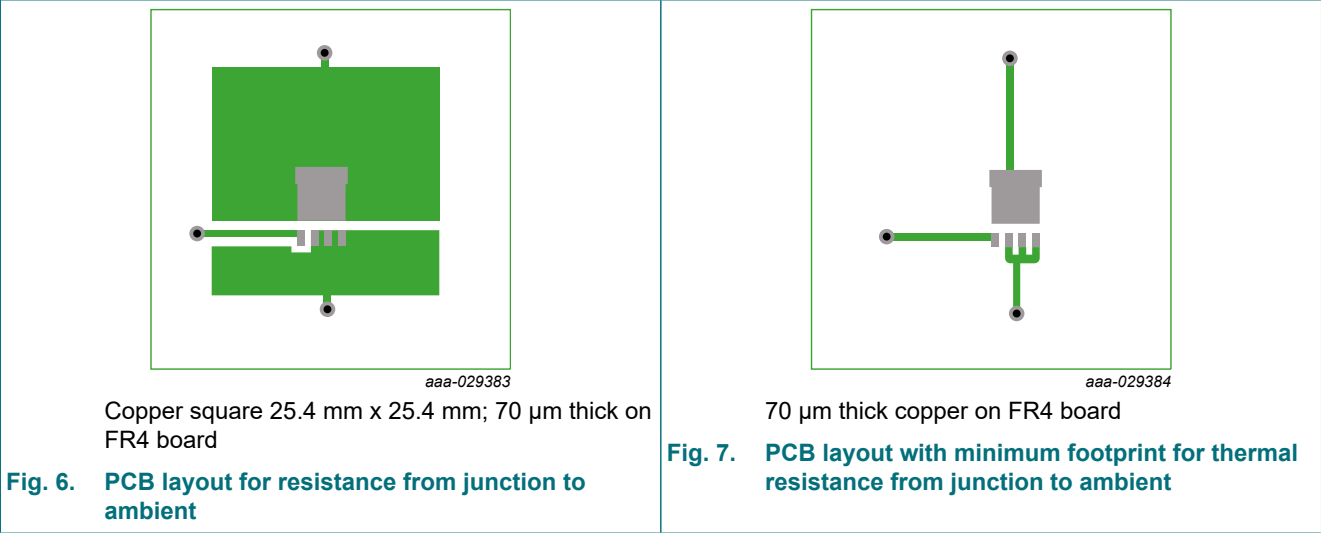


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		80	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		72	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 11		2	2.6	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C		-	1.6	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C		-	3	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 150 °C		-	-6.4	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _J = 25 °C		-	0.02	1	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _J = 125 °C		-	3	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12		-	1.6	1.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 100 °C; Fig. 13		-	2.6	3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 13		-	-	4.2	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.8	1.6	3.2	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		77	155	232	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		-	83	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		36	60	84	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	34	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	26	-	nC
Q _{GD}	gate-drain charge			7	23	53	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 40 V; T _J = 25 °C; Fig. 14 ; Fig. 15		-	5.2	-	V
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 0.5 MHz; T _J = 25 °C; Fig. 16		7340	12235	17140	pF
C _{oss}	output capacitance			1710	2843	4560	pF
C _{rss}	reverse transfer capacitance			7	64	169	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; R _L = 1.6 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	46	-	ns
t _r	rise time			-	42	-	ns
t _{d(off)}	turn-off delay time			-	79	-	ns
t _f	fall time			-	46	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17		-	0.78	1	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	54	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 18	[1]	-	60	-	nC

[1] includes capacitive recovery

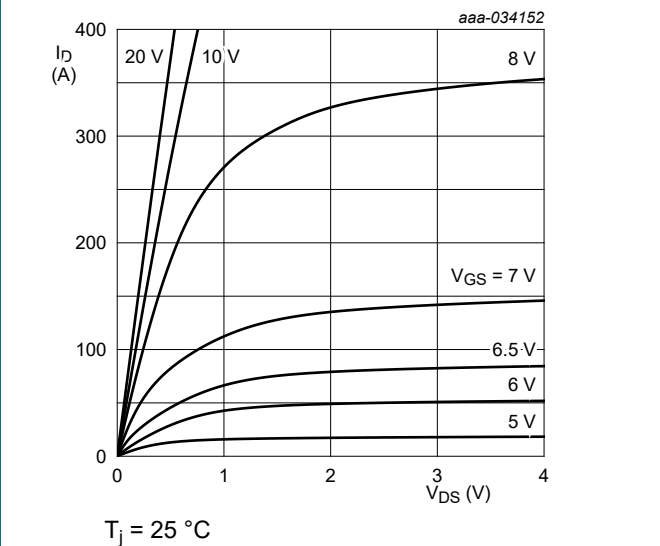


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

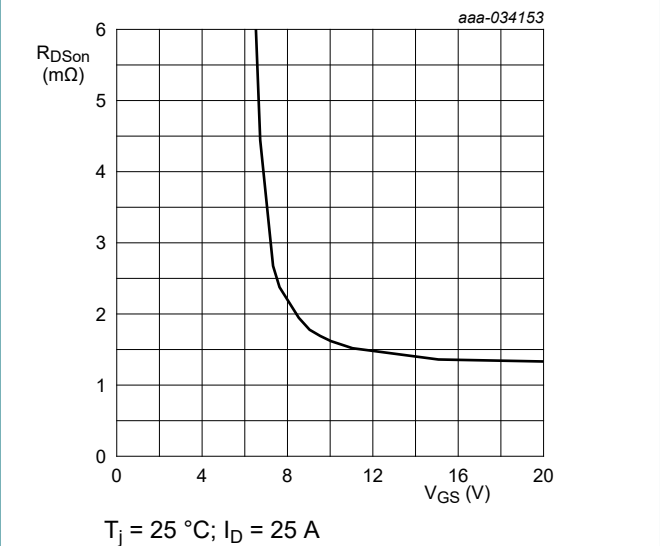


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

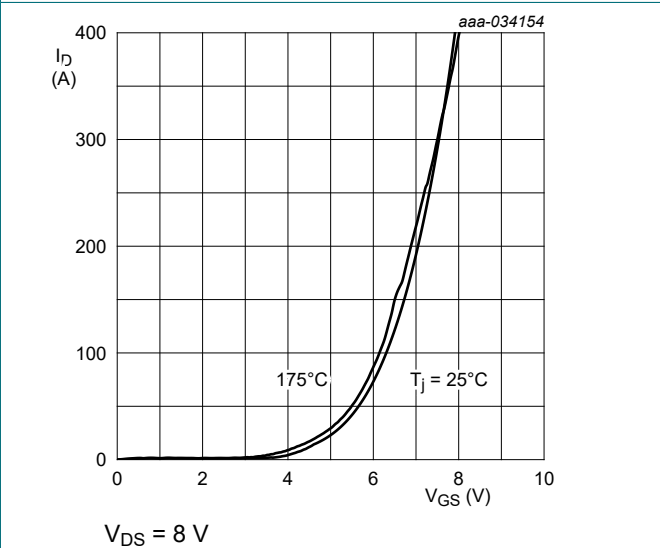


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

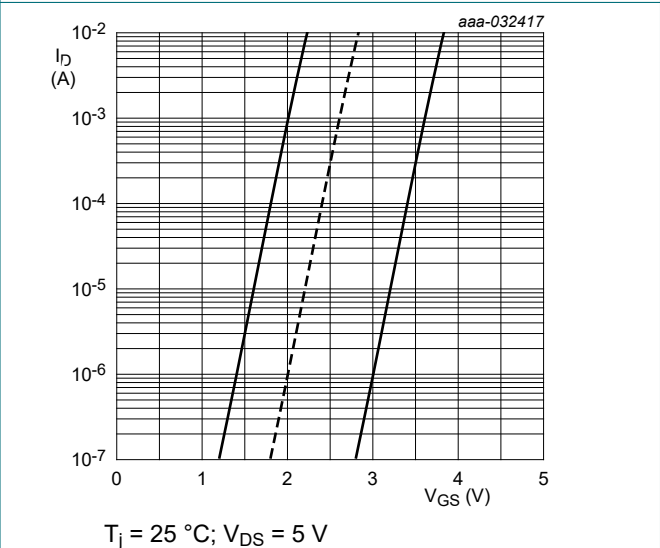


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

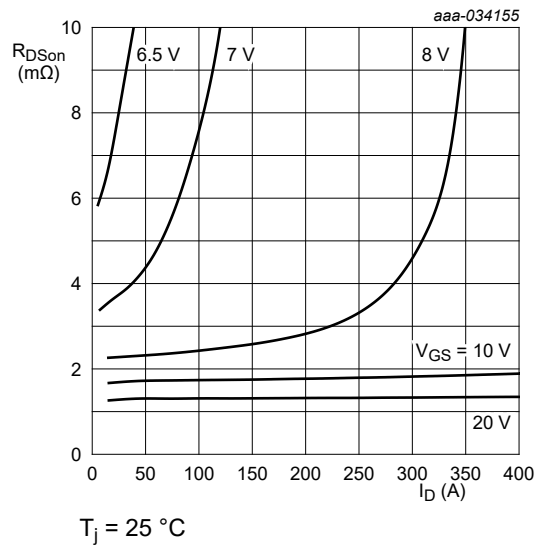


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

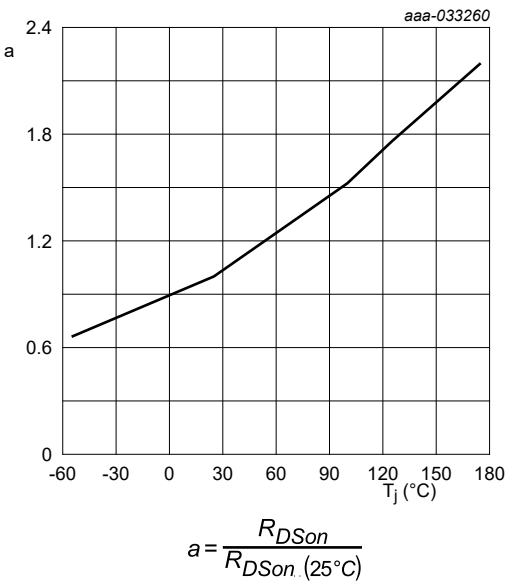


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

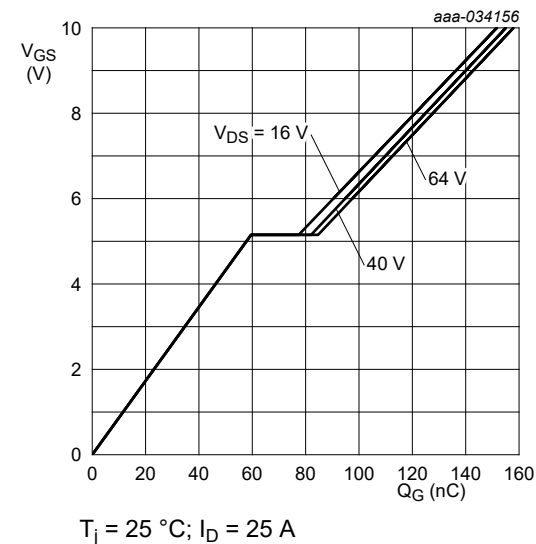


Fig. 14. Gate-source voltage as a function of gate charge; typical values

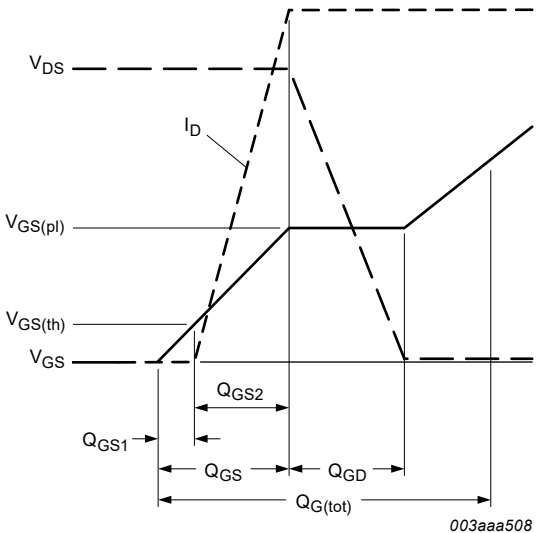


Fig. 15. Gate charge waveform definitions

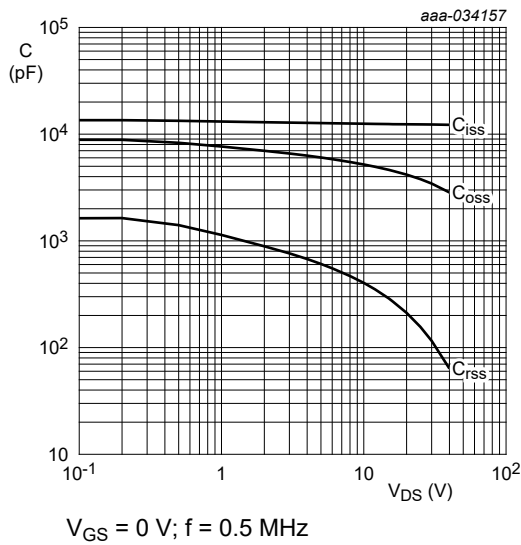


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

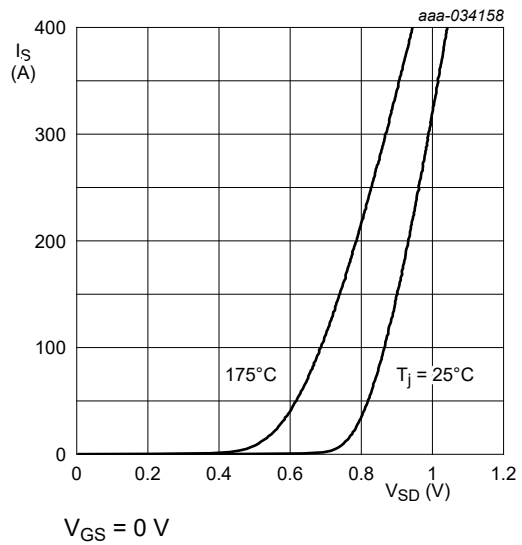


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

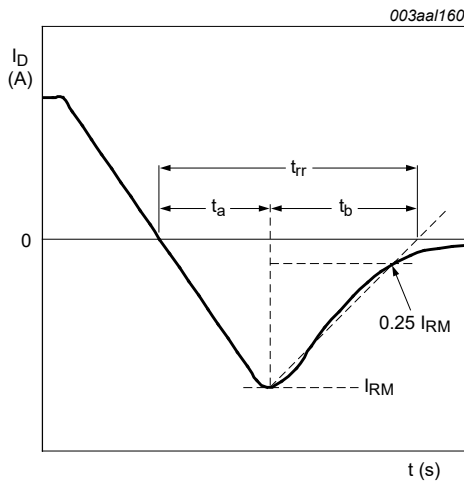


Fig. 18. Reverse recovery timing definition

11. Package outline

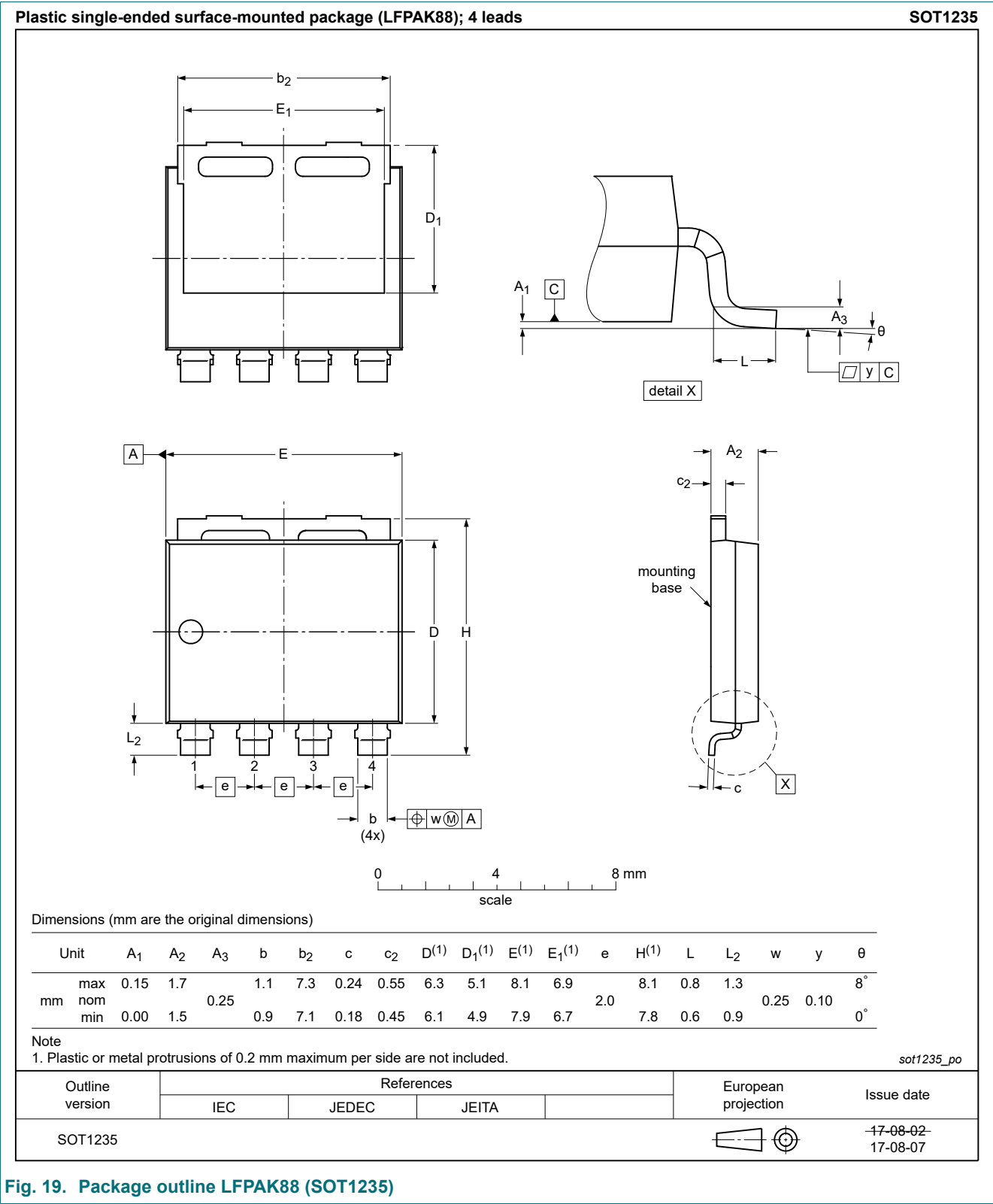


Fig. 19. Package outline LPAK88 (SOT1235)

12. Soldering

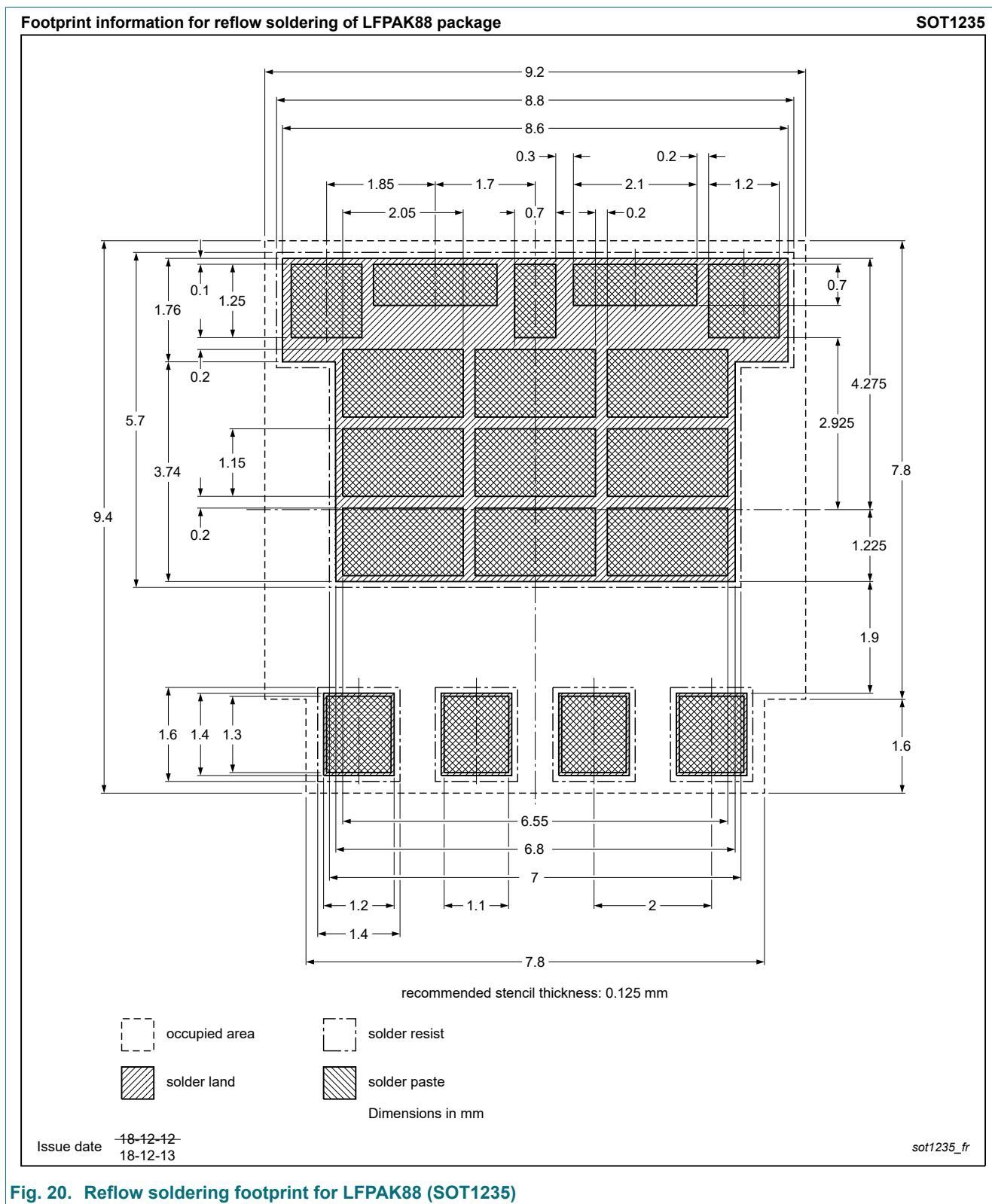


Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking..... 2

8. Limiting values..... 3

9. Thermal characteristics..... 4

10. Characteristics..... 6

11. Package outline..... 10

12. Soldering..... 11

13. Legal information.....12

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