PSMN1R0-100ASE

N-channel, 100 V, 1.04 mOhm, MOSFET with enhanced SOA in CCPAK1212 package

7 February 2024 **Objective data sheet**

1. General description

N-channel enhancement mode MOSFET in a CCPAK1212 package qualified to 175 °C.
Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN1R0-100ASE delivers very low R_{DSon} and enhanced safe operating area performance in a high-reliability copper-clip package (CCPAK1212).

PSMN1R0-100ASE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Opertating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- CCPAK1212 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	-	400	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	1.07	kW
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	0.82	1.04	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 2		-	49	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 3	[2]	-	122	-	nC

[1] Max current will be demonstrated through application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] includes capacitive recovery

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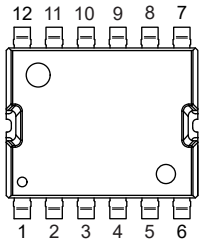
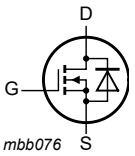
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 CCPAK1212 (SOT8000A)	
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-100ASE	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A

7. Limiting values

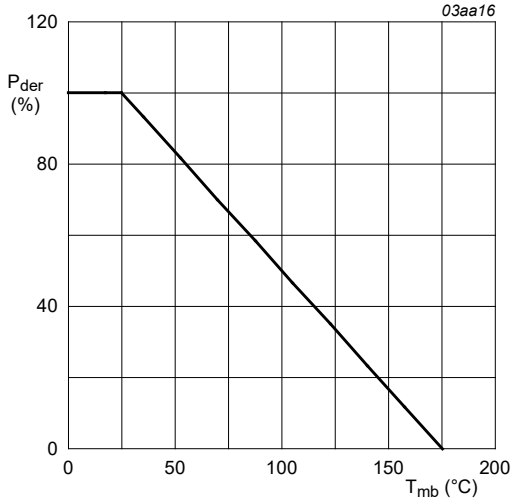
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	1.07	kW
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	400	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	282	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1600	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	400	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1600	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 116 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[2]	-	1561	mJ

[1] Max current will be demonstrated through application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	0.14	K/W

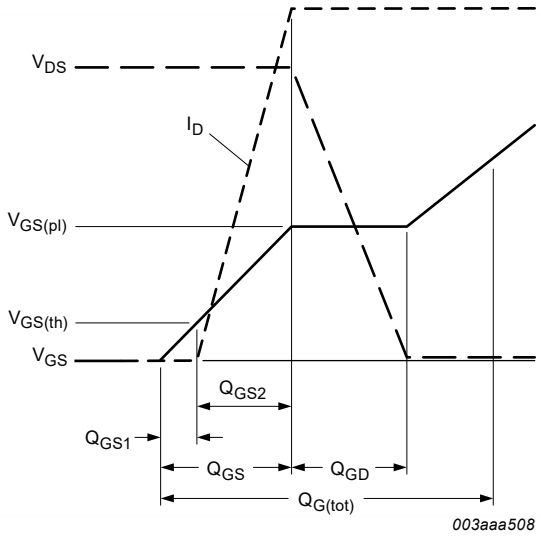
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2	2.6	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.6	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	5	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	[tbd]	[tbd]	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
				-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	0.82	1.04	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C		-	[tbd]	[tbd]	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		-	[tbd]	[tbd]	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	2.5	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 2		[tbd]	316	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	168	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 2		[tbd]	102	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C		-	68	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	34	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 2		-	49	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; T_j = 25 °C		-	[tbd]	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	24498	[tbd]	pF
C_{oss}	output capacitance			[tbd]	5222	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	69	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	77	-	ns
t_r	rise time			-	74	-	ns
$t_{d(off)}$	turn-off delay time			-	187	-	ns
t_f	fall time			-	104	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 3		-	87	-	ns
Q_r	recovered charge		[1]	-	122	-	nC

[1] includes capacitive recovery



T_j = 25 °C; I_D = A

Fig. 2. Gate-source voltage as a function of gate charge; typical values

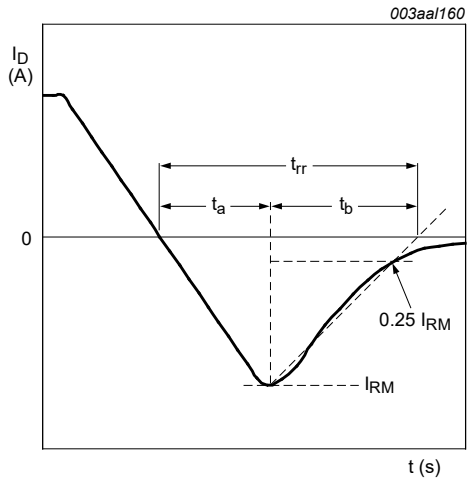
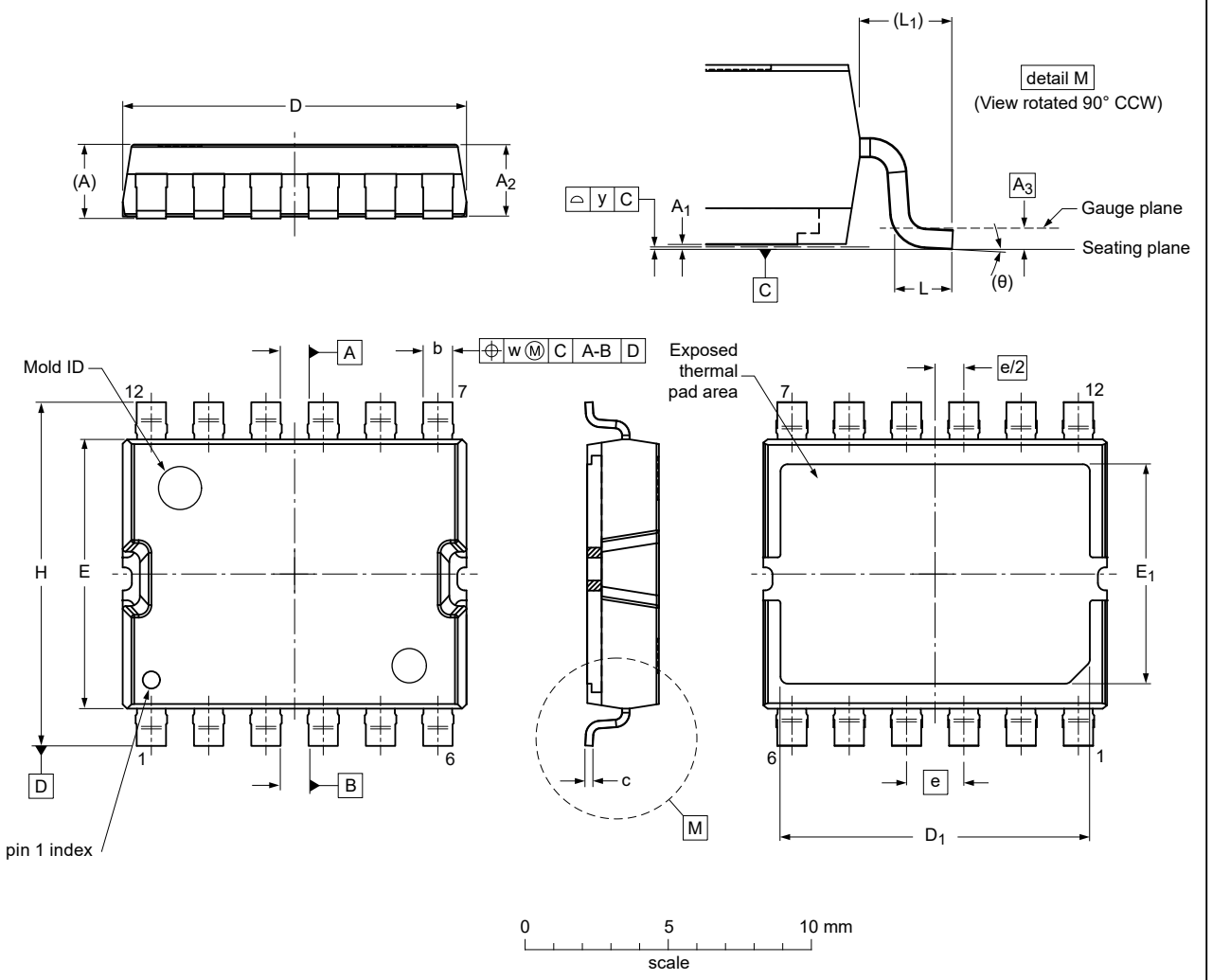


Fig. 3. Reverse recovery timing definition

10. Package outline

Plastic, surface mounted copper clip package (CCPAK1212);
13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body **SOT8000A**



Dimensions (mm are the original dimensions)

Unit[1]		A(ref)	A_1	A_2	A_3	b	c	D	D_1	E	E_1	e	H	L	L_1(ref)	w	y	θ(ref)
mm	max		0.13	2.65		1.12	0.30	12.15	10.95	9.55	7.40		12.15	1.0				
	nom	2.75			0.25							2.0			1.3	0.20	0.1	4°
	min		0	2.4		0.93	0.22	11.85	10.65	9.25	7.10		11.85	0.6				

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included for dimension E.

sot8000a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8000A						~~23-09-28~~ 23-12-12

Fig. 4. Package outline CCPAK1212 (SOT8000A)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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