



# PSMN041-80YL

N-channel 80 V 41 mΩ logic level MOSFET in LPAK56

1 May 2013

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in LPAK56 package. This product has been designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive
- LPAK56 package is footprint compatible with other Power-SO8 types
- Qualified to 175 °C

## 3. Applications

- DC-to-DC converters
- Load switch
- TV power supplies

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>J</sub> ≥ 25 °C; T <sub>J</sub> ≤ 175 °C		-	-	80	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <a href="#">Fig. 1</a>		-	-	25	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	-	64	W
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 12</a>		-	32.8	41	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 12</a>		-	-	103	mΩ
Dynamic characteristics							
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; V <sub>DS</sub> = 64 V;		-	4.3	-	nC
Q <sub>G(tot)</sub>	total gate charge	T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	21.9	-	nC



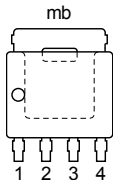
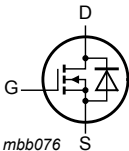
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 25\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a>	-	-	23.9	mJ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN041-80YL	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN041-80YL	04180

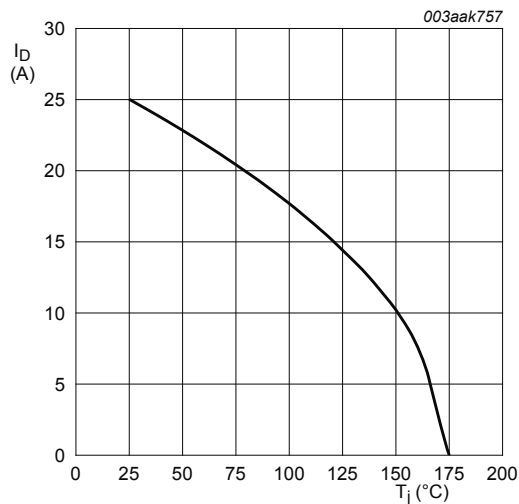
## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

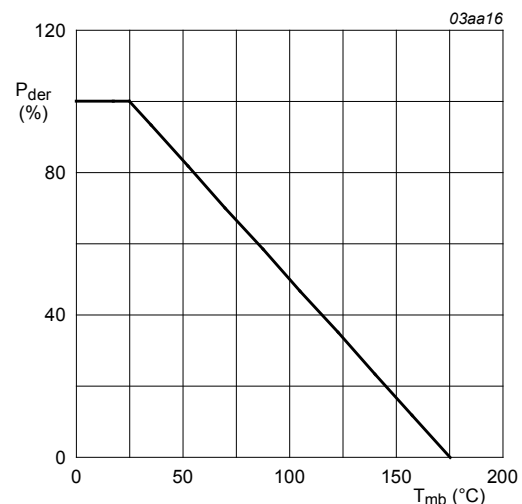
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 1</a>	-	18	A

Symbol	Parameter	Conditions		Min	Max	Unit
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	25	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 4</a>		-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>		-	64	W
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	54	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	100	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 25\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a>		-	23.9	mJ



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 10V$$



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

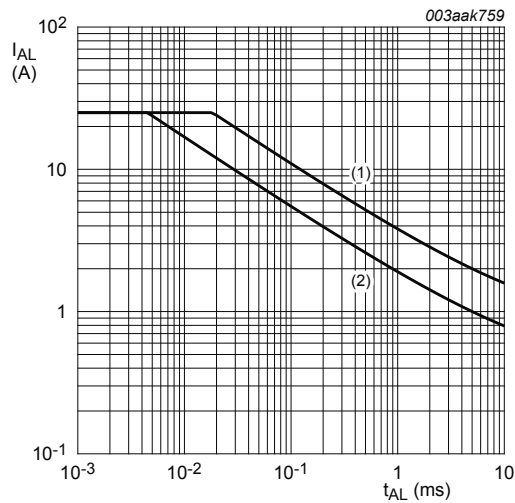


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j(jnt)} = 25^{\circ}C$ ; (2)  $T_{j(jnt)} = 100^{\circ}C$

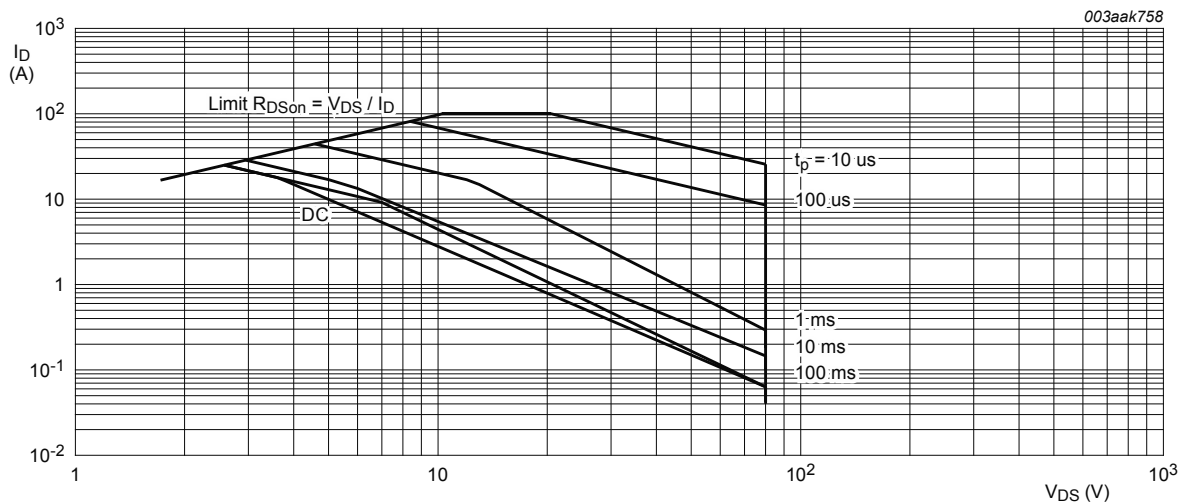


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.13	2.33	K/W

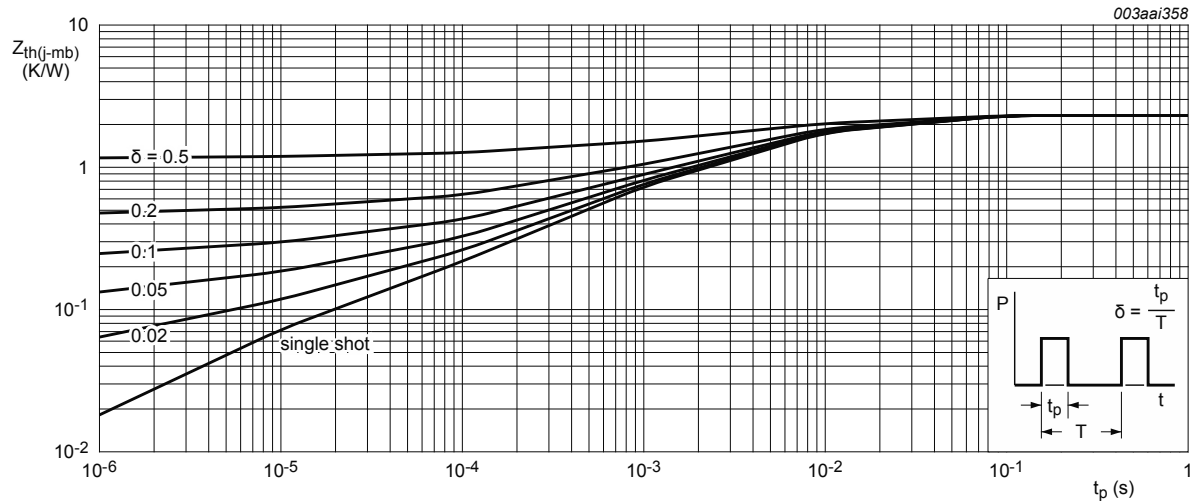


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_J = -55 ^\circ C$	72	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_J = 25 ^\circ C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_J = 175 ^\circ C$ ; <a href="#">Fig. 10</a>	0.5	-	-	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_J = -55 ^\circ C$ ; <a href="#">Fig. 10</a>	-	-	2.45	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_J = 25 ^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	1.4	1.7	2.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 V$ ; $V_{GS} = 0 V$ ; $T_J = 25 ^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 80 V$ ; $V_{GS} = 0 V$ ; $T_J = 175 ^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -16 V$ ; $V_{DS} = 0 V$ ; $T_J = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = 16 V$ ; $V_{DS} = 0 V$ ; $T_J = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 5 A$ ; $T_J = 25 ^\circ C$ ; <a href="#">Fig. 12</a>	-	32.8	41	mΩ
		$V_{GS} = 5 V$ ; $I_D = 5 A$ ; $T_J = 175 ^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 12</a>	-	-	113	mΩ
		$V_{GS} = 10 V$ ; $I_D = 5 A$ ; $T_J = 175 ^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 12</a>	-	-	103	mΩ
		$V_{GS} = 5 V$ ; $I_D = 5 A$ ; $T_J = 25 ^\circ C$ ; <a href="#">Fig. 12</a>	-	35.7	45	mΩ
$R_G$	gate resistance	$f = 1 MHz$	-	2.02	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	21.9	-	nC
		I <sub>D</sub> = 5 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	11.9	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	2.5	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge			-	1.7	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge			-	0.8	-	nC
Q <sub>GD</sub>	gate-drain charge			-	4.3	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 64 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	2.4	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>		-	1180	-	pF
C <sub>oss</sub>	output capacitance			-	99	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	54	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 60 V; R <sub>L</sub> = 10 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C		-	8.6	-	ns
t <sub>r</sub>	rise time			-	11.2	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	16.1	-	ns
t <sub>f</sub>	fall time			-	10.5	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>		-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 5 A; dI <sub>S</sub> /dt = 100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C		-	21.3	-	ns
Q <sub>r</sub>	recovered charge			-	22	-	nC

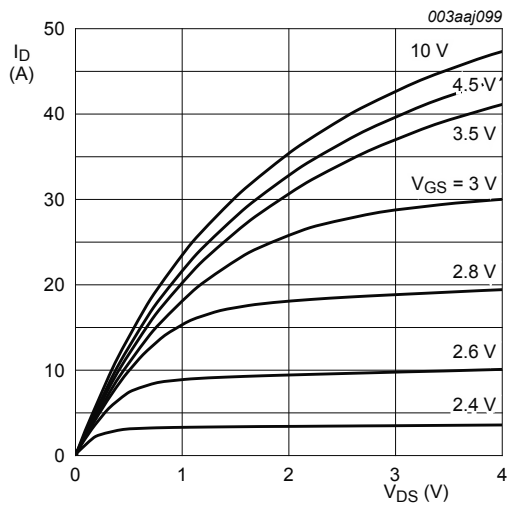


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

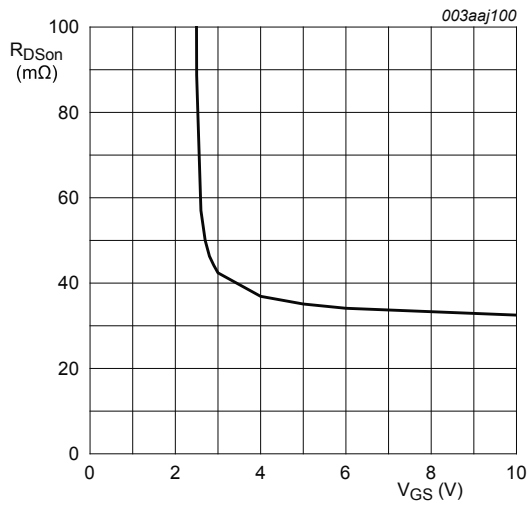


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

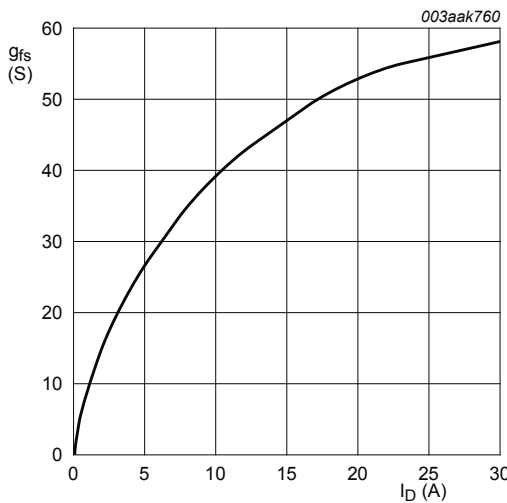


Fig. 8. Forward transconductance as a function of drain current; typical values

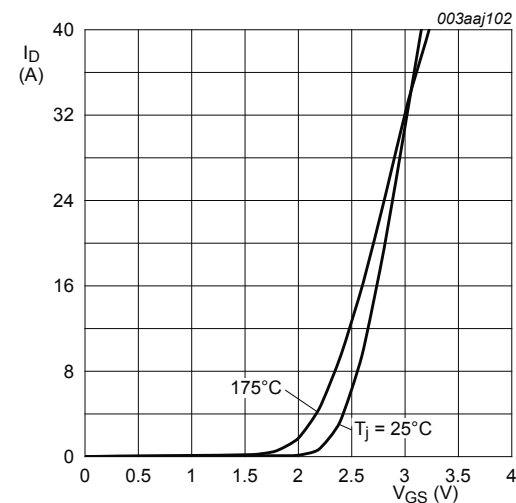
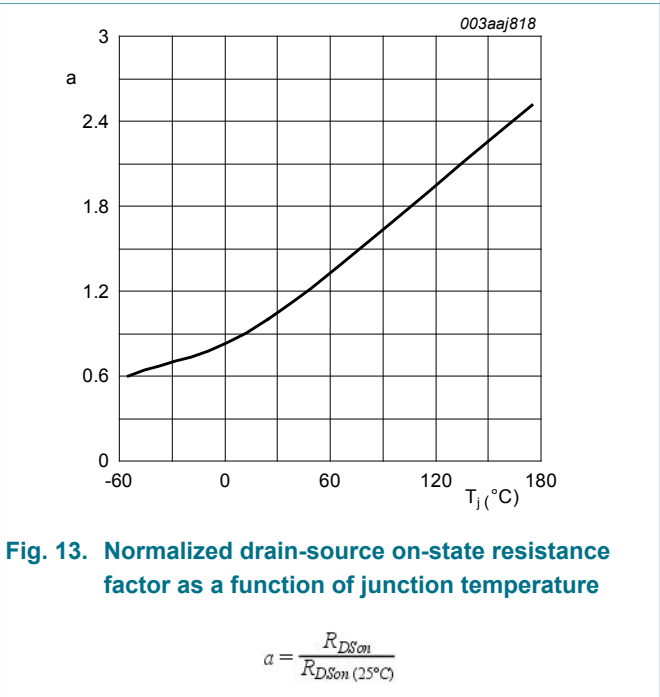
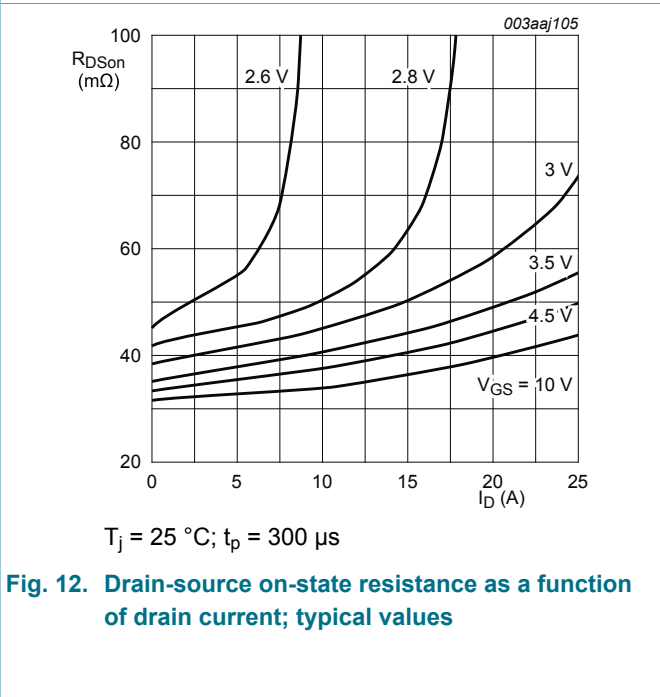
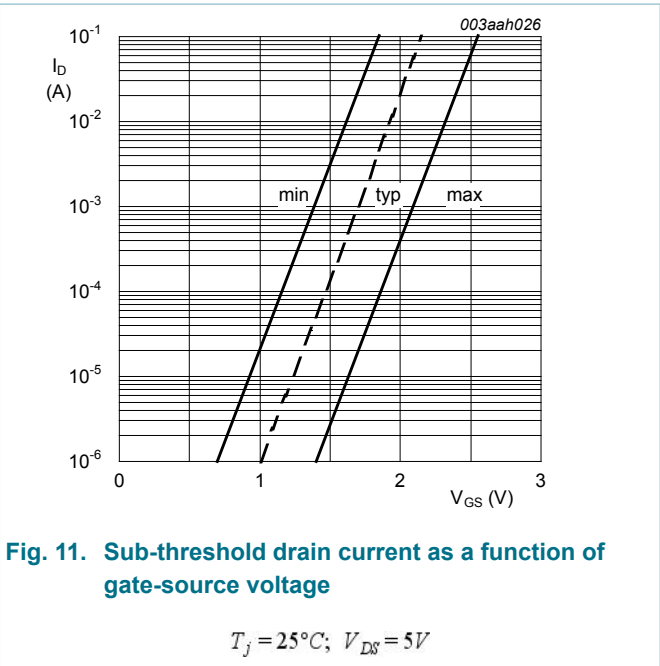
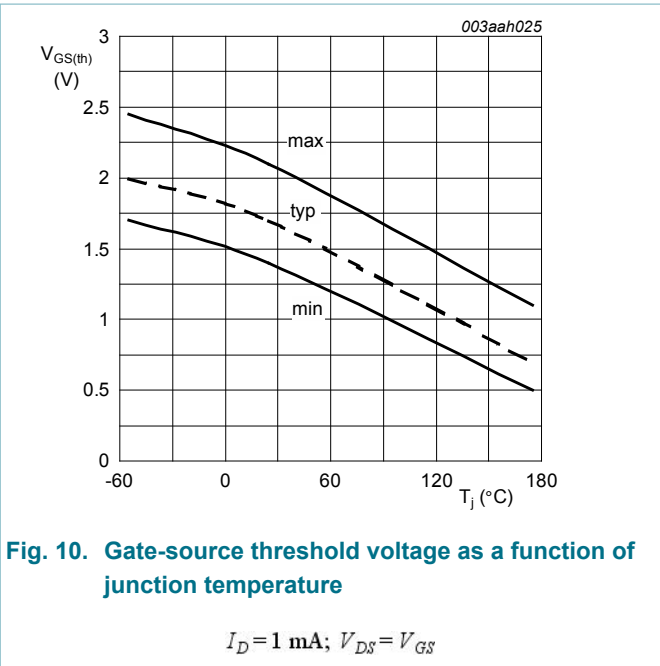


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values





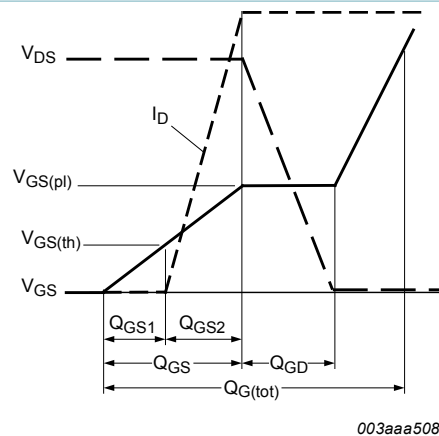


Fig. 14. Gate charge waveform definitions

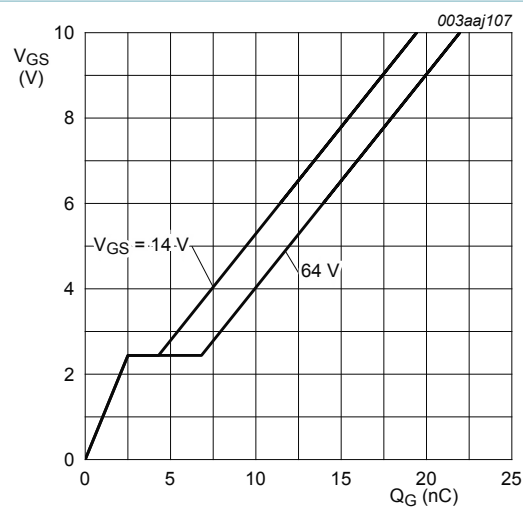


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$

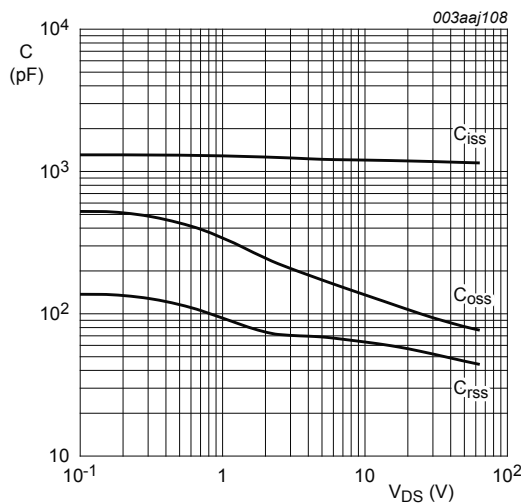


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

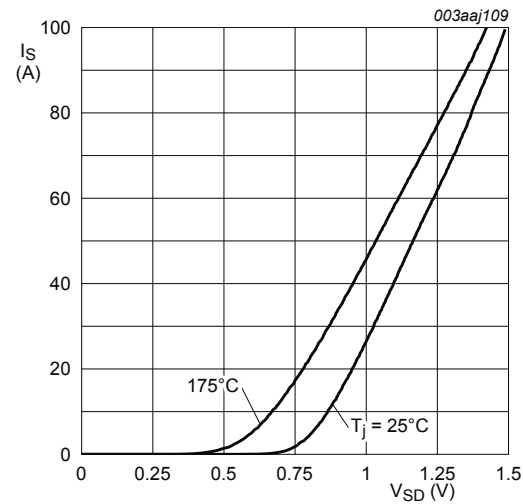


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

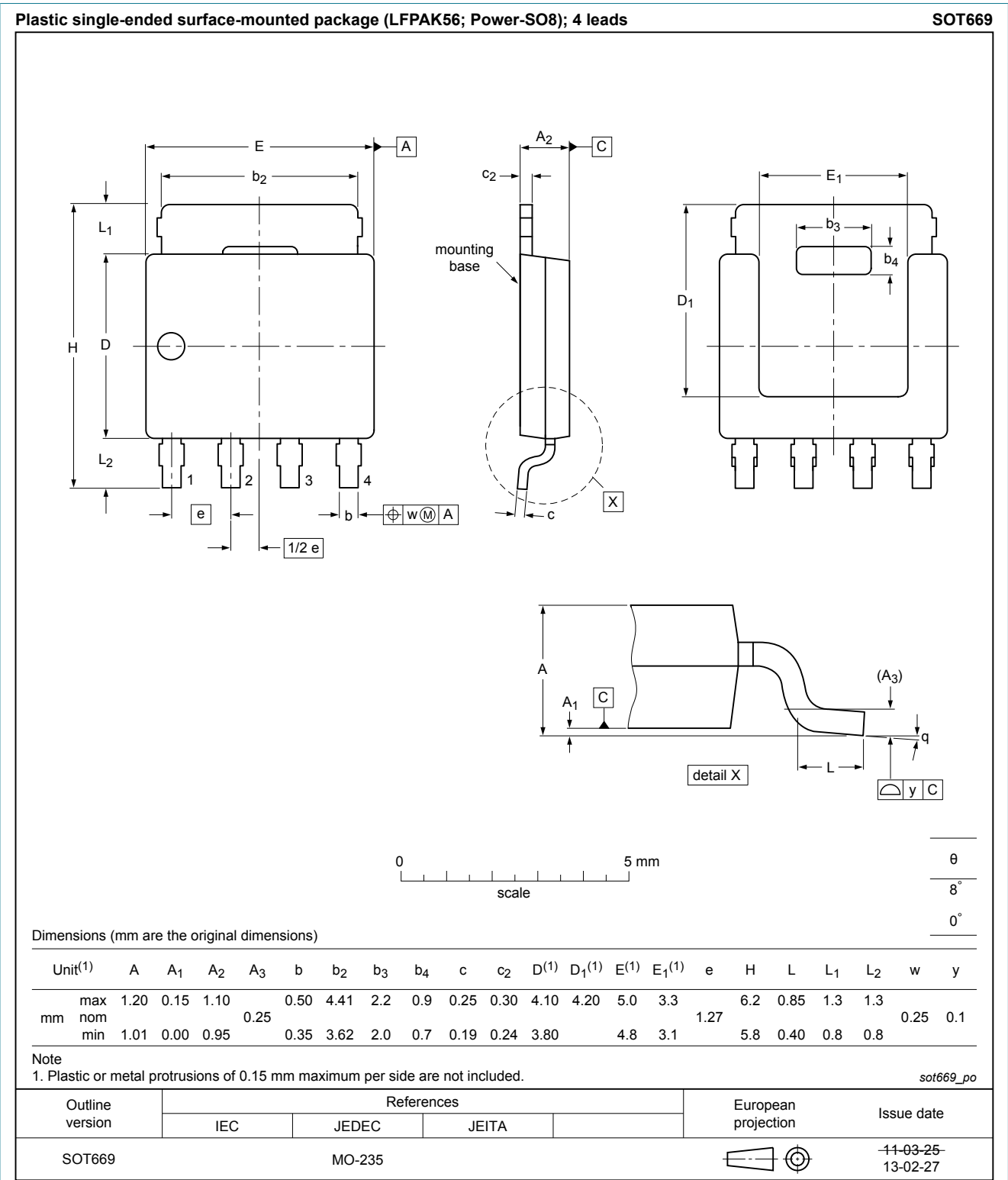


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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