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ISDN PC Adapter Circuit
IPAC

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1 Overview

The ISDN PC Adapter Circuit IPAC integrates all necessary functions for a host based ISDN access solution on a single chip.

It includes the S-transceiver (Layer 1), an HDLC controller for the D-channel and two protocol controllers for each B-channel. They can be used for HDLC protocol or transparent access. The system integration is simplified by several host interface configurations selected via pin strapping. They include multiplexed and demultiplexed interface options as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations.

The IPAC combines the functions of the ISDN Subscriber Access Controller (ISAC-S PEB 2086) and the High-Level Serial Communications Controller Extended for Terminals (HSCX-TE PSB 21525) providing additional features and enhanced functionality.

The FIFO size of the B-channel buffers is 2x64 bytes per channel and per direction. The S-transceiver supports other terminal relevant operation modes like line termination subscriber side (LT-S) and line termination trunk side (LT-T). A multi-line ISDN solution to support both S and U (2B1Q) line coding is simplified as well as multi-line solution with up to 3 S-interfaces.

An auxiliary I/O port has been added with interrupt capabilities on two input lines. These programmable I/O lines may be used to connect a DTMF receiver or other peripheral components to the IPAC which need software control or have to forward status information to the host. Peripheral data controllers can transfer data on a PCM interface which is mapped into the B-channels on the IOM-2 interface.

Three programmable LED outputs can be used to indicate certain status information, one of them is capable to indicate the activation status of the S-interface automatically.

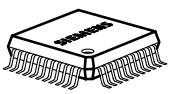
The IPAC is produced in advanced CMOS technology.

SIEMENS

ISDN PC Adapter Circuit **PSB 2115**
IPAC **PSF 2115**

Version 1.1 **CMOS**

1.1 Features



P-MQFP-64

P-TQFP-64

- Single chip host based ISDN solution
- Integrates S-transceiver, D-channel, B-channel protocol controller
- Replaces solutions based on ISAC-S TE PSB 2186 and HSCX-TE PSB 21525
- Easy adjustment of software using ISAC-S and HSCX-TE
- Various types of protocol support depending on operating mode (Non-auto mode, transparent mode)
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- Enlarged FIFO buffers (2x64 byte) per B-channel and per direction
- S-transceiver with TE, LT-S and LT-T modes
- D-channel FIFO buffers with 2x32byte
- D-channel access mechanism in all modes
- D-channel priority handler on IOM-2 for intelligent NT applications
- Software reset (required for Windows95)
- Programmable I/O interface with 2 interrupt inputs
- PCM interface for non IOM-2 compatible peripheral data controllers
- Programmable timer (1 ... 63 ms) for continuous or single interrupts
- Reduced register address space due to indirect address mode option
- 3 programmable LED outputs, one can indicate S bus activation status automatically
- 8-bit multiplexed or demultiplexed bus interface
- Siemens/Intel or Motorola µP interface

1.2 Logic Symbol

The logic symbol shows all functions of the IPAC. It must be noted, that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.

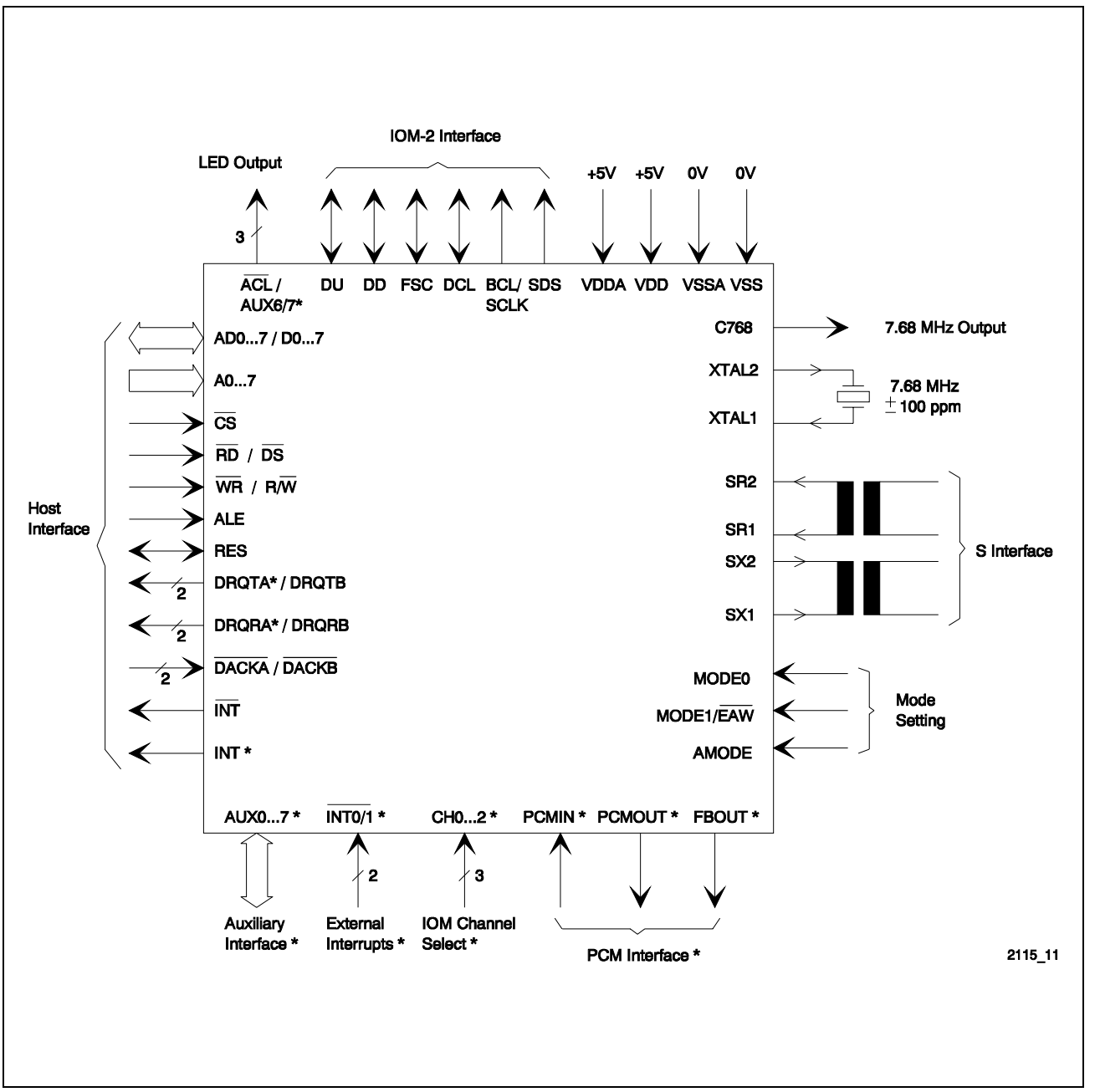


Figure 1 Logic Symbol

1.3 Pin Configuration

Figure 2 shows the pin configuration for P-MQFP-64 and for P-TQFP-64 packages.

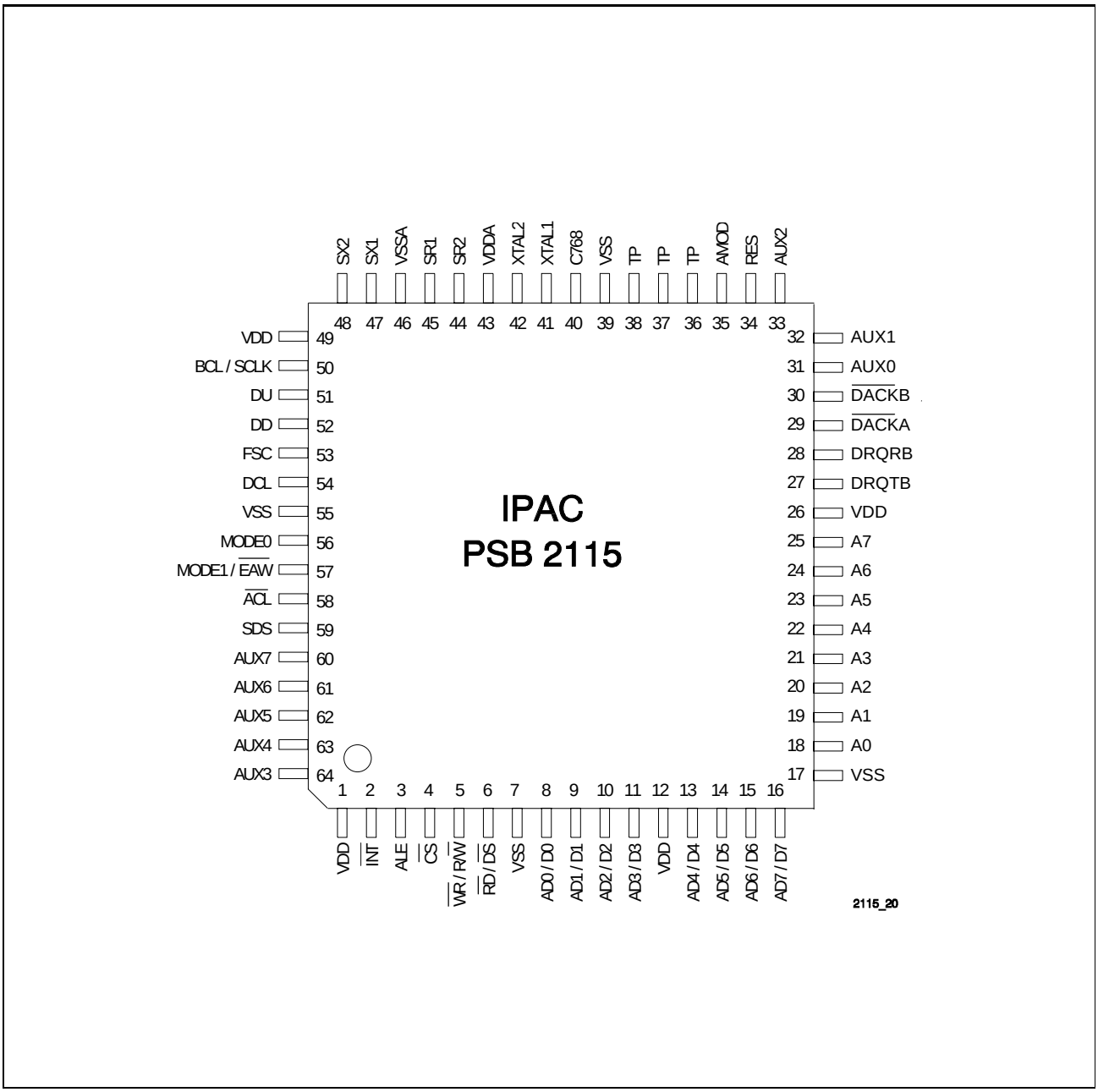


Figure 2 Pin Configuration

1.4 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Microprocessor Interface			
8 9 10 11 13 14 15 16	AD0-7 D0...7	I/O I/O	**Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the host system to the IPAC and data between the host system and the IPAC. **Non-Multiplexed Bus Mode:** **Data bus.** Transfers data between the host system and the IPAC.
18 19 20 21 22 23 24 25	A0-A7	I	**Non-Multiplexed Bus Mode:** Address bus transfers addresses from the host system to the IPAC. For indirect address mode only A0 is valid. **Multiplexed Bus Mode** Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD.
6	$\overline{RD}$ $\overline{DS}$	I I	**Read** Indicates a read access to the registers (Intel bus mode). **Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
5	$\overline{WR}$ R/$\overline{W}$	I I	**Write** Indicates a write access to the registers (Intel bus mode). **Read/Write** A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).
4	$\overline{CS}$	I	**Chip Select** A LOW on this line selects the IPAC for a read/write operation.

Pin No.	Symbol	Input (I) Output (O)	Function
3	ALE	I	**Address Latch Enable** A HIGH on this line indicates an address on the external address/data bus (multiplexed bus type only). ALE also selects the microprocessor interface type (multiplexed or non multiplexed).
2	$\overline{\text{INT}}$	OD	**Interrupt Request** This low active signal is activated when the IPAC requests an interrupt. It is an open drain output.
27	DRQTB	O	**DMA Request Transmitter** (channel B) The transmitter of the IPAC requests DMA data transfer by activating this line. The DRQTB remains HIGH as long as the transmit FIFO requires data transfer. The amount of data bytes to be transferred from system memory to the IPAC (= byte count) must be written first to the XBCH, XBCL register. Always blocks of data (n x 64 bytes + REST, n=0, 1, ..) are transferred till the byte count is reached. DRQTB is deactivated immediately following the falling edge of the last $\overline{\text{WR}}$ cycle. Note: To support DMA for channel A, the DRQTA line is available in TE mode only (see pin AUX0).
28	DRQRB	O	**DMA Request Receiver** (channel B) The receiver of the IPAC requests DMA data transfer by activating this line. The DRQRB remains HIGH as long as the receive FIFO requires data transfer, thus always blocks of data (64, 32, 16, 8 or 4 bytes) are transferred. DRQRB is deactivated immediately following the falling edge of the last read cycle. Note: To support DMA for channel A, the DRQRA line is available in TE mode only (see pin AUX1).

Pin No.	Symbol	Input (I) Output (O)	Function
29 30	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/B) When LOW, this input signal from the DMA controller indicates to the IPAC, that the requested DMA cycle controlled via DRQTA/B and DRQRA/B is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with $\overline{\text{RD}}$, if DMA has been requested from the receiver, or with $\overline{\text{WR}}$, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If $\overline{\text{DACKA/B}}$ is active, the input on pins A0-7 is ignored and the FIFO's are implicitly selected. If the $\overline{\text{DACKA/B}}$ signals are not used, these pins must be connected to VDD.

Auxiliary Interface

31	AUX0	I/O	**Auxiliary Port 0** **TE-Mode: DRQTA (output)** **DMA Request Transmitter** (channel A) The transmitter of the IPAC requests DMA data transfer by activating this line. The DRQTA remains HIGH as long as the transmit FIFO requires data transfer. The amount of data bytes to be transferred from system memory to the IPAC (= byte count) must be written first to the XBCH, XBCL register. Always blocks of data (n x 64 bytes + REST, n=0, 1, ..) are transferred till the byte count is reached. DRQTA is deactivated immediately following the falling edge of the last $\overline{\text{WR}}$ cycle. **LT-T/LT-S Mode: CH0 (input)** **IOM-2 Channel Select 0** Together with CH1 (pin AUX1) and CH2 (pin AUX2), this pin selects one of eight channels on the IOM-2 interface.

Pin No.	Symbol	Input (I) Output (O)	Function
32	AUX1	I/O	**Auxiliary Port 1** **TE-Mode: DRQRA (output)** **DMA Request Receiver** (channel A) The receiver of the IPAC requests DMA data transfer by activating this line. The DRQRA remains HIGH as long as the receive FIFO requires data transfer, thus always blocks of data (64, 32, 16, 8 or 4 bytes) are transferred. DRQRA is deactivated immediately following the falling edge of the last read cycle. **LT-T/LT-S Mode: CH1 (input)** **IOM-2 Channel Select 1** Together with CH0 (pin AUX0) and CH2 (pin AUX2), this pin selects one of eight channels on the IOM-2 interface.
33	AUX2	I/O	**Auxiliary Port 2** **TE-Mode: AUX2 (input)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **TE-Mode: INT (output)** This high active signal is activated when the IPAC requests an interrupt (invers polarity of $\overline{\text{INT}}$ line). **LT-T/LT-S Mode: CH2 (input)** **IOM-2 Channel Select 2** Together with CH0 (pin AUX0) and CH1 (pin AUX1), this pin selects one of eight channels on the IOM-2 interface.

Pin No.	Symbol	Input (I) Output (O)	Function
64	AUX3	I/O	**Auxiliary Port 3** **TE-Mode: AUX3 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: FBOUT (output)** **FSC/BCL Output** This pin is programmable to output either an FSC clock which is derived from the DCL input divided by 192 (in LT-T: SCLK output provides 1.536 MHz) or a single bit clock from the IOM-2 interface, especially to serve non IOM-2 compatible peripheral devices on the PCM interface.
63	AUX4	I/O	**Auxiliary Port 4** **TE-Mode: AUX4 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: PCMIN (input)** **PCM Data Input** On this line the IPAC receives 8-bit data, which is transmitted from a peripheral device. This data is mapped to a B-Channel timeslot on IOM-2.
62	AUX5	I/O	**Auxiliary Port 5** **TE-Mode: AUX5 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S Mode: PCMOUT (output)** **PCM Data Output** On this line the IPAC transmits 8-bit data, which is received by a peripheral device. This data is taken from a B-Channel timeslot on IOM-2.

Pin No.	Symbol	Input (I) Output (O)	Function
61 60	AUX6 AUX7	I/O	**Auxiliary Port 6/7** **All Modes: $\overline{\text{INT0/1}}$** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. Additionally, as input they can generate a maskable interrupt to the host, which is either edge or level triggered. An internal pull up resistor is connected to these pins. As outputs an LED can directly be connected to these pins. **LT-T mode:** AUX7 can also be programmed to output the S/G bit signal from the IOM-2 DD line (LT-T mode only).

IOM-2 Interface

53	FSC	I/O	**Frame Sync** Synchronisation signal. The rising edge indicates the beginning of the IOM frame (HIGH during channel 0 in TE mode).
54	DCL	I/O	**Data Clock** IOM clock signal of twice the IOM data rate. The first rising edge is used to transmit data, the second falling edge is used to sample data.
51	DU	I/O(OD)	**Data Upstream** IOM data signal in upstream direction.
52	DD	I/O (OD)	**Data Downstream** IOM data signal in downstream direction.
50	BCL/ SCLK	O	**Bit Clock/S-clock** **TE-Mode:** Bit clock output, identical to IOM data rate. **LT-T Mode:** 1.536 MHz output synchronous to S-interface. **LT-S Mode:** Bit clock output derived from the DCL input clock divided by 2.

Pin No.	Symbol	Input (I) Output (O)	Function
59	SDS	O	**Serial Data Strobe** Programmable strobe signal, selecting either one or two channels (8 or 16 bit strobe length) on the IOM-2 or PCM interface.

Miscellaneous

34	RES	I/O	**Reset** A HIGH on this input forces the IPAC into a reset state. The minimum pulse length is four DCL-clock periods or four ms (see **table 29**). If the terminal specific functions are enabled, the IPAC may also supply a reset signal.
35	AMODE	I	**Address Mode** Selects between direct and indirect register access. A HIGH selects indirect address mode and a LOW selects the direct register access.
56	MODE0	I	**Mode 0 Select** A LOW selects TE-mode and a HIGH selects LT-T and LT-S mode (see MODE1/$\overline{\text{EAW}}$).
57	MODE1 $\overline{\text{EAW}}$	I I	**Mode 1 Select / External Awake** The pin function depends on the setting of MODE0. If MODE0=1: **Mode 1 Select** A LOW selects LT-S mode and a HIGH selects LT-T mode. If MODE0=0: **External Awake** If a falling edge on this input is detected, the IPAC generates an interrupt and, if enabled, a reset pulse.
58	$\overline{\text{ACL}}$	O	**Activation LED** This pin can either function as a programmable output or automatically indicate the activated state of the S interface by a logic ’0’. An LED with pre-resistance may directly be connected to $\overline{\text{ACL}}$.
47 48	SX1 SX2	O O	**S-Bus Transmitter Output** Differential output for the S-transmitter. positive negative

Pin No.	Symbol	Input (I) Output (O)	Function
45 44	SR1 SR2	I I	**S-Bus Receiver Input** Differential inputs for the S-receiver.
41	XTAL1	I	**Oscillator Input** Input pin of oscillator or input from external clock source. 7.68 MHz crystal or clock required.
42	XTAL2	O	**Oscillator Output** Output pin of oscillator. Not connected if external clock source is used.
40	C768	O	**Clock Output** A 7.68 MHz clock is output to support other devices, e.g. further IPACs in a multiline application. This clock is not synchronous to the S interface.
36 37 38	TP	I	Test Pins. These pins are not used for normal operation. They must be connected to GND.

Power Supply

1 12 26 49	VDD	I	Digital Supply Voltage +5V (+/- 5%)
43	VDDA	I	Analog Supply voltage +5V (+/- 5%)
7 17 39 55	VSS	I	Digital GND
46	VSSA	I	Analog GND

1.5 Functional Block Diagram

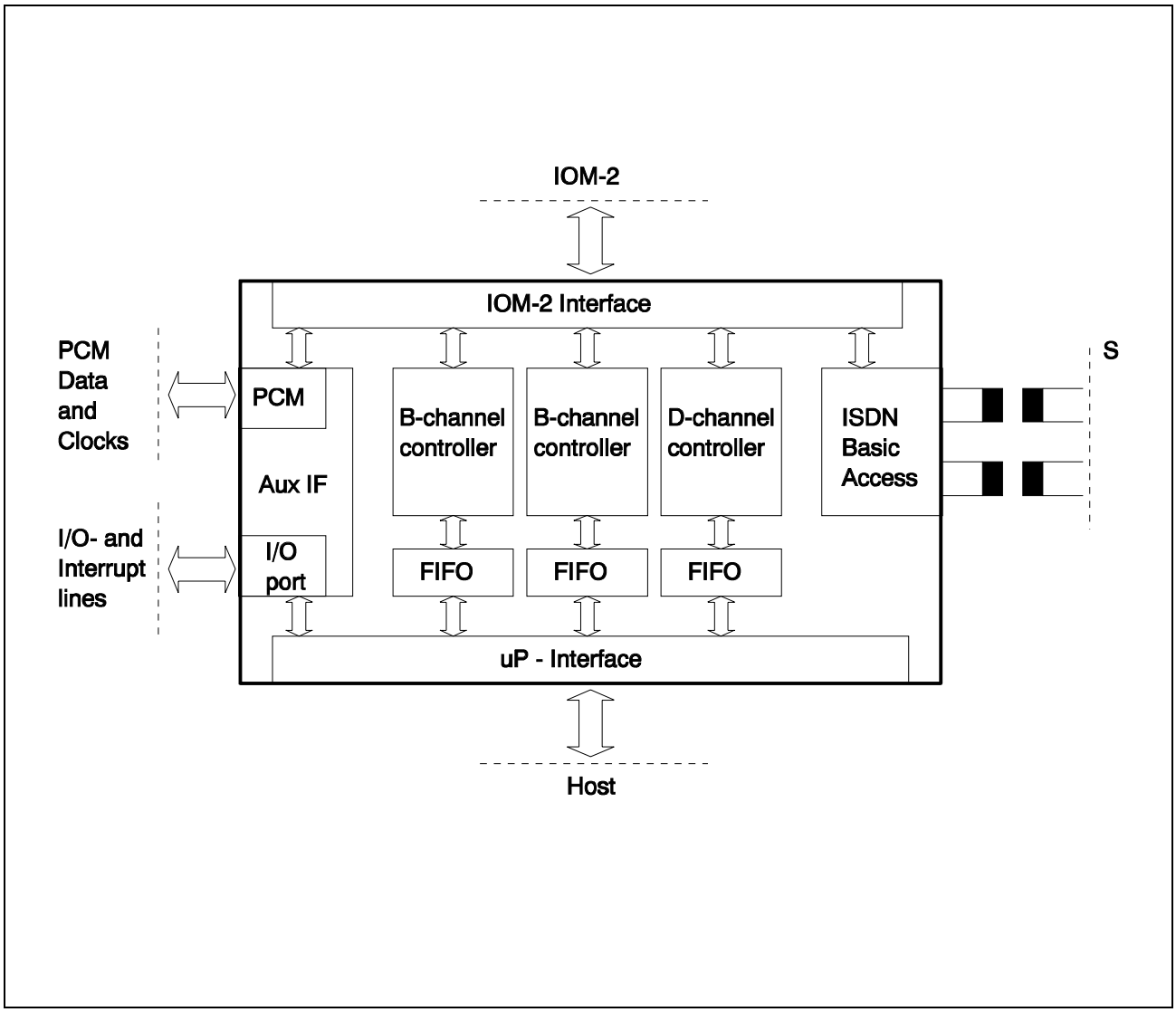


Figure 3 Block Diagram

1.6 System Integration

The IPAC is suited for all host based applications.

ISDN PC Adapter Card for S Interface

An ISDN adapter card for a PC is built around the IPAC using a USB, PCI or PnP interface device depending on the PC interface (**figure 4**). The IPAC can be connected to any bus interface logic and since it provides the possibility of a one-device terminal architecture, interfacing directly to the printer port applications is rather easy.

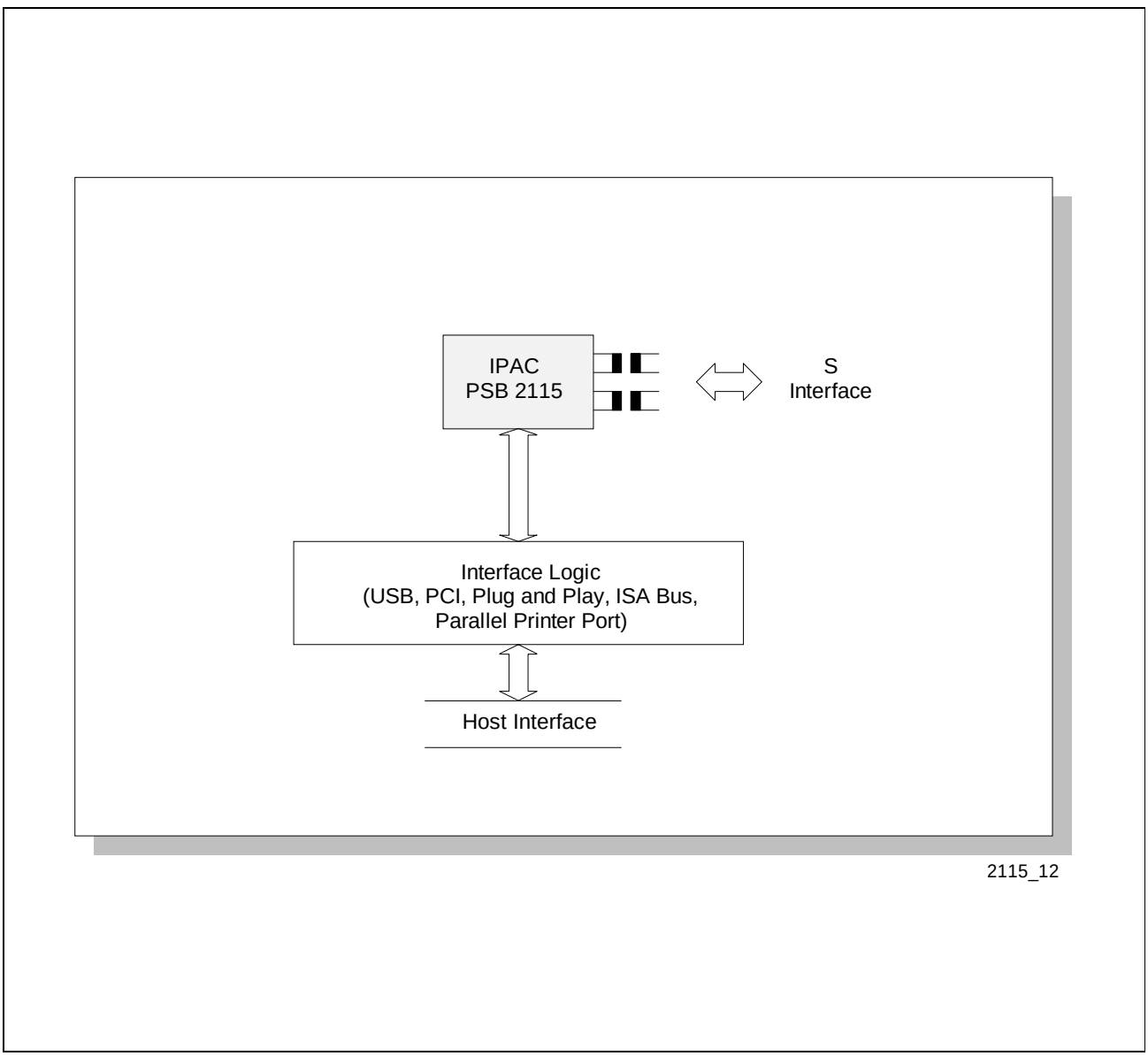


Figure 4 ISDN PC Adapter Card for S Interface

ISDN PC Adapter Card for U or S Interface

An ISDN adapter card which supports both U and S interface may be realized using the IPAC together with the PSB 21910 IEC-Q TE (**figure 5**). The S interface may be configured for TE or LT-S mode supporting intelligent NT configurations.

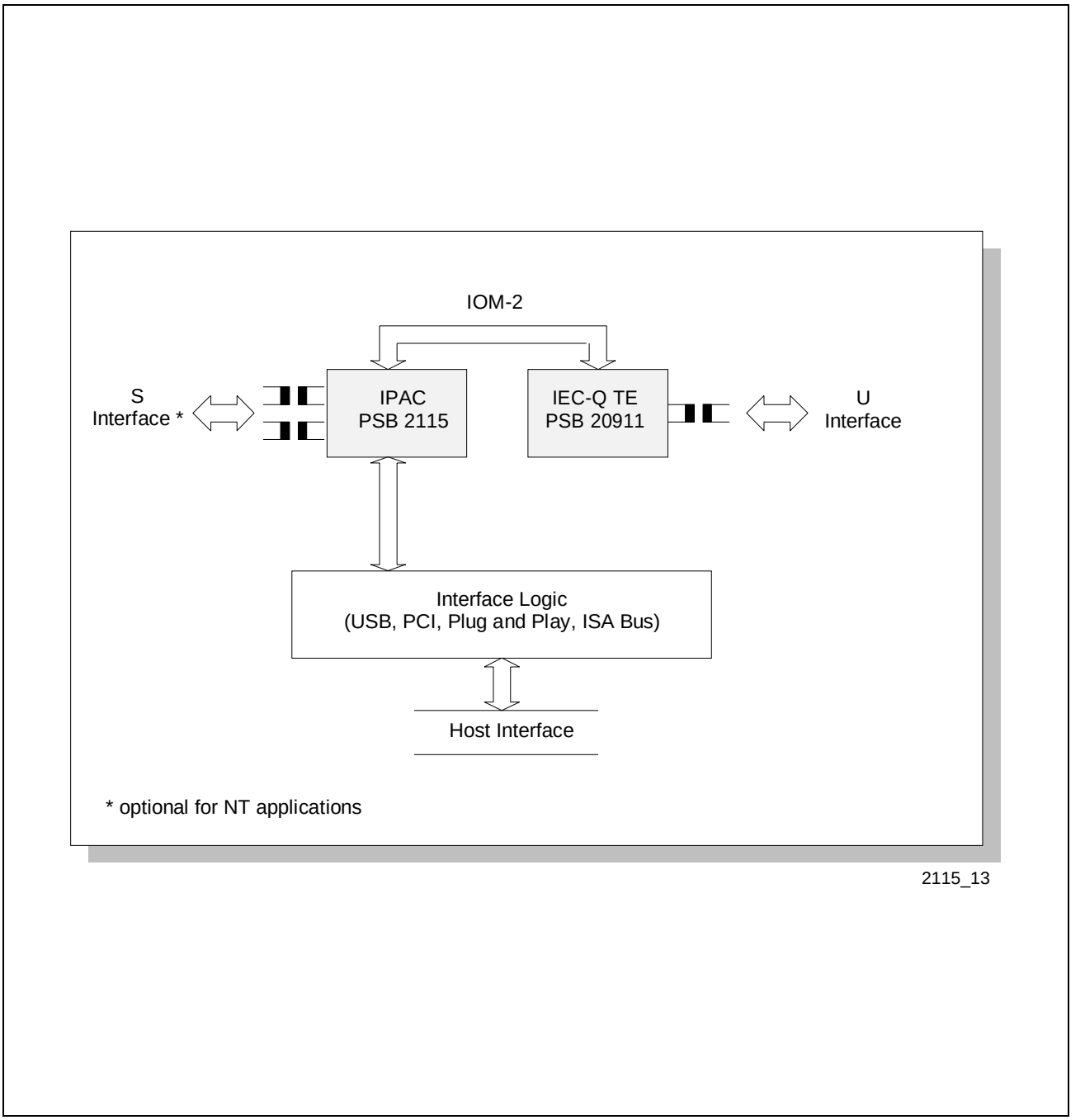


Figure 5 ISDN PC Adapter Card for U or S interface

ISDN Voice/Data Terminal

Figure 6 shows a voice data terminal developed on a PC card, where the IPAC provides its functionality as data controller + S interface within a two chip solution. During ISDN calls the ARCOFI-SP PSB 2163 provides for speakerphone functions and includes a DTMF generator. Additionally, a DTMF receiver or keypad may be connected to the auxiliary interface of the IPAC (LT-T mode).

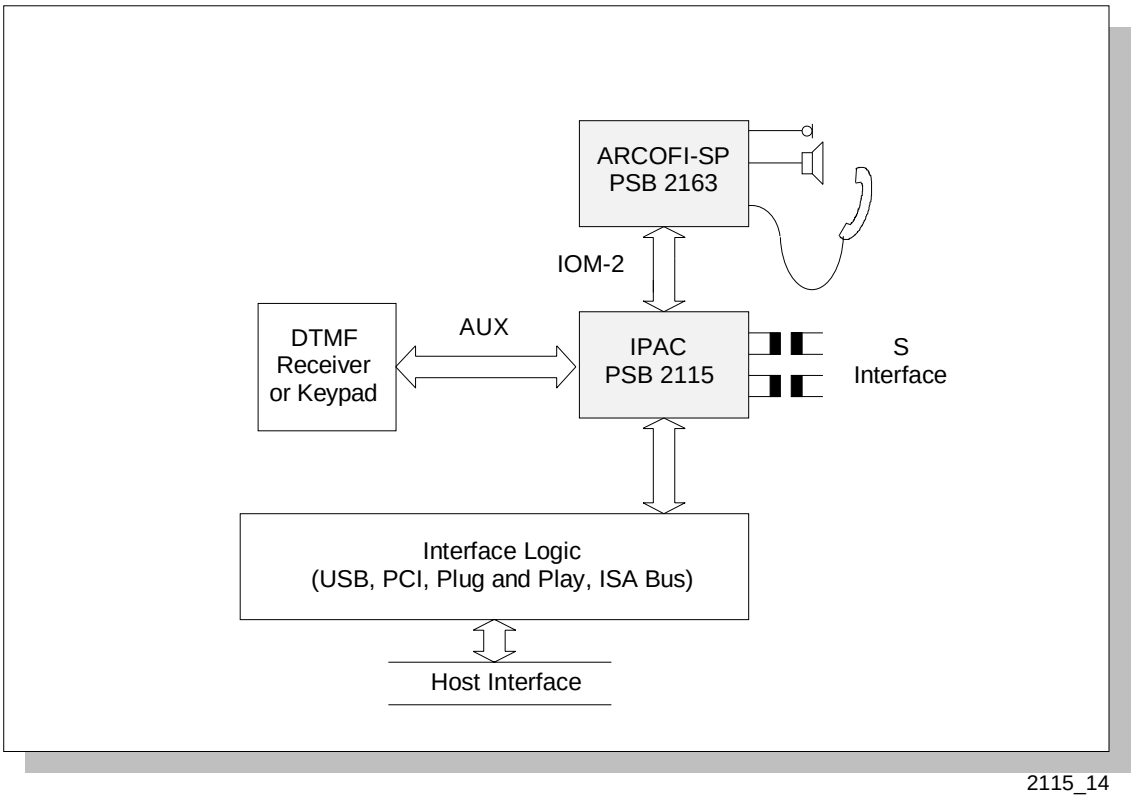


Figure 6 ISDN Voice/Data Terminal

ISDN Stand-alone Terminal with POTS interface

The IPAC (LT-T mode) can be integrated in a microcontroller based stand-alone terminal (**figure 7**) that is connected to the communications interface of a PC. The SICOFI2-TE PSB 2132 enables connection of analog terminals (e.g. telephones or fax) to the dual channel POTS interface.

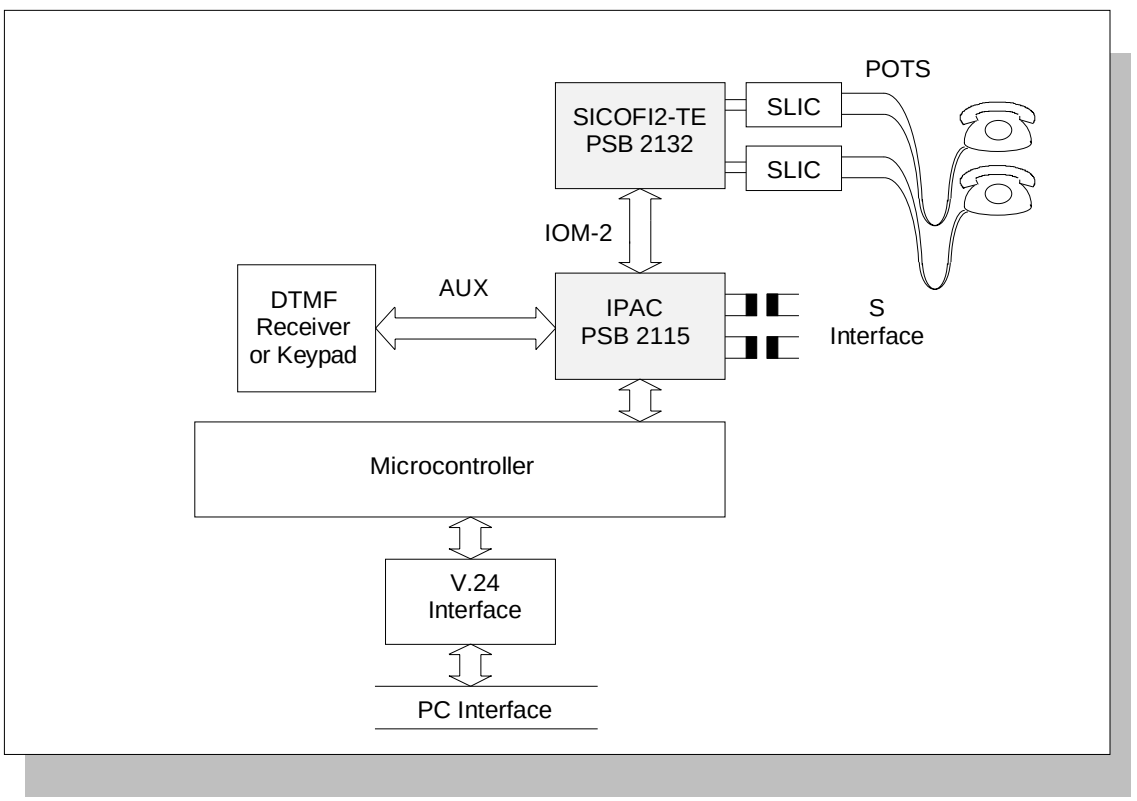


Figure 7 ISDN Stand-Alone Terminal with POTS interface

Multiline PC-Adapter

Up to three S-interfaces can be combined using one IOM interface (**figure 8**). All three IPACs are configured for LT-T mode in different channels. The SCLK output is used for DCL clock and the FSC clock is generated by one device. Only one 7.68 MHz crystal is required for the three IPACs as they provide a buffered output clock derived from the XTAL1 clock input.

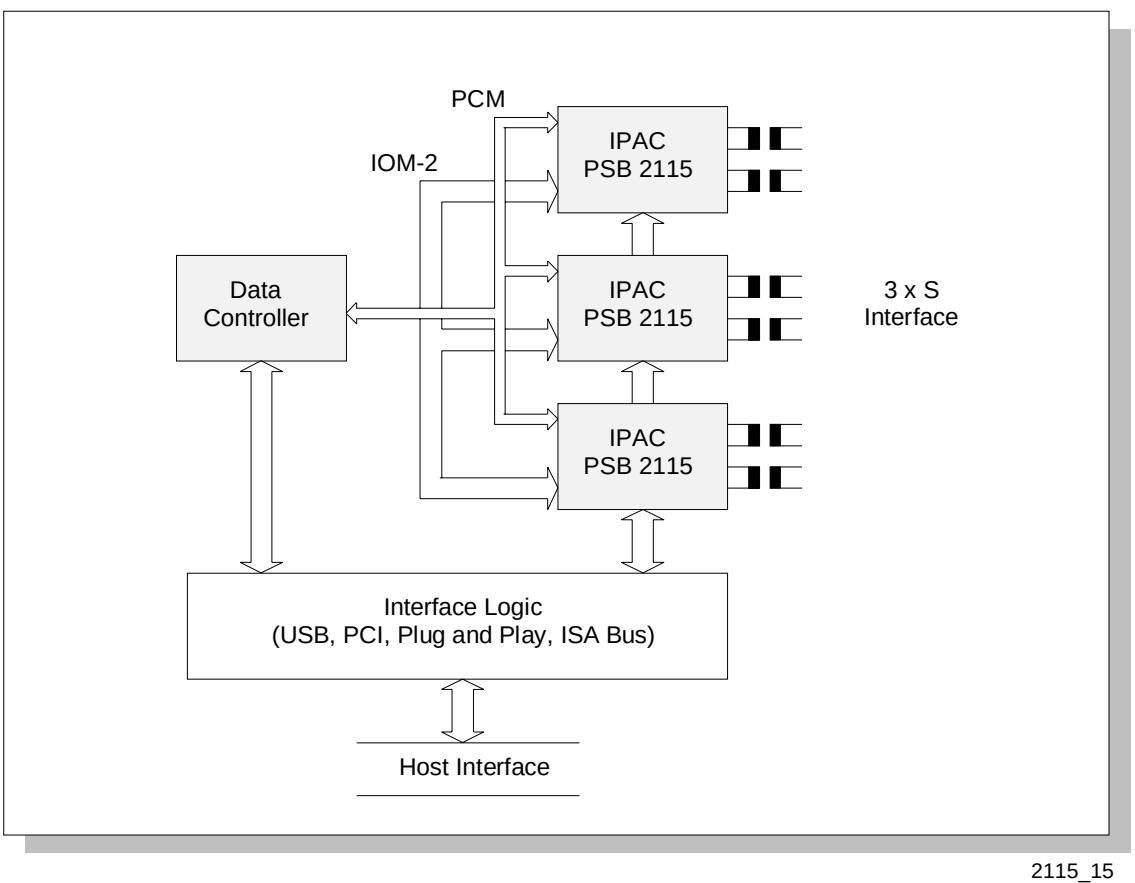


Figure 8 Multiline PC-Adapter

2 Functional Description

The ISDN PC Adapter Circuit IPAC replaces solutions which are based on ISAC-S TE PSB 2186 and HSCX-TE PSB 21525. Most of the functions of both devices are integrated on the IPAC with further modifications and improvements on certain features. Therefore the functional and operational description is quite similar to these devices.

2.1 B-Channel Operation

The HDLC controller of each channel can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies most requirements.

There are 4 different operating modes which can be set via the MODEB register.

- Non-Auto Mode (MODEB: MDS1, MDS0 = 01)
- Transparent Mode 1 (MODEB: MDS1, MDS0, ADM = 101)
- Transparent Mode 0 (MODEB: MDS1, MDS0, ADM = 100)
- Extended Transparent Modes 0; 1 (MODEB: MDS1, MDS0 = 11)

2.1.1 Non-Auto Mode (MODEB: MDS1, MDS0 = 01)

Characteristics: address recognition, arbitrary window size.

All frames with valid addresses are forwarded directly to the system memory.

According to the selected address mode, the IPAC can perform a 2-byte or 1-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FE_H or FC_H (group address) as well as with two individually programmable values in RAH1 and RAH2 registers.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the IPAC can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match with any of the address combinations, are ignored by the IPAC.

The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFOB. The HDLC control field and additional information can also be read from special registers (RHCRB, RSTAB), however, the register contents are only valid for the last received frame and values of previous frames are overwritten. If several frames are stored in the RFIFOB the information should be read from the FIFO contents.

In non-auto mode, all frames are treated similarly.

2.1.2 Transparent Mode 1 (MODEB: MDS1, MDS0, ADM = 101)

Characteristics: address recognition high byte

Only the high byte of a 2-byte address field will be compared. The whole frame except the first address byte will be stored in RFIFOB. RAL1 contains the second and RHCRB the third byte following the opening flag.

2.1.3 Transparent Mode 0 (MODEB: MDS1, MDS0, ADM = 100)

Characteristics: no address recognition

No address recognition is performed and each frame will be stored in the RFIFOB. RAL1 contains the first and RHCRB the second byte following the opening flag.

2.1.4 Extended Transparent Modes 0, 1 (MODEB: MDS1, MDS0 = 11)

Characteristics: fully transparent

In extended transparent modes, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/ check, bit-stuffing mechanism. This allows user specific protocol variations or the usage of Character Oriented Protocols (such as IBM BISYNC).

Data transmission is always performed out of the XFIFOB. In extended transparent mode 0 (ADM = 0), data reception is done via the RAL1 register, which always contains the actual data byte assembled at the DD pin. In extended transparent mode 1 (ADM = 1), the receive data are additionally shifted into the RFIFOB.
Also refer to **chapter 2.1.8** and **2.1.9**.

2.1.5 Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames as affected by different operating modes.

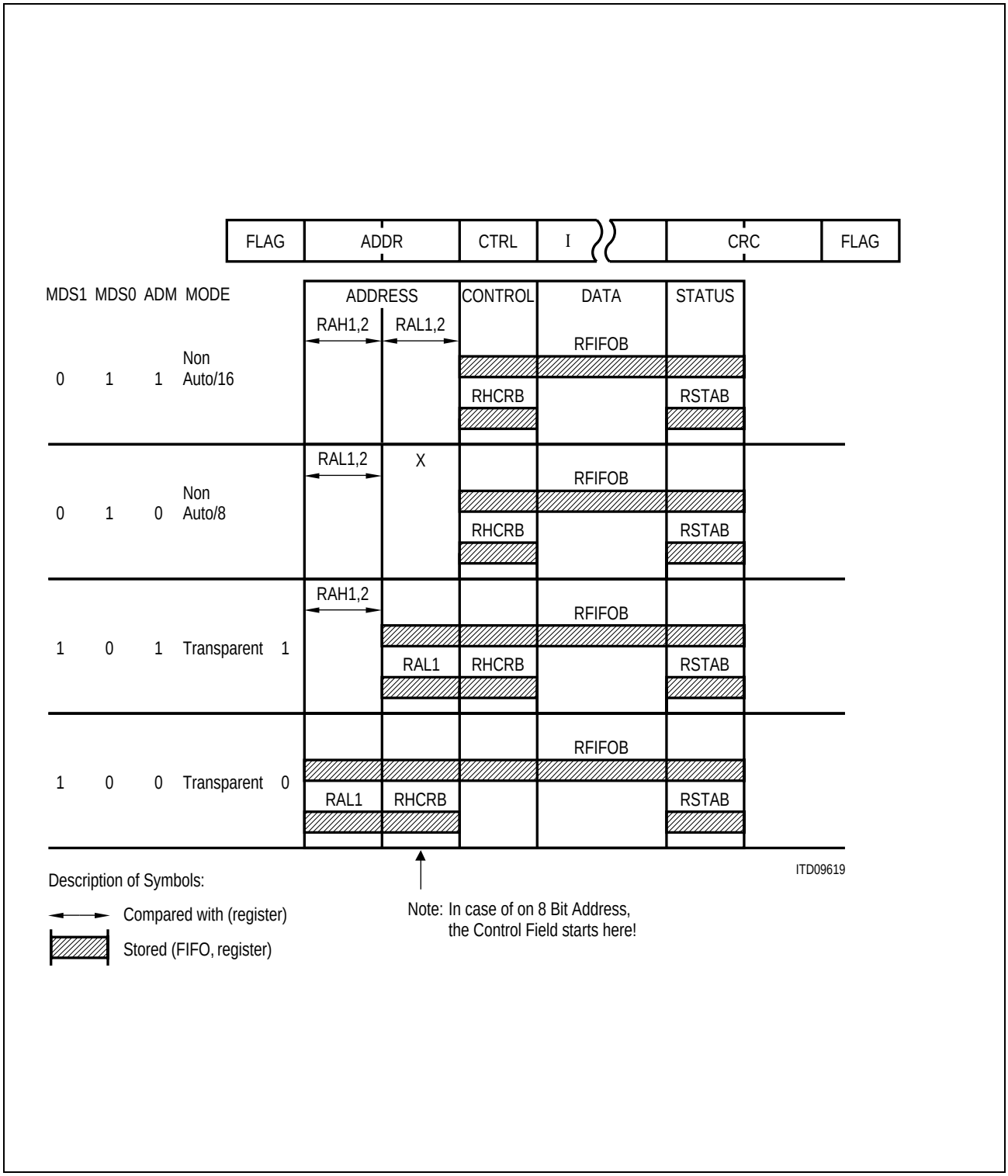


Figure 9 Receive Data Flow of IPAC

2.1.6 Transmit Data Flow

Transparent frames can be transmitted as shown below.

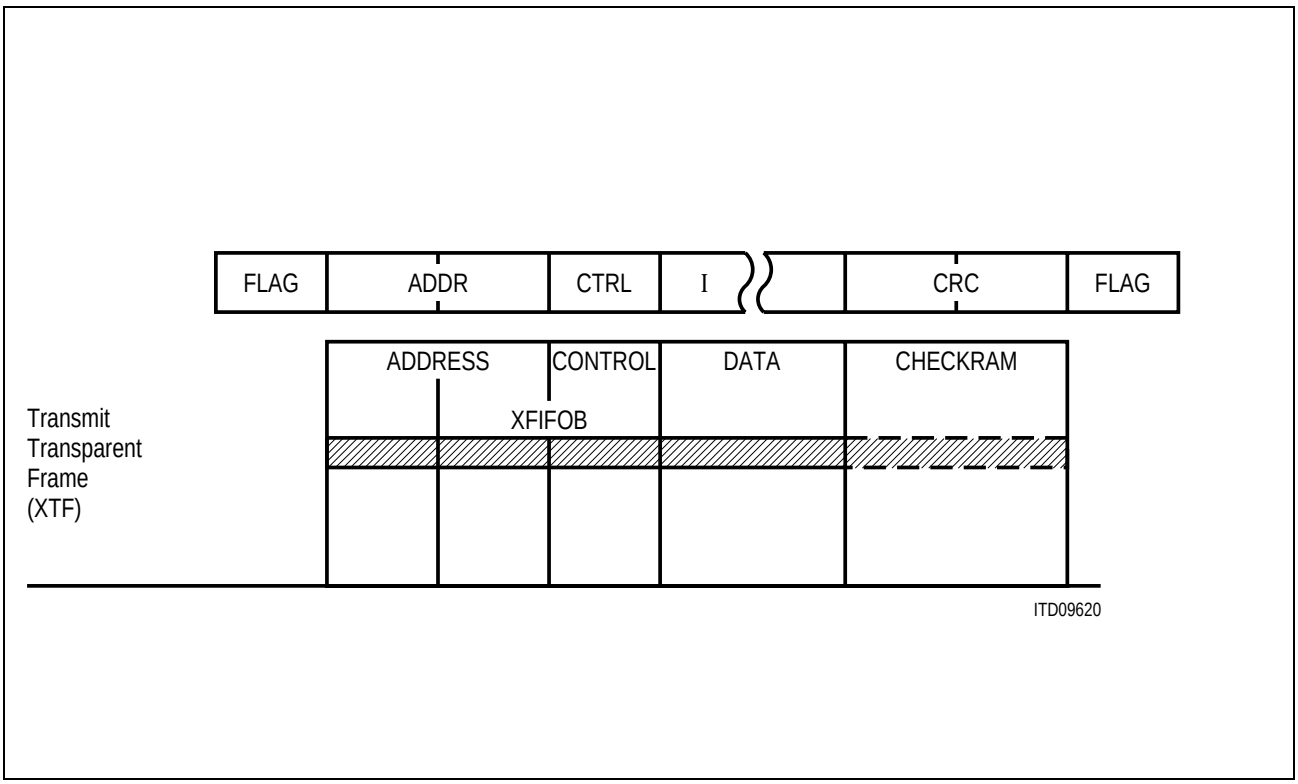


Figure 10 Transmit Data Flow of IPAC

For transparent frames (command XTF via CMDRB register), the address and the control fields have to be entered in the XFIFOB. This is possible in all operating modes.

2.1.7 Serial Interface

The two serial interfaces of the IPAC provide two fully independent channels for B-channel communication.

2.1.7.1 Clock Mode 5 (Time-Slots)

This operating mode has been designed for application in time-slot oriented PCM systems. It is well known as “Clock Mode 5“ from the HSCX-TE PSB 21525.

The receive and transmit clock is identical for both channels and is generated from the double rate bit clock at the DCL pin, i.e. the bit clock frequency is DCL/2. The IPAC receives and transmits only during certain time-slots of programmable width (1 … 256 bit, via RCCR and XCCR registers) and location with respect to a frame synchronization signal, which is determined via the FSC pin. One of up to 64 time-slots can be programmed independently for receive and transmit direction via TSAR and TSAX registers, and an additional clock shift of 0 … 7 bits via TSAR, TSAX, and CCR2 registers. Together with bits XCS0 and RCS0 (LSB of clock shift), located in the CCR2 register, there are 9 bits to determine the location of a time-slot.

According to the value programmed via those bits, the receive/transmit window (time-slot) starts with a delay of 1 (minimum delay) up to 512 clock periods following the frame synchronization signal and is active during the number of clock periods programmed via RCCR, XCCR (number of bits to be received/transmitted within a time-slot) as shown in **figure 11**.
Within one frame the B1-channel occupies bit 0...7 and the B2-channel bit 8...15. Considering the minimum delay of 1 bit, the host programs the previous channel with 7 bits clock shift in order to access a certain channel.

Table 1 Programming of Timeslots

Timeslot	TSAR/TSAX	RCS0...2
0 (B1-channel)	No. of previous channel (see note)	7
1 (B2-channel)	0	7

Note: The previous channel of the B1-channel is the last of the IOM-2 frame, e.g. in TE mode (DCL=1.536 MHz) the channel number is 11 (12th timelsot).

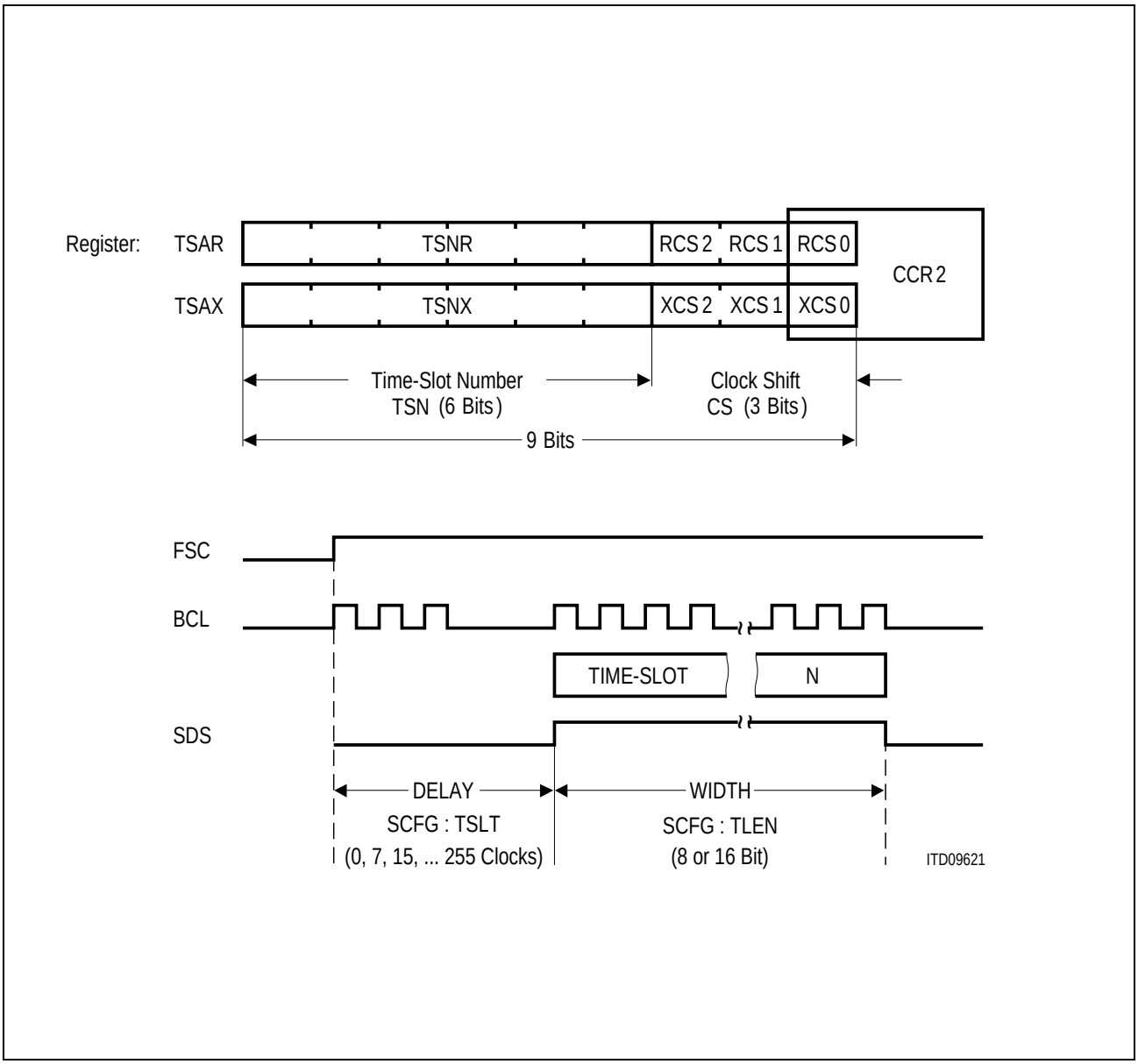


Figure 11 Location of Time-Slots

Note: In extended transparent mode the width of the time-slots has to be n × 8 bit.

The active time-slot can additionally be indicated by a programmable strobe signal SDS of which the output is set to log 1 during the active window.

2.1.7.2 Data Encoding

In the point-to-point configuration, the IPAC supports both NRZ and NRZI data encoding (selectable via CCR1 register).

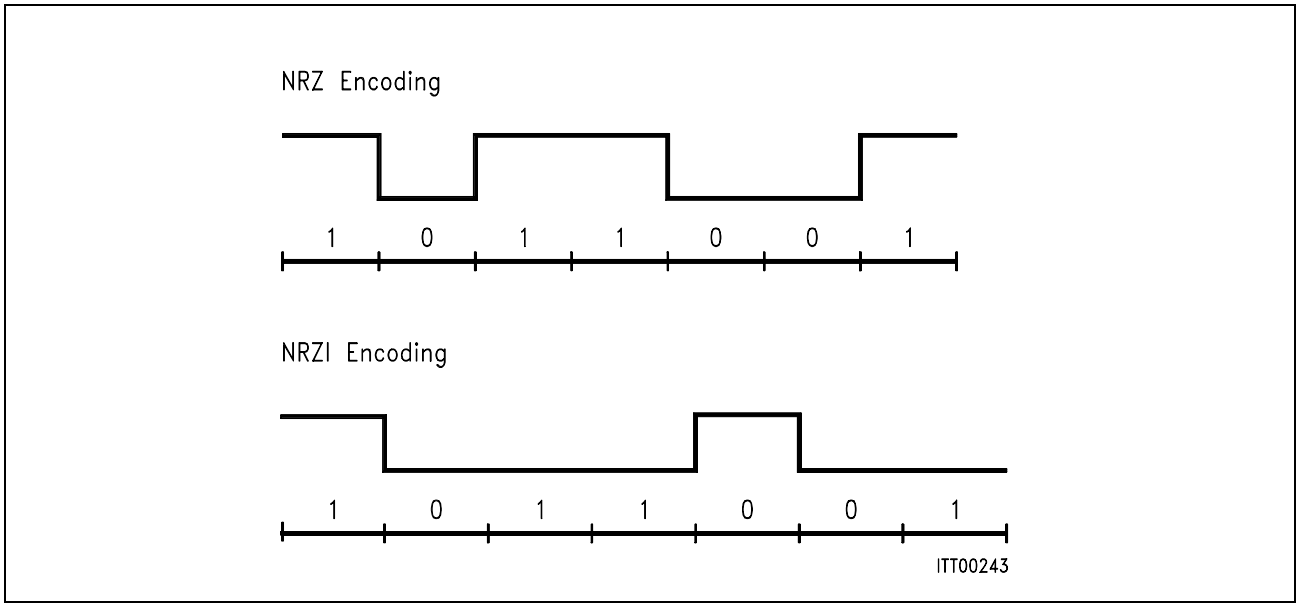


Figure 12 NRZ Encoding/NRZI Encoding

During NRZI encoding, level changes are interpreted as log 0, and no changes in level as log 1.

Data output on the IOM interface is performed with the rising edge of DCL, data input with the second falling DCL clock edge.

2.1.8 Fully Transparent Transmission and Reception

When programmed to the extended transparent mode via the MODEB register (MDS1, MDS0 = 11), each channel of the IPAC supports fully transparent data transmission and reception without HDLC framing overhead, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing mechanism.

In order to enable fully transparent data transfer, RAC bit in MODEB has to be reset and FF_H has to be written to XAD1, XAD2 and RAH2.

Data transmission is always performed out of the transmit FIFO by directly shifting the contents of the XFIFOB via the serial transmit data pin (DU). Transmission is initiated by setting CMDRB : XTF (08_H); end of transmission is indicated by EXIRB : EXE (40_H).

In receive direction, the character currently assembled via the receive data line (DD) is available in the RAL1 register. Additionally, in extended transparent mode 1 (MODEB: MDS1, MDS0, ADM = 111), the received data is shifted into the RFIFOB.

This feature can be profitably used e.g. for:

- user specific protocol variations
- the application of character oriented protocols (e.g. BISYNC)
- test purposes, line intentionally violation of HDLC protocol rules (e.g. wrong CRC)

The valid timeslot for data access on IOM-2 can be selected by setting timeslot position and timeslot length.

For a timeslot length greater than 8-bit (e.g. 16-bit) the access to the selected timeslots on IOM-2 is not synchronized to the frame sync signal FSC. For example if the valid 16-bit timeslot is programmed to B1 and B2, the IPAC does not ensure that transmission is started in B1 of the very first IOM-2 frame, it may also start with B2 and then continue with B1 and B2 in the next frame.

It should be noted that in extended transparent mode 1 an invalid octett is output on IOM-2 before the first valid octett from the XFIFOB is transmitted. In receive direction the first 3 ocetetts of each 64-byte RFIFOB block are invalid and should be discarded.

2.1.9 Cyclic Transmission (Fully Transparent)

If the extended transparent mode is selected, the IPAC supports the continuous transmission of the transmit FIFO's contents.

After having written 1 to 64 bytes to the XFIFOB, the command
XREP.XTF.XME
via the CMDR register (bit 7 … 0 = '00101010' = 2AH) forces the IPAC to repeatedly transmit the data stored in the XFIFOB via DU pin.

The cyclic transmission continues until a reset command (CMDRB : XRES) is issued, after which continuous '1'-s are transmitted.

Note: In DMA-mode the command XREP, XTF has to be written to CMDRB.

2.1.10 Continuous Transmission (DMA Mode only)

If data transfer from system memory to the IPAC is done by DMA (DMA bit in XBCH set), the number of bytes to be transmitted is usually defined via the Transmit Byte Count registers (XBCH, XBCL : bits XBC11 ... XBC0).

Setting the „Transmit Continuously“ (XC) bit in XBCH, however, the byte count value is ignored and the DMA interface of the IPAC will continuously request for transmit data any time 64 bytes can be stored in the XFIFOB.

This feature can be used e.g. to

- continuously transmit voice or data onto a PCM highway, or to
- transmit frames exceeding the byte count programmable via XBCH, XBCL (frames with more than 4095 bytes).

Note: If the XC bit is reset during continuous transmission, the transmit byte count becomes valid again, and the IPAC will request the amount of DMA transfers programmed via XBC11 ... XBC0. Otherwise the continuous transmission is stopped when a data underrun condition occurs in the XFIFOB, i.e. the DMA controller does not transfer further data to the IPAC. In this case continuous ’1’-s (idle), without appending a CRC, are transmitted.

2.1.11 Receive Length Check Feature

The IPAC offers the possibility to supervise the maximum length of received frames and to terminate data reception in case this length is exceeded.

This feature is controlled via the special Receive Length Check Register (RLCR).

The function is enabled by setting the RC (Receive Check) bit in RLCR and programming the maximum frame length via bits RL5 … RL0[1)] .

According to the value written to RL5 … RL0, the maximum receive length can be adjusted in multiples of 64-byte blocks as follows:

$$\text{MAX. LENGTH} = (\text{RL} + 1) \times 64.$$

All frames exceeding this length are treated as if they have been aborted from the opposite station, i.e. the CPU is informed via a

[1)] The frame length includes all bytes which are stored in the RFIFOB.

– RME interrupt, and the
– RAB bit in RSTA register is set!

To distinguish between frames really aborted from the opposite station, the receive byte count (readable from RBCHB, RBCLB registers) exceeds the maximum receive length (via RL5 … RL0) by one or two bytes in this case.

The check includes all data that is copied into the RFIFOB. It does not include the address byte(s) if address recognition is selected. It includes the RSTAB value in all operating modes.

2.1.12 Data Inversion

When NRZ data encoding has been selected, the IPAC may transmit and receive data inverted, i.e. a ‘one’ bit is transmitted as phys. zero (0 V) and a ‘zero’ bit as phys. one (+ 5 V) via the DU line.

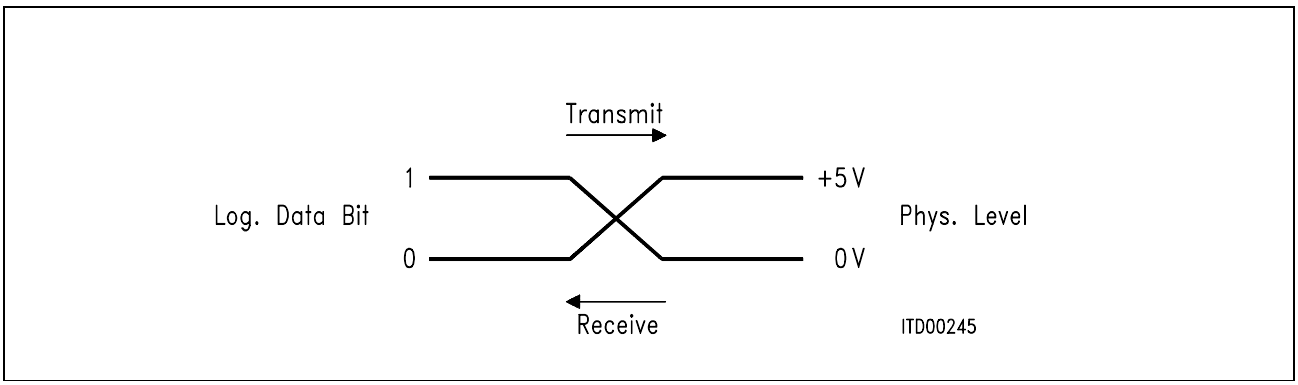


Figure 13 Data Inversion

This feature is selected by setting the DIV bit in the CCR2 register.

2.2 D-Channel Operation

2.2.1 Layer-2 Functions for HDLC

The D-Channel HDLC controller in the IPAC is responsible for the data link layer using HDLC/SDLC based protocols.

The IPAC can be configured to support data link layer to a degree that best suits system requirements. Multiple links may be handled simultaneously due to the address recognition capabilities, as explained in **section 2.2.1.1**.

The IPAC supports point-to-point protocols such as LAPB (Link Access Procedure Balanced) used in X.25 networking.

For ISDN, one particularly important protocol is the **Link Access Procedure for the D channel** (LAPD).

LAPD, layer 2 of the ISDN D-channel protocol (CCITT I.441) includes functions for:

– Provision of one or more data link connections on a D channel (multiple LAP). Discrimination between the data link connections is performed by means of a data link connection identifier (DLCI = SAPI + TEI)
– HDLC-framing
– Application of a balanced class of procedure in point-multipoint configuration.

The HDLC transceiver in the IPAC performs the framing functions used in HDLC/SDLC based communication: flag generation/recognition, bit stuffing, CRC check and address recognition.

The FIFO structure with two 64-byte pools for transmit and receive directions and an intelligent FIFO controller permit flexible transfer of protocol data units to and from the µC system.

2.2.1.1 Message Transfer Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be programmed in a flexible way, to satisfy different system requirements.

For the address recognition the IPAC contains four programmable registers for individual SAPI and TEI values SAP1-2 and TEI1-2, plus two fixed values for “group” SAPI and TEI, SAPG and TEIG.

There are 5 different operating modes which can be set via the MODED register:

Auto Mode (MDS2, MDS1 = 00)

Characteristics:
– Full address recognition (1 or 2 bytes).
– Normal (mod 8) or extended (mod 128) control field format
– Automatic processing of numbered frames of an HDLC procedure.

If a 2-byte address field is selected, the high address byte is compared with the fixed value FE_H or FC_H (group address) as well as with two individually programmable values in SAP1 and SAP2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) dependent on the setting of the CRI bit in SAP1, and will be excluded from the address comparison.

Similarly, the low address byte is compared with the fixed value FF_H (group TEI) and two compare values programmed in special registers (TEI1, TEI2). A valid address will be recognized in case the high and low byte of the address field match one of the compare values. The IPAC can be called (addressed) with the following address combinations:

– SAP1/TEI1
– SAP1/FF_H
– SAP2/TEI2
– SAP2/FF_H
– FE_H(FC_H)/TEI1
– FE_H(FC_H)/TEI2
– FE_H(FC_H)/FF_H

Only the logical connection identified through the address combination SAP1, TEI1 will be processed in the auto mode, all others are handled as in the non-auto mode. The logical connection handled in the auto mode must have a window size 1 between transmitted and acknowledged frames. HDLC frames with address fields that do not match with any of the address combinations, are ignored by the IPAC.

In case of a 1-byte address, TEI1 and TEI2 will be used as compare registers. According to the X.25 LAPB protocol, the value in TEI1 will be interpreted as COMMAND and the value in TEI2 as RESPONSE.

The control field is stored in RHCRD register and the I field in RFIFOD. Additional information is available in RSTAD.

Non-Auto Mode (MDS2, MDS1 = 01)

Characteristics:
Full address recognition (1 or 2 bytes)
Arbitrary window sizes

All frames with valid addresses are accepted and the bytes following the address are transferred to the µP via RHCRD and RFIFOD. Additional information is available in RSTAD.

Transparent Mode 1 (MDS2, MDS1, MDS0 = 101).

Characteristics: TEI recognition

A comparison is performed only on the second byte after the opening flag, with TEI1, TEI2 and group TEI (FF_H). In case of a match, the first address byte is stored in SAPR, the (first byte of the) control field in RHCRD, and the rest of the frame in the RFIFOD. Additional information is available in RSTAD.

Transparent Mode 2 (MDS2, MDS1, MDS0 = 110).

Characteristics: no address recognition

Every received frame is stored in RFIFOD (first byte after opening flag to CRC field). Additional information can be read from RSTAD.

Transparent Mode 3 (MDS2, MDS1, MDS0 = 111).

Characteristics: SAPI recognition

A comparison is performed on the first byte after the opening flag with SAP1, SAP2 and group SAPI (FE_H/FC_H). In the case of a match, all the following bytes are stored in RFIFOD. Additional information can be read from RSTAD.

2.2.1.2 Reception of Frames

A 2x32-byte FIFO buffer (receive pools) is provided in the receive direction.

The control of the data transfer between the CPU and the IPAC is handled via interrupts.

There are two different interrupt indications concerned with the reception of data:

– RPF (**R**eceive **P**ool **F**ull) interrupt, indicating that a 32-byte block of data can be read from the RFIFOD and the received message is not yet complete.
– RME (**R**eceive **M**essage **E**nd) interrupt, indicating that the reception of one message is completed, i.e. either
  • one message ≤ 32 bytes, or
  • the last part of a message ≥ 32 bytes

is stored in the RFIFOD.

Depending on the message transfer mode the address and control fields of received frames are processed and stored in the receive FIFO or in special registers as depicted in **figure 15**.

The organization of the RFIFOD is such that, in the case of short (≤ 32 bytes), successive messages, up to two messages with all additional information can be stored. The contents of the RFIFOD would be, for example, as shown in **figure 14**.

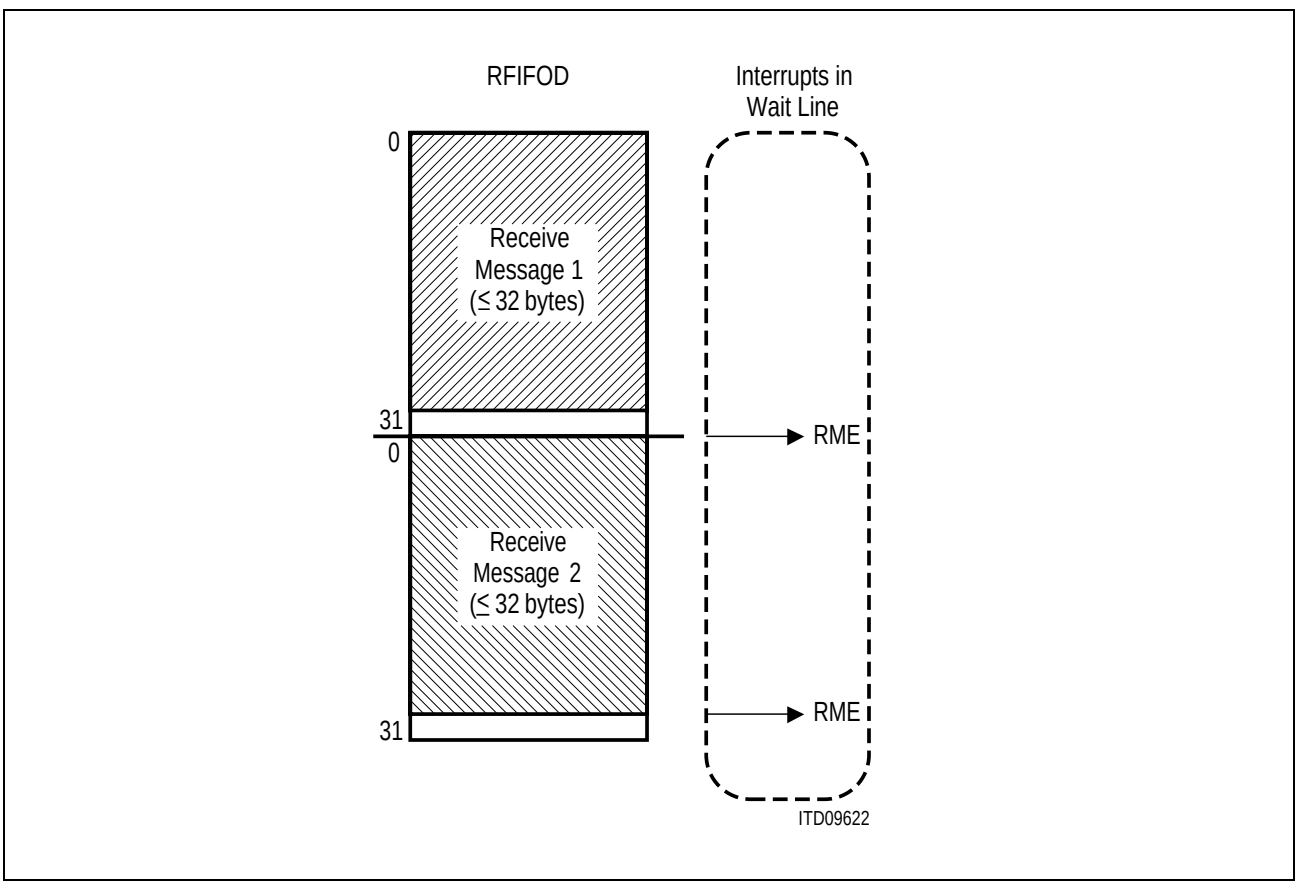


Figure 14 Contents of RFIFOD (short message)

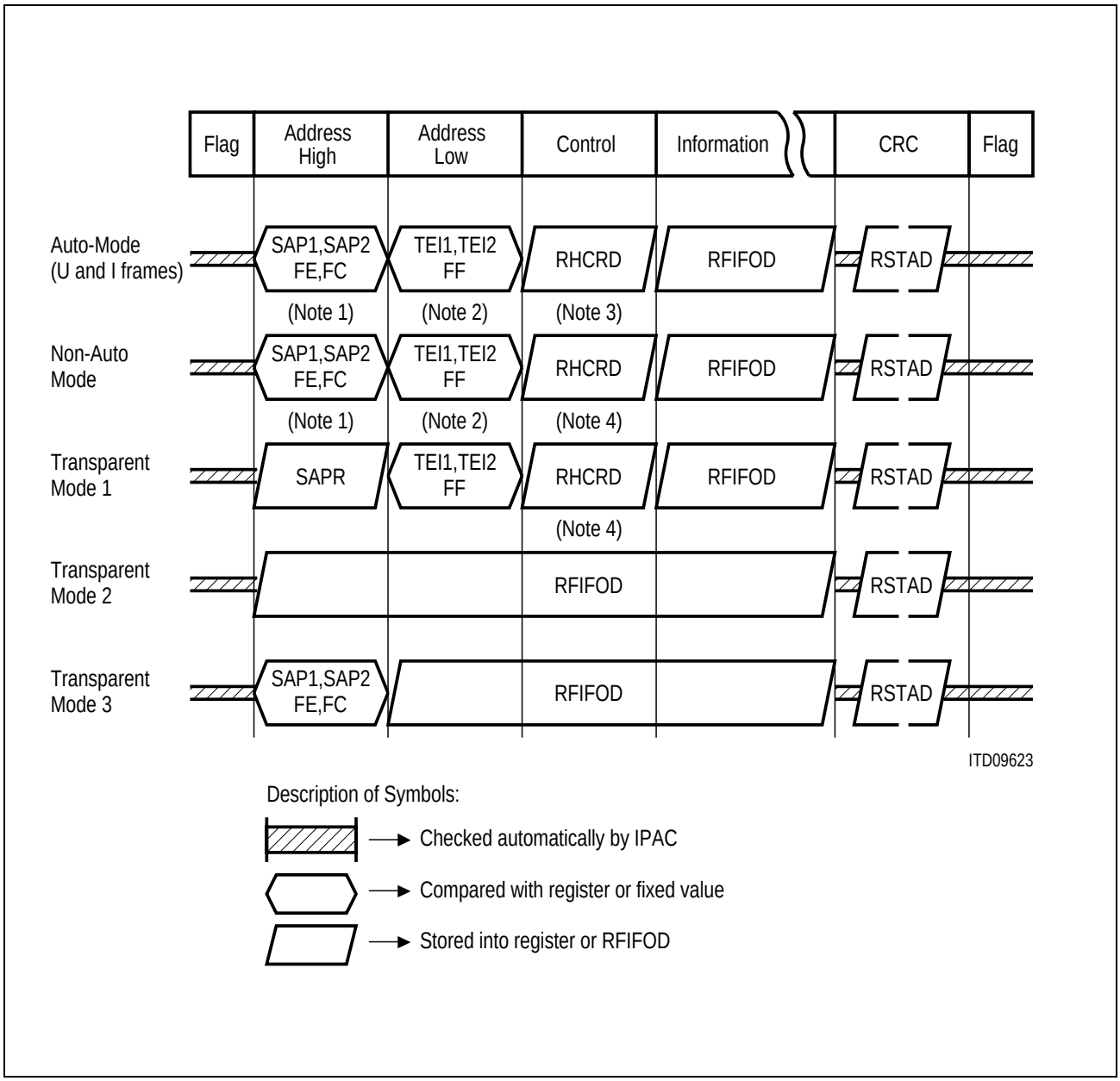


Figure 15 Receive Data Flow

Note 1: Only if a 2-byte address field is defined (MDS0 = 1 in MODED register).

Note 2: Comparison with Group TEI (FF_H) is only made if a 2-byte address field is defined (MDS0 = 1 in MODED register).

Note 3: In the case of an extended, modulo 128 control field format (MCS = 1 in SAP2 register) the control field is stored in RHCRD in compressed form (I frames).

Note 4: In the case of extended control field, only the first byte is stored in RHCRD, the second in RFIFOD.

When 32 bytes of a message longer than that are stored in RFIFOD, the CPU is prompted to read out the data by an RPF interrupt. The CPU must handle this interrupt before more than 32 additional bytes are received, which would cause a “data overflow” (**figure 16**). This corresponds to a maximum CPU reaction time of 16 ms (data rate 16 kbit/s).

After a remaining block of less than or equal to 16 bytes has been stored, it is possible to store the first 16 bytes of a new message (see **figure 16**).

The internal memory is now full. The arrival of additional bytes will result in “data overflow” and a third new message in “frame overflow”.

The generated interrupts are inserted together with all additional information into a wait line to be individually passed to the CPU.

After an RPF or RME interrupt has been processed, i.e. the received data has been read from the RFIFOD, this must be explicitly acknowledged by the CPU issuing a RMC (Receive Message Complete) command.

The IPAC can then release the associated FIFO pool for new data. If there is an additional interrupt in the wait line it will be generated after the RMC acknowledgment.

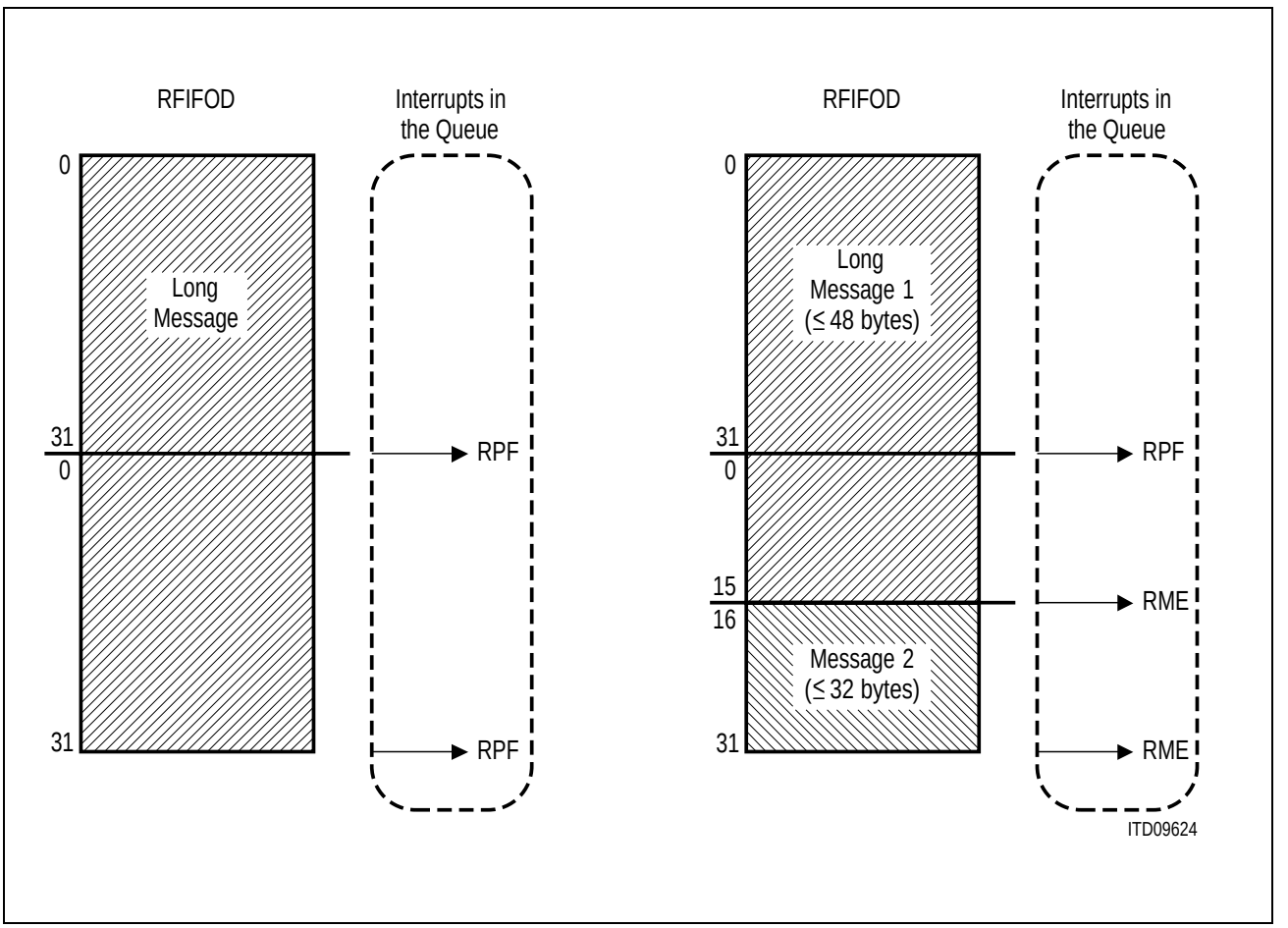


Figure 16 Contents of RFIFOD (long message)

Information about the received frame is available for the µP when the RME interrupt is generated, as shown in **table 2**.

Table 2 Receive Information at RME Interrupt

Information	Register	Bit	Mode
First byte after flag (SAPI of LAPD address field)	SAPR	–	Transparent mode 1
Control field	RHCRD	–	Auto mode, I (modulo 8) and U frames
Compressed control field	RHCRD	–	Auto mode, I frames (modulo 128)
2nd byte after flag	RHCRD	–	Non-auto mode, 1-byte address field
3rd byte after flag	RHCRD	–	Non-auto mode, 2-byte address field Transparent mode 1
Type of frame (Command/ Response)	RSTAD	C/R	Auto mode, 2-byte address field Non-auto mode, 2-byte address field Transparent mode 3
Recognition of SAPI	RSTAD	SA1-0	Auto mode, 2-byte address field Non-auto mode, 2-byte address field Transparent mode 3
Recognition of TEI	RSTAD	TA	All except Transparent mode 2,3
Result of CRC check (correct/ incorrect)	RSTAD	CRC	All
Data available in RFIFOD (yes/no)	RSTAD	RDA	All
Abort condition detected (yes/no)	RSTAD	RAB	All
Data overflow during reception of a frame (yes/no)	RSTAD	RDO	All
Number of bytes received in RFIFOD	RBCLD	RBC4-0	All
Message length	RBCLD RBCHD	RBC11-0	All

2.2.1.3 Transmission of Frames

A 2×32 byte FIFO buffer (transmit pools) is provided in the transmit direction.

If the transmit pool is ready (which is true after an XPR interrupt or if the XFW bit in STARD is set), the CPU can write a data block of up to 32 bytes to the transmit FIFO. After this, data transmission can be initiated by command.

The transmission of transparent frames (command: XTF) and I frames (command: XIF) is shown in **figure 17**.

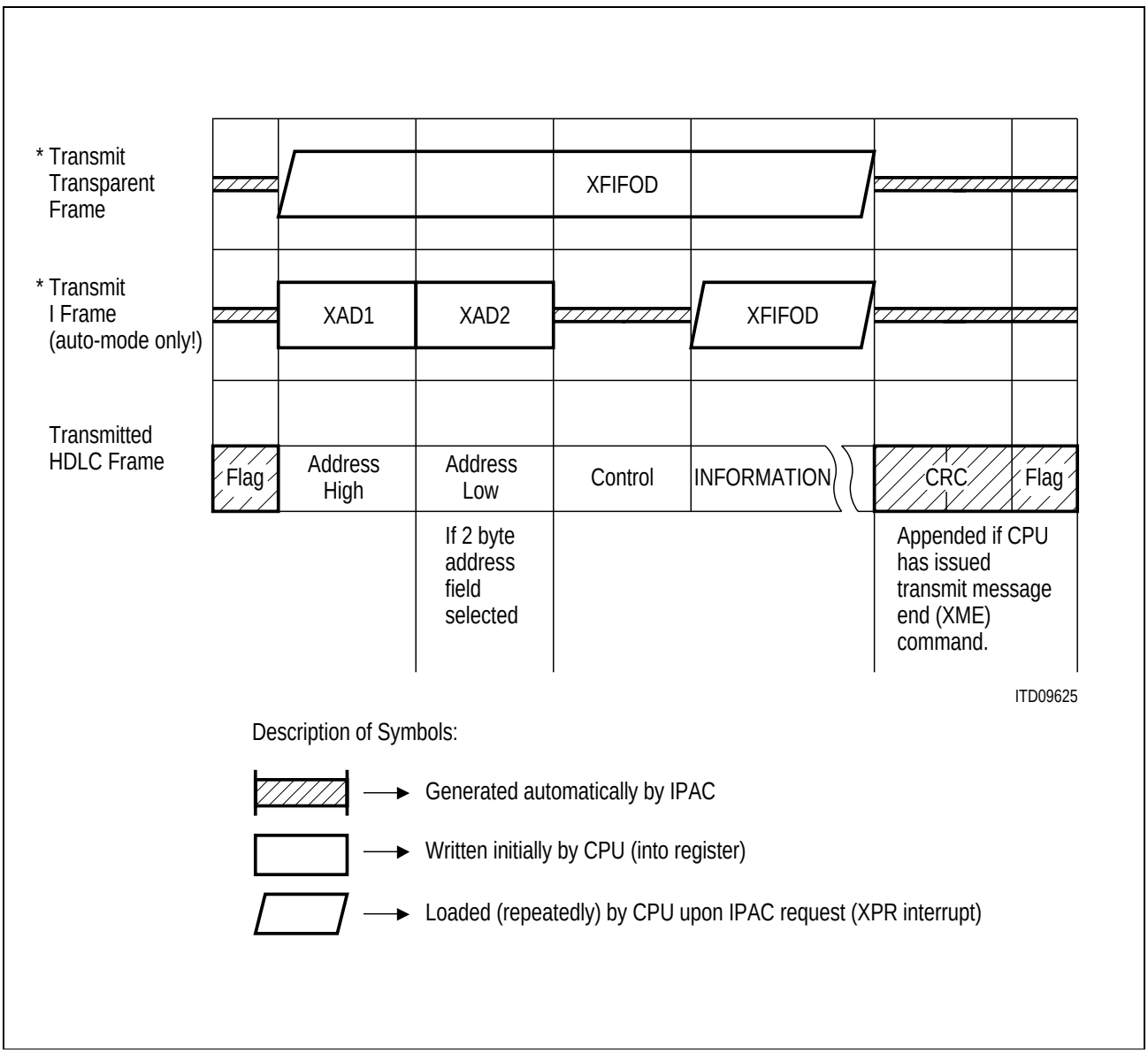


Figure 17 Transmit Data Flow

For transparent frames, the whole frame including address and control field must be written to the XFIFOD.

The transmission of **I frames** is possible only if the IPAC is operating in the auto mode. The address and control field is autonomously generated by the IPAC and appended to the frame, only the data in the information field must be written to the XFIFOD.

If a 2-byte address field has been selected, the IPAC takes the contents of the XAD 1 register to build the high byte of the address field, and the contents of the XAD 2 register to build the low byte of the address field.

Additionally the C/R bit (bit 1 of the high byte address, as defined by LAPD protocol) is set to “1” or “0” depending on whether the frame is a command or a response.

In the case of a 1-byte address, the IPAC takes either the XAD 1 or XAD 2 register to differentiate between command or response frame (as defined by X.25 LAPB).

The control field is also generated by the IPAC including the receive and send sequence number and the poll/final (P/F) bit. For this purpose, the IPAC internally manages send and receive sequence number counters.

In the auto mode, S frames are sent autonomously by the IPAC. The transmission of U frames, however, must be done by the CPU. U frames must be sent as transparent frames (XTF), i.e. address and control field must be defined by the CPU.

Once the data transmission has been initiated by command (XTF or XIF), the data transfer between CPU and IPAC is controlled by interrupts.

The IPAC repeatedly requests another data packet or block by means of an XPR interrupt, every time no more than 32 bytes are stored in the XFIFOD.

The processor can then write further data to the XFIFOD and enable the continuation of frame transmission by issuing an XIF/XTF command.

If the data block which has been written last to the XFIFOD completes the current frame, this must be indicated additionally by setting the XME (Transmit Message End) command bit. The IPAC then terminates the frame properly by appending the CRC and closing flag.

If the CPU fails to respond to an XPR interrupt within the given reaction time, a data underrun condition occurs (XFIFOD holds no further valid data). In this case, the IPAC automatically aborts the current frame by sending seven consecutive “ones” (ABORT sequence).

The CPU is informed about this via an XDU (Transmit Data Underrun) interrupt.

It is also possible to abort a message by software by issuing an XRES (Transmitter RESet) command, which causes an XPR interrupt.

After an end of message indication from the CPU (XME command), the termination of the transmission operation is indicated differently, depending on the selected message transfer mode and the transmitted frame type.

If the IPAC is operating in the auto mode, the window size (= number of outstanding unacknowledged frames) is limited to 1; therefore an acknowledgment is expected for every I frame sent with an XIF command. The acknowledgment may be provided either by a received S or I frame with corresponding receive sequence number (see **figure 14**).

If no acknowledgment is received within a certain time (programmable), the IPAC requests an acknowledgment by sending an S frame with the poll bit set (P = 1) (RR or RNR). If no response is received again, this process is repeated in total CNT times (retry count, programmable via TIMR1 register).

The termination of the transmission operation may be indicated either with:

– XPR interrupt, if a positive acknowledgment has been received,
– XMR interrupt, if a negative acknowledgment has been received, i.e. the transmitted message must be repeated (XMR = Transmit Message Repeat),
– TIN interrupt, if no acknowledgment has been received at all after CNT times the expiration of the time period t_1 (TIN = Timer INterrupt, XPR interrupt is issued additionally).

Note: Prerequisite for sending I frames in the auto mode (XIF) is that the internal operational mode of the timer has been selected in the MODED register (TMD bit = 1).

The transparent transmission of frames (XTF command) is possible in all message transfer modes. The successful termination of a transparent transmission is indicated by the XPR interrupt.

A transmission may be aborted from the outside (E ≠ D) which has the effect that the stop/go bit is set to 1, provided DIM1-0 (MODED register) are programmed appropriately. An example of this is the occurrence of an S bus D-channel collision. If this happens before the first FIFO pool has been completely transmitted and released, the IPAC will retransmit the frame automatically as soon as transmission is enabled again. Thus no µP interaction is required.

On the other hand, if a transmission is inhibited by the Stop/Go bit after the first pool has already been released (and XPR generated), the IPAC aborts the frame and requests the processor to repeat the frame with an XMR interrupt.

In LT-T mode the Stop/Go bit can be output on pin AUX7 which may be used for test purposes.

2.3 Control Procedures

Control procedures describe the commands and messages required to control the IPAC PSB 2115 in different modes and situations. This chapter shows the user how to activate and deactivate the device under various circumstances. In order to keep this chapter as application oriented as possible only actions and reactions the user needs to initiate or may observe are mentioned.

2.3.1 Activation Initiated by Exchange (LT-S)

	TE/LT-T IOM®-2			**LT-S IOM®-2**				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	; Initial state is G1 deactivated
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	; and F3 Power Down
←	C/I	RSY	(0100b)	**C/I**	**AR**	**(1000b)**	¯	; Start activation
←	C/I	AR	(1000b)	C/I	AR	(1000)	→	
←	C/I	AI	(1100b)	C/I	AI	(1100)	→	; Activation completed
→	C/I	AR8/AR10	(1000b/1001b)					

2.3.2 Activation Initiated by Terminal (TE/LT-T)

The following scheme illustrates how a terminal initiates an activation.

	TE/LT-T IOM®-2			**LT-S IOM®-2**				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	; Initial state is G1 Deactivated
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	; and F3 Power Down
_	**C/I**	**TIM**	**(0000b)**					; Request timing (IOM clocks)
←	C/I	PU	(0111b)					
_	**C/I**	**AR8**	**(1000b)**					
_	**TIM Release**							; Start Activation
←	C/I	RSY	(0100b)					; Transfer to G3 Activated
←	C/I	AR	(1000b)	C/I	AR	(1000b)	→	;
←	C/I	AI	(1100b)	C/I	AI	(1100b)	→	;

2.3.3 Deactivation

A deactivation of the S-interface can only be initiated by the exchange side (IPAC in LT-S mode). It is possible to begin a deactivation process from all interim activation states, i.e. not only from the fully activated state. The following example nevertheless assumes that the line is fully activated when the deactivation is initialized.

	TE/LT-T IOM®-2			**LT-S IOM®-2**				
←	C/I	AI8	(1100b)	C/I	AI	(1100b)	→	; Initial state
←	C/I	DR	(0000b)	**C/I**	**DR**	**(0000b)**	¯	; start deactivation
_	**C/I**	**DI**	**(1111b)**	C/I	TIM	(0000b)	→	;
←	C/I	DC	(1111b)	C/I	DI	(1111b)	→	; “G1 Deactivated”
				C/I	**DC**	**(1111b)**	¯	; Transfer to “F3 Power Down” (only in intelligent NT mode, not in LT-S mode

2.3.4 D-Channel Access Control

D-channel access control was defined to guarantee all connected TEs and HDLC controllers a fair chance to transmit data in the D-channel. **Figure 18** illustrates that collisions are possible on the TIC- and the S-bus.

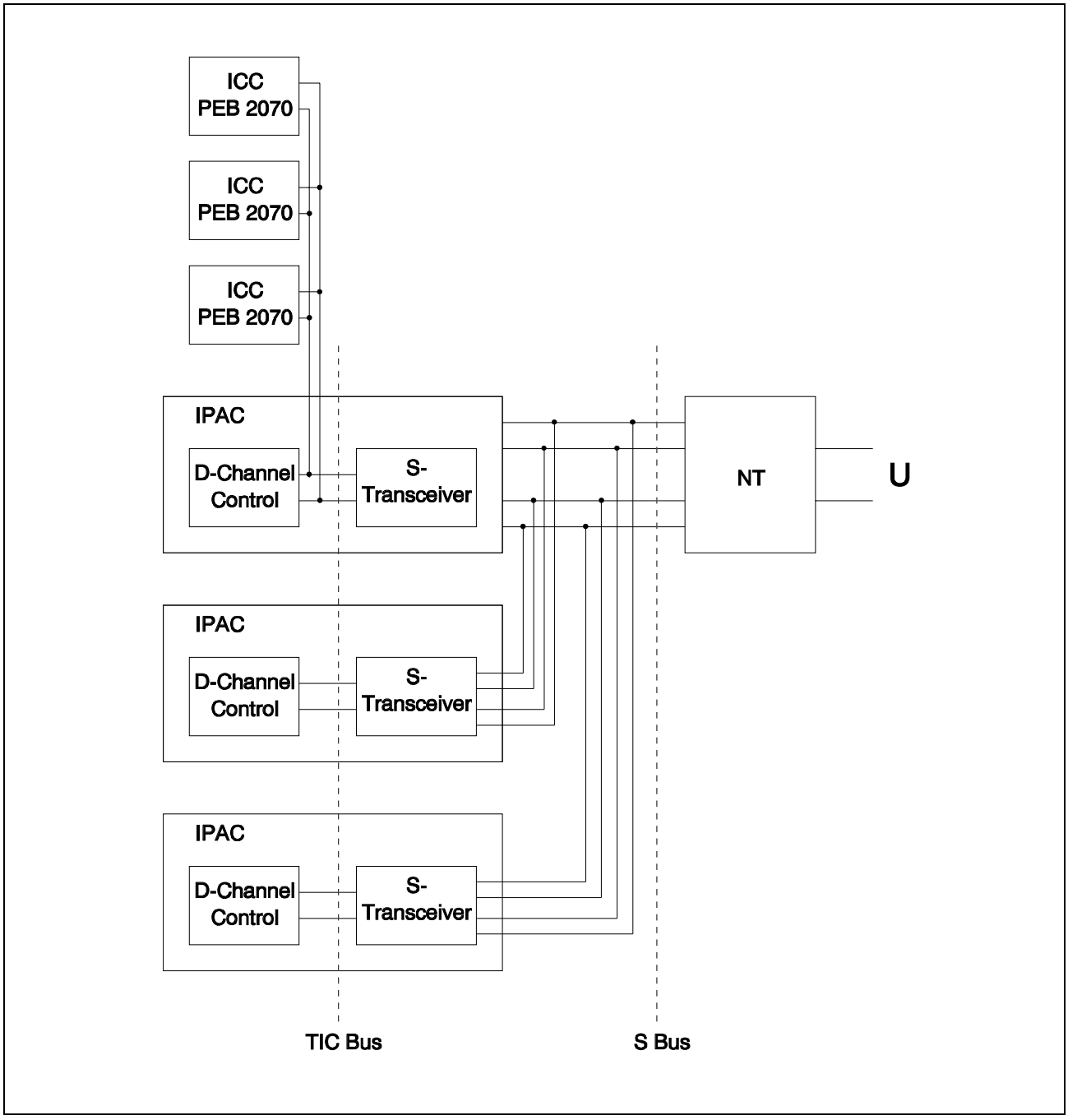


Figure 18 D-Channel Access Control on TIC Bus and S Bus

The TIC bus is used to control D-channel access on the IOM interface when more than one HDLC controller is connected. This configuration is illustrated in the above figure for TE1 where three ICCs are connected to one IOM-2 bus.

On the S bus the D-channel control is handled according to the ITU recommendation I.430. This control mechanism is required everytime a point to multipoint configuration is implemented (NT → TE1 … TE8).

While the S-bus collision detection is handled by the S interface control of the IPAC, TIC bus access is mainly controlled by the D-Channel HDLC controller of the IPAC or from external devices on the IOM-2 interface (e.g. ICC).

The following sections describe both control mechanisms because the TIC bus, although largely handled by the HDLC controller, represents an important part of D-channel access.

2.3.4.1 TIC Bus D-Channel Control in TE

The TIC bus was defined to organize D- and C/I channel access when two or more D- and C/I channel controllers can access the same IOM-2 timeslot. Bus access is controlled by five bits in IOM-2 channel No. 2 (see **section 2.7.1**):

Upstream:	BAC	Bus access control bit
	TBA0 … 2	TIC bus address bits 0 … 2
Downstream:	S/G	Stop/Go bit

When a controller wants to write to the D or C/I channel the following procedure is executed:

1. Controller checks whether BAC bit is set to ONE. If this is not the case access currently is not allowed: the controller has to postpone transmission. Only if BAC = 1 the controller may continue with the access procedure.
2. The controller transmits its TIC bus address (TBA0…2). This is done in the same frame in which BAC = “1” was recognized. On the TIC bus binary “ZERO”s overwrite binary “ONE”s. Thus low TIC bus addresses have higher priority.
3. After transmitting a TIC bus address bit, the value is read back (with the falling edge) to check whether its own address has been overwritten by a controller with higher priority. This procedure will continue until all three address bits are sent and confirmed.
   In case a bit is overwritten by an external controller with higher priority, the controller asking for bus access has to withdraw immediately from the bus by setting all TIC bus address bits to ONE.
4. If access was granted, the controller will put the D-channel data onto the IOM-2 bus in the following frame provided the S/G bit is set to ZERO (i.e. S-bus free to transmit). The BAC bit will be set to ZERO by the controller to block all remaining controllers.
   In case the S/G bit is ONE this prevents only the D-channel data to be switched

through to the IOM-2 bus. The TIC bus request remains unaffected (i.e. if access was granted the TIC address and BAC bit are activated). As soon as the S-bus D-channel is clear and the S/G bit was set back to “GO” the controller will commence with data transmission.
The S/G Bit generation in IOM-2 channel 2 is handled automatically by the IPAC operating in TE mode.

5. After the transmission of an HDLC frame has been completed the D-Channel controller withdraws from the TIC bus for two IOM-2 frames. This also applies when a new HDLC frame is to be transmitted in immediate succession. With this mechanism it is ensured that all connected controllers receive an equally fair chance to access the TIC bus.

2.3.4.2 S-Bus Priority Mechanism for D-Channel

The S-bus access procedure specified in ITU I.430 was defined to organize D-channel access with multiple TEs connected to a single S-bus.

To implement collision detection the D (channel) and E (echo) bits are used. The D-channel S-bus condition is indicated towards the IOM-2 interface with the S/G bit (see previous section).

The access to the D-channel is controlled by a priority mechanism which ensures that all competing TEs are given a fair access chance. This priority mechanism discriminates among the kind of information exchanged and information exchange history: Layer-2 frames are transmitted in such a way that signalling information is given priority (priority class 1) over all other types of information exchange (priority class 2). Furthermore, once a TE having successfully completed the transmission of a frame, it is assigned a lower level of priority of that class. The TE is given back its normal level within a priority class when all TEs have had an opportunity to transmit information at the normal level of that priority class.

The priority mechanism is based on a rather simple method: A TE not transmitting layer-2 frames sends binary 1s on the D-channel. As layer-2 frames are delimited by flags consisting of the binary pattern “01111110” and zero bit insertion is used to prevent flag imitation, the D-channel may be considered idle if more than seven consecutive 1s are detected on the D-channel. Hence by monitoring the D echo channel, the TE may determine if the D-channel is currently used by another TE or not.

A TE may start transmission of a layer-2 frame first when a certain number of consecutive 1s has been received on the echo channel. This number is fixed to 8 in priority class 1 and to 10 in priority class 2 for the normal level of priority; for the lower level of priority the number is increased by 1 in each priority class, i.e. 9 for class 1 and 11 for class 2.

A TE, when in the active condition, is monitoring the D echo channel, counting the number of consecutive binary 1s. If a 0 bit is detected, the TE restarts counting the number of consecutive binary 1s. If the required number of 1s according to the actual

level of priority has been detected, the TE may start transmission of an HDLC frame. If a collision occurs, the TE immediately shall cease transmission, return to the D-channel monitoring state, and send 1s over the D-channel.

2.3.4.3 S-Bus D-channel Control in TEs

If the IPAC is not in a point-to-point configuration in TE mode, D-channel collision on the S-bus can occur. For this purpose the characteristic of the D-channel Mode register must be programmed to DIM2-0 = 001 or 011 (refer to **table 27** of **chapter 4.3.7**) for D-channel collision resolution according to ITU I.430.

In this case the IPAC continuously compares the D data bits with the received E-echo bits. Depending on the priority class selected (8 or 10), the S/G bit is controlled in a way that data transmission by the internal D-channel controller or by an externally connected ICC will start after the appropriate number of E-bits set to ’1’ are detected by the layer 1 transceiver.

The priority class (priority 8 or priority 10) is selected by transferring the appropriate activation command via the Command/Indication (C/I) channel of the IOM-2 interface to the IPAC S-interface. If the activation is initiated by a TE, the priority class is selected implicitly by the choice of the activation command. If the S-interface is activated from the NT, an activation command selecting the desired priority class should be programmed at the TE on reception of the activation indication (AI8). In the activated state the priority class may be changed whenever required by simply programming the desired activation request command (AR8 or AR10).

Application

1. Priority Class 8/10 Selection with NT Initiated Activation

	TE IOM®-2			LT-S (NT) IOM®-2				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	
←	C/I	RSY	(0100b)	C/I	**AR**	**(1000b)**	¯	; Start activation from
←	C/I	AR	(1000b)	C/I	AR	(1000b)	→	; NT side
←	C/I	AI	(1100b)					;
_	**C/I**	**AR8**	**(1000b)**	C/I	Al	(1100b)	→	; Allocate highest priority
	D: transfer HDLC frame			C/I	**AI**	**(1100b)**	¯	; (e.g. for signaling data)
_	**C/I**	**AR10**	**(1001b)**					; Allocate lower priority
	D: transfer packet data							; for packet data
←	C/I	AI10	(1101b)					

2. Priority Class 8/10 Selection with TE Initiated Activation

	TE IOM®-2			NT IOM®-2				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	
_	**C/I**	**TIM**	**(0000b)**					; Request timing (IOM clocks)
←	C/I	PU	(0111b)					
_	**C/I**	**AR10**	**(1001b)**					; Activation with second
_	**C/I**	**TIM Release**		C/I	AR	(1000b)	→	; priority (e.g. for packet data)
←	C/I	RSY	(0100b)	**C/I**	**AR**	**(1000b)**	¯	
←	C/I	AR	(1000b)	C/I	AI	(1100b)	→	
←	C/I	AI10	(1101b)	**C/I**	**AI**	**(1100b)**	¯	;
	D: transfer packet data							
_	**C/I**	**AR8**	**(1000b)**					; Allocate highest priority
	D: transfer HDLC frame							
←	C/I	AI8	(1100b)					

2.3.4.4 S-Bus D-Channel Control in LT-T

In LT-T mode the IPAC is primarily considered to be in a point-to-point configuration. In these configurations no S-bus D-channel collision can occur, therefore the default setting after resetting the IPAC is transparent (IOM-2 $\rightarrow$ S-bus) D-channel transmission.

In case a point to multipoint configuration is implemented, the characteristic of the D-channel Mode register must be programmed to DIM2-0 = 001 or 011 (refer to **table 27** of **chapter 4.3.7**) for D-channel collision resolution according to ITU I.430.

Priority allocation is identical to that described for the TE mode.

2.3.4.5 D-Channel Control in the Intelligent NT (TIC- and S-Bus)

In intelligent NT applications both the IPAC and one or more D-channel controllers on the S interface and/or the IOM-2 interface have to share a single upstream D-channel.

The intelligent NT configuration involves a layer-1 device (e.g. IEC-Q TE) operating in TE mode (1.536 MHz DCL rate) and an IPAC in LT-S mode with its D-channel controller operating in TE timing mode (D-channel transmitting in IOM-2 channel 0).

The IPAC incorporates an elaborate statemachine for D-channel priority handling on IOM-2. For the access to the D-channel a similar arbitration mechanism as on the S interface (writing D-bits, reading back E-bits) is performed for the local D-channel sources (local access), i.e. for the IPAC D-channel controller and for a D-channel controller connected to the IOM-2 interface (e.g. ICC PEB 2070). Due to this an equal and fair access is guaranteed for all D-channel sources on both the S interface and the IOM-2 interface.

For this purpose the IPAC is set in LT-S mode with its layer 1 function programmed to channel 1 and NT state machine activated. Therefore the layer 1 uses the C/I1 channel (which is realized by the layer 2 function), however the B1-, B2- and D-channels have to be mapped in IOM channel 0.

The layer 2 function is configured to TE timing mode (D- and C/I-channel controller transmits on C/I0 and evaluates C/I0 and C/I1) with S/G bit evaluation (refer to **table 27** of **chapter 4.3.7**). The priority handler for D-channel access on IOM-2 is enabled and the priority 8 or 10 is selected.

The configuration settings of the IPAC in intelligent NT applications are summarized in **table 3**.

Table 3 IPAC Configuration Settings in Intelligent NT Applications

Functional Block	Configuration Description	Configuration Setting
Layer 1	Select LT-S mode	Pins: MODE0 = 1 MODE1 = 0
	Select IOM-2 channel 1	Pins: CH2-0 = 001
	Activate NT state machine	MON-8 Configuration Register: FSMM = 1
	Map channels B1, B2 and D to IOM channel 0	MON-8 IOM-2 Channel Register: B1L = 1, B2L = 1, DL = 1
Layer 2	Select TE timing mode	Register: SPCR:SPM = 0
	Enable S/G bit evaluation	Register: MODED:DIM2-0 = 001
	Enable D-channel priority handler on IOM-2	Register: CONF:IDH = 1
	Select priority 8 or 10 for D-channel priority handler on IOM-2	Register: SCFG:PRI

With the configuration settings shown above the IPAC in intelligent NT applications provides for equal access to the D-channel for terminals connected to the S-interface and for D-channel sources on IOM-2.
For a detailed understanding the following sections provide a complete description on the procedures used by the D-channel priority handler on IOM-2, although this may not be necessary to use this mode.

1. NT D-Channel Controller Transmits Upstream

In the initial state (’Ready’ state) neither the local D-channel sources nor any of the terminals connected to the S-bus transmit in the D-channel.

The IPAC S-transceiver thus receives BAC = “1” (IOM-2 DU line) and transmits S/G = “0” (IOM-2 DD line). The access will then be established according to the following procedure:

- Local D-channel source verifies that BAC bit is set to ONE (currently no bus access).
- Local D-channel source issues TIC bus address and verifies that no controller with higher priority requests transmission.
- Local D-channel source issues BAC = “0” to block other sources on IOM-2 and starts D-channel transmission.
- IPAC S-transceiver transmits inverted echo channel (E bits) on the S-bus to block all connected S-bus terminals (E = $\overline{D}$).
- Local D-channel source commences with D data transmission on IOM-2 as long as it receives S/G = “0”.
- After D-channel data transmission is completed the controller sets the BAC bit to ONE.
- IPAC S-transceiver pulls S/G bit to ONE (’Ready’ state) to block the D-channel controller on IOM-2.
- IPAC S-transceiver transmits non-inverted echo (E = D).
- IPAC S-transceiver pulls S/G bit to ZERO (’Idle’ state) as soon as n D-bits = ’1’ are counted on IOM-2 (see note) to allow for further D-channel access.

Note: Right after transmission the S/G bit is pulled to ’1’ until n successive D-bits = ’1’ occur on the IOM-2 interface. As soon as n D-bits = ’1’ are seen, the S/G bit is set to ’0’ and the IPAC D-channel controller may start transmission again. This allows an equal access for D-channel sources on IOM-2 and on the S interface.
The number n depends on configuration settings (selected priority 8 or 10) and the condition of the previous transmission, i.e. if an abort was seen (n = 8 or 10, respectively) or if the last transmission was successful (n = 9 or 11, respectively).

Figure 19 illustrates the signal flow in an intelligent NT and the algorithm of the D-channel priority handler on IOM-2 implemented in the IPAC.

2. Terminal Transmits D-Channel Data Upstream

The initial state is identical to that described in the last paragraph. When one of the connected S-bus terminals needs to transmit in the D-channel, access is established according to the following procedure:

- IPAC S-transceiver (in intelligent NT) recognizes that the D-channel on the S-bus is active.
- IPAC S-transceiver sets S/G = 1 to block local D-channel sources.
- IPAC S-transceiver transfers S-bus D-channel data transparently through to the upstream IOM-2 bus (IOM-2 channel 0).
- After D-channel transmission has been completed by the terminal and the IPAC S-transceiver in the intelligent NT recognizes the idle condition (i.e. eight consecutive D=1) on the S-bus D-channel, the S/G bit is set to ZERO.

For both cases described above the exchange indicates via the A/B bit (controlled by layer 1) that D-channel transmission on this line is permitted (A/B = “1”). Data transmission could temporarily be prohibited by the exchange when only a single D-channel controller handles more lines (A/B = “0”, ELIC-concept).
In case the exchange prohibits D data transmission on this line the A/B bit is set to “0” (block). For U_{PN} applications with S extension this forces the intelligent NT IPAC S-transceiver to transmit an inverted echo channel on the S-bus, thus disabling all terminal requests, and switches S/G to $\overline{A/B}$, which blocks the D-channel controller in the intelligent NT.

Note: Although the IPAC S-transceiver operates in LT-S mode and is pinstrapped to IOM-2 channel 0 or 1 it will write into IOM-2 channel 2 at the S/G bit position.

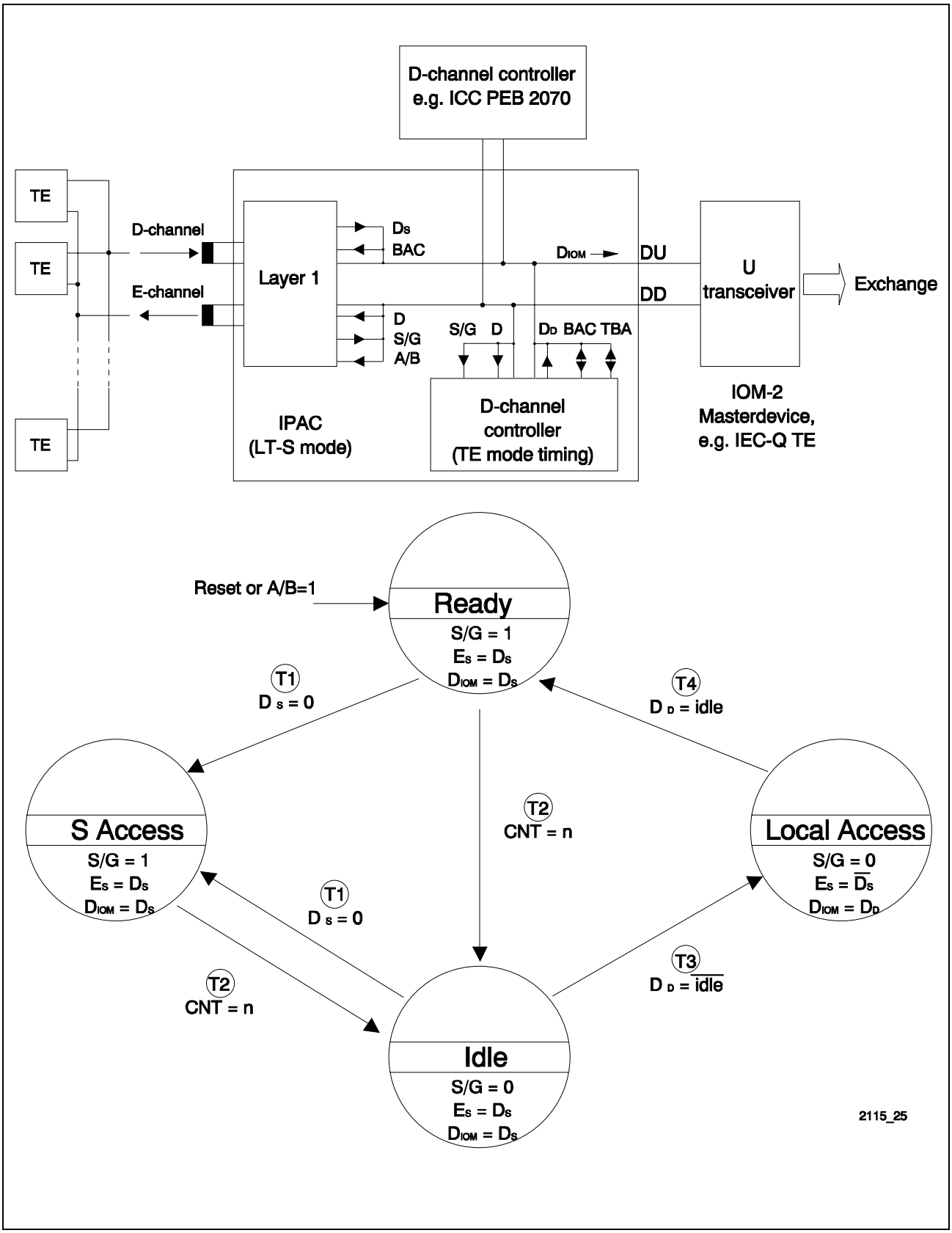


Figure 19 Data Flow for Collision Resolution Procedure in Intelligent NT

The state machine for D-channel access in the intelligent NT describes four states and four types of conditions for state transition:

States	
Ready	The D-channel is transparent to the layer 1 ($D_{IOM} = D_S$) and no device occupies the D-channel (BAC=1). The echo bits correspond to the received D-bits on the S-interface. The layer 2 is blocked (S/G=1) until the required number (priority) of D=1 are counted on IOM-2.
Idle	This state is identical to the 'Ready' state, except the layer 2 may also start transmission on the D-channel (S/G=0).
S Access	The D-channel is transparent to the layer 1 and occupied by a source on the S-interface. The layer 2 is blocked (S/G=1).
Local Access	The D-channel is occupied by the IPAC D-channel controller or by another D-channel controller on IOM-2. This is indicated by BAC=0. The Echo-bits are set to '$\overline{D}$' (terminals on S are blocked).
State transition conditions	
T1	A terminal on the S-interface has started transmission on the D-channel (D_S=0). Preceeding this, the required number of D=1 (according to the priority setting) was written and read back (E-bits) on the S-interface.
T2	The required number of D=1 is counted on the IOM-2 interface, so the IPAC D-channel controller may start transmission again.
T3	The IPAC layer 2 controller has started transmission on the D-channel ($D_D = \overline{idle}$).
T4	The IPAC layer 2 controller has stoped transmission on the D-channel (D_D = idle), i.e. the end flag of the previous frame or an abort is detected.

The number n of D=1 which has to be counted on IOM-2 by the state machine for state transition T2 is described in the table below:

	Previous transmission of NT D-channel controller	
Configured Priority	successful (end flag seen)	not successful (abort seen)
Prio = 8 (SCFG:PRI=0)	n = 9	n = 8
Prio = 10 (SCFG:PRI=1)	n = 11	n = 10

Note: D=idle implies that 8 consecutive '1' are detected on the D-channel.

2.3.5 IOM®-2 Interface Channel Switching

In order to realize intelligent NT configurations the IPAC provides basic switching functions. These include:

- Individual channel transfer from the selected (i.e. pin strapped) IOM-2 channel (channel 0 or 1) to IOM-2 channel 0.
- Individual channel reversion on input and output lines.

All switching functions are controlled via the MON-8 “IOM-2 channel” register (see MON-8 description). The following sections illustrate a variety of possible switching combinations typical for the intelligent NT. To facilitate the description of the switching function **figure 20** illustrates a typical intelligent NT with the speech CODEC ARCOFI combined with several terminals. Monitor programming for both ARCOFI and IPAC can only be performed in monitor channel 1.

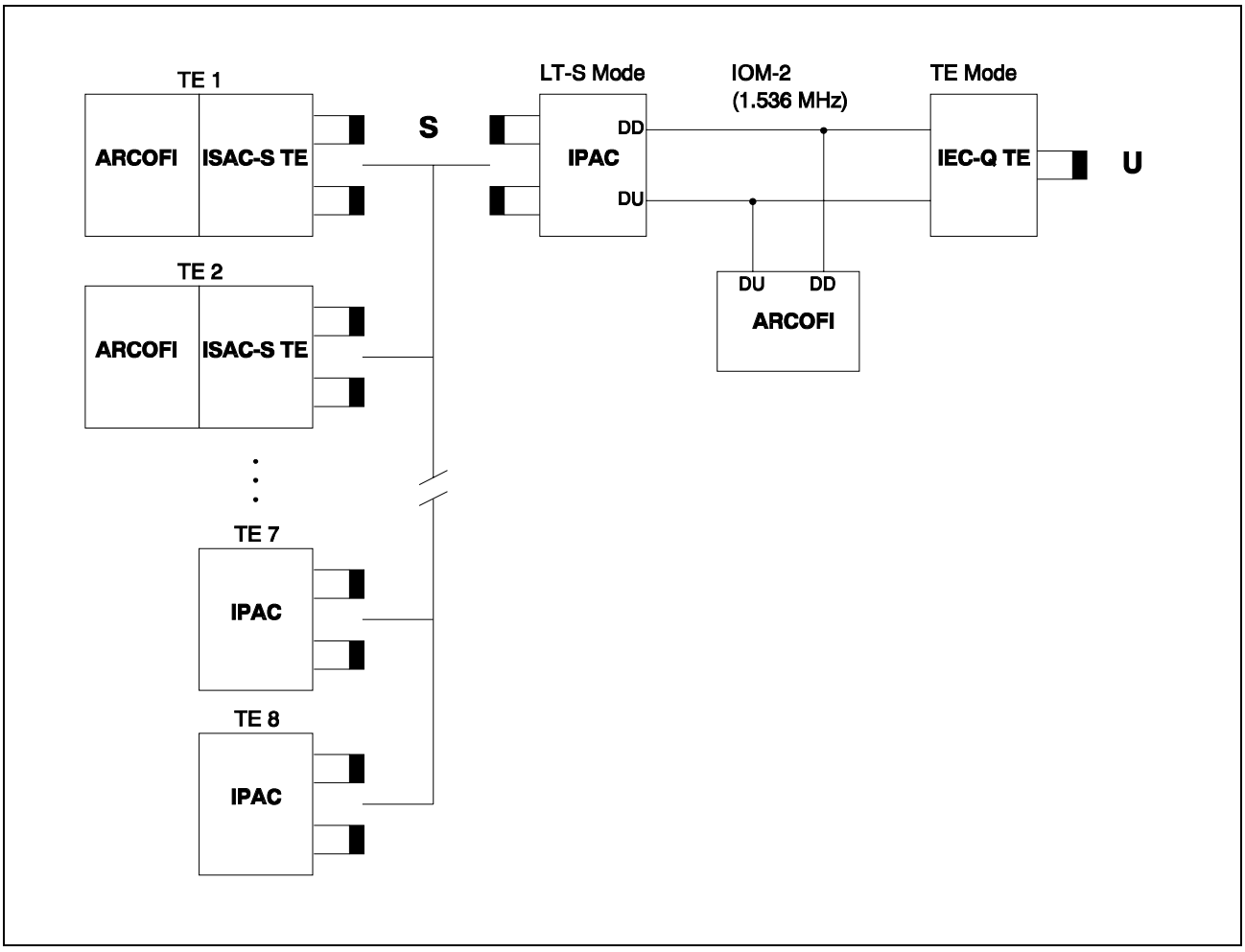
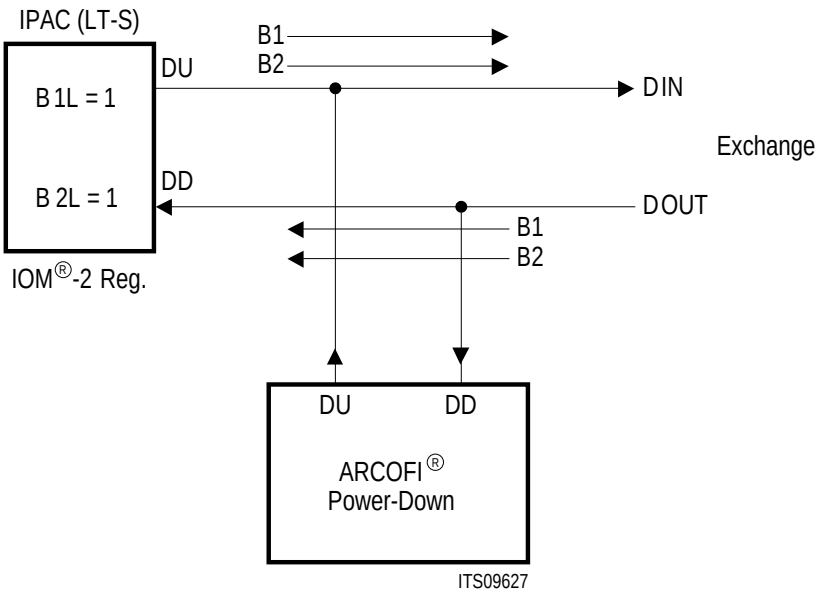


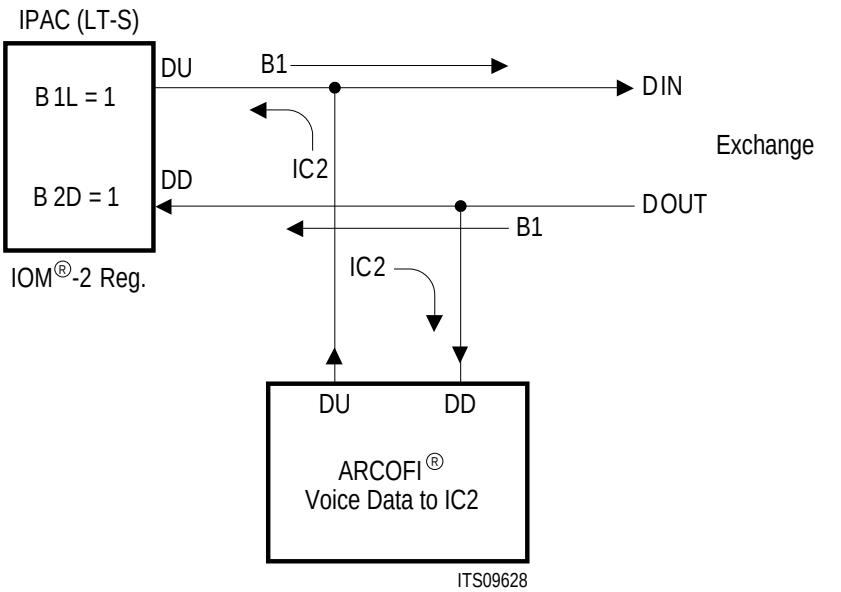
Figure 20 Intelligent NT-Configuration for IOM®-2 Channel Switching

The following four examples illustrate typical switching operations. Three of them are programmed in the “IOM-2 Channel” register, example No. 4 makes use of the “Loopback” register. All register bits related to the B1 or B2 channel are set to ZERO unless otherwise stated.

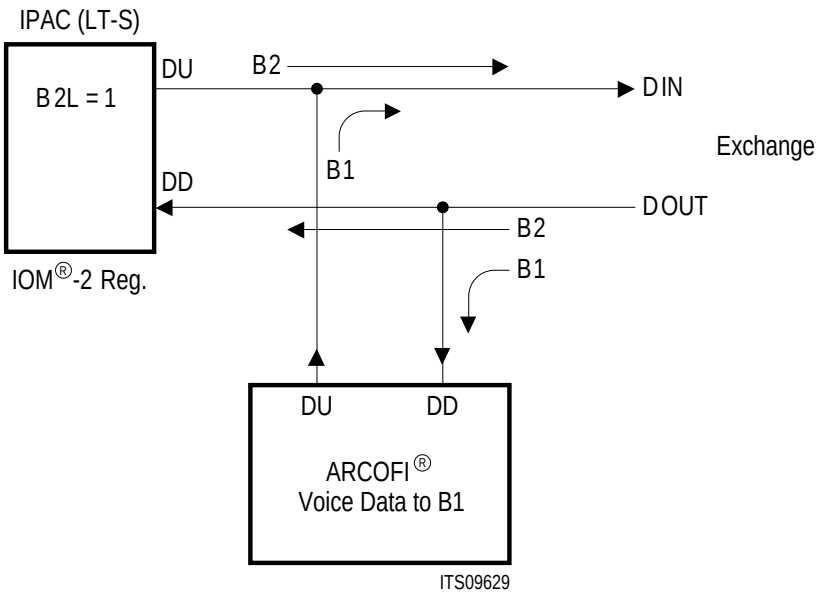
1. Connection B1 (e.g. TE1) → Exchange, B2 (e.g. TE8) → Exchange



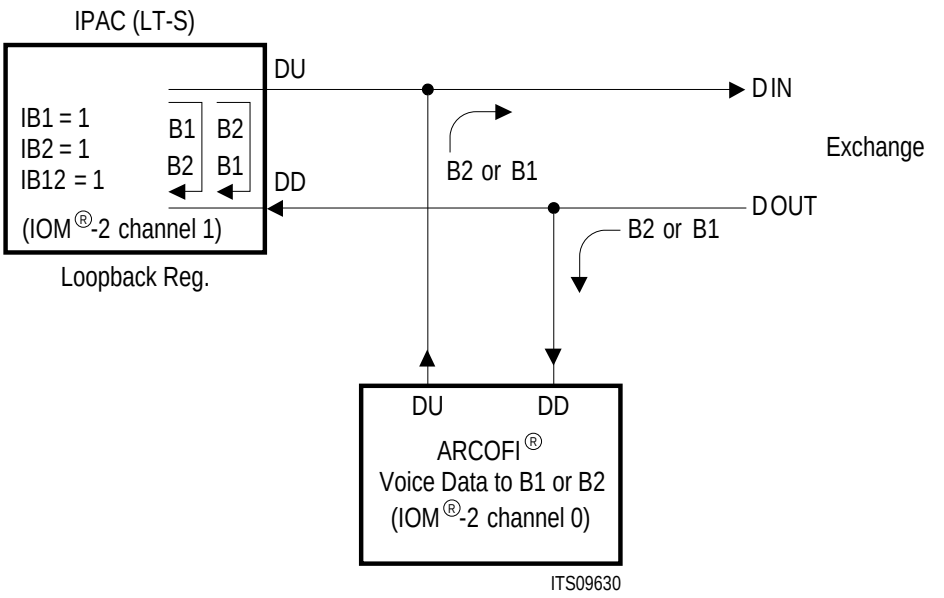
2. Connection B1 (e.g. TE1) → Exchange, B2 (e.g. TE8) → U-TE



3. Connection U-TE (B1) → Exchange, B2 (e.g. TE1) → Exchange



4. Connection TE1 (B1) ↔ TE8 (B2), U-TE (B1 or B2) → Exchange



2.4 S/T Interface

2.4.1 Operating Modes

The S-transceiver supports terminal mode (TE), line termination subscriber side mode (LT-S) and line termination trunk side mode (LT-T). The selection is performed by two mode pins (see **table 4**), additionally the B-channel receive and transmit data paths are switched to DU or DD line depending on the mode (**figure 21**). In other words, the DU line always carries data which is transferred from the subscriber to the central office and the DD line carries data which comes from the central office to the subscriber. Therefore the direction of DU and DD is mode dependent:

- DU is input, DD is output (TE and LT-T)
- DU is output, DD is input (LT-S)

In LT-S and LT-T mode the $\overline{\text{EAW}}$ pin is used as the second mode pin.

Table 4 Mode Setting

	MODE0	MODE1/ $\overline{\text{EAW}}$	Transmit-data on S	Receive-data on S
TE-mode	0	$\overline{\text{EAW}}$	DU on IOM	DD on IOM
LT-T mode	1	1	DU on IOM	DD on IOM
LT-S mode	1	0	DD on IOM	DU on IOM

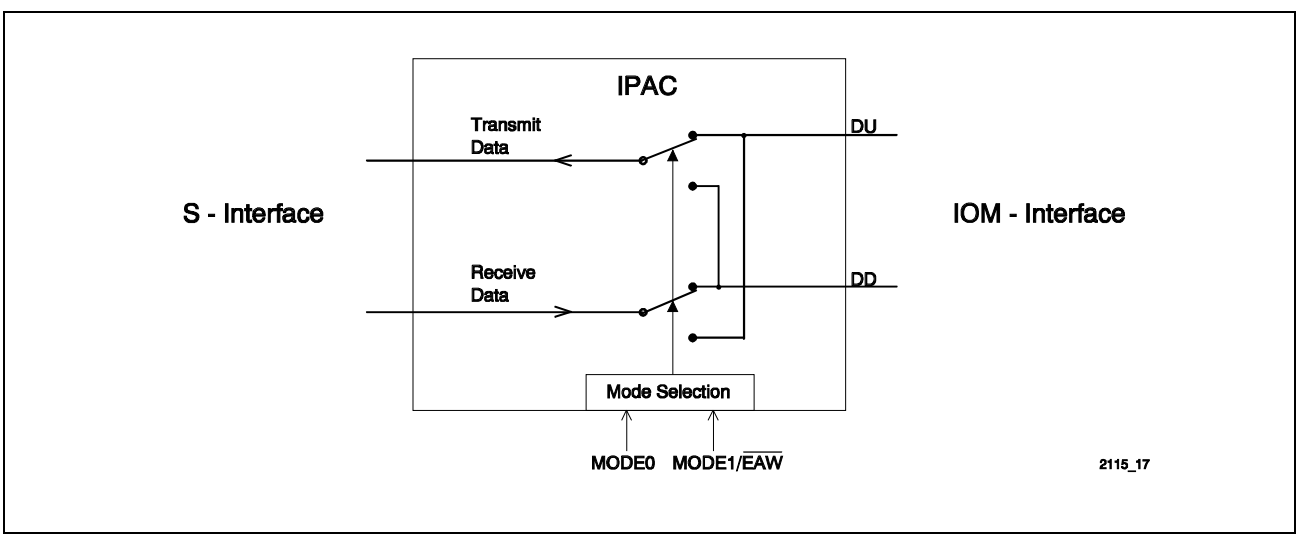


Figure 21 Data Path Switching

2.4.2 S/T-Interface Coding

Transmission over the S/T-interface is performed at a rate of 192 kbit/s. Pseudo-ternary coding with 100 % pulse width is used (**see following section**). 144 kbit/s are used for user data (B1+B2+D), 48 kbit/s are used for framing and maintenance information. The IPAC uses two symmetrical, differential outputs (SX1, SX2) and two symmetrical, differential inputs (SR1, SR2). These signals are coupled via external circuitry and two transformers onto the 4 wire S-interface. The nominal pulse amplitude on the S-interface is 750 mV (zero-peak).

The following figure illustrates the code used. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with two exceptions:
The first binary ZERO following the framing balance bit is of the same polarity as the framing-balancing bit (required code violation) and the last binary ZERO before the framing bit is of the same polarity as the framing bit.

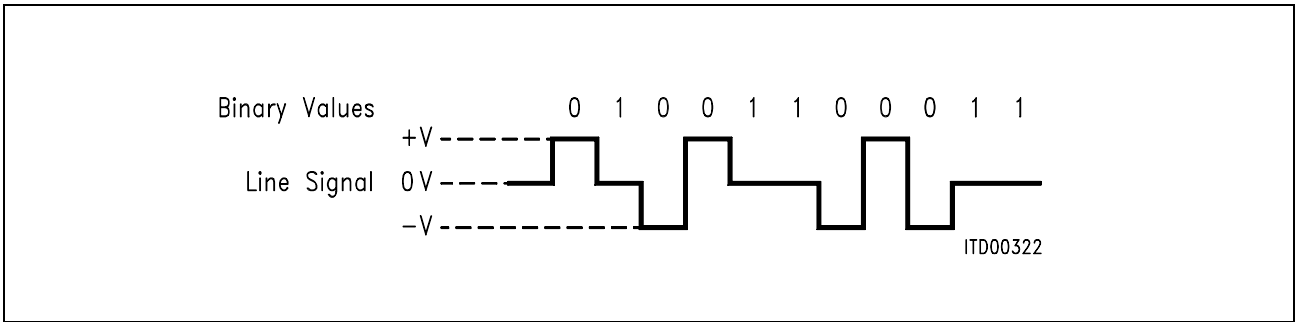


Figure 22 S/T -Interface Line Code (without code violation)

A standard S/T frame consists of 48 bits. In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

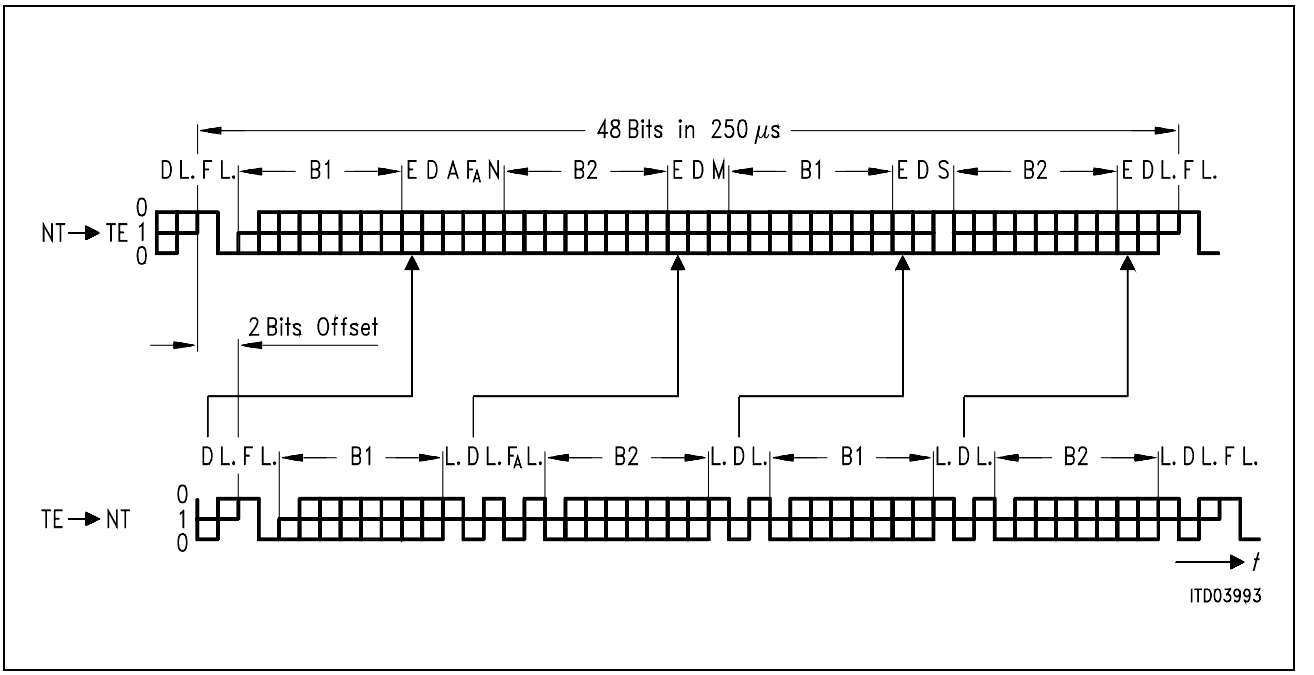


Figure 23 Frame Structure at Reference Points S and T (ITU I.430)

– F	Framing Bit	F = (0b) → identifies new frame (always positive pulse)
– L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
– D	D-Channel Data Bit	Signaling data specified by user
– E	D-Channel Echo Bit	E = D → no D-channel collision. ZEROs overwrite ONEs
– F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
– N		N = $\overline{F_A}$
– B1	B1-Channel Data Bit	User data
– B2	B2-Channel Data Bit	User data
– A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
– S	S-Channel Data Bit	S_1 or S_2 channel data (see note below)
– M	Multiframing Bit	M = (1b) → Start of new multi-frame

Note: The ITU I.430 standard specifies S1 - S5 for optional use.
The IPAC supports S1 - S2.

2.4.3 S/T-Interface Multiframing

According to ITU recommendation I.430 a multi-frame provides extra layer 1 capacity in the TE-to-NT direction through the use of an extra channel between the TE and NT (Q-channel). The Q bits are defined to be the bits in the F_A bit position.

In the NT-to-TE direction the S channel bits are used for information transmission. Two S channels (S1 and S2) out of five possible S channels can be accessed by the IPAC.

The S and Q channels are accessed via the IOM-2 interface monitor channel.

The following table shows the S and Q bit positions within the multi-frame.

Table 5 Multiframe Structure

Frame Number	NT-to-TE F_A Bit Position	NT-to-TE M Bit	NT-to-TE S Bit	TE-to-NT F_A Bit Position
1	ONE	ONE	S11	Q1
2	ZERO	ZERO	S21	ZERO
3	ZERO	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO	ZERO
6	ONE	ZERO	S12	Q2
7	ZERO	ZERO	S22	ZERO
8	ZERO	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO	ZERO
11	ONE	ZERO	S13	Q3
12	ZERO	ZERO	S23	ZERO
13	ZERO	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO	ZERO
16	ONE	ZERO	S14	Q4
17	ZERO	ZERO	S24	ZERO
18	ZERO	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO	ZERO
1	ONE	ONE	S11	Q1
2	ZERO	ZERO	S21	ZERO

In **TE** and **LT-T** mode the IPAC identifies the Q-bit position (after multi-frame synchronization has been established) by waiting for the F_A bit inversion in the received S/T-interface data stream (F_A [NT $\rightarrow$ TE] = binary ONE). After successful identification, the Q data will be inserted at the upstream (TE $\rightarrow$ NT) F_A bit position. When synchronization is not achieved or lost, it mirrors the received F_A bits.

Multi-frame synchronization is achieved after two complete multi-frames have been detected with reference to F_A/N bit and M bit positions. Multi-frame synchronization is lost after two or more bit errors in F_A/N bit and M bit positions have been detected in sequence, i.e. without a complete valid multi-frame between.

The multi-frame synchronization can be disabled by programming (MFD-bit in MON-8 configuration register).

2.4.4 S/T Transceiver Control

2.4.4.1 MON-8 Commands (Internal Register Access)

The S/T transceiver of the IPAC PSB 2115 contains four internal registers. Access to these registers is only possible via the IOM-2 monitor channel. The following registers are implemented in the IPAC:

- Configuration Register
- Loop-back Register
- IOM-2 Channel Register
- SM/CI Register

The structure of MON-8 write and read request/response commands are shown in the three tables below:

Table 6 MON-8 “Write to Register” Structure

1. Byte								2. Byte							
1	0	0	0	r	r	r	r	D7	D6	D5	D4	D3	D2	D1	D0
MON-8				Reg. Address				Register Data Write							

Table 7 MON-8 “Read Register Request” Structure

1. Byte								2. Byte							
1	0	0	0	0	0	0	0	0	0	0	0	r	r	r	r
MON-8												Reg. Address			

The response issued by the IPAC after having received a “Read Register Request” has the following structure.

Table 8 MON-8 “Read Response” Structure

1. Byte								2. Byte							
1	0	0	0	r	r	r	r	D7	D6	D5	D4	D3	D2	D1	D0
MON-8				Reg. Adr. Confirmation				Register Data Read							

The following sections describe the register features.

2.4.4.2 MON-8 Configuration Register

In the configuration register the user programs the IPAC for different operational modes, and selects required S-bus features.

The following paragraphs describe the application relevance of all individual configuration register bits.

Address: 1h

MFD	0	FSMM	LP	SQM	RCVE	C/W/P	0

RD/WR

Value after Reset: 00_H

MFD	Multi-Frame-Disable. Selects whether multiframe generation (LT-S) or synchronization (TE, LT-T) is prohibited (MFD=1) or allowed (MFD=0). Enable multiframing if S/Q channel data transfer is desired. If MFD=1 no S/Q MONITOR messages are released. When reading this register the bit indicates whether multiframe synchronization has been established (MFD=1) or not (MFD=0).
FSMM	Finite State Machine Mode. By programming this bit the user has the possibility to exchange the state machines of LT-S and NT, i.e. an IPAC pin strapped for LT-S operates with a NT state machine. All other operation mode specific characteristics are retained. This function is used in intelligent NT configurations where the IPAC needs to be pin-strapped to LT-S mode but the state machine of an NT is desirable.
LP	Loop Transparency. In case analog loop-backs are closed with C/I = ARL or bit SC in the loop-back register, the user may determine with this bit, whether the data is forwarded to the S/T-interface outputs (transparent) or not. The default setting depends on the operational mode. TE/LT-T modes: 0 = non transparent 1 = transparent ext. loop LT-S mode: 0 = transparent 1 = non transparent In LT-S by default transparency is selected (LP=0), for LT-T and TE non-transparency is standard (LP=0).

SQM	Selects the SQ channel handling mode. In non-auto mode operation, the IPAC issues S1 and Q messages in the IOM-2 monitor channel only after a change has been detected. The S2 channel is not available in non-auto mode. In transparent mode monitor messages containing the S1, S2 and Q data are forwarded to IOM-2 once per multiframe (5 ms), regardless of the data content. Programming the SQM bit is only relevant if multiframing on S/T is selected (bit MFD configuration register). See also MON-1 and MON-2 monitor messages.
RCVE	Receive Code Violation Errors. The user has the option to issue a C/I error code (CVR) everytime an illegal code violation has been detected. The implementation is realized according to ANSI T1.605.
C/W/P	This bit has three different meanings depending on the operational mode of the IPAC: In **LT-S** mode the S/T bus configuration is programmed. For point-to-point or extended passive bus configurations an adaptive timing recovery must be chosen. This allows the IPAC to adapt to cable length dependent round trip delays. In **LT-T** mode the user selects the amount of permissible wander before a C/I code warning will be issued by the IPAC. The warning may be sent after 25 µs (C/W/P=1) or 50 µs (C/W/P=0). **Note:** The C/I indication SLIP which will be issued if the specified wander has been exceeded, is only a warning. Data has not been lost at this stage. In **TE** mode this bit is not used

2.4.4.3 MON-8 Loop-Back Register

The loop-back register controls all analog (S/T-interface) and digital (IOM-2 interface) loop-backs. Additionally the wake-up mode can be programmed.

Address: 2h	AST	SB1	SB2	SC	IB1	IB2	1	IB12	RD/WR

Value after Reset: 02_H

.

AST	Asynchronous Timing. Defines the length of the Timing signal (DU = 0) on IOM-2. If synchronous timing is selected (AST=0) the IPAC in LT-S mode will issue the timing request only in the C/I channel of the selected timeslot (C/I = 0000b). This mode is useful for applications where IOM-2 clock signals are not switched off. Here the IPAC can pass the TE initiated activation via C/I = 0000b in IOM-2 cannel 0 upstream to the U-interface device. In case IOM-2 clocks can be turned off during power-down or the LT-S IPAC is pin-strapped to a different timeslot than the U-interface device, synchronous timing signals will not succeed in waking the U-interface device. Under these circumstances asynchronous timing needs to be programmed (AST=1). Here the line DU is set to ZERO for a period long enough to wake any U-interface device, independent of timeslot or clocks. Typically asynchronous timing is programmed for intelligent NT applications (IPAC pin-strapped to LT-S with NT state machine). **Note:** The asynchronous timing option is restricted to configurations with the IPAC operating with NT state machine (i.e., LT-S pin-strap & FSMM bit programmed).
SB1	Closes the loop-back for B1 channel data close to the activated S/T-interface (i.e., loop-back IOM-2 data) in LT-S mode.
SB2	Closes the loop-back for B2 channel data close to the activated S/T-interface (i.e., loop-back IOM-2 data) in LT-S mode.
SC	Close complete analog loop-back (2B+D) close to the S/T-interface. Corresponds to C/I = ARL. Transparency is optional. Operational in LT-S mode.
IB1	Close the loop-back for B1 channel close to the IOM-2 interface (i.e. loop-back S/T data). Transparent. IB1 and IB2 may be closed simultaneously.

IB2	Close the loop-back for B2 channel close to the IOM-2 interface (i.e. loop-back S/T data). Transparent. IB1 and IB2 may be closed simultaneously.
IB12	Exchange B1 and B2 channels. IB1 and/or IB2 need to be programmed also. Loops back data received from S/T and interchanges it, i.e. B1 input (S/T) $\rightarrow$ B2 output (S/T) and vice versa.

2.4.4.4 MON-8 IOM®-2 Channel Register

The features accessible via the IOM-2 Channel register allow to implement simple switching functions. These make the IPAC the ideal device for intelligent NT applications. Please refer also to the section “IOM-2 channel switching”. Two types of manipulation are possible: the transfer from the pin-strapped IOM-2 channel (0 … 7) into IOM-2 channel 0 and a change of the B1, B2 and D data source.

Address: 3h

B1L	B1D	B2L	B2D	DL	0	CIL	CIH

RD/WR

Value after Reset: 00_H

B1L	Transfers the B1 channel from its pin-strapped location into IOM-2 channel 0.
B1D	Direction of the B1 channel. The normal direction (input/output) of DU and DD depends on the mode and is shown in **table 4** below. By setting B1D the direction for the B1 data channel is inverted.
B2L	Transfers the B2 channel from its pin-strapped location into IOM-2 channel 0.
B2D	Direction of the B2 channel. The normal direction (input/output) of DU and DD depends on the mode and is shown in **table 4** below. By setting B2D the direction for the B2 data channel is inverted.
DL	Transfers the D-channel from its pin-strapped location into IOM-2 channel 0.
CIL	C/I Channel location: The timeslot position of the C/I Channel can be programmed as “normal“ (LT-S and LT-T modes: pin strapped IOM-2 channel, TE mode: IOM-2 channel 0) or “fixed“ to IOM-2 channel 0 (regardless the selected mode).
CIH	C/I Channel handling: Normally the C/I commands are read from the pin-strapped IOM-2 channel. With this bit programmed C/I channel access is only possible via the SM/CI register.

Table 9 DU/DD Direction

	MODE0	**MODE1 /$\overline{\text{EAW}}$**	**Transmit data on S**	**Receive data on S**
TE-mode	0	$\overline{\text{EAW}}$	DU (input)	DD (output)
LT-T mode	1	1	DU (input)	DD (output)
LT-S mode	1	0	DD (input)	DU (output)

2.4.4.5 MON-8 SM/CI Register

This multifeature register allows access to the C/I channel and controls the monitor time-out.

Address: 4h	CI3	CI2	CI1	CI0	TOD	0	0	0	RD/WR

Value after Reset: $X0_H$ (X contains the C/I code)

C/I	Allows the user to access the C/I channel if the CIH bit in the IOM-2 register has been set previously. If the CIH bit was not programmed the content of the CI bits will be ignored and the IPAC will access the IOM-2 C/I channel. When reading the SM/CI register these bits will always return the current C/I indication (independent of CIH bit).
TOD	Time Out Disable. Allows the user to disable the monitor time-out function. Refer to section “Monitor Timeout” for details.

2.5 Layer-1 Functions for the S/T Interface

The common functions in all operating modes are:

– line transceiver functions for the S/T interface according to the electrical specifications of CCITT I.430;
– conversion of the frame structure between IOM and S/T interface;
– conversion from/to binary to/from pseudo-ternary code;
– level detect.
– Mode specific functions are:

- receive timing recovery for point-to-point, passive bus and extended passive bus configuration;
- S/T timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation by handling of the global echo bit;
- activation/deactivation procedures, triggered by primitives received over the IOM C/I channel or by INFO's received from the line;
- execution of test loops.

The wiring configurations in user premises, in which the IPAC can be used, are illustrated in **figure 24**.

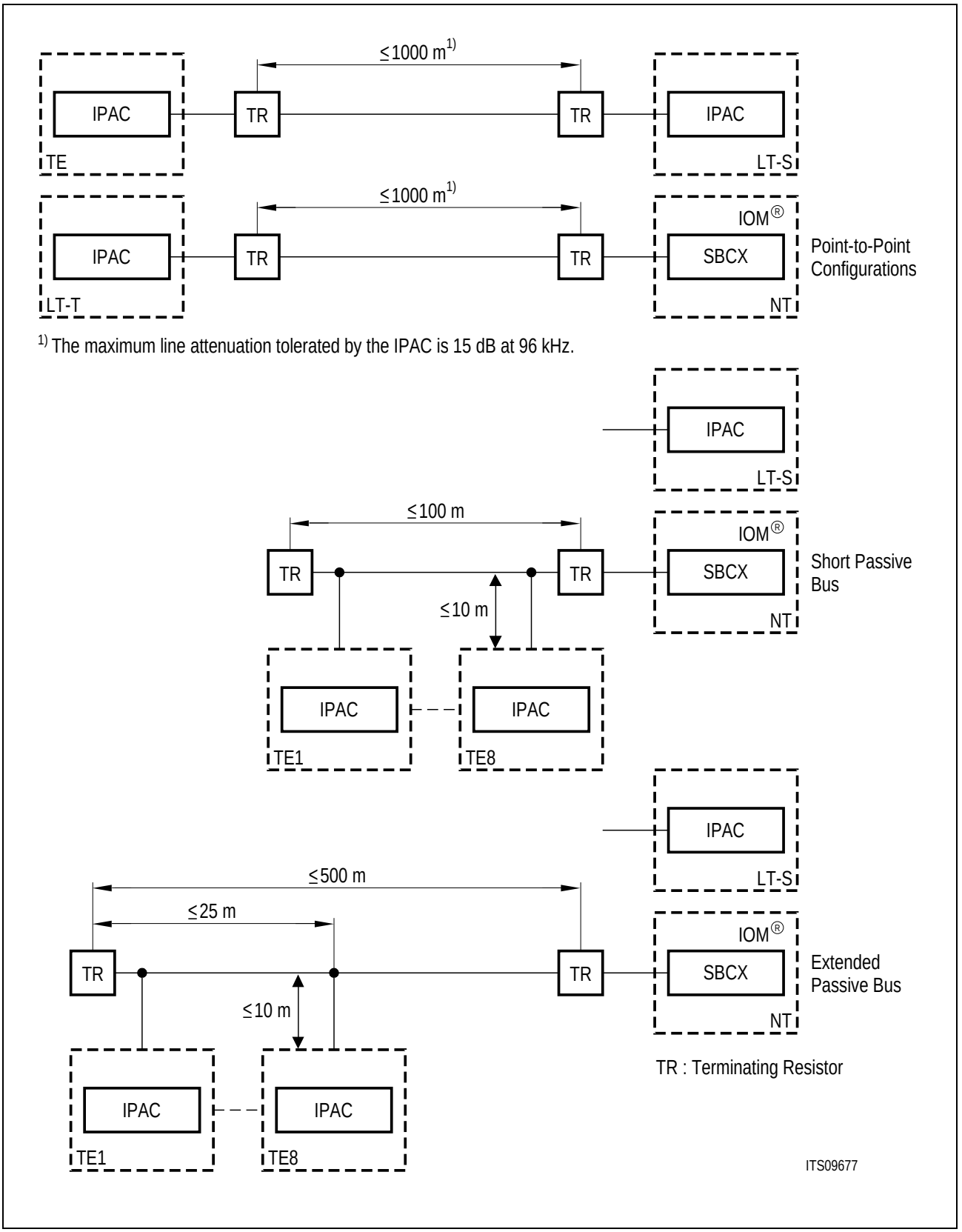


Figure 24 Wiring Configurations in User Premises

2.5.1 Analog Functions

For both receive and transmit direction, a 2:1 transformer is used to connect the ISAC-S transceiver to the 4 wire S/T interface (CONF:AMP=0). As an option, the receiver can also be operated with a 1:1 transformer (CONF:AMP=1). The connections are shown in **figure 25**.

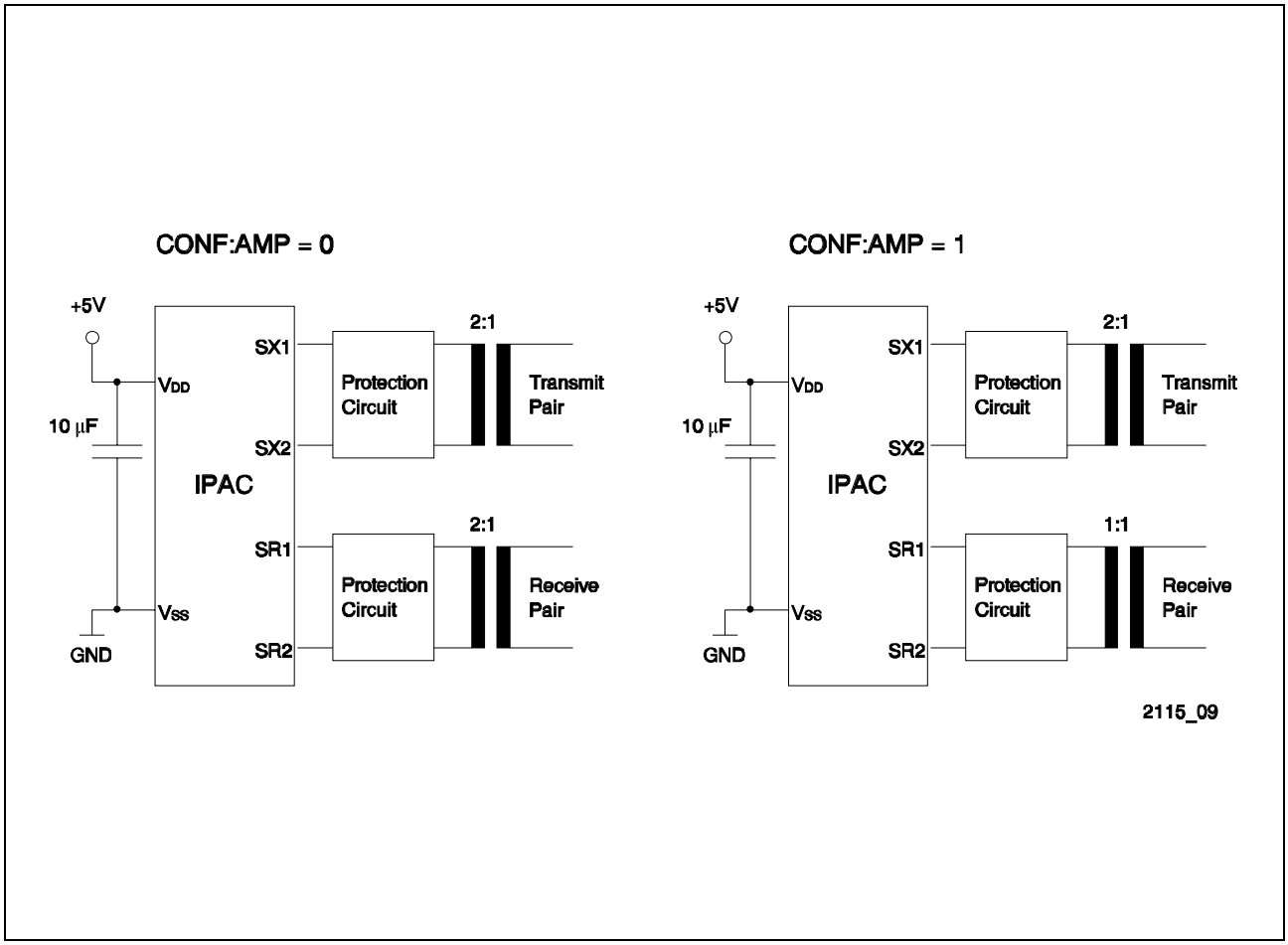


Figure 25 Connection of the Line Transformers and Power Supply to the IPAC

The external transformers are needed in both receive and transmit direction to provide for isolation and transform voltage levels according to CCITT recommendations.

The equivalent circuits of the integrated receiver and transmitter are shown in **figure 26**.

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as a current limited voltage source.

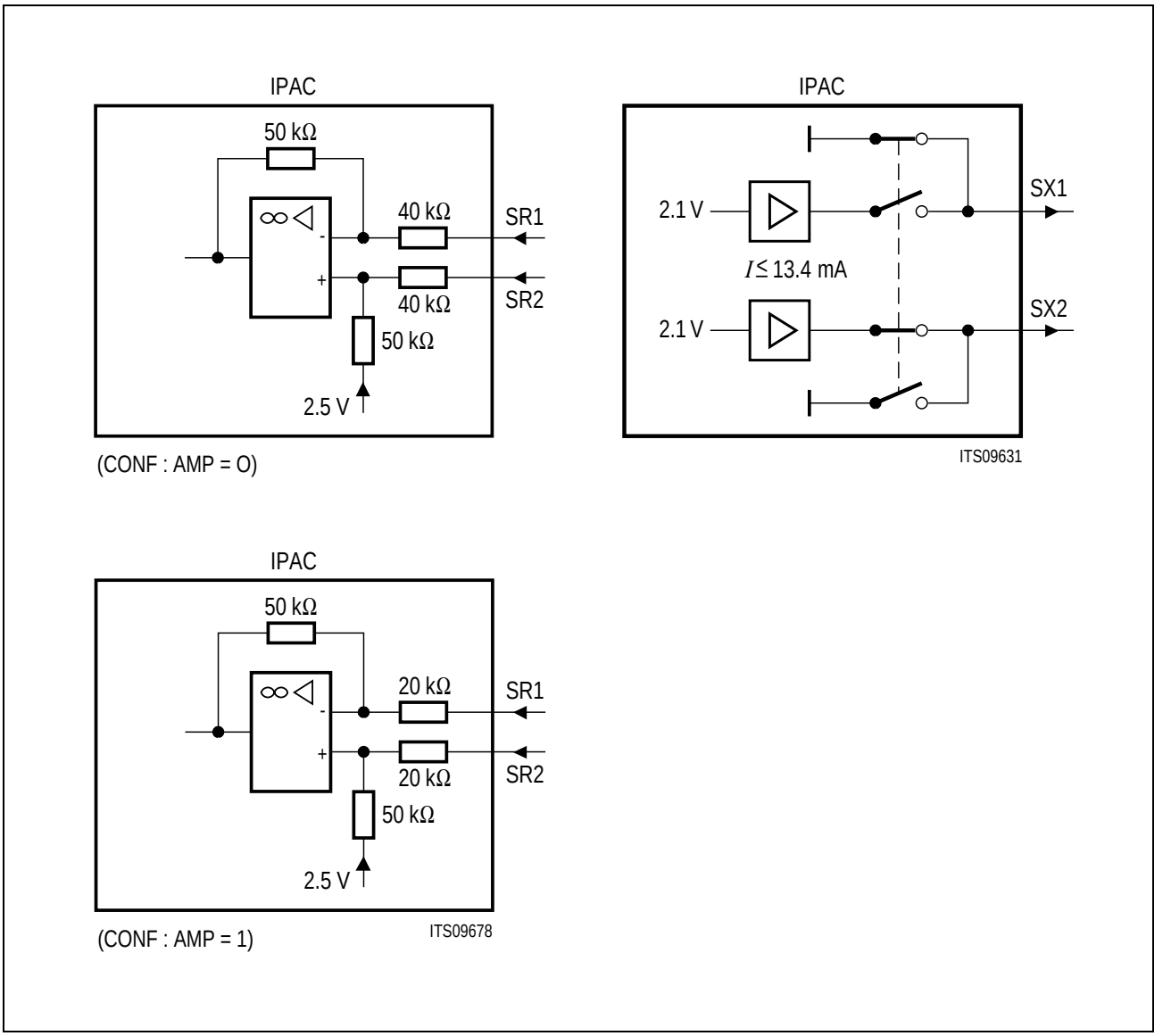


Figure 26 Equivalent Internal Circuits of Receiver and Transmitter Stages

The transmitter of the PSB 2115 IPAC is identical to that of the well known PEB 2086 ISAC-S, hence, the line interface circuitry should be similar. The external resistors (24 ... 33 Ω) are required in order to adjust the output voltage to the pulse mask (nominal 750 mV according CCITT I.430) on the one hand and in order to meet the output impedance of minimum 20 Ω (transmission of a binary zero according to CCITT I.430) on the other hand.

The S-bus receiver of the PSB 2115 is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2.

The S-bus receiver of the PSB 2115 is symmetrical, which allows for a simple external circuitry and PCB layout to meet the I.430 receiver input impedance specification.

2.5.2 S/T Interface Circuitry

2.5.2.1 S/T Interface Pre-Filter Compensation

To compensate for the extra delay introduced into the receive and transmit path by the external circuit, the delay of the transmit data can be reduced by 260 ns (i.e. two oscillator cycles). Therefore PDS of the CONF register must be programmed to “1“.

This delay compensation might be necessary in order to comply with the "total phase deviation input to output" requirement of CCITT recommendation I.430 which specifies a phase deviation in the range of – 7% to + 15% of a bit period.

2.5.2.2 External Protection Circuitry

The CCITT specification for both transmitter and receiver impedances in TEs results in a conflict with respect to external S-protection circuitry requirements:

– To avoid destruction or malfunctioning of the S-device it is desirable to drain off even small overvoltages reliably.
– To meet the 96 kHz impedance test specified for transmitters and receivers (for TEs only, CCITT sections 8.5.1.2a and 8.6.1.1) the protection circuit must be dimensioned such that voltages below 2.4 V are not affected (1.2 V CCITT amplitude multiplied by transformer ratio 1:2).

  This requirement results from the fact that this test is to be performed with no supply voltage being connected to the TE. Therefore the second reference point for overvoltages V_{DD}, is tied to GND. Then, if the amplitude of the 96 kHz test signal is greater than the combined forward voltages of the diodes, a current exceeding the specified one may pass the protection circuit.

The following recommendations aim at achieving the highest possible device protection against overvoltages while still fulfilling the 96 kHz impedance tests.

If the device is not used in TE or LT-T applications, the four diodes could be bridged and the 5.4 V Zener diode could be omitted.

Protection Circuit for Transmitter

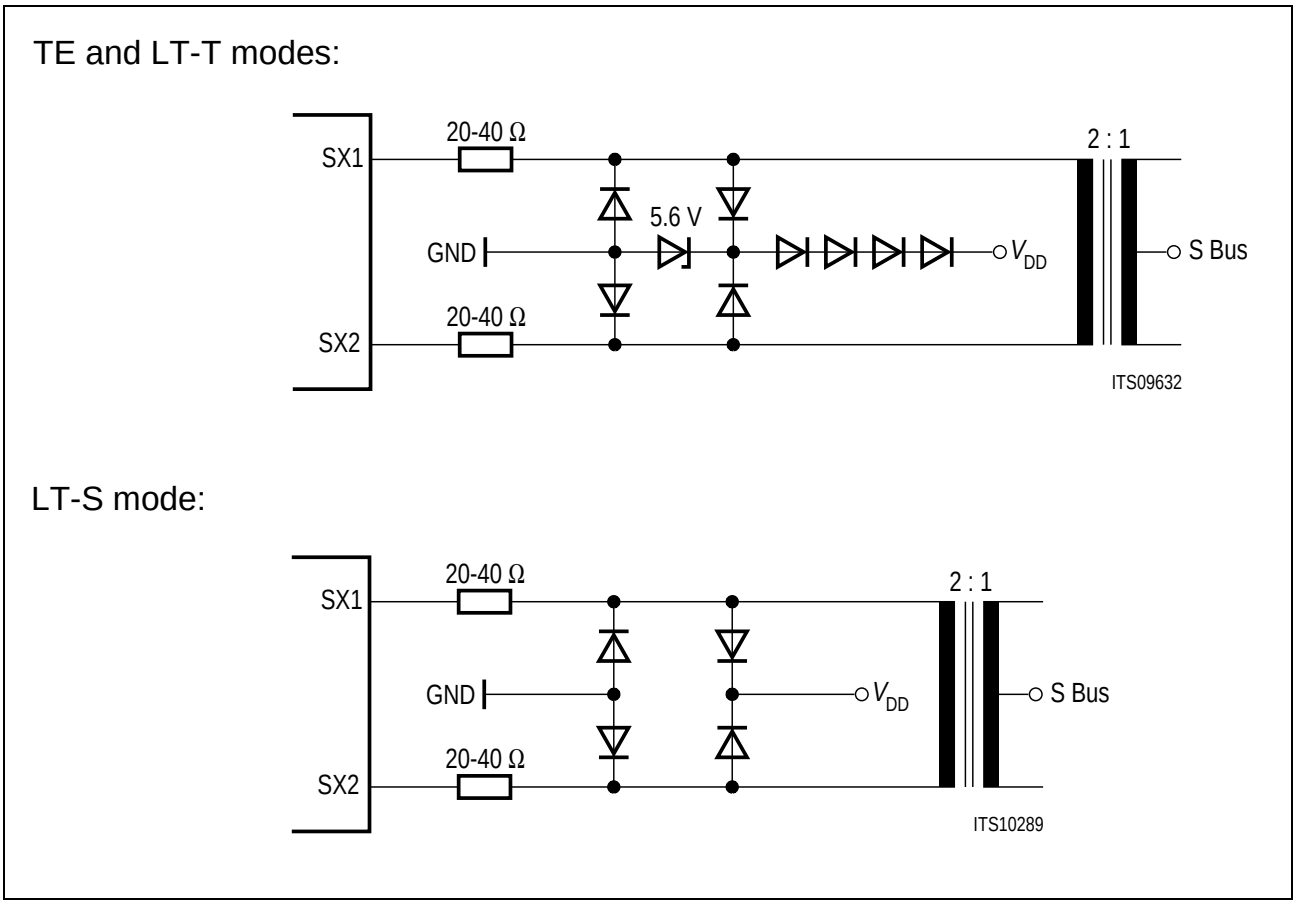


Figure 27 External Circuitry for Transmitters

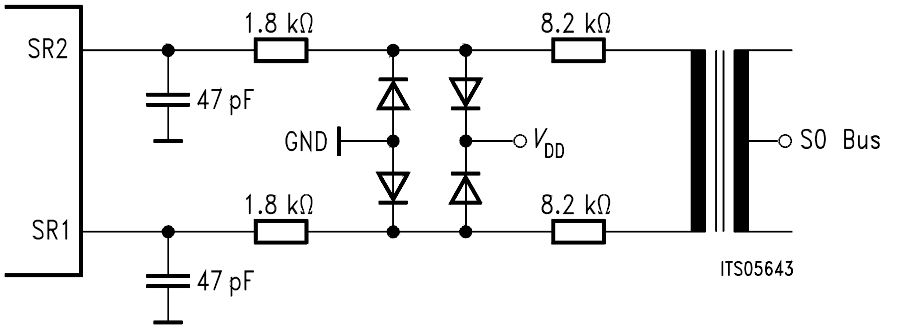
Figure 27 illustrates the secondary protection circuit recommended for the transmitter. An ideal protection circuit should limit the voltage at the SX pins from – 0.4 V to V_{DD} + 0.4 V.

Via the two resistors (typ. 20 ... 40 Ω) the transmitted pulse amplitude is adjusted to comply with the requirements. Two mutually reversed diode paths (low capacitive diodes are recommended, e.g. 1N4151) protect the device against positive or negative overvoltages on both lines.

The pin voltage range is increased from – 0.7 V to V_{DD} + 3.5 V. The resulting forward voltage will prevent the protection circuit to become active if the 96 kHz test signal is applied while no supply voltage is present. In TE / LT-T modes the 5.6 V zener diode is provided to be completely on the safe side, however, system tests may reveal that it can be omitted.

Protection Circuit for Receivers

Figure 28 illustrates the external circuitry used in combination with a symmetrical receiver. Protection of symmetrical receivers is rather comfortable.



Note: Capacitors are optional for noise reduction (up to 47 pF)

Figure 28 External Circuitry for Symmetrical Receivers

Between each receive line and the transformer a 10 kΩ resistor is used. This value is split into two resistors: one between transformer and protection diodes for current limiting during the 96 kHz test, and the second one between input pin and protection diodes to limit the maximum input current ot the chip.

With symmetrical receivers no difficulties regarding LCL measurements are observed; compensation networks thus are obsolete.

In order to comply to the physical requirements of CCITT recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compability (EMC), the IPAC needs additional circuitry.

2.5.3 Receiver Functions

2.5.3.1 Receiver Characteristics

In order to additionally reduce the bit error rate in severe conditions, the IPAC performs oversampling of the received signal and uses majority decision logic.

The receiver consists of a differential to single ended input stage, a peak detector and a set of comparators. Additional noise immunity is achieved by digital oversampling after the comparators. The following **figure 29** describes the functional blocks of the receiver (for receiver tansformer ratio 2:1). The equivalent internal circuit for transformer ratio 1:1 (CONF:AMP=1) is shown in **figure 26**.

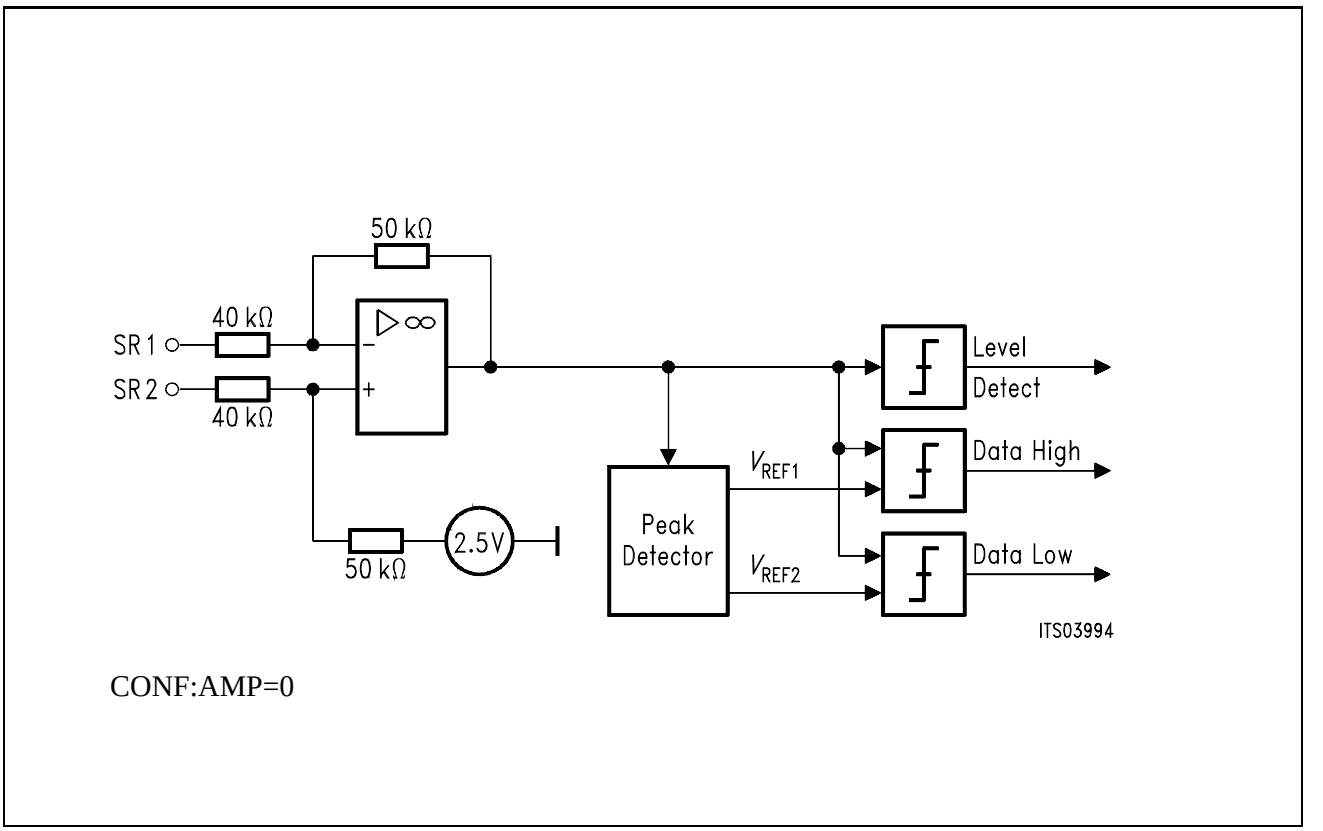


Figure 29 Receiver Circuit

The input stage works together with external 10 kΩ resistors to match the input voltage to the internal thresholds. The data detection thresholds are chosen to 35 % of the peak voltage to increase the performance in extended passive bus configurations. However they never go below 85 mV with respect to the line signal level. This guarantees a maximum line attenuation of at least 13 dB in point-to-point configurations with a margin of more than 70 mVpp with respect to the specified 100 mVpp noise.

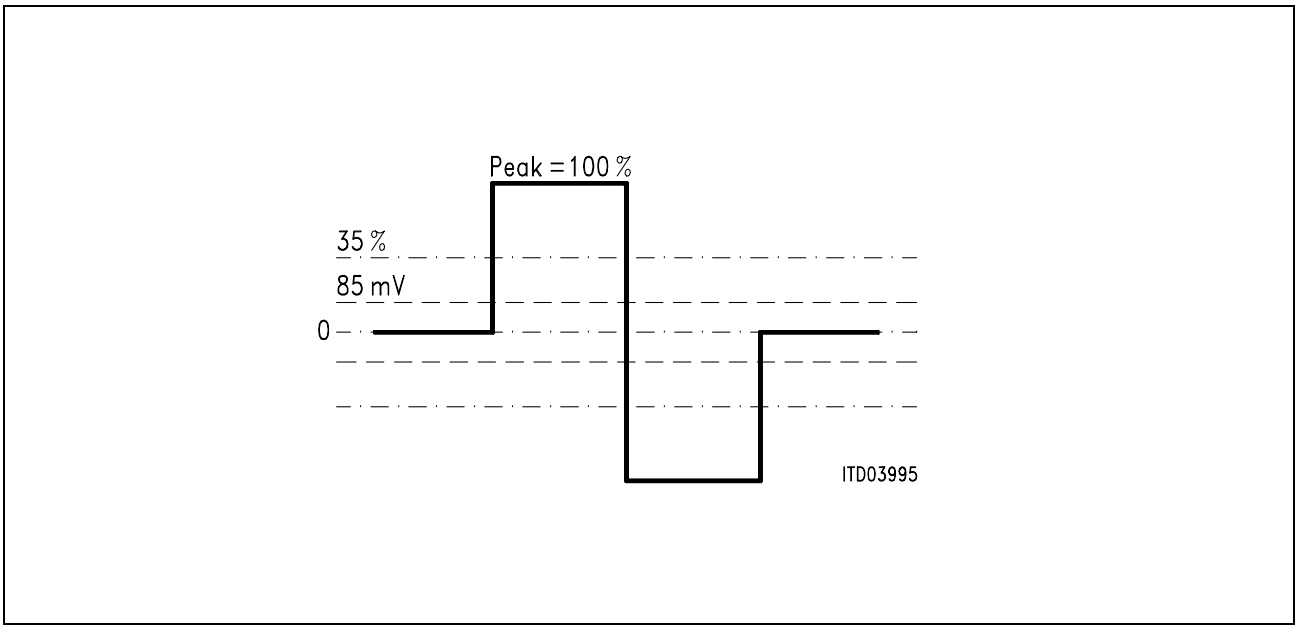


Figure 30 Receiver Thresholds

The peak detector requires maximum 2 µs to reach the peak value while storing the peak level for at least 250 µs (RC > 1 ms).

The additional level detector for power up/down control works with fixed thresholds at 100 mV. The level detector monitors the line input signals to detect whether an INFO is present. In TE and LT-T mode, when closing an analog loop, it is therefore possible to indicate an incoming signal during activated loop. In LT-S analog loop-back mode the level detector monitors its own loop signal and an incoming signal is not recognized.

2.5.3.2 Level Detection Power Down (TE mode)

If CONF:CFS is set to “0“, the clocks are also provided in power down state, whereas if CFS is set to “1“, only an analog level detector is active in power down state. All clocks, including the IOM interface, are stopped. The data lines are "high", whereas the clocks are "low".

An activation initiated from the exchange side (Info 2 on S-bus detected) will have the consequence that a clock signal is provided automatically.

From the terminal side an activation must be started by setting and resetting the SPU-bit in the SPCR register and writing TIM to CIX0 or by resetting CFS=0.

2.5.4 S/T Transmitter Disable

The transmitter of the S/T interface can be disabled by configuration (see **figure 31**). By default (SCFG:TXD=0) both the S/T receiver and transmitter are active, but in order to reduce power consumption, the transmitter can be disabled (SCFG:TXD=1) separately.

In power down mode the power consumption is reduced to a minimum and the IPAC recognizes the activation of the S/T interface (incoming call). With several terminals connected to the S/T interface, another terminal may keep the interface activated although the IPAC does not establish a connection. In this case the IPAC receiver will monitor for incoming calls while the transmitter is disabled, thus reducing power consumption.

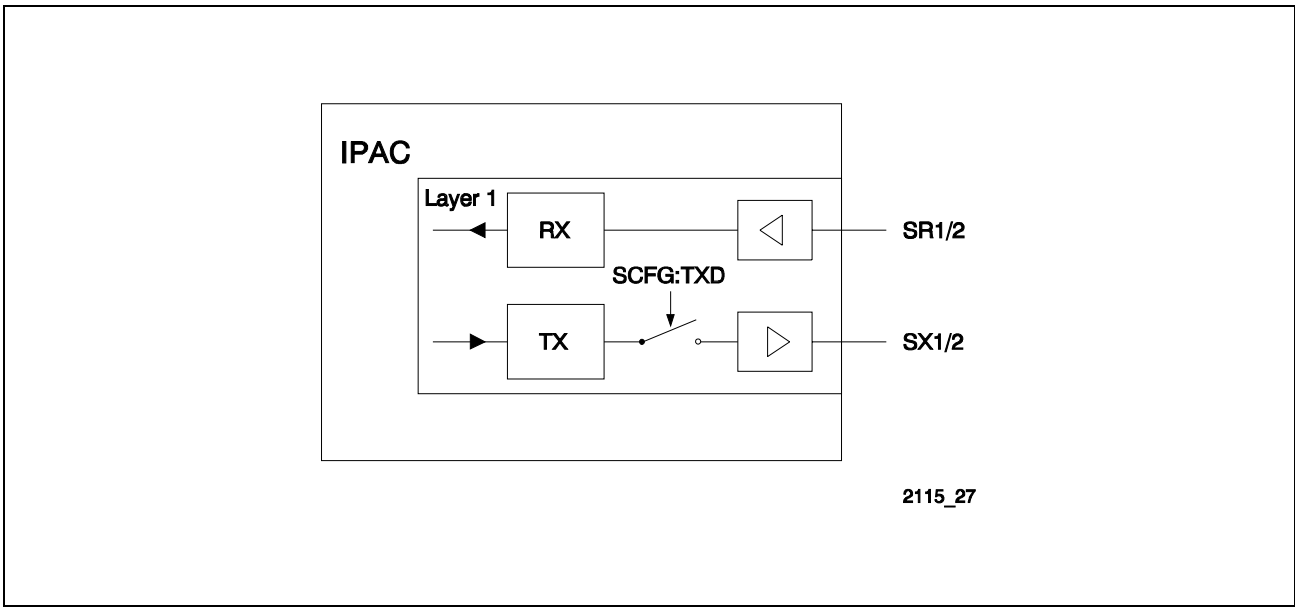


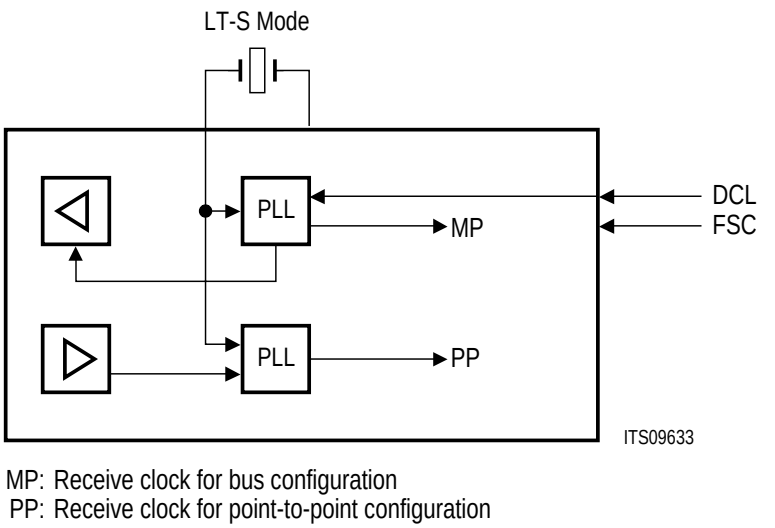
Figure 31 Disabling of S/T Transmitter

2.5.5 Timing Recovery

LT-S

In LT-S mode, the 192-kHz transmit bit clock is synchronized to the IOM clock. In the receive direction two cases have to be distinguished depending on whether a bus or a point-to-point operation is programmed in MON-8 Configuration Register (**see figure 32**):

– In a bus configuration (C/W/P=0), the 192-kHz receive bit clock is identical to the transmit bit clock, shifted by 4.6 µs with respect to the transmit edge. According to CCITT I.430, the receive frame is shifted by two bits with respect to the transmit frame.
– In a point-to-point or extended passive bus configuration (C/W/P=1), the 192-kHz receive bit clock is recovered from the receive data stream on the S interface. According to CCITT I.430, the receive frame can be shifted by 2-8 bits with respect to the transmit frame at the LT-S. However, note that other shifts are also allowed by the IPAC (including 0).



MP: Receive clock for bus configuration
PP: Receive clock for point-to-point configuration

Figure 32 Clock System of the IPAC in LT-S Mode

TE and LT-T

In TE/LT-T applications, the transmit and receive bit clocks are derived, with the help of the DPLL, from the S interface receive data stream. The received signal is sampled several times inside the derived receive clock period, and a majority logic is used to additionally reduce bit error rate in severe conditions (**see chapter 2.5.3**). The transmit frame is shifted by two bits with respect to the received frame.

In TE mode the output clocks (DCL, FSC etc.) are synchronous to the S interface timing.

In LT-T mode the IPAC provides a 1.536 MHz clock on the SCLK pin synchronous to the S interface. This can be used as the reference clock for an external PLL which provides the FSC and DCL clocks. Since the IPAC provides different dividers, the clocks can also be generated internally from the DCL input connected to SCLK (see **chapter 2.8.2.2**).

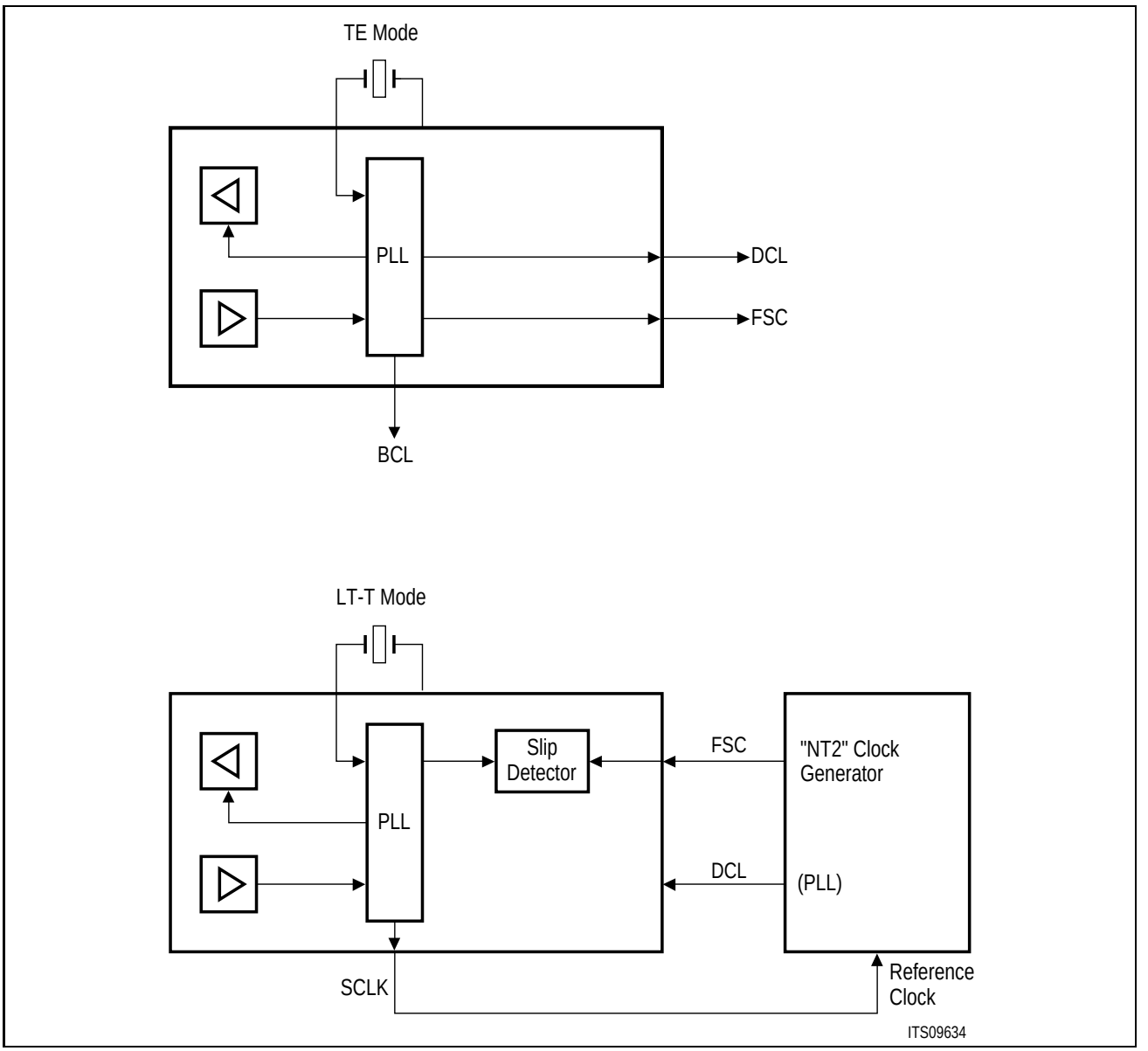


Figure 33 Clock System of the IPAC in TE and LT-T Modes

2.5.6 Activation/Deactivation

An incorporated finite state machine controls ISDN layer-1 activation/deactivation according to CCITT.

Setting of the IPAC for CTS Test Procedures for Frame Alignment

The IPAC needs to be programmed for multiframe operation with the Q-bits set to "1".

MON-8 Configuration Register : MFD = 0
MON-1 Command/Message = 0001 1111B (1Fh)

Frame Alignment Tests

For frame alignment tests the following settings are valid:

- n = 2
- m = 3 or 4

2.5.7 Activation Indication via Pin ACL

The activated state of the S-interface is directly indicated via pin $\overline{\text{ACL}}$ (Activation LED). An LED with pre-resistance may directly be connected to this pin and a low level is driven on $\overline{\text{ACL}}$ as soon as the layer 1 is activated (see **figure 34**).

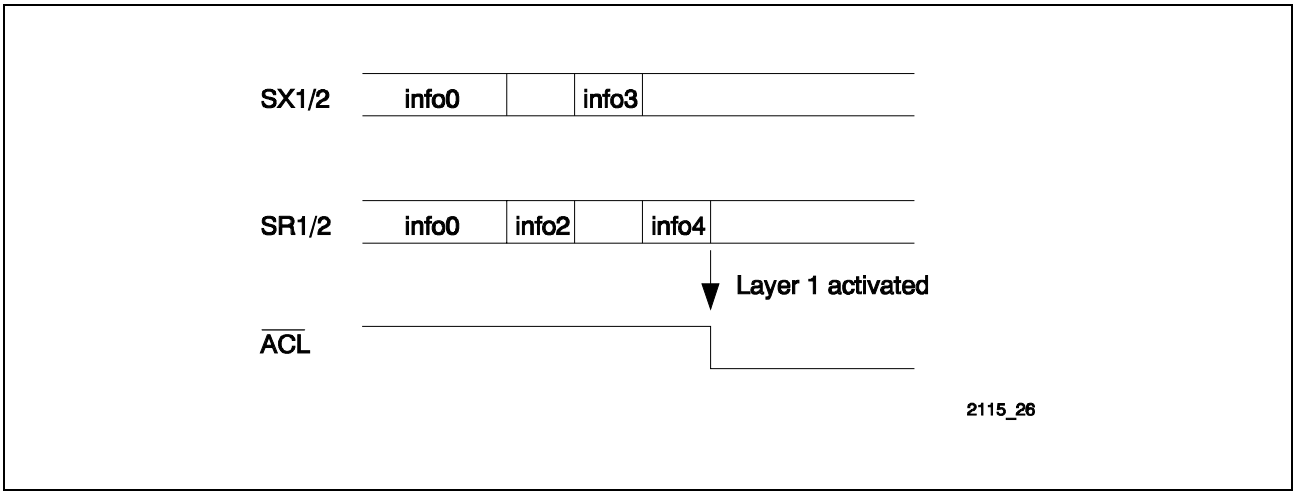


Figure 34 ACL Indication of Activated Layer 1

By default (PCFG:ACL=0) the state of layer 1 is indicated at pin $\overline{\text{ACL}}$. If the automatic indication of the activated layer 1 is not required, the state on pin $\overline{\text{ACL}}$ can also be programmed by the host (see **figure 35**).
If PCFG:ACL=1 the LED on pin $\overline{\text{ACL}}$ can be switched on (PCFG:LED=1) and off (PCFG:LED=0) by the host.

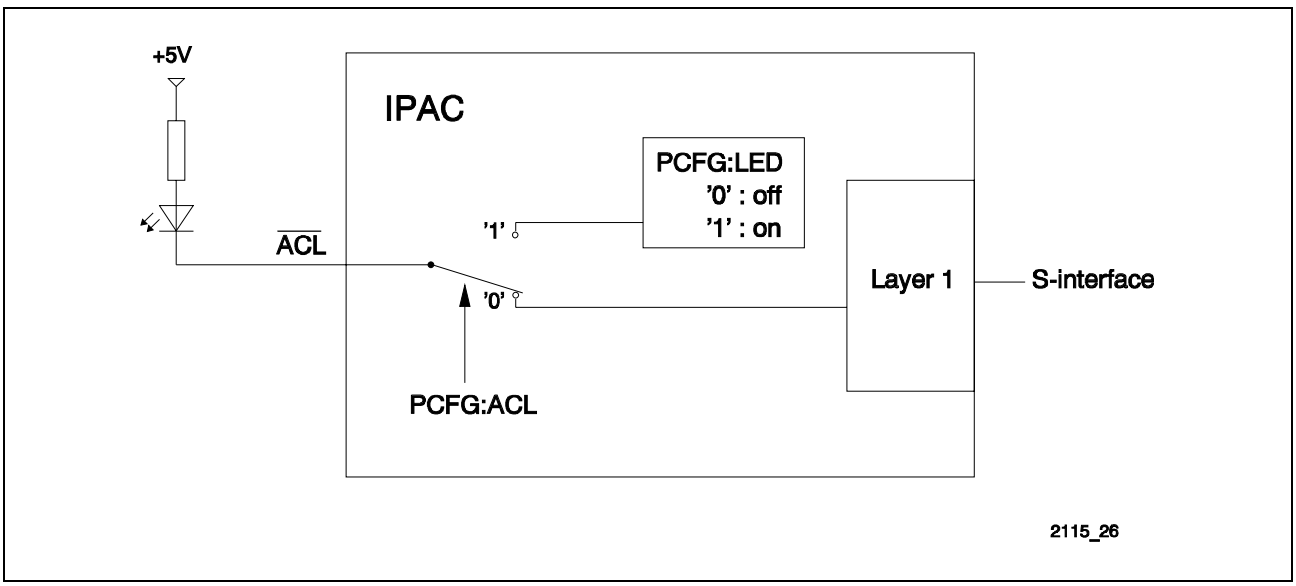


Figure 35 ACL Configuration

2.5.8 Terminal Specific Functions (TE mode only)

In addition to the standard functions supporting the ISDN basic access, the IPAC contains optional functions, useful in various terminal configurations.

The terminal specific functions are enabled by setting bit TSF (STCR register) to “1”. This has two effects:

- In TE mode the MODE1/$\overline{\text{EAW}}$ line is defined as External Awake input, but additionally this function is only enabled by setting STCR:TSF=1
- Second, the interrupts SAW and WOV (EXIRD register) are enabled:
  – SAW (Subscriber Awake) generated by a falling edge on the $\overline{\text{EAW}}$ line
  – WOV (Watchdog Timer Overflow) generated by the watchdog timer. This occurs when the processor fails to write two consecutive bit patterns in ADF1:

ADF1

WTC1	WTC2	

Watchdog Timer Control 1,0.

The WTC1 and WTC2 bits have to be successively written in the following manner within 128 ms:

	WTC1	WTC2
1. 2.	1 0	0 1

As a result the watchdog timer is reset and restarted. Otherwise a WOV is generated.

Deactivating the terminal specific functions is only possible with a hardware reset.

Having enabled the terminal specific functions via TSF = 1, the user can make the IPAC generate a reset signal by programming the Reset Source Select **RSS** bit (CIX0 register), as follows:

0 → A reset signal is generated as a result of

– a falling edge on the $\overline{\text{EAW}}$ line (subscriber awake)
– a C/I code change (exchange awake).
– layer-1 part leaves power down state and supplies DCL and FSC clocks.

A falling edge on the $\overline{\text{EAW}}$ line also forces the DU line of the IOM interface to zero.

Note: In case the layer-1 part of the IPAC is switched off (CONF:TEM=1), a falling edge on $\overline{\text{EAW}}$ should normally induce the attached layer-1 device to leave the power down state and supply clocking to IPAC via DCL and FSC.

A corresponding interrupt status (CIC or SAW) is also generated.

1 → A reset signal is generated as a result of the expiration of the watchdog timer (indicated by the WOV interrupt status).

Note: The watchdog timer is not running when the IPAC is in the power-down state (IOM not clocked).

Note: Bit RSS has a significance only if terminal specific functions are activated (TSF=1).

The RSS bit should be set to “1” by the user when the IPAC is in power-up to prevent an edge on the $\overline{\text{EAW}}$ line or a change in the C/I code from generating a reset pulse.

Switching RSS from 0 to 1 or from 1 to 0 resets the watchdog timer.

The reset pulse generated by the IPAC (output via RES pin) has a pulse width of 5 ms and is an active high signal. It has no internal reset function.

Before and after this reset pulse the RES pin is input.

2.5.9 Test Functions

2.5.9.1 B-Channel Test Mode

To provide for fast and efficient testing, the IPAC can be operated in the test mode by setting the TLP bit in the MODEB register.

The serial data input and output (DU – DD) are connected generating a local loopback between XFIFOB and RFIFOB.

The DD input is ignored and DU remains active.

As a result, the user can perform a simple test of the HDLC channels of the IPAC.

2.5.9.2 D-Channel and S/T Interface Test Mode

The IPAC provides several test and diagnostic functions for D-Channel and S/T interface which can be grouped as follows:

– digital loop via TLP (Test Loop, SPCR register) command bit (**figure 36**): TX-path of layer 2 is internally connected with RX-path of layer 2, output from layer 1 (S/T) on DD is ignored; this is used for testing D-channel functionality excluding layer 1 (loopback between XFIFOD and RFIFOD) and excluding the B-channel controller;

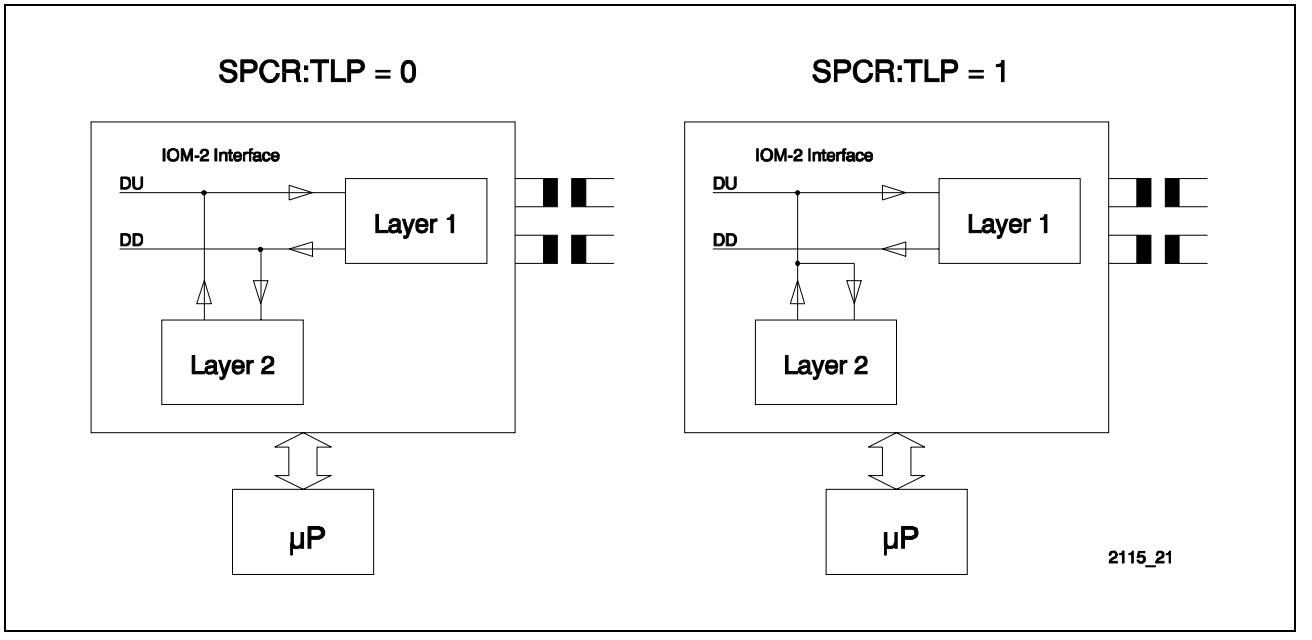


Figure 36 Layer 2 Test Loops

– test of layer-2 functions while disabling all layer-1 functions and pins associated with them (including clocking in TE mode), via bit TEM (Test Mode in CONF register); the IPAC is then fully compatible to the ICC (PEB 2070) seen at the IOM interface.

– loop at the analog end of the S interface;

TE / LT-T mode

Test loop 3 is activated with the C/I channel command Activate Request Loop (ARL). An S interface is not required since INFO3 is looped back internally to the receiver. When the receiver has synchronized itself to this signal, the message "Test Indication" (or "Awake Test Indication") is delivered in the C/I channel. No signal is transmitted over the S interface.
In the test loop mode the S interface awake detector is enabled, i.e. if a level is detected (e.g. Info 2/Info 4) this will be reported by the Awake Test Indication (ATI). The loop function is not effected by this condition and the internally generated 192-kHz line clock does not depend on the signal received at the S interface.

LT-S mode

Test loop 2 is likewise activated over the IOM interface with Activate Request Loop (ARL). No S line is required. INFO4 is looped back internally to the receiver and also sent to the S interface. When the receiver is synchronized, the message "AIU" is sent in the C/I channel. In the test loop mode the S interface awake detector is disabled, and echo bits are set to logical "0".

– special loops are programmed via C2C1-0 and C1C1-0 bits (register SPCR)

– transmission of special test signals on the S/T interface according to the modified AMI code are initiated via a C/I command written in CIX0 register (**cf. chapter 3.6**).

Two kinds of test signals may be sent by the IPAC:

- single pulses and
- continuous pulses.

The single pulses are of alternating polarity, one S interface bit period wide, 0.25 ms apart, with a repetition frequency of 2 kHz. Single pulses can be sent in all applications. The corresponding C/I command in TE, LT-S and LT-T applications is SSZ (Send single zeros).

Continuous pulses are likewise of alternating polarity, one S-interface bit period wide, but they are sent continuously. The repetition frequency is 96 kHz. Continuous pulses may be transmitted in all applications. This test mode is entered in LT-S, LT-T and TE applications with the C/I command SCZ.

2.6 Microprocessor Interface

2.6.1 Operation Modes

The IPAC is programmed via an 8-bit parallel microprocessor interface. Easy and fast microprocessor access is provided by 8-bit address decoding on the chip.

The IPAC provides three types of µP buses (see **table 10**), which are selected via pin ALE:

Table 10 Bus Operation Modes

(1)	ALE tied to V_{DD}	**Motorola** type with control signals **$\overline{CS}$, R/$\overline{W}$, $\overline{DS}$**
(2)	ALE tied to V_{SS}	**Siemens/Intel non-multiplexed** bus type with control signals **$\overline{CS}$, $\overline{WR}$, $\overline{RD}$**
(3)	Edge on ALE	**Siemens/Intel multiplexed** address/data bus type with control signals **$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE**

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

Note: If the multiplexed address/data bus type (3) is selected, the unused address pins A0-A7 must be tied to V_{DD}.

Register Addressing Modes

The common way to read write registers is for non-multiplexed mode to set the register address to the address bus and then access the register location. In multiplexed mode, the address on the address/data bus is latched in, before a read or write access to the register is performed.

The IPAC provides two different ways to access its register contents. In the direct mode the register address to be read or written is directly set on the bus in the way described above. This mode is selected, if the address select mode pin AMODE is set to 0.

As a second option, the IPAC allows for indirect access of the registers (AMODE=1). Only the LSB of the address line is used to select either the ADDRESS register or the DATA register. The host writes the register address to the ADDRESS register (write only register), before it reads/writes data from/to the corresponding register location through the DATA register. **Figure 37** shows both register addressing modes.

In indirect address mode (AMOD=1) all other address lines except A0 are not evaluated by the IPAC. They may be tied to log. ’0’ or ’1’, however they must not be left open.

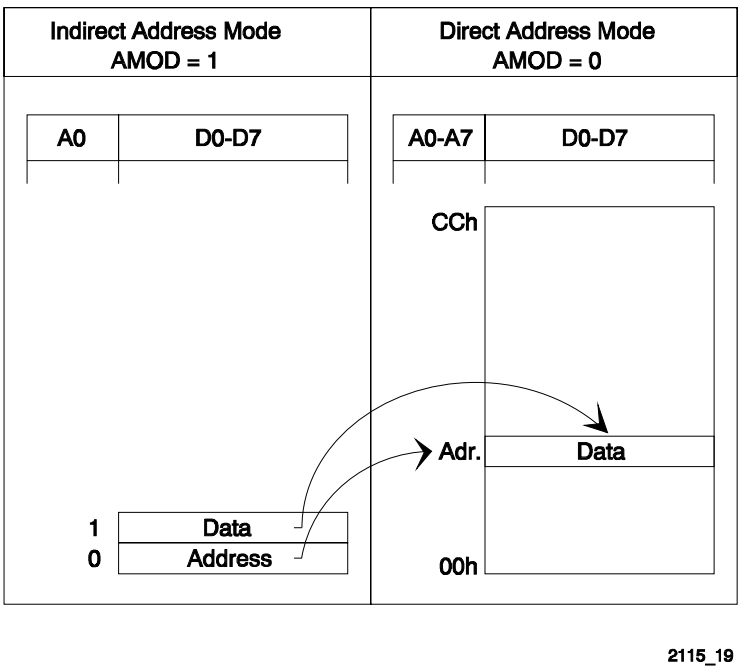


Figure 37 Indirect Register Address Mode

2.6.2 Register Set

The communication between the host and the IPAC is done via a set of directly or indirectly accessible 8-bit registers. The host sets the operating modes, controls function sequences and gets status information by writing or reading these registers (Command/ Status transfer).

Each of the two B-channels of the IPAC is controlled via an equal, but totally independent register file (channel A and channel B). Additional registers are available for D-channel control, the PCM and the Auxiliary interface.

2.6.3 Data Transfer Mode

Data transfer between the system memory and the IPAC for both transmit and receive direction is controlled either by interrupts (Interrupt Mode), or independently from host interaction using the IPAC's 4-channel DMA interface (DMA Mode). DMA transfer is available for transfer of B-channel data only and not for D-channel data.

After RESET, the IPAC operates in Interrupt Mode, where data transfer must be done by the host. The user selects the DMA Mode by setting the DMA bit in a register. In TE mode both channels can independently be operated in either Interrupt or DMA Mode (e.g. Channel A in DMA mode, Channel B in interrupt mode). In LT-S and LT-T mode, only channel B can be operated either in Interrupt or DMA mode, channel A can only be operated in Interrupt mode.

2.6.4 Interrupt Interface

Special events in the IPAC are indicated by means of a single interrupt output, which requests the host to read status information from the IPAC or transfer data from/to the IPAC.

Two interrupt lines with invers polarity are available to meet the requirements of different kinds of applications. A low active interrupt output $\overline{\text{INT}}$ (pin 2) can be connected to a pull up resistor together with further interrupt sources on the system. This pin is available in all modes.
The inverted interrupt signal is available in TE mode only if pin AUX2 (pin 33) is programmed as output (see **chapter 2.8.1**). This may be used in single chip solutions (e.g. PC cards) with only one interrupt source that can directly be connected to the ISA bus. This high active interrupt line INT is not available in LT-modes and in TE-mode with AUX2 used as input (default after reset).

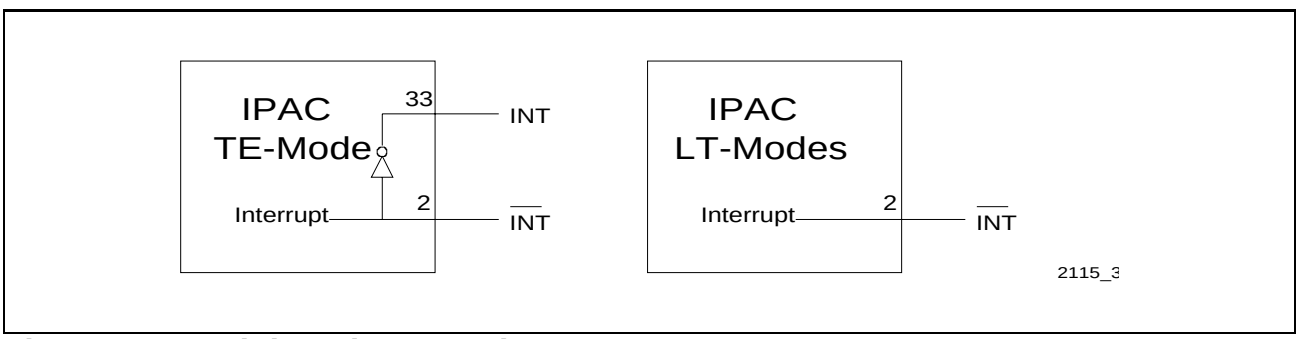


Figure 38 High and Low Active Interrupt Output

Since only one interrupt request output is provided, the cause of an interrupt must be determined by the host reading the IPAC's interrupt status registers.

The structure of the interrupt status registers is shown in **figure 39**.

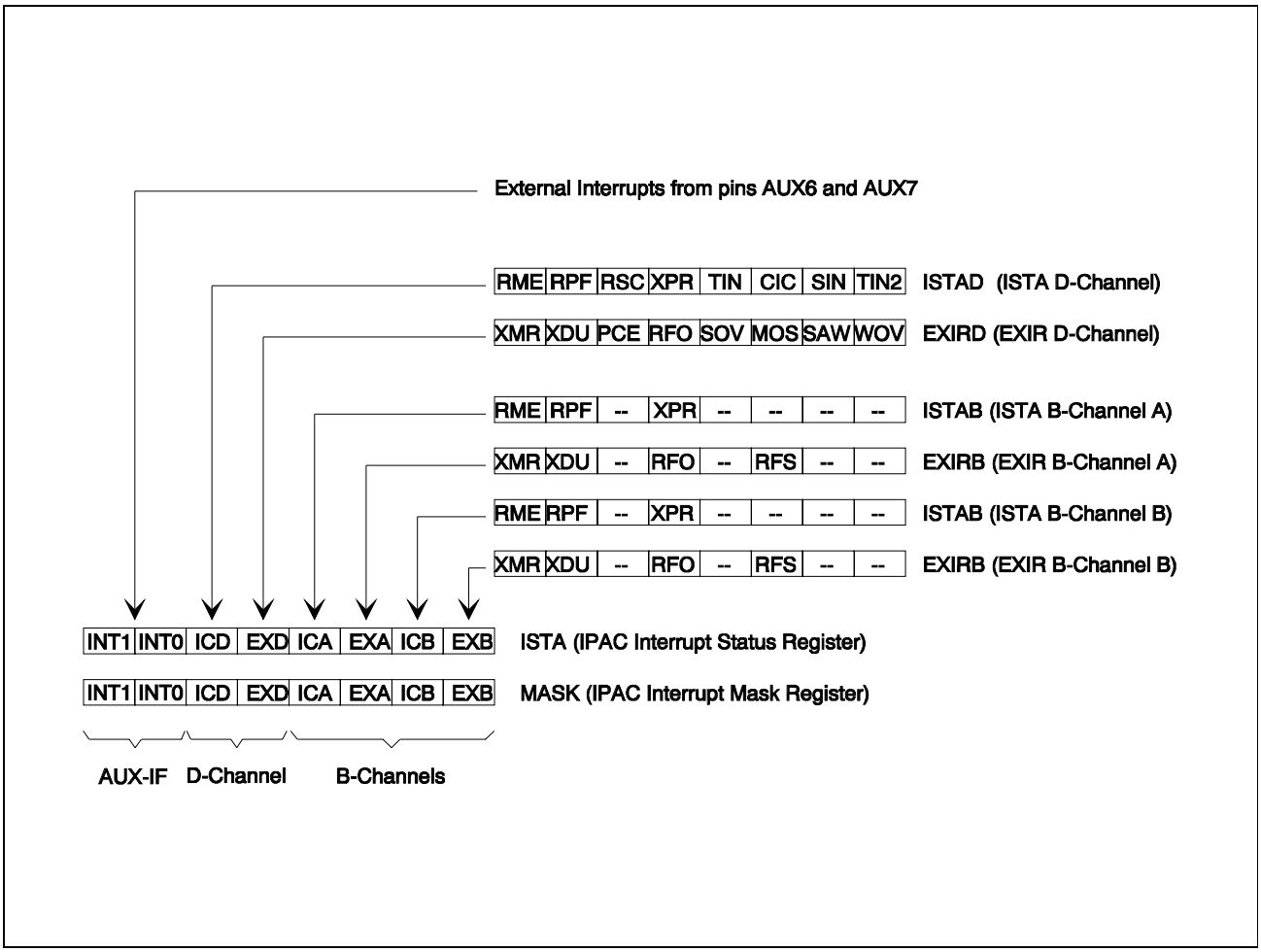


Figure 39 IPAC Interrupt Status Registers

Two interrupt indications can be read directly from the ISTA register and another six interrupt indications from separate interrupt status registers and extended interrupt registers for the B-channels (ISTAB, EXIRB, each for B-Channel A and B) and the D-channel (ISTAD, EXIRD).

Each interrupt source can individually be disabled by setting the corresponding mask bit in the interrupt mask register.

An overview of the interrupt sources is given below, a detailed description of the interrupt structure is provided in **chapter 3.3**.

Table 11 Auxiliary Interface Interrupts

Bit	Register	Interrupt
INT0/1	ISTA	External Interrupt 0/1

Table 12 D-Channel Interrupts

Bit	Register	Interrupt
ICD	ISTA	ISTA D-Channel
EXD	ISTA	EXIR D-Channel

Receive Interrupts:

Bit	Register	Interrupt
RPF	ISTAD	Receive Pool Full
RME	ISTAD	Receive Message End
RFO	EXIRD	Receive Frame Overflow

Transmit Interrupts:

Bit	Register	Interrupt
XPR	ISTAD	Transmit Pool Ready
XMR	EXIRD	Transmit Message Repeat
XDU	EXIRD	Transmit Data Underrun
RSC	ISTAD	Receive Status Change

Special Condition Interrupts:

Bit	Register	Interrupt
TIN	ISTAD	Timer Interrupt
CIC	ISTAD	C/I-Channel Change
SIN	ISTAD	Synchronous Transfer Interrupt
TIN2	ISTAD	Timer 2 Interrupt
SOV	EXIRD	Synchronous Transfer Overflow

Table 12 D-Channel Interrupts

MOS	EXIRD	MONITOR Status
SAW	EXIRD	Subscriber Awake
WOV	EXIRD	Watchdog Timer Overflow

Table 13 B-Channel Interrupts

Bit	Register	Interrupt
ICA/ ICB	ISTA	ISTA B-Channel A/B
EXA/ EXB	ISTA	EXIR B-Channel A/B

Receive Interrupts:

Bit	Register	Interrupt
RPF	ISTAB	Receive Pool Full
RME	ISTAB	Receive Message End
RFO	EXIRB	Receive Frame Overflow
RFS	EXIRB	Receive Frame Start

Transmit Interrupts:

Bit	Register	Interrupt
XPR	ISTAB	Transmit Pool Ready
XMR	EXIRB	Transmit Message Repeat
XDU	EXIRB	Transmit Data Underrun

2.6.5 DMA Interface

To support efficient data exchange between system memory and the FIFOs an additional DMA-interface is provided. The FIFOs have separate DMA-request lines for each direction (DRQRA/B for Receive FIFO, DRQTA/B for Transmit FIFO) and a common DMA-acknowledge input for receive and transmit direction ($\overline{\text{DACKA}}/\overline{\text{B}}$). The DMA-controller has to operate in the level triggered, demand transfer mode. If the DMA-controller provides a DMA-acknowledge signal, each bus cycle implicitly selects the top of FIFO and neither address nor chip select is evaluated. If no $\overline{\text{DACKA}}/\overline{\text{B}}$ signal is supplied, normal read/write operations (providing addresses) must be performed (memory to memory transfer).

In the paragraphs below the following abbreviations are used:

DRQR = DRQRA or DRQRB
DRQT = DRQTA or DRQTB
$\overline{\text{DACK}}$ = $\overline{\text{DACKA}}$ or $\overline{\text{DACKB}}$

The IPAC activates the DRQT and DRQR-lines as long as data transfers are needed from/to the specific FIFOs.

A special timing scheme is implemented to guarantee safe DMA-transfers regardless of DMA-controller speed.

If in transmit direction a DMA-transfer of n bytes is necessary (n < 64 or the remainder of a long message), the DRQT-pin is active up to the rising edge of $\overline{\text{WR}}$ of DMA-transfer (n-1). If $n \geq 64$ the same behavior applies additionally to transfers 63, 127, …, $((k \times 64) - 1)$. DRQT is activated again with the next rising edge of $\overline{\text{DACK}}$, if there are further bytes to transfer (**figure 41**). When a fast DMA-controller is used (> 16 MHz), byte n (or bytes $k \times 64$) will be transferred before DRQT is deactivated from the IPAC. In this case pin DRQT is not activated any more up to the next block transfer (**figure 40**).

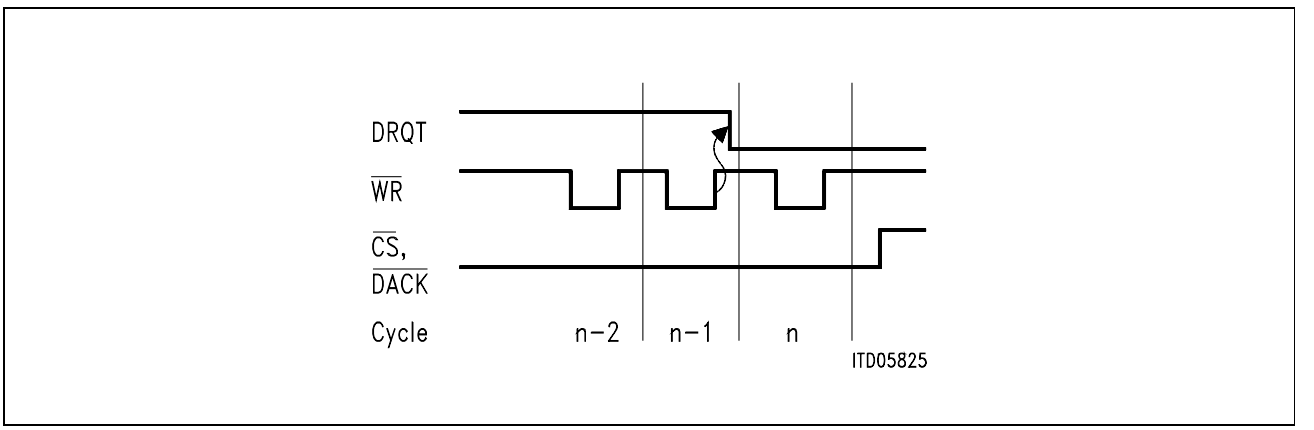


Figure 40 Timing Diagram for DMA-Transfers (fast) Transmit (n < 64, remainder of a long message or n = k × 64)

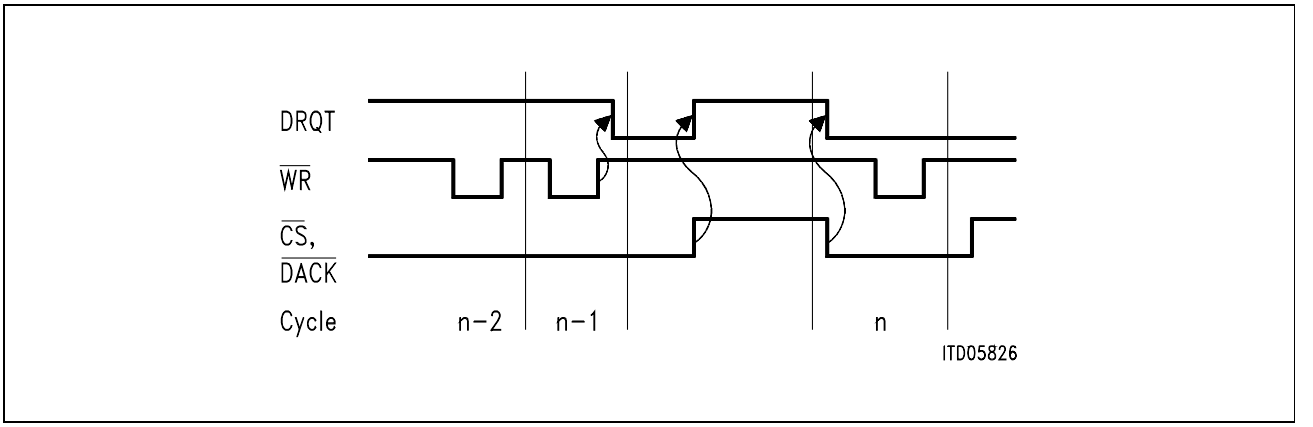


Figure 41 Timing Diagram for DMA-Transfers (slow) Transmit (n < 64, remainder of a long message or n = k × 64)

In receive direction the behavior of pin DRQR is implemented correspondingly. If k × 64 bytes are transferred, pin DRQR is deactivated with the rising edge of $\overline{RD}$ of DMA-transfer ((k × 64) – 1) and it is activated again with the next rising edge of $\overline{DACK}$, if there are further bytes to transfer (**figure 43**). When a fast DMA-controller is used (> 16 MHz), byte n (or bytes k × 64) will be transferred immediately (**figure 42**).

However, if 4, 8, 16, 32 or 64 bytes have to be transferred (only these discrete values are possible in receive direction), DRQR is deactivated with the falling edge of $\overline{RD}$ (**figure 44**).

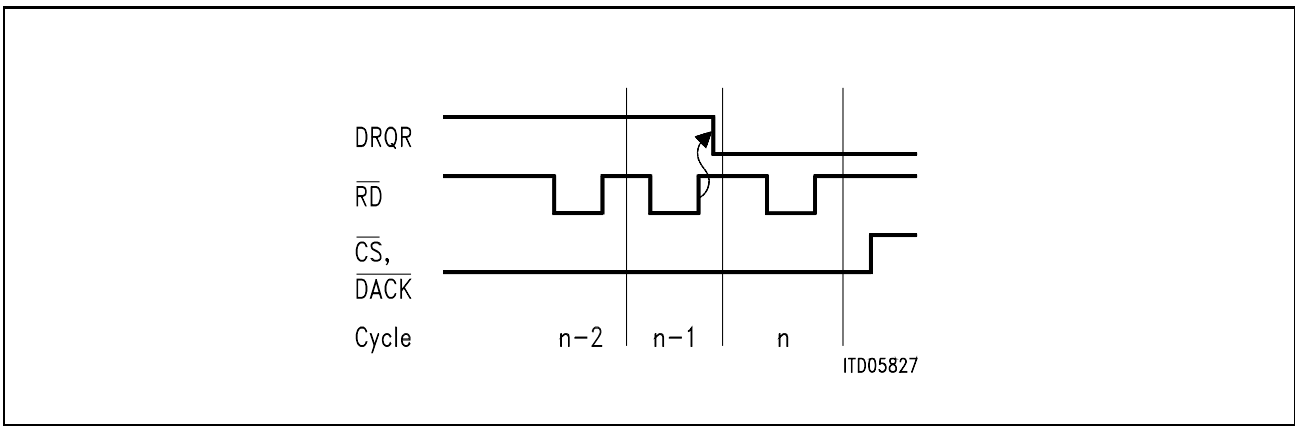


Figure 42 Timing Diagram for DMA-Transfer (fast) Receive (n = k × 64)

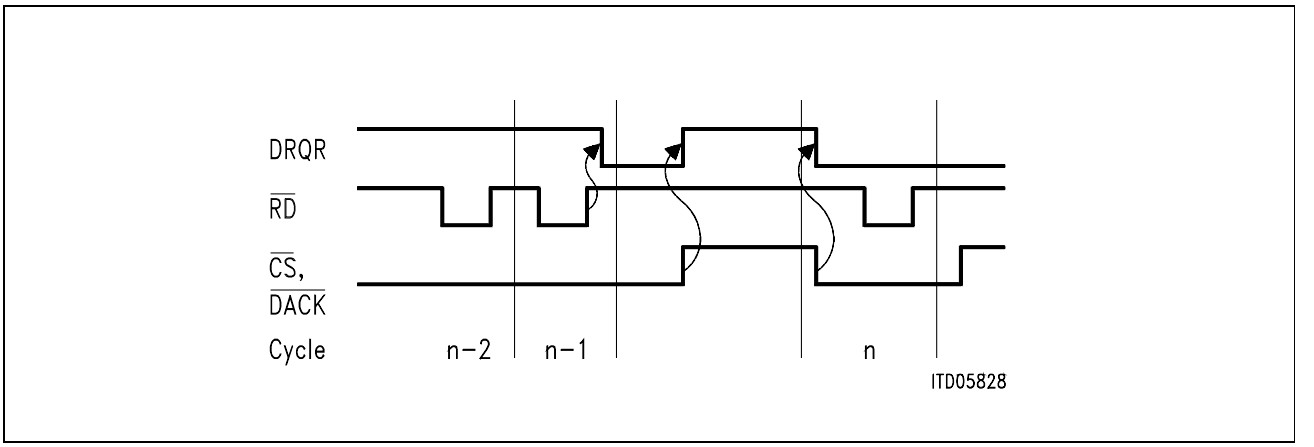


Figure 43 Timing Diagram for DMA-Transfers (slow) Receive (n = k × 64)

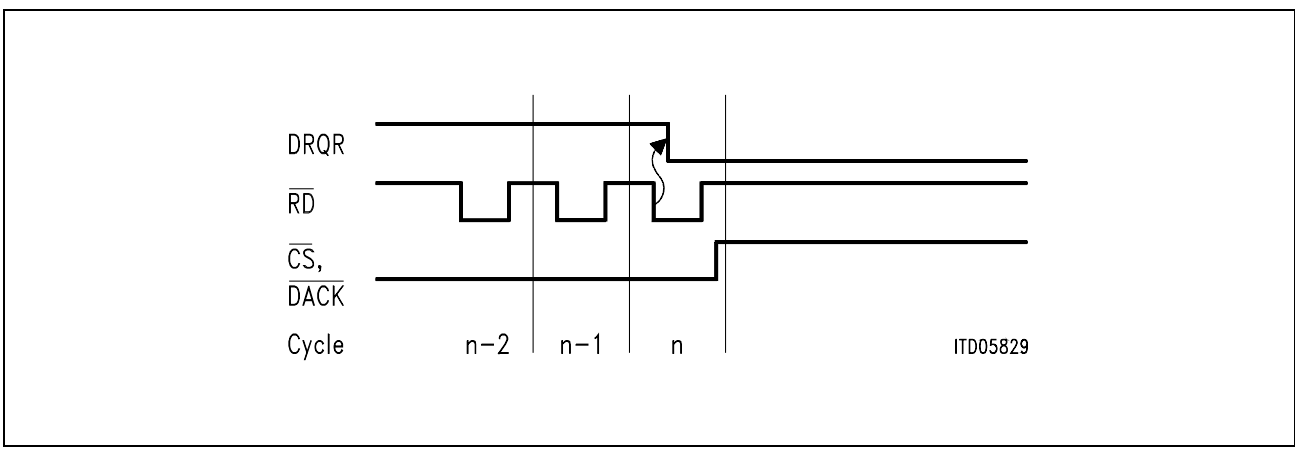


Figure 44 Timing Diagram for DMA-Transfers (slow or fast) Receive (n = 4, 8, 16 or 32)

Generally it is the responsibility of the DMA-controller to perform the correct bus cycles as long as a request line is active.

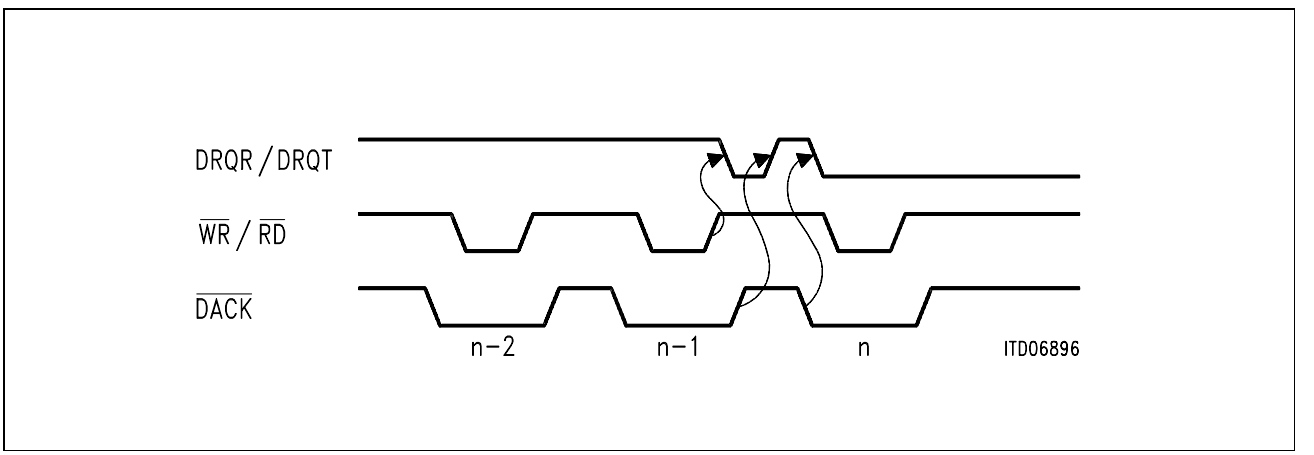


Figure 45 DMA-Transfers with Pulsed DACK (read or write)

If a pulsed $\overline{\text{DACK}}$-signal is used the DRQR/DRQT-signal will be deactivated with the rising edge of RD/WR-operation (n-1) but activated again with the following rising edge of DACK. With the next falling edge of $\overline{\text{DACK}}$ ($\overline{\text{DACK}}$ ‘n’) it will be deactivated again (see **figure 45**).

This behaviour might cause a short negative pulse on the DRQR/DRQT-line depending on the timing of $\overline{\text{DACK}}$ vs. $\overline{\text{RD}}$/$\overline{\text{WR}}$.

2.6.6 FIFO Structure for B-Channels

In both transmit and receive direction 128 byte deep FIFO's are provided for the intermediate storage of B-Channel data between the serial interface and the CPU interface. The FIFO's are divided into two halves of 64 bytes, where only one half is accessible to the CPU at any time.

The organization of the Receive FIFO (RFIFOB) is such, that in the case of a frame at most 128 bytes long, the whole frame may be stored in the RFIFOB. After the first 64 bytes have been received, the IPAC prompts to read the 64 byte block by means of interrupt or DMA request (RPF interrupt or activation of DRQR line). This block remains in the RFIFOB until a confirmation is given to the IPAC acknowledging the transfer of the data block. This confirmation is either a RMC (Receive Message Complete) command via the CMDRB register in Interrupt Mode or is implicitely achieved in DMA mode after 64 byte have been read from the RFIFOB. As a result, it's possible to read out the data block any number of times until the RMC command is issued.

The configuration of the RFIFO prior to and after acknowledgment is shown in **figure 46**.

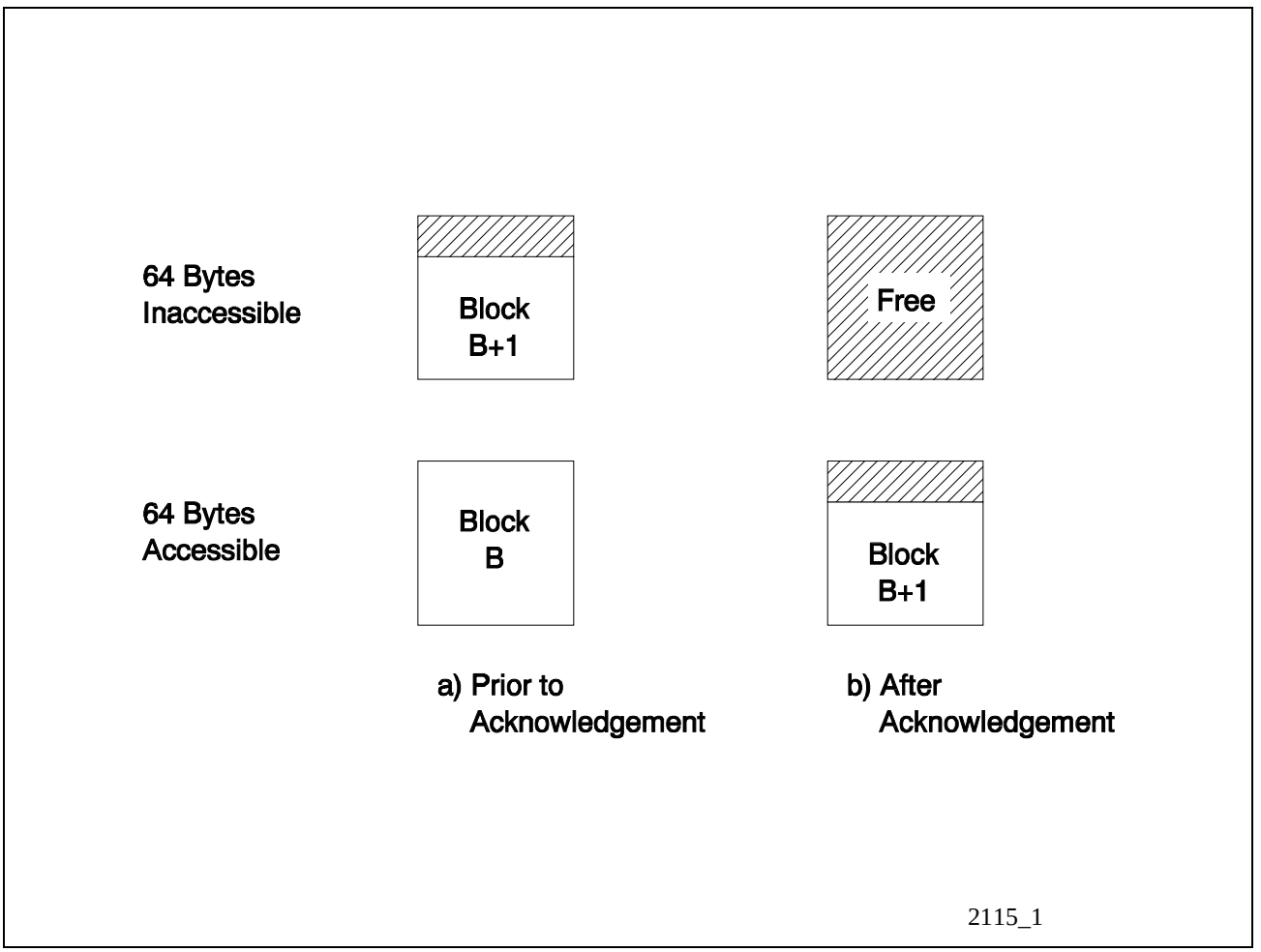


Figure 46 Configuration of RFIFOB (Long Frames)

If frames longer than 128 bytes are received, the device will repeatedly prompt to read out 64 byte data blocks via interrupt.

In the case of several shorter frames, up to 17 may be stored in the IPAC.

If the accessible half of the RFIFOB contains a frame i (or the last part of frame i), up to 16 short frames may be stored in the other half (i + 1, … , i + n) meanwhile, prior to frame i being fetched from the RFIFOB.

This is illustrated in **figure 47**.

For a description of a transmit and receive sequence please refer to **chapter 3.4**.

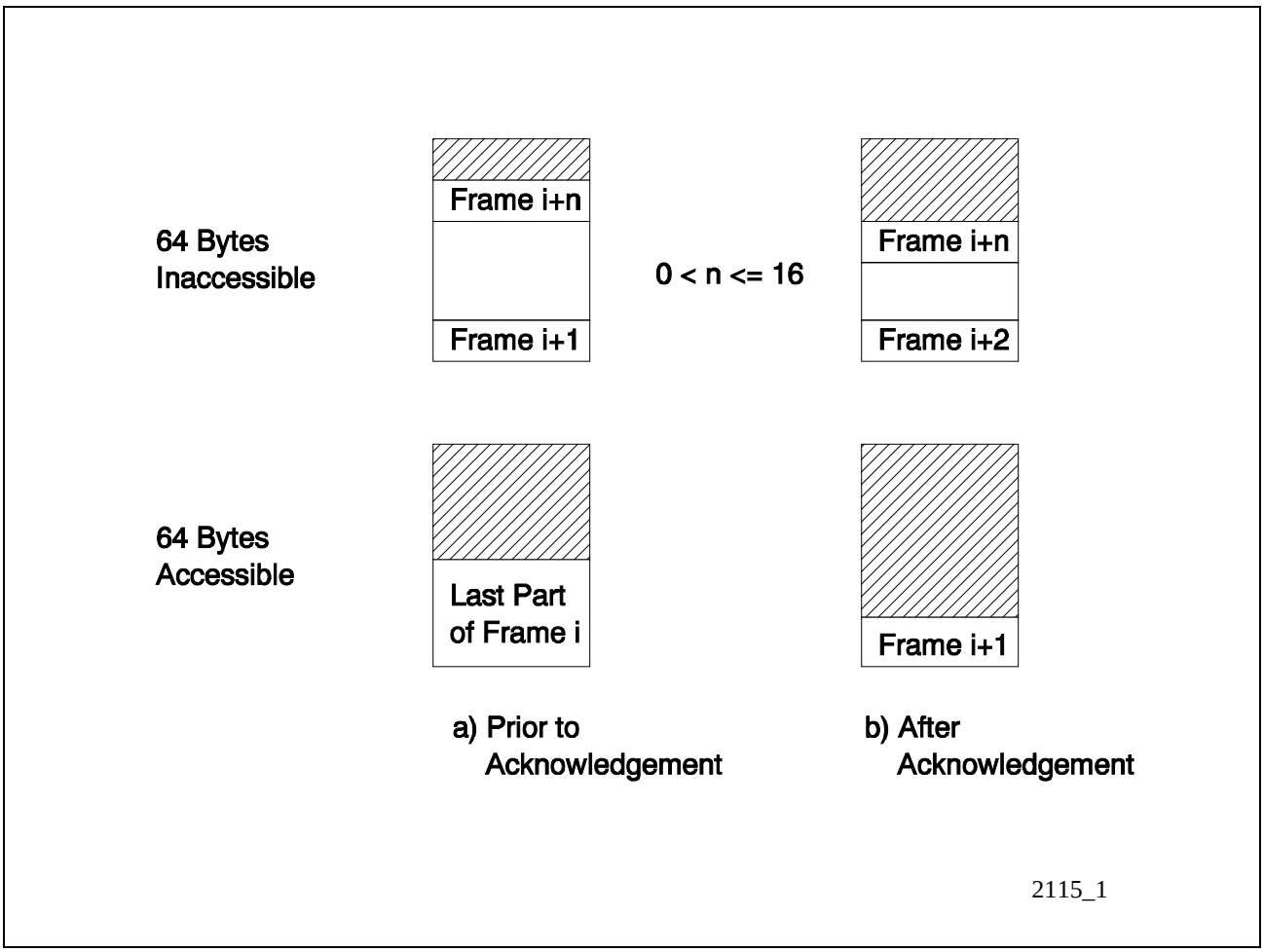


Figure 47 Configuration of RFIFOB (Short Frames)

Note: The number of 17 frames applies e.g. for the IPAC operating in the non-auto mode (address recognition), and short frames only containing the HDLC Address and Control field are received. Since the address is not stored, the control field is always stored first in the RFIFOB, and an additional status byte is always appended at the end of each frame in the RFIFOB, these frames will occupy two bytes.

2.6.7 Timer Modes

The IPAC provides two timers which can be used for various purposes:

TIMR1 - Timer 1 Register (Adr. $A3_H$)
TIMR2 - Timer 2 Register (Adr. CC_H)

Timer 1 provides two modes of operation which can be selected by the 'Timer Mode' bit in MODED register (**figure 48**):

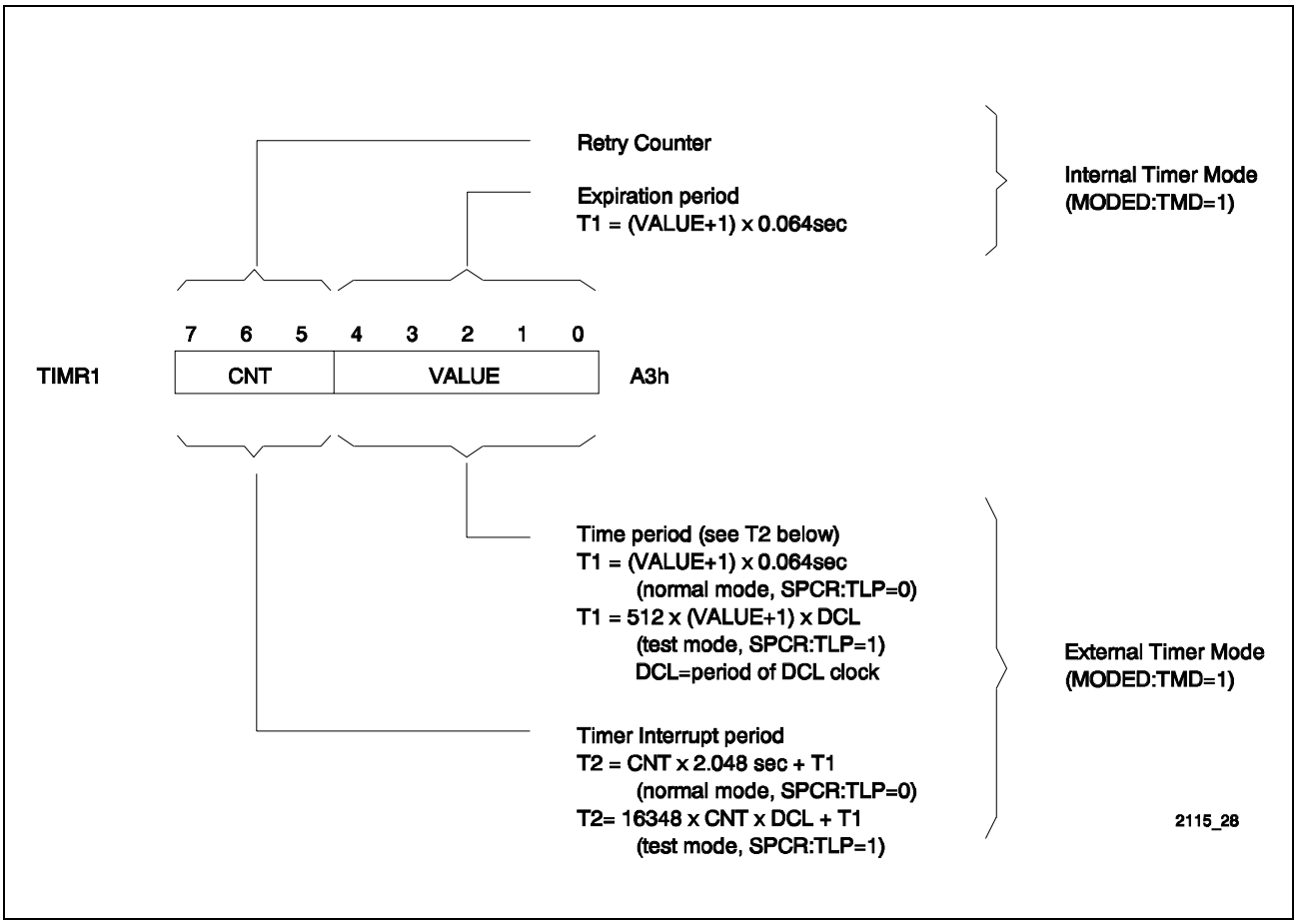


Figure 48 Timer 1 Register

1. Internal Timer Mode (MODED:TMD=1)

In the internal mode the timer is used internally by the IPAC D-channel controller for timeout and retry conditions for handling of LAPD/HDLC protocol, i.e. this mode is only used in automode.
The number of S commands 'N1' which are transmitted autonomously by the IPAC after expiration of time period T1 (see note) is indicated in parameter CNT. The internal prodedure is started after begin of an I-frame transmission or after

an ’RNR’ S-frame has been received. A timer interrupt (ISTAD:TIN) is generated after the last retry. The procedure is stopped when either a TIN interrupt is generated or the TIMR1 register is written or when a positive or negative acknowledgement is received.
CNT can have any value up to 6, with CNT=7 the number of retries is unlimited.

A detailed description for the use of the internal timer mode is provided with the automode description (see **chapter 2.2.1.3**).

*Note: The time period T1 is determined by the parameter VALUE (**chapter 4.3.8**).*

2. External Timer Mode (MODED:TMD=0)

In the external mode the host controls the timer by setting bit CMDRD:STI to start the timer and by writting register TIMR1 to stop the timer.
After time period T2 an interrupt (ISTAD:TIN) is generated continuously (if CNT=7) or once (if CNT<7). Two time periods T2 are defined for normal mode (SPCR:TLP=0) and for test mode (SPCR:TLP=1), i.e when test loop is activated.

Timer 2 can be used as a general purpose timer, similar to the ’External Timer Mode’ of Timer 1. The host can configure a timer interrupt to the host which is indicated in ISTAD:TIN2. If TIMR2:TMD=0 the timer is operating in count down mode, i.e. an interrupt is only generated once after the programmed timer length. A periodic interrupt is generated if TIMR2:TMD=1.

The timer length (for count down timer) or the timer period (for periodic timer), respectively, can be configured to a value between 1 - 63 ms (TIMR2:CNT). If CNT=0 the timer function is disabled (see **figure 49**).

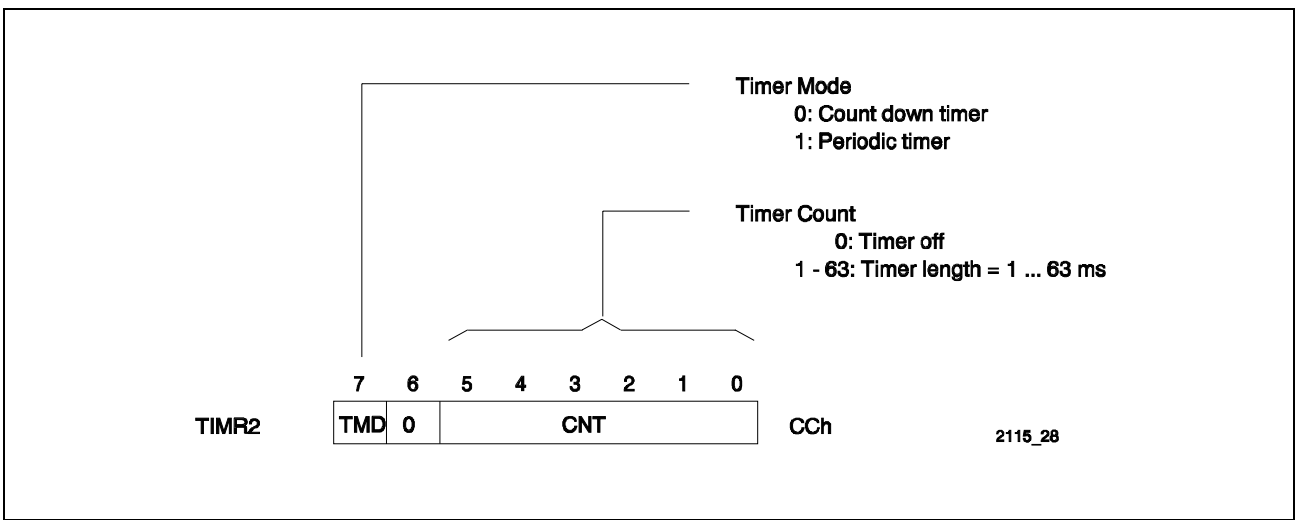


Figure 49 Timer 2 Register

2.6.8 Software Reset

The host can issue a reset command to the IPAC which has the same functionality as a hardware reset. In register C9h bit POTA2:SRES (Software Reset) is used to release the reset which has only effect on the internal functional blocks of the IPAC. The reset pin RES (pin 34) is not activated.

The duration of the reset is controlled by the host, i.e. SRES is set to ’1’ by the host and the reset state is active until SRES is set to ’0’. The host must ensure the required reset timing of the IPAC which is 4 ms.

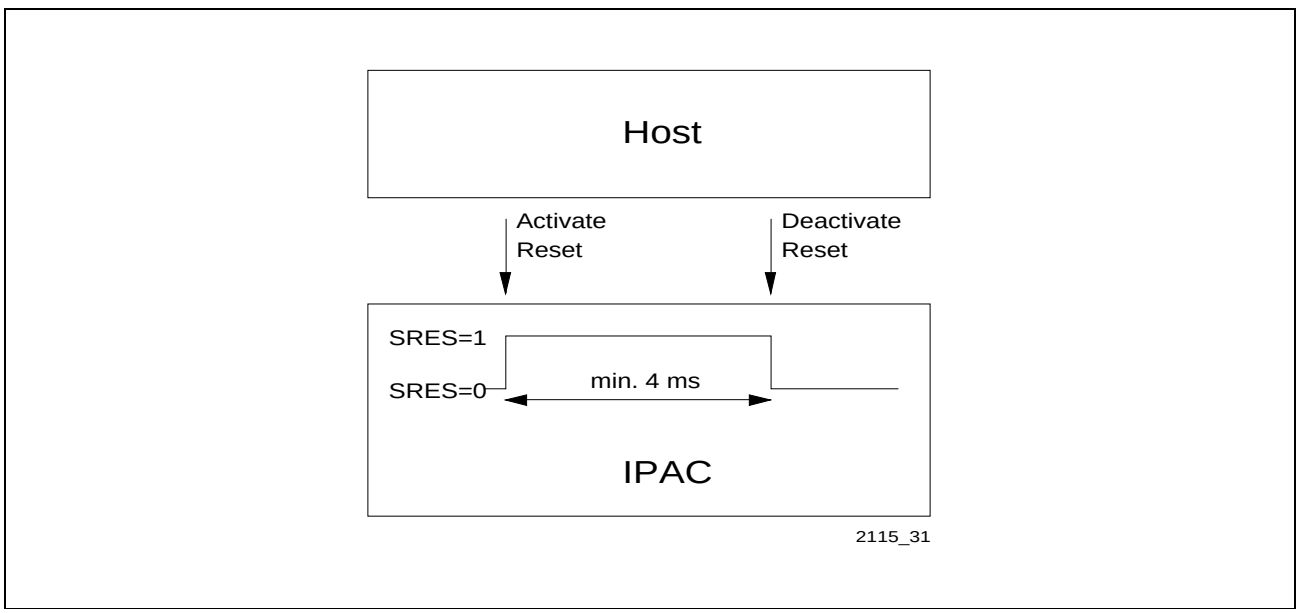


Figure 50 Reset Timing

2.7 IOM®-2 Interface

2.7.1 IOM®-2 Frame Structure / Timing Modes

The IOM-2 is a generalization and enhancement of the IOM-1. While the basic frame structure is very similar, IOM-2 offers further capacity for the transfer of maintenance information. In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules.

The channel structure of the IOM-2 is depicted in **figure 51**.

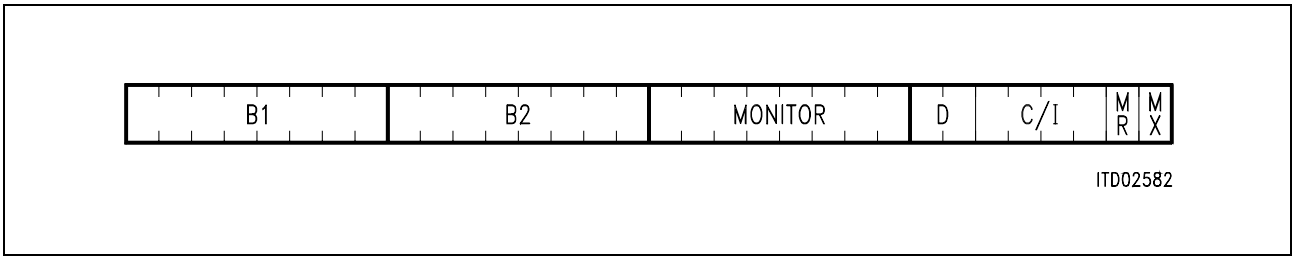


Figure 51 Channel Structure of IOM®-2

- The 64-kbit/s channels, B1 and B2, are conveyed in the first two octets.
- The third octet (monitor channel) is used for transferring maintenance information between the layer-1 functional blocks (e.g. IEC-Q TE) and the layer-2 controller (**see chapter 2.7.4**).
- The fourth octet (control channel) contains

– two bits for the 16-kbit/s D channel
– four command/indication bits for controlling activation/deactivation and for additional control functions
– two bits MR and MX for supporting the handling of the MONITOR channel.

The IOM-2 frame structure depends on whether TE- or non-TE mode is selected, via pins MODE0 and MODE1:

	MODE0	**MODE1/$\overline{\text{EAW}}$**
TE mode	0	$\overline{\text{EAW}}$
LT-T mode	1	1
LT-S mode	1	0

Note: In TE mode pin MODE1 is not required for mode selection but used as $\overline{EAW}$.

Non-TE timing mode

This mode is used in LT-S and LT-T applications. The frame is a multiplex of eight IOM-2 channels (**figure 52**), each channel has the structure as shown in **figure 51**.

The IPAC is assigned to one of the eight channels (0 to 7) via pin strapping (CH0-2), however the host can reprogram the selected timeslot in ADF1:CSEL0-2.

Thus the data rate per subscriber connection (corresponding to one channel) is 256 kbit/s, whereas the bit rate is 2048 kbit/s.

The IOM-2 interface signals are:

DU, DD	2048 kbit/s
DCL	4096 kHz input
FSC	8 kHz input

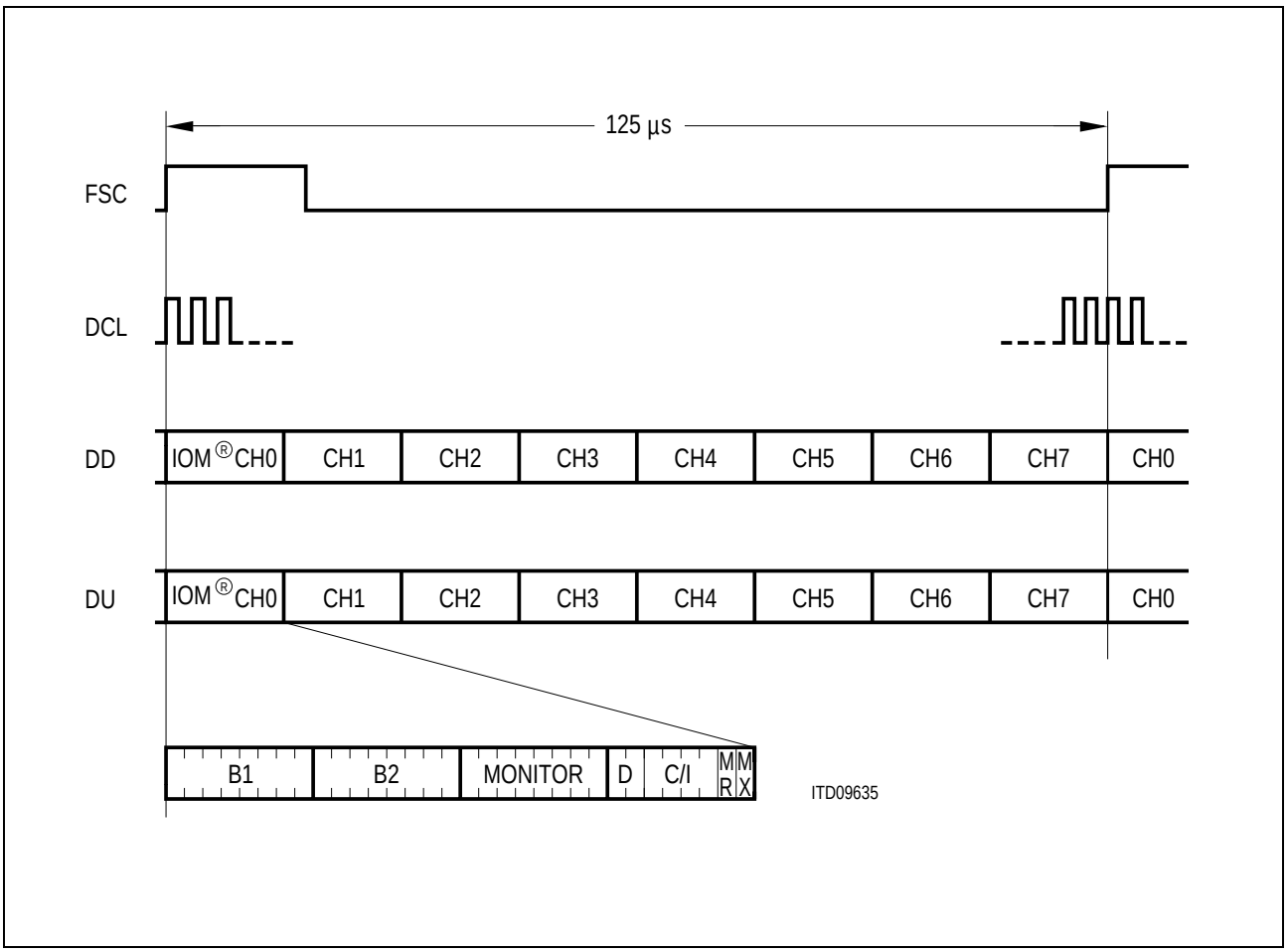


Figure 52 Multiplexed Frame Structure of the IOM®-2 Interface in Non-TE Timing Mode

TE Timing Mode

The frame is composed of three channels (**figure 53**):

- Channel 0 contains 144 kbit/s (for 2B+D) plus MONITOR and Command/Indication channels for the layer-1 device.
- Channel 1 contains two 64-kbit/s intercommunication channels plus MONITOR and Command/Indication channels for other IOM-2 devices.
- Channel 2 is used for IOM bus arbitration (access to the TIC bus). Only the Command/ Indication bits are used in channel 2. **See section 2.7.6** for details.

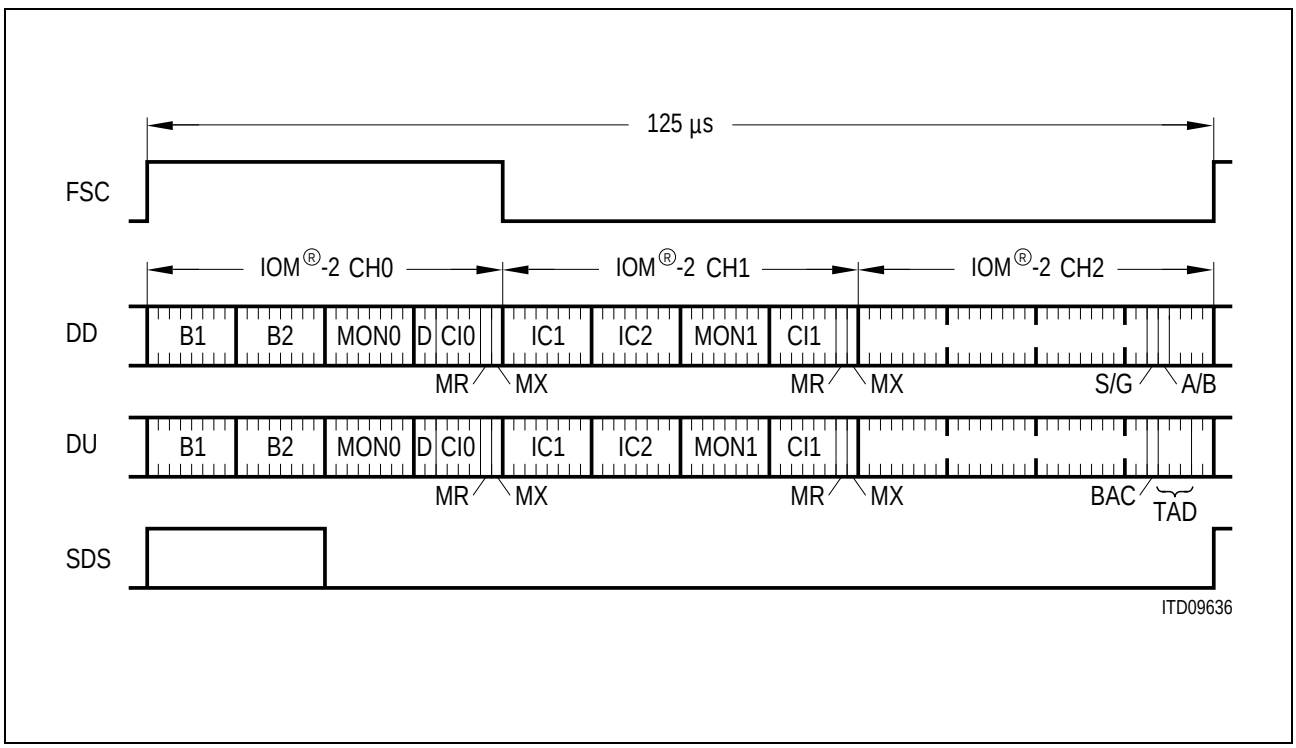


Figure 53 Definition of IOM®-2 Channels in Terminal Timing Mode

The IOM-2 signals are:

DU, DD 768 kbit/s (DU = data upstream = input, DD = data downstream = output)

DCL 1536 kHz output

FSC 8 kHz output

In addition, to support standard combos/data devices the following signals are generated as outputs:

BCL 768 kHz bit clock

SDS 8 kHz programmable data strobe signal for selecting an 8-bit timeslot (e.g. channel B1) or 16-bit timeslot (e.g. B1 and B2).

Strobe Signal

A data strobe signal is generated with every 8-kHz frame. It is active high for a duration of either 8 or 16 bits (SCFG:TLEN) and its start position is programmable to one of up to 32 channels (SCFG:TSLT) with respect to the FSC signal.

Since the IOM-2 and PCM interface are synchronous in their channel structure, the SDS signal may be used for external devices connected to either of these interfaces.

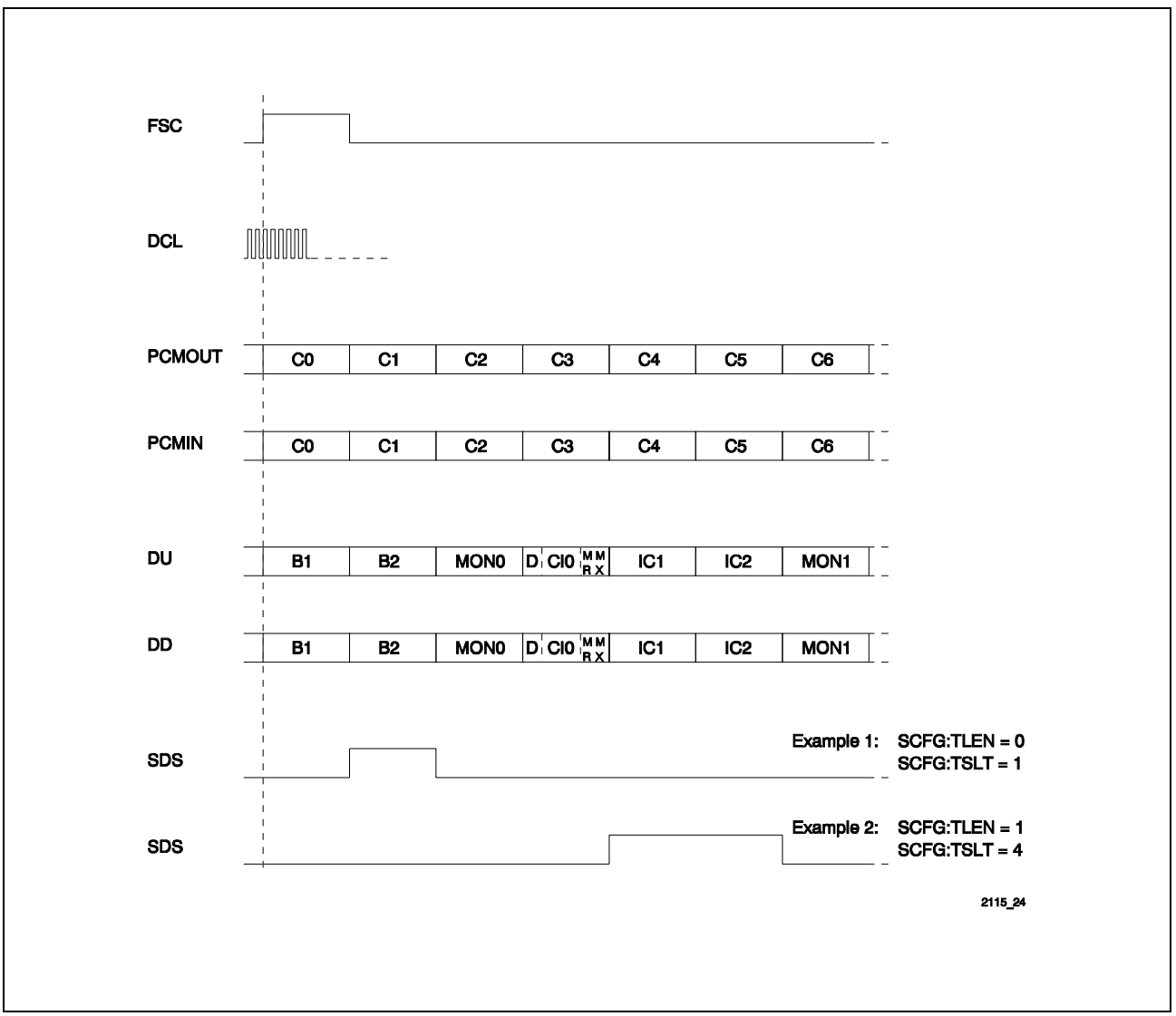


Figure 54 Data Strobe Signal Generation

Figure 54 shows two examples for the generation of a strobe signal. In example 1 the SDS is active during channel B2 on IOM-2 and during channel 1 (C1) on PCM, whereas in the second example SDS goes high during IC1 and IC2 on IOM-2 and during channel 4 and 5 (C4, C5) on PCM.

2.7.2 IOM®-2 Interface Connections

Output Driver Selection

FSC and DCL are push pull outputs (TE mode).

The output type of the IOM datalines is selectable via bit CONF:ODS. ODS set to 0 selects open drain (reset value) and ODS set to 1 selects push pull outputs.

Normally the IOM-2 interface is operated in the "open drain" mode (ODS=0) in order to take advantage of the bus capability. In this case pull-up resistors (1 kΩ – 5 kΩ) are required on DU and DD.
In push pull mode (ODS=1) DU and DD are also high impedant outside the active timeslot the IPAC is programmed to.

IOM-2 OFF Function

The IOM-2 interface can be switched off for external devices via bit IOF in the CONF register. The output lines can be set to tristate if bit CONF:IOF is set to 1, so DU/DD, FSC, DCL and SDS are high impedant, else the selection in ODS determines the output driver characteristic (push pull or open drain).
In Non-TE mode the clocks FSC and DCL are not switched off from the IOM-2 interface for IOF=1 but remain as input, however the datalines DU and DD are tristate.

IOM-2 Direction Control

The direction of the IOM-2 data lines depends on the mode selected by pins MODE0 and MODE1/$\overline{\text{EAW}}$ for the Layer 1 block and by the configuration of CCR2:SOC for the B-channel HDLC controller and SPCR:SDL for the D-channel controller (see **figure 55**).
According to the mode selection (see **chapter 2.7.1**) the layer 1 controller always carries data from the subscriber to the central office on DU and data in the opposite direction on DD.
For test applications, the direction of DU and DD can be reversed separately for the B-channel controller and for the layer 2 block. For normal operation both bits CCR2:SOC and SPCR:SDL should be set to 0 in TE and LT-T mode and should be set to 1 in LT-S mode.

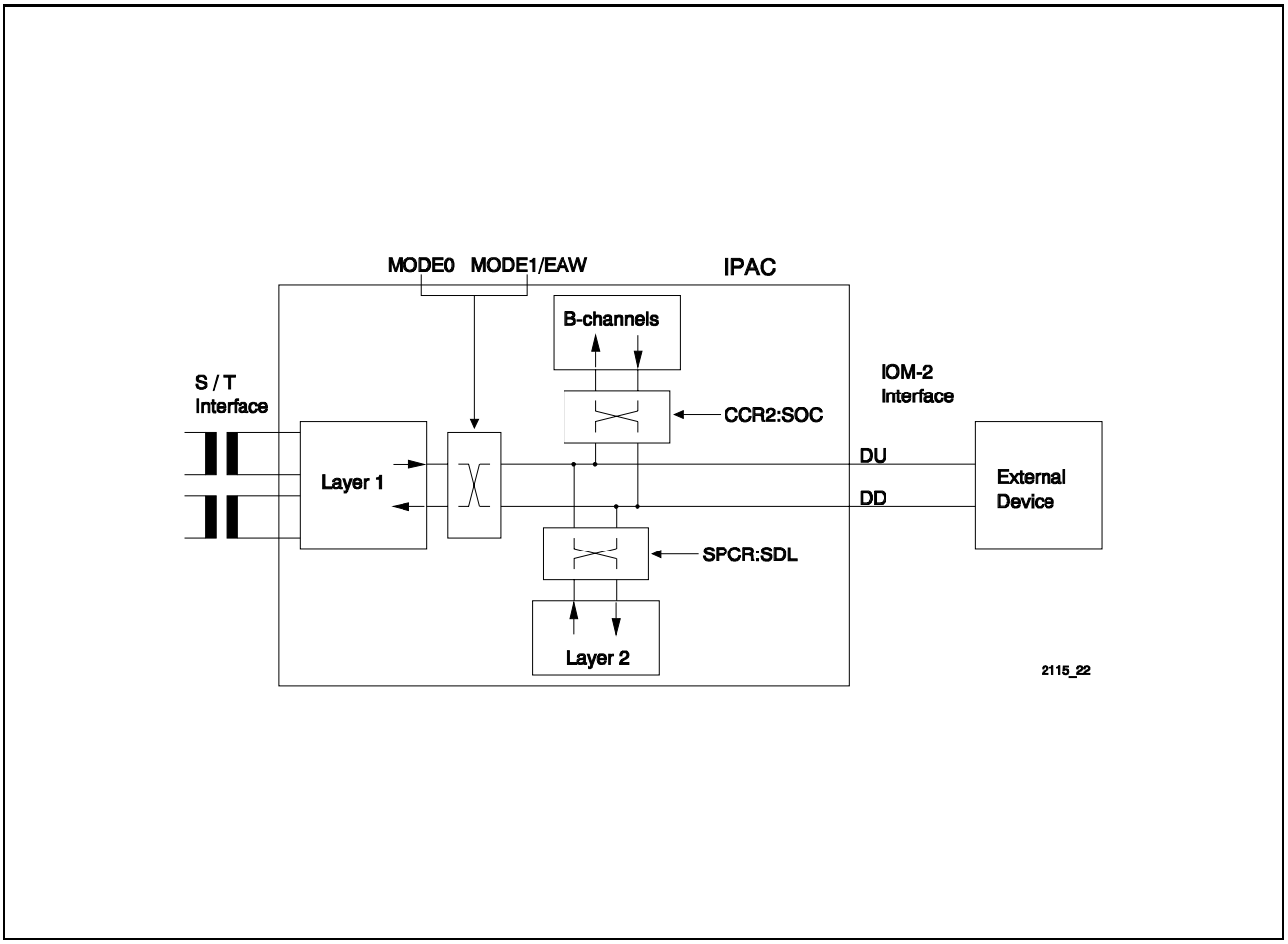


Figure 55 IOM-2 Direction Control

Terminal Mode

In TE mode the IOM-2 interface has the 12-byte frame structure consisting of channels 0, 1 and 2 (**see figure 53**):

– DD carries the 2B+D channels from the S/T interface, and the MONITOR 0 and C/I 0 channels coming from the S/T controller;
– DU carries the 2B+D channels towards the S/T interface, and the MONITOR 0 and C/I 0 channels to the layer-1.

Channel 1 of the IOM-2 interface is used for internal communication in terminal applications. The IPAC is operated as a master device and communicates with slave devices via MONITOR 1 and C/I 1 channels:

– DD carries the MONITOR 1 and C/I 1 channels as output to peripheral devices (e.g. voice/data module);
– DD carries the IC channels as output to other devices, if programmed (C×C1 – 0 = 01 in register SPCR).

Bit 5 of the last byte in channel 2 on DD is used to indicate the S bus state (Stop/Go bit). If required (cf. DIM2-0, MODED register), the S/G bit is evaluated for D-channel access handling and bits 2 to 5 of the last byte on DU (BAC and TAD) are used for TIC bus access arbitration (**see chapter 2.7.6**).

Figure 56 shows the connection in a multifunctional terminal with the IPAC as a master and an external device (e.g. ICC PEB 2070) as a slave device.

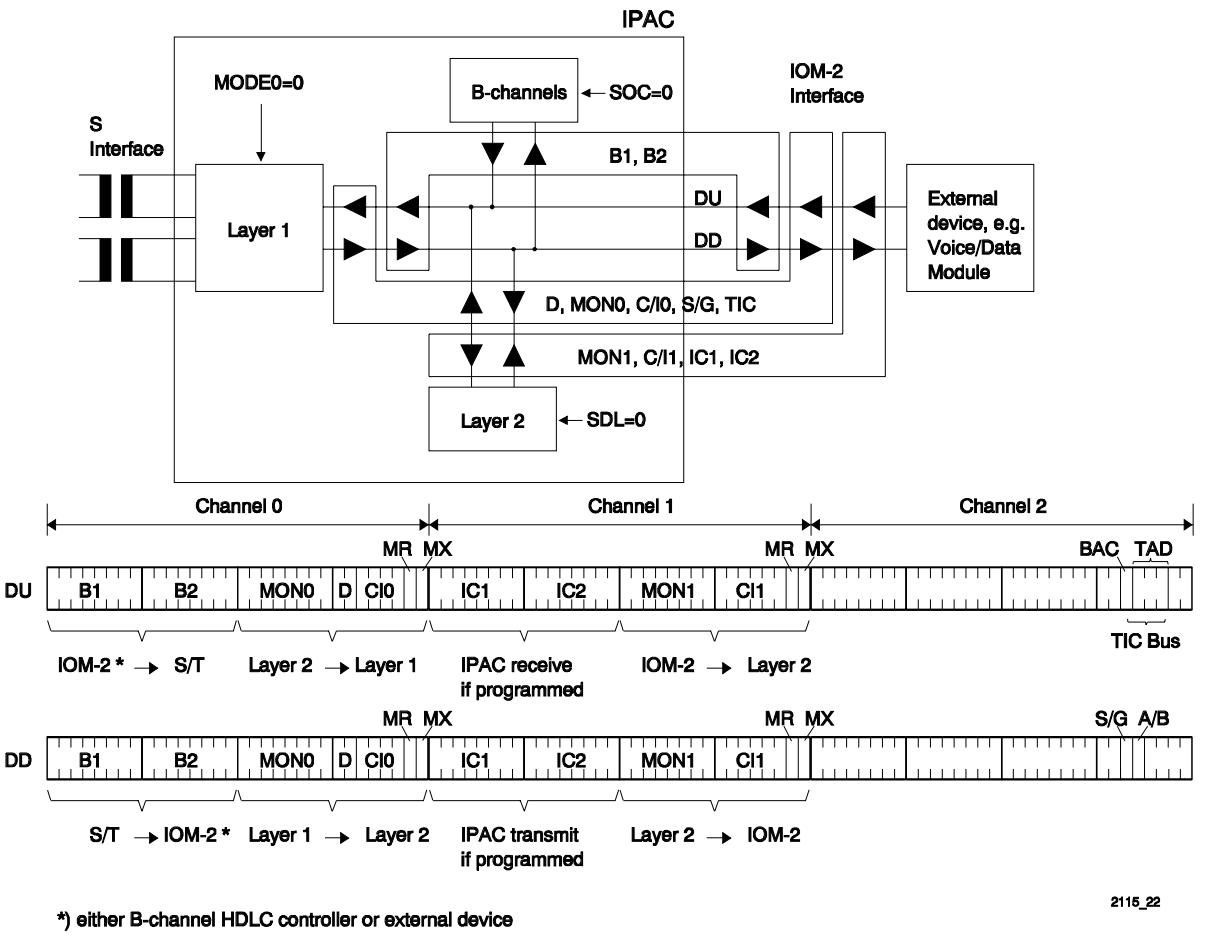


Figure 56 IOM-2 Data Ports DU/DD in Terminal Mode (MODE0=0)

Non-Terminal Mode / LT-T Mode

Outside the selected 4-byte subscriber channel, both DU and DD are inactive.

The reset value for the active channel can be selected by pin strapping (in LT-S and LT-T modes by CH0-2), however after reset the host can reconfigure the active IOM-2 channel for layer 2 in ADF1:CSEL0-2. This reconfiguration is not valid for layer 1 and B-channel HDLC.

The flow of data is similar as in TE mode except that there is only one active 4-byte channel in LT modes compared to three channels in TE mode (see **figure 57**).

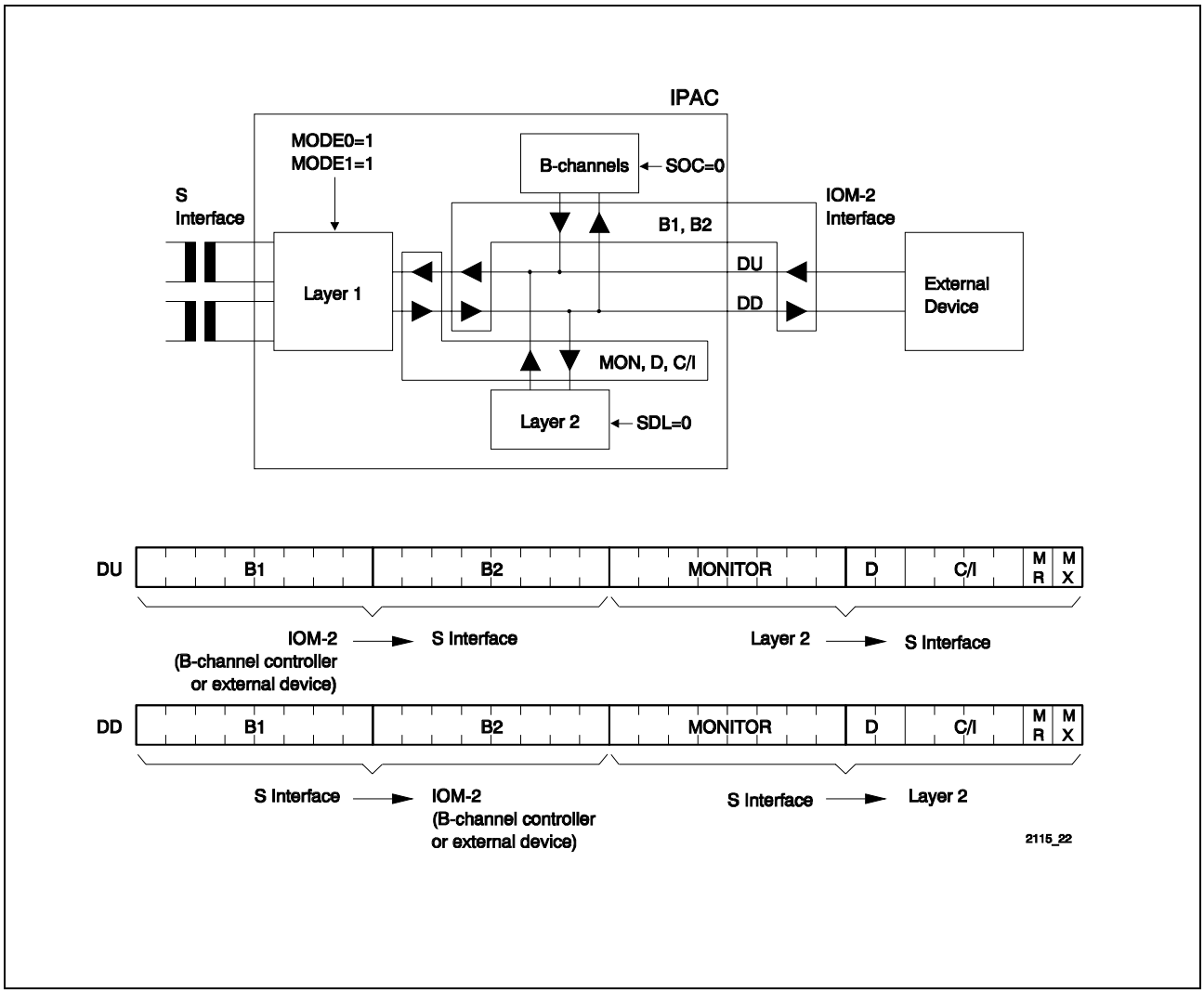


Figure 57 IOM-2 Data Ports DU/DD in LT-T Mode (MODE0=1, MODE1=1)

Non-Terminal Mode / LT-S Mode

Similar as in LT-T mode, both DU and DD are inactive outside the selected 4-byte subscriber channel.

Also the reset value for the active channel can be selected by pin strapping (in LT-S and LT-T modes by CH0-2), however after reset the host can reconfigure the active IOM-2 channel for layer 2 in ADF1:CSEL0-2. This reconfiguration is not valid for layer 1 and B-channel HDLC.

Inside the programmed 4-byte subscriber channel (**see figure 58**):

– DU carries the 2B+D channels coming from S/T interface, and the MONITOR and C/I channels from the layer-1
– DD carries the 2B+D channels towards the S/T interface, and the MONITOR and C/I channels to the layer-1.

By configuration of bit SDL (Switch Data Line, SPCR register) the data lines of the layer 2 controller of the IPAC can be switched. If SDL is set to ’0’, the layer 2 controller sends the MONITOR, D and C/I-channels on DU, normally carried by DD, i.e. normally destined to layer 1 S/T interface. This feature can be used for test purposes, e.g. to send the D-channel towards the system instead of the subscriber (see **figure 59**).

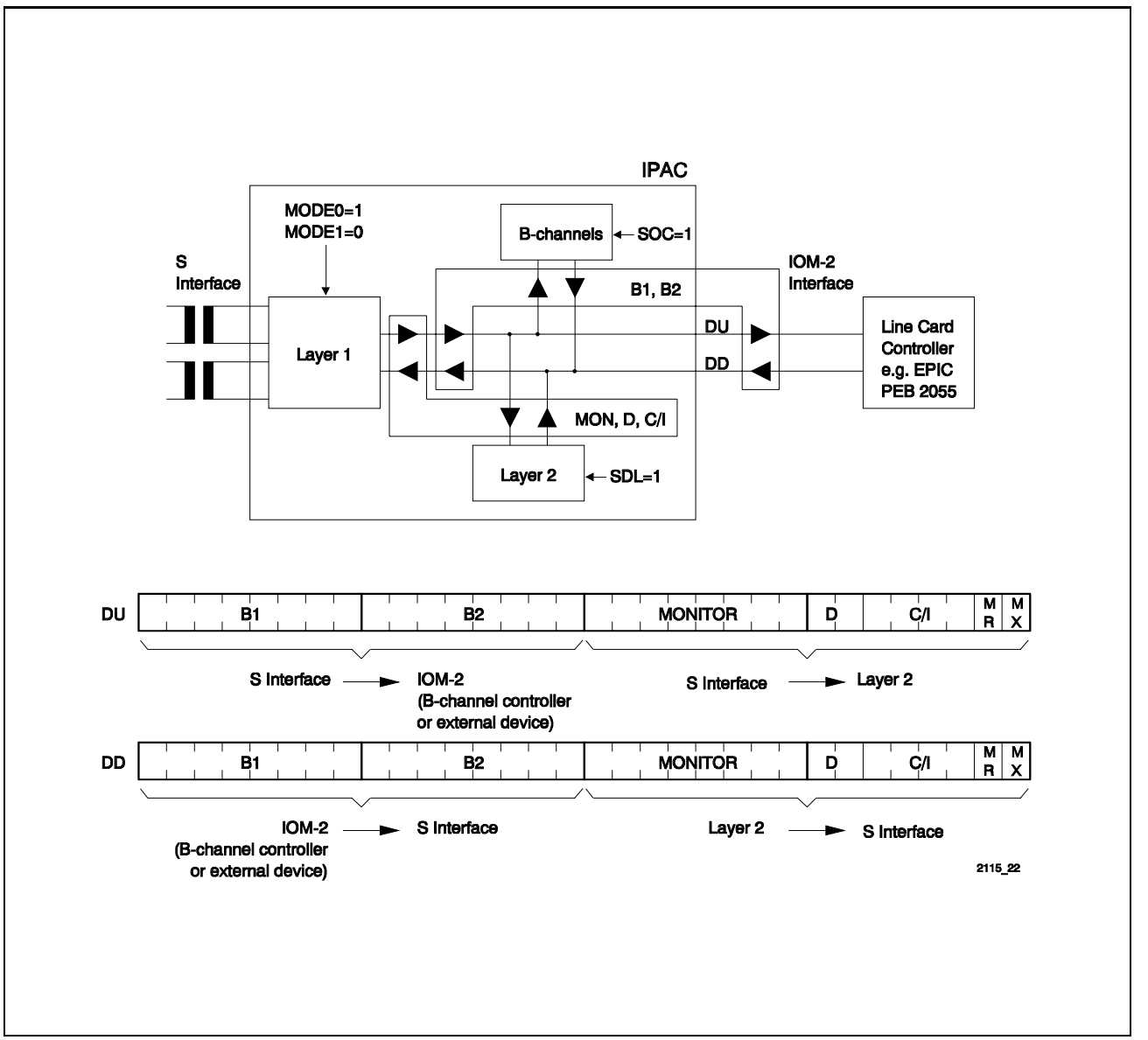


Figure 58 IOM-2 Data Ports DU/DD in LT-S Mode (MODE0=1, MODE1=0) with Normal Layer 2 Direction (SPCR:SDL=1)

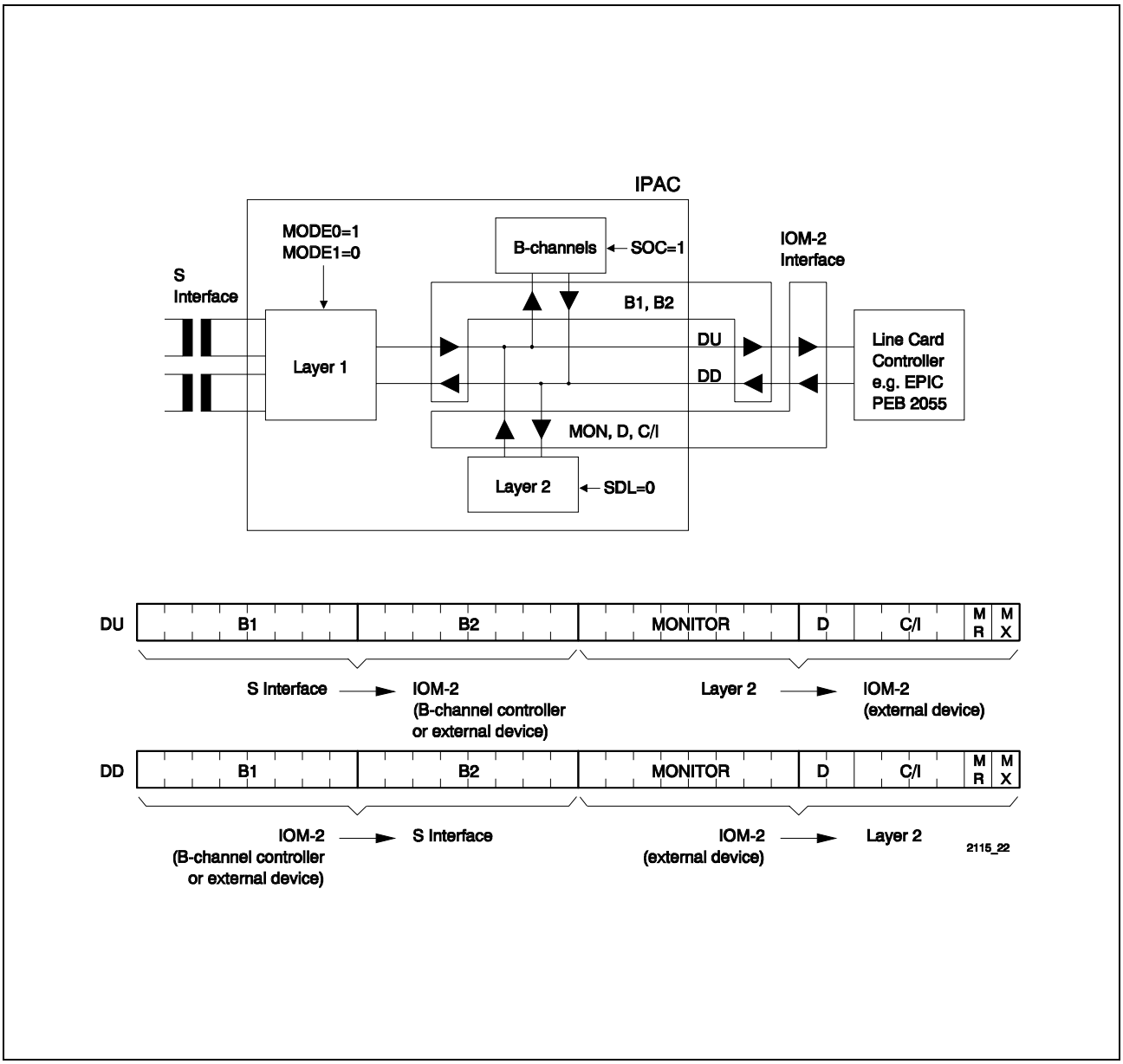


Figure 59 IOM-2 Data Ports DU/DD in LT-S Mode (MODE0=1, MODE1=0) with Inversed Layer 2 Direction (SPCR:SDL=0)

2.7.3 Microprocessor Access to B and IC Channels

In IOM-2 terminal mode (TE mode, MODE0=0) the microprocessor can access the B and IC (intercommunication) channels at the IOM-2 interface by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. Furthermore it is possible to loop back the B-channels from/to the S/T interface or to loop back the IC channels from/to the IOM-2 interface without µP intervention.

These access and switching functions are selected with the Channel Connect bits (CxC1, CxC0) in the SPCR register (**table 14, figure 60**).

External B-channel sources (voice/data modules) connected to the IOM-2 interface can be disconnected with the IOM off function (CONF:IOF) in order to not disturb the B-channel access (**see figure 60**).

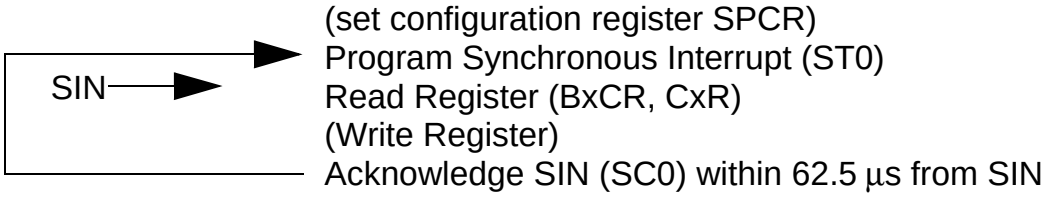
If the B-channel access is used for transferring 64 kbit/s voice/data information directly from the µP port to the ISDN S/T interface, the access can be synchronized to the IOM interface by means of a synchronous transfer interrupt programmed in the STCR register.

Table 14 µP Access to B/IC Channels (IOM®-2)

CxC1	CxC0	CxR Read	CxR Write	BxCR Read	Output to IOM-2	Applications
0	0	ICx	-	Bx	-	Bx monitoring, ICx monitoring
0	1	ICx	ICx	Bx	ICx	Bx monitoring, ICx looping from/to IOM-2
1	0	-	Bx	Bx	Bx	Bx access from/to S; Transmission of a constant value in Bx channel to S
1	1	Bx	Bx	-	Bx	Bx looping from S; transmission of a variable pattern in Bx channel to S

Note: x=1 for channel 1 or 2 for channel 2

The general sequence of operations to access the B/IC channels is:



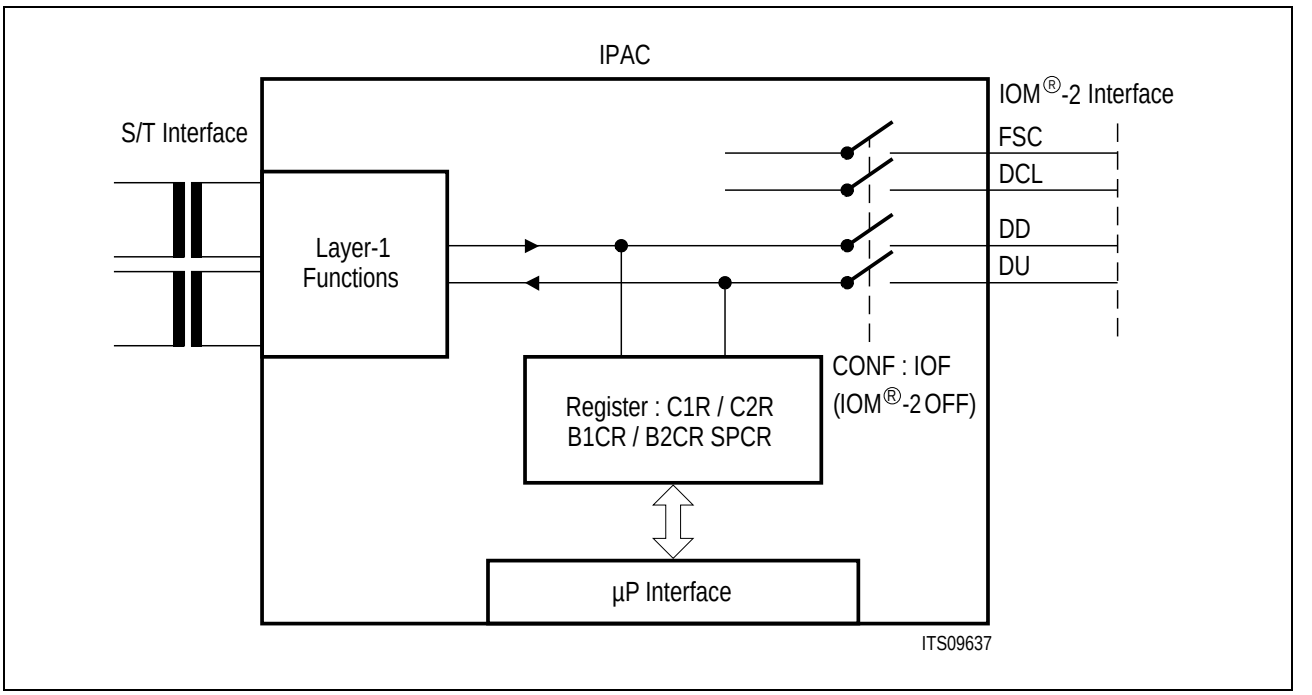


Figure 60 Principle of B/IC Channel Access in IOM®-2 Terminal Mode

(a) SPCR:C×C1, C×C0 = 00
B× monitoring, IC× monitoring

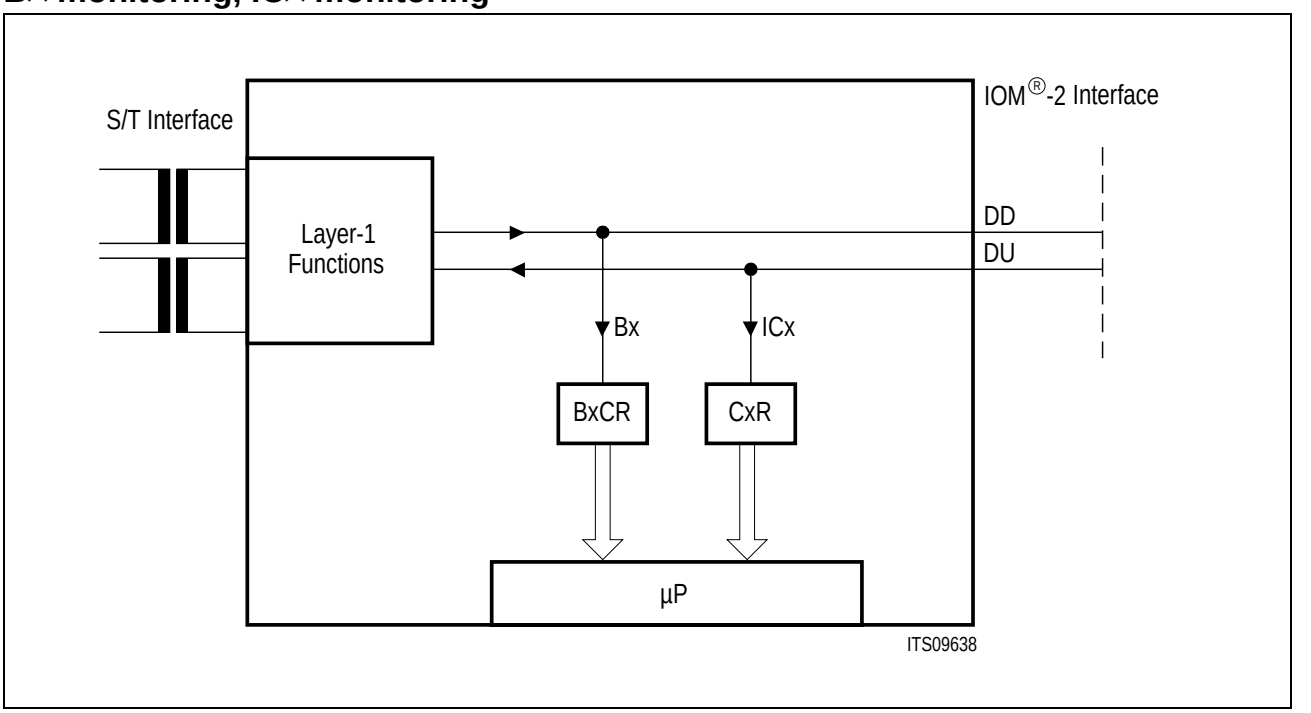
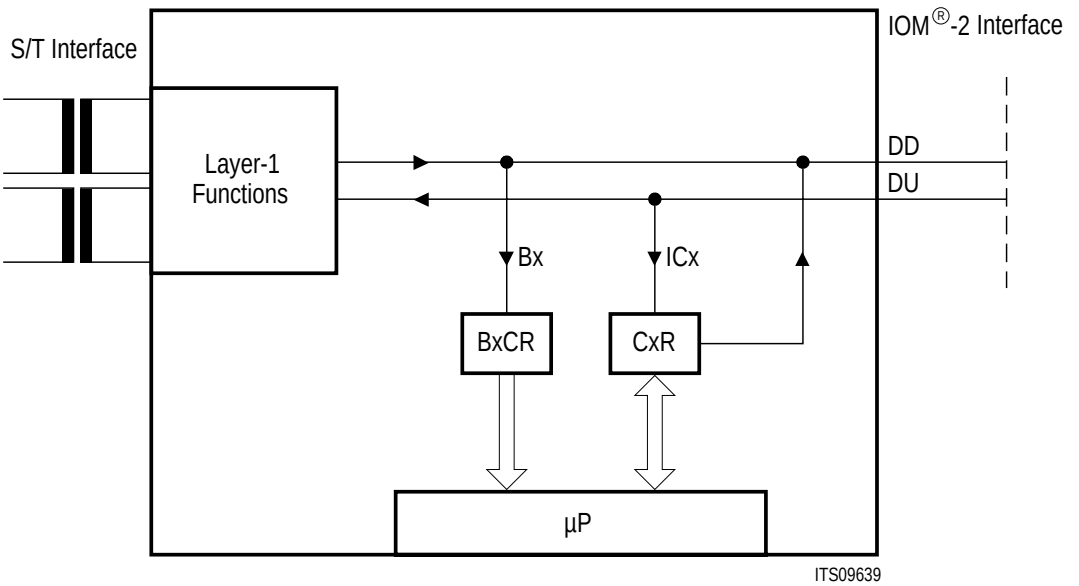
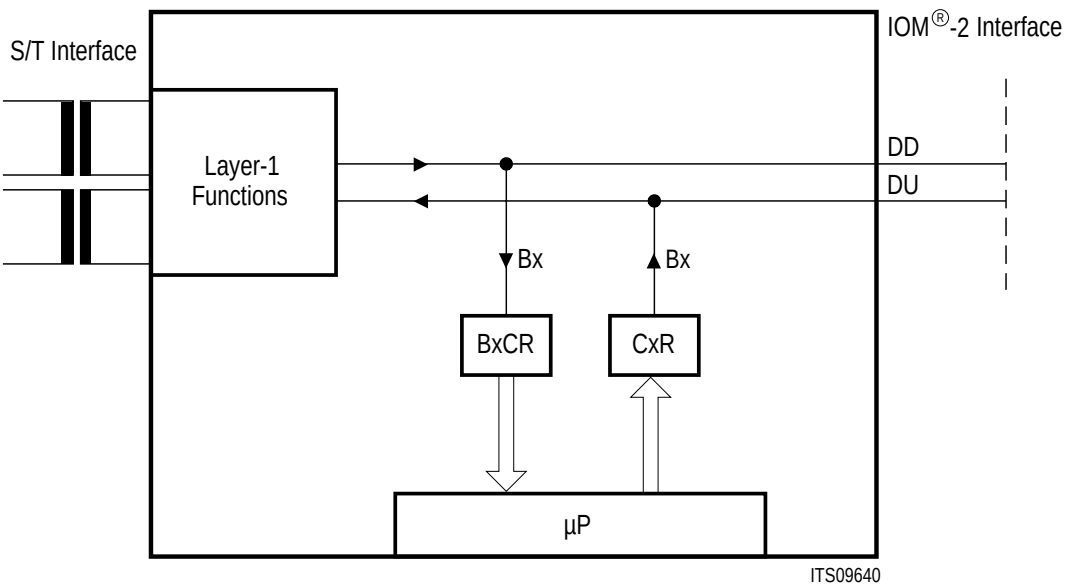


Figure 61 Access to B and IC Channels in IOM®-2 Terminal Mode

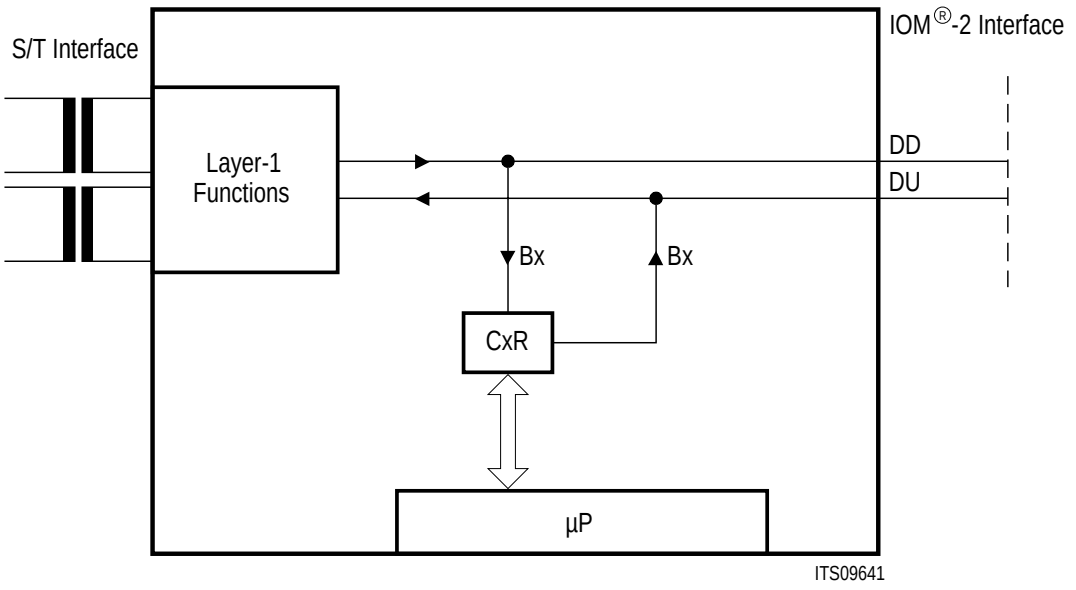
(b) SPCR:C×C1, C×C0 = 01
B× monitoring, IC× looping



(c) SPCR:C×C1, C×C0 = 10
B× access from/to S/T
transmission of constant value to S/T



(d) SPCR:C×C1, C×C0 = 11
B× looping from/to S/T
transmission of variable pattern to S/T



2.7.4 MONITOR Channel Handling

In IOM-2 mode, the MONITOR channel protocol is a handshake protocol used for high speed information exchange between the IPAC and other devices in MONITOR channel "0" or "1" (**see figure 53**). In the non-TE mode, only one MONITOR channel is available ("MONITOR channel 0").

The MONITOR channel protocol is necessary:

- For programming and controlling the layer-1 part of the IPAC over MONITOR channel 0. The layer 1 registers are not directly accessible to the host for read and write accesses via the common register set.
- For programming and controlling external devices attached to the IOM-2 interface when the layer-1 part of the IPAC is disabled (CONF:TEM). Examples of such devices are: layer-1 transceivers (using MONITOR channel 0), and peripheral V/D modules (using MONITOR channel 1) that do not need a parallel microcontroller interface, such as the Audio Ringing Codec Filter ARCOFI PSB 2163.
- For data exchange between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the MONITOR channel avoids the necessity of a dedicated serial communication path between the two systems. This greatly simplifies the system design of terminal equipment (**figure 62**).

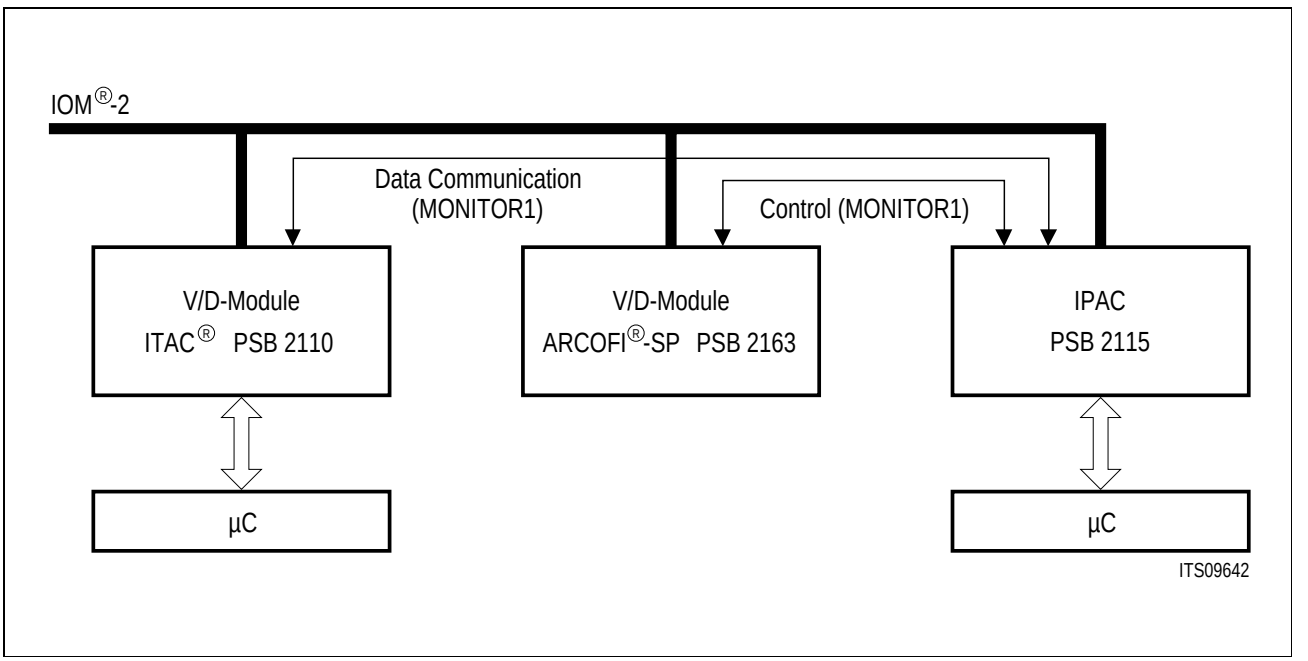


Figure 62 Examples of MONITOR Channel Applications in IOM®-2 TE Mode

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR0 or 1) and MONITOR Channel Transmit (MX0 or 1) bits. For example: data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a "1" (idle) in MR, MX by setting the control bit MRC1, 0 or MXC1, 0 to "0" (MONITOR Control Register MOCR), or enable the control of these bits internally by the IPAC according to the MONITOR channel protocol. Thus, before a data exchange can begin, the control bit MRC(1, 0) or MXC(1, 0) should be set to "1" by the microprocessor.

The MONITOR channel protocol is illustrated in **figure 63**. Since the protocol is identical in MONITOR channel 0 and MONITOR channel 1 (available in TE mode only), the index 0 or 1 has been left out in the illustration.

The relevant **status bits** are:

- MONITOR Channel Data Received MDR (MDR0, MDR1)
- MONITOR Channel End of Reception MER (MER0, MER1)

for the **reception** of MONITOR data, and

- MONITOR Channel Data Acknowledged MDA (MDA0, MDA1)
- MONITOR Channel Data Abort MAB (MAB0, MAB1)

for the **transmission** of MONITOR data (Register: MOSR)

In addition, the status bit:

MONITOR Channel Active MAC (MAC0, MAC1)
indicates whether a transmission is in progress (Register: STARD).

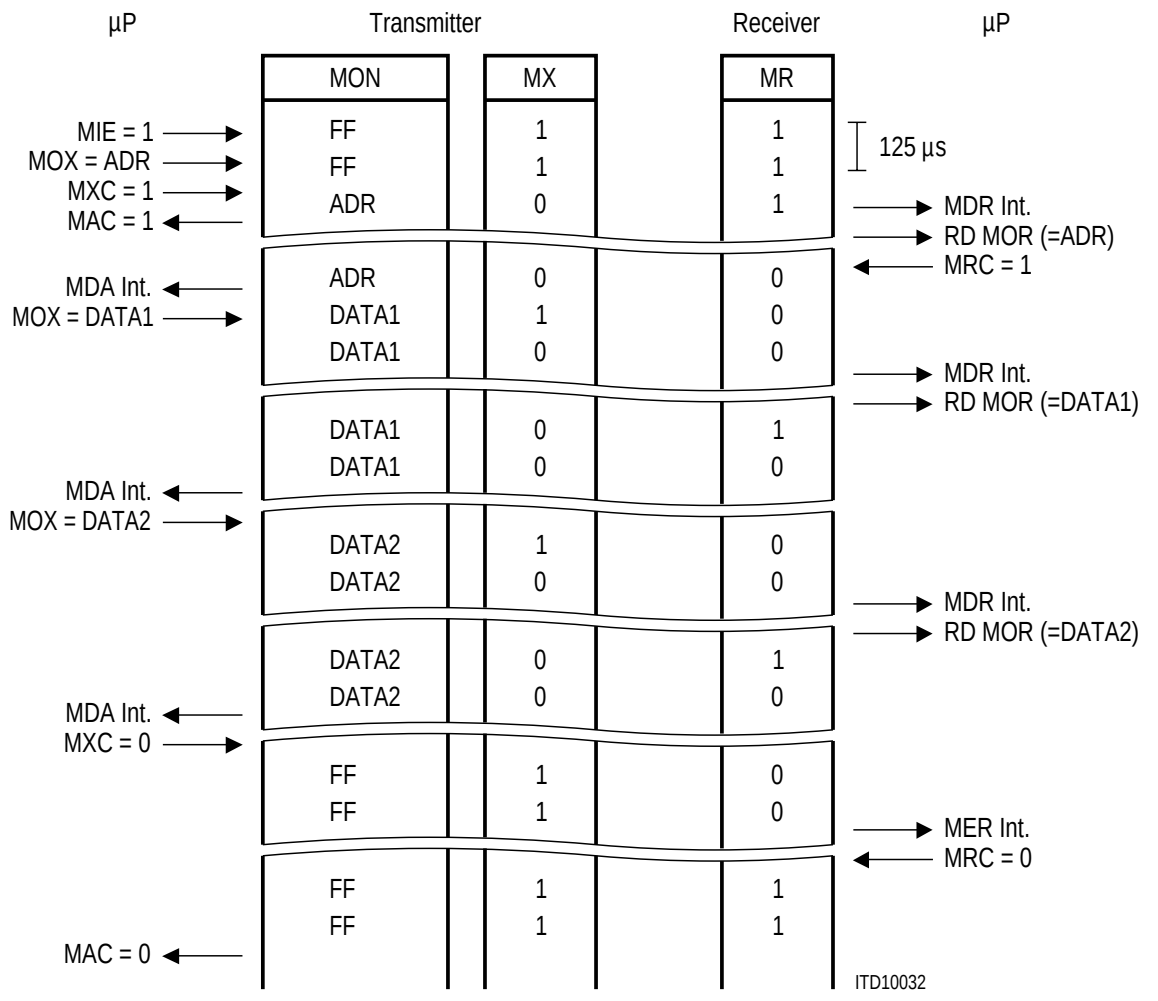


Figure 63 MONITOR Channel Protocol (IOM®-2)

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a "0" in the MONITOR Channel Active MAC status bit.

After having written the MONITOR Data Transmit (MOX) register, the microprocessor sets the MONITOR Transmit Control bit MXC to "1". This enables the MX bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates an MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to "1" to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol. In addition, it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable to "1".

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to "0". This causes a MONITOR Data Acknowledge MDA interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate an MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the MONITOR channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the MONITOR Transmit Control bit MXC to "0". This enforces an inactive ("1") state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the MONITOR Channel Active MAC bit return to "0".

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to "0". An aborted transmission is indicated by a MONITOR Channel Data Abort MAB interrupt status at the transmitter.

2.7.4.1 Handshake Procedure

Structure

The structure of the monitor channel is 8 bit wide, located at bit position 16-23 in every time slot (assuming that the first bit in a time slot is located at bit position 0). Monitor messages sent to the IPAC are 1 or 2 bytes long, monitor messages returned by the IPAC are 0, 1, 2, or 5 bytes long depending on the command. Transmission of multiple monitor bytes is specified by IOM-2. For handshake control in multiple byte transfers, bit 30, monitor read “MR”, and bit 31 monitor transmit “MX”, of every time slot are used.

Verification

A double last-look criterion is implemented for both bytes of the monitor message.

Codes

3 categories of monitor messages are supported by the IPAC:

- MON-1 S_1/Q channel
- MON-2 S_2 channel
- MON-8 Register access

The order of listing corresponds to the priority attributed to each category. MON-1 messages will be transmitted first, MON-8 messages last in case several messages are initiated simultaneously.

The monitor channel is full duplex and operates on a pseudo-asynchronous basis, i.e. while data transfer on the bus takes place synchronized to frame synchronization, the flow of monitor data is controlled by the MR and MX bits. Monitor data will be transmitted repeatedly until its reception is acknowledged.

Figure 65 illustrates a monitor transfer at maximum speed. The transmission of a 2-byte monitor command followed by a 2-byte IPAC response requires a minimum of 12 IOM-2 frames. In case the controller is able to confirm the receipt of first IPAC response byte in the frame immediately following the MX transition on DOUT from HIGH to LOW (i.e. in frame No. 6), 1 IOM frame may be saved.

Note:

Transmission and reception of monitor messages can be performed simultaneously by the IPAC. This feature is used by the IPAC to send back the response before the transmission from the controller is completed (IPAC does not wait for EOM from controller).

M1/2: Monitor message 1. and 2. byte

R1/2: Monitor response 1. and 2. byte

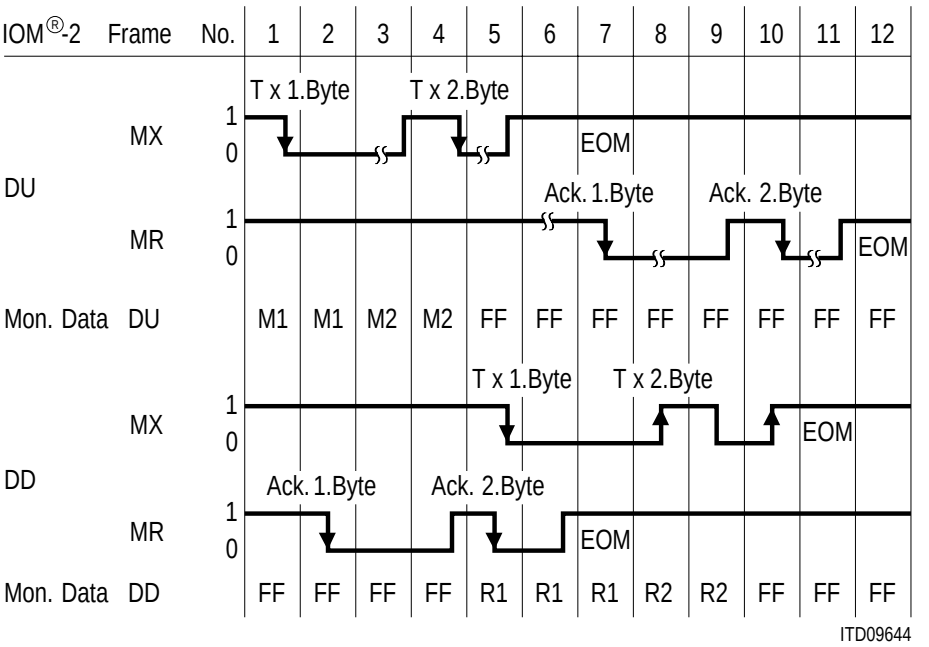


Figure 64 Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. HIGH) for two or more successive IOM frames, the channel is considered idle in this direction.

Standard Transmission Procedure

1. The first byte of monitor data is placed by the external controller (e.g. ICC, EPIC) on the DU line of the IPAC and MX is activated (LOW; frame No 1).
2. The IPAC reads the data of the monitor channel and acknowledges by setting the MR bit of DD active if the transmitted bytes are identical in two received frames (frame No. 2 because the IPAC reads and compares data already while the MX bit is not activated).
3. The second byte of monitor data is placed by the controller on DU and the MX bit is set inactive for one single IOM frame. This is performed at a time convenient to the controller.
4. The IPAC reads the new data byte in the monitor channel after the rising edge of MX has been detected. In the frame immediately following the MX transition active-to-inactive, the MR bit of DD is set inactive. The MR transition inactive-to-active exactly one IOM frame later is regarded as acknowledgment by the external controller (frame No. 4-5).

The response of the IPAC will always be sent immediately after the 2. byte has been received and acknowledged.

5. After both monitor data bytes have been transferred to the IPAC, the controller transmits “End of Message” (EOM) by setting the MX bit inactive for two or more IOM frames (frame No. 5-6).
6. In the frame following the transition of the MX bit from active to inactive, the IPAC sets the MR bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR bit inactive (frame No. 6). The transmission of the monitor command by the controller is complete.
7. If the IPAC is requested to return an answer it will commence with the response as soon as the second controller byte was acknowledged (i.e. response starts in frame 5).

   The procedure for the response is similar to that described in points 1-6 except for the transmission direction. It is assumed that the controller does not latch monitor data. For this reason one additional frame will be required for acknowledgment.

   Transmission of the 2. monitor byte will be started by the IPAC in the frame immediately following the acknowledgment of the first byte. The IPAC does not delay the monitor transfer.

Error Treatment and Transmission Abort

In case the IPAC does not detect identical monitor messages in two successive frames, transmission is not aborted. Instead the IPAC will wait until two identical bytes are received in succession.

Transmission is aborted only if errors in the MR/MX handshake protocol occur. An abort is indicated by setting the MR bit inactive for two or more IOM-2 frames. The controller must react with EOM. This situation is illustrated in the following figure.

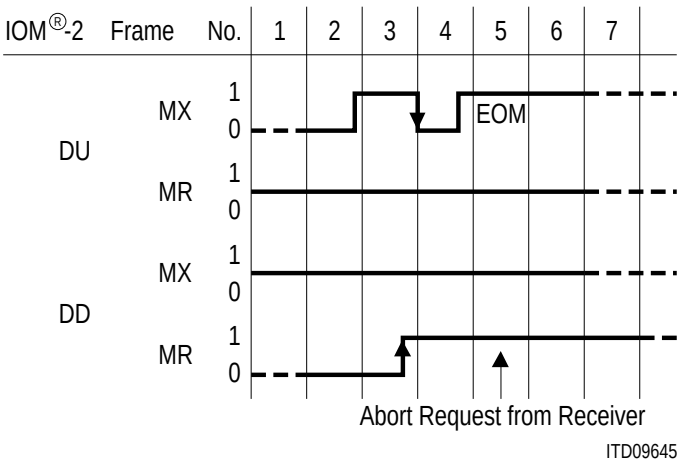


Figure 65 Abortion of Monitor Channel Transmission

2.7.4.2 Monitor Procedure Timeout (TOD)

The IPAC can operate with or without the “Monitor Timeout Procedure”. The TOD bit in the SM/CI (Timeout Disable) controls the timeout function. TOD = ZERO enables the function, TOD = ONE disables it.

With the timeout procedure enabled, the IPAC checks the monitor status once per multi-frame. This check is performed at the same time the 20th (i.e. last) S-frame is transmitted within the S-interface multi-frame structure.

In case the monitor is active the current status of the monitor channel is saved. This condition will be compared with the status at the next check (i.e. 5 ms later). If the condition of the monitor channel has not changed within this period the IPAC assumes a lock-up situation.

The IPAC will resolve this lock-up situation by transmitting on DD a EOM (End of Message) command (MX bit set to ONE for 2 IOM frames). After the transmission of EOM the IPAC will retransmit the previous monitor channel data. No monitor channel data will therefore be lost.

2.7.4.3 MON-1, MON-2 Commands (S/Q Channel Access)

Function: MON-1 and MON-2 commands provide access to the IPAC internal S/Q registers. MON1 controls the S_1 and Q channel, MON-2 controls the S_2 channel on the S-interface. In order to synchronize onto multiframing pulses (TE, LT-T modes) and issue monitor-messages (LT-S mode) the MFD (Multi-frame disable) bit in the configuration register must be set to ZERO.
MON-1 and MON-2 commands may be passed at any instant provided the S-interface is activated. They are always one byte long.

Direction S $\rightarrow$ IOM:

In the direction S-interface to IOM interface a 1 byte buffer is implemented. Every time a S/Q message has been received on the S-interface which needs to be forwarded to the IOM interface this message will be saved in a latch. This latch allows retransmission of the old S/Q data on IOM in case the message has not been read by the controller before a monitor timeout occurred.
While the latched data has not been read correctly from the monitor channel the S/Q receiver will not reload the latch. Thus the IOM controller must read out the S/Q messages from IOM once per 5 ms (multi-frame period). If this is not guaranteed S/Q channel data may be lost.

Direction IOM $\rightarrow$ S:

No buffering is available in the direction IOM-interface to S-interface.
The IPAC will acknowledge a S/Q command correctly and transfer the command into an internal S/Q transmit buffer if this command is received during frame numbers 1-17. Once a command has been transferred into the internal transmit register new S/Q commands received during frames 1-17 will not be accepted by the IPAC (i.e. no acknowledgment issued with MR bit). During frame numbers 18-20 however the monitor channel data is transferred directly into the transmit register. During this period previously accepted S/Q data could therefore be overwritten. To avoid this situation the controller must be programmed to send no more than one S/Q command per multi-frame (5 ms).

Note that for both S_1 and S_2 channel a separate transmit register is reserved. The above stated restriction thus applies only to S/Q commands referring to the same channel.
Transmission of the stored data will commence with the new multi-frame.

Priority: MON-1 commands have the highest priority, MON-2 command are treated with second priority.

Modes: Non-auto mode and transparent mode are available in all operational modes. The SQM (SQ Mode) bit selects transparent mode (ONE) and non-auto mode (ZERO).

Non-Auto Mode

In non-auto mode only MON-1 functions to access the S_1 and Q channel are available. MON-2 messages (for S_2 channel access) are ignored.

In non-auto mode monitor messages are only released after new data has been received. In this mode traffic on the IOM monitor channel is reduced. The controller only receives changes in the S_1 or Q channel reducing its processing demands as well.

Transparent Mode

In transparent mode all S/Q channels are available to the user. MON-1 commands/ messages service the S_1 and Q channel, MON-2 commands/messages related exclusively to the S_2 channel. In this mode the data received on S_1, S_2 or Q will be forwarded directly to the IOM-interface. No comparison with previously sent data is performed so that one MON-1 and one MON-2 monitor message will be issued every 5 ms (once per multi-frame) in TE or LT-T modes. In LT-S mode one MON-1 message will indicate every multi-frame the current Q channel data received.

Codes:

MON-1 Command/Message (S_1/Q channel)

1 Byte							
0	0	0	1	S_{11}/Q	S_{12}/Q	S_{13}/Q	S_{14}/Q
MON-1				Data			

S1: Data in S_1 channel (LT-S input on IOM-2; TE, LT-T output on IOM-2)

Q: Data in Q channel (TE, LT-T input on IOM-2; LT-S output on IOM-2)

MON-2 Command/Message (S_2 channel)

1 Byte							
0	0	1	0	S_{21}	S_{22}	S_{23}	S_{24}
MON-2				Data			

S_2: Data in S_2 channel (LT-S input on IOM-2; TE, LT-T output on IOM-2)

2.7.4.4 MON-8 Commands (Register Access)

MON-8 commands provide access to the IPAC internal registers. MON-8 commands allow to configure the S/T transceiver of the IPAC.

MON-8 Commands are specified in detail in chapter **2.4.4 S/T Transceiver Control**.

2.7.5 C/I-Channel Handling

The Command/Indication channel carries real-time status information between the IPAC and another device connected to the IOM.

1) One C/I channel (called C/I0) conveys the commands and indications between the layer-1 and the layer-2 parts of the IPAC. This channel is available in all timing modes (TE and non-TE). It can be accessed by an external layer-2 device e.g. to control the layer-1 activation/deactivation procedures. C/I0 channel access may be arbitrated via the TIC bus access protocol in the IOM-2 terminal timing mode (pin MODE0=0). In this case the arbitration is done in C/I channel 2 (**see figure 53**).

The C/I0 channel is accessed via register CIR0 (in receive direction, layer-1 to layer-2) and register CIX0 (in transmit direction, layer-2 to layer-1). The C/I0 code is four bits long.

A listing and explanation of the layer-1 C/I codes can be found in **chapter 3.6.2**.

In the receive direction, the code from layer-1 is continuously monitored, with an interrupt being generated anytime a change occurs (ISTAD:CIC). A new code must be found in two consecutive IOM frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2) A second C/I channel (called C/I1) can be used to convey real time status information between the IPAC and various non-layer-1 peripheral devices e.g. PSB 2163 ARCOFI-SP. The channel consists of six bits in each direction. It is available only in the IOM-2 TE timing mode (**see figure 53**).

The C/I1 channel is accessed via registers CIR1 and CIX1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

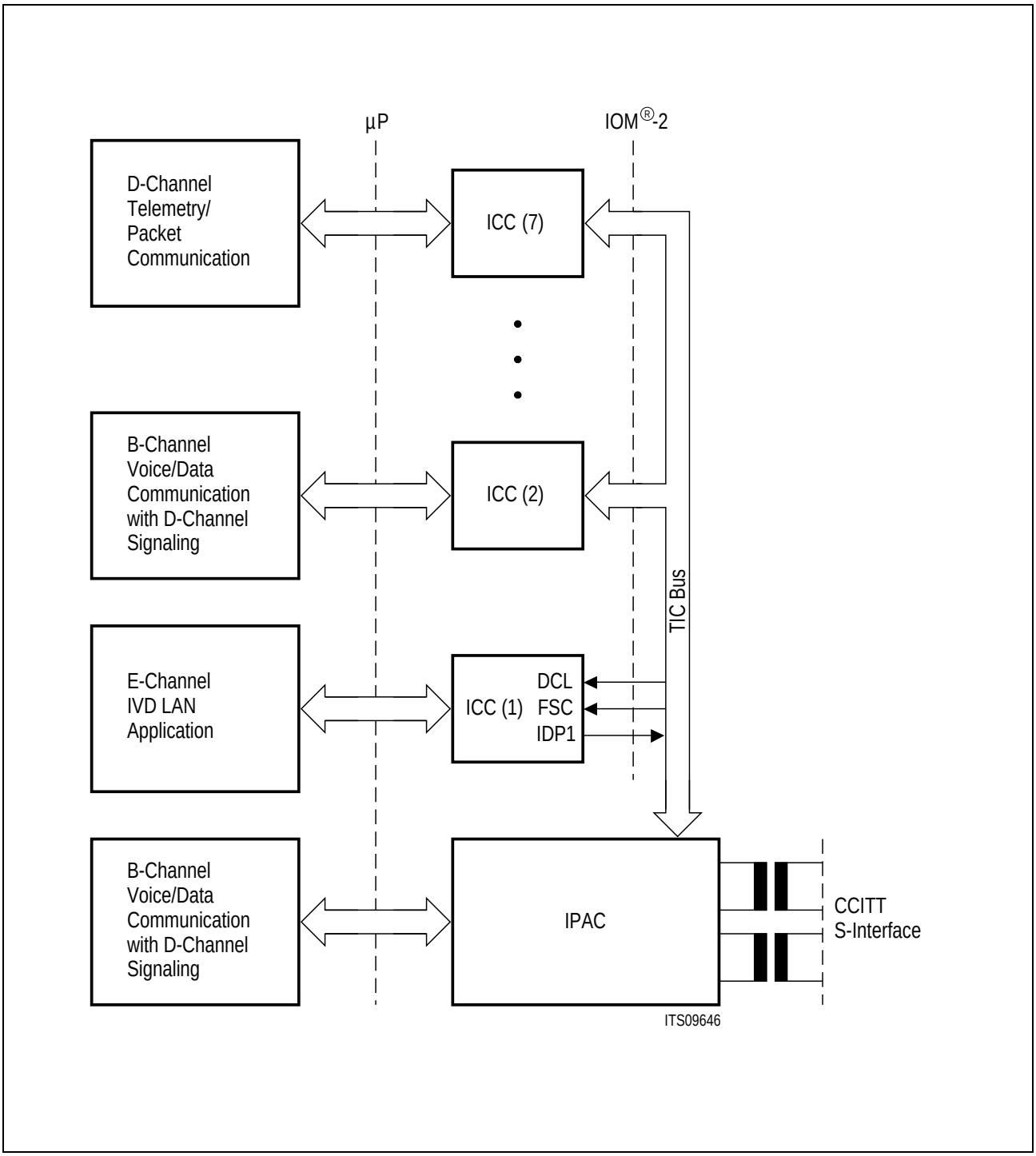


Figure 66 Applications of TIC Bus in IOM®-2 Bus Configuration

2.7.6 TIC Bus Access

In IOM-2 interface mode the TIC bus capability is only available in TE mode. The arbitration mechanism implemented in the last octet of IOM channel 2 of the IOM-2 interface allows the access of external communication controllers (up to 7) to the layer-1 functions provided in the IPAC and to the D channel. (TIC bus; **see figure 66**). To this effect the outputs of the controllers (ICC:ISDN Communication Controller PEB 2070) are wired-or-and connected to pin DU. The inputs of the ICCs are connected to pin DD. External pull-up resistors on DU/DD are required. The arbitration mechanism must be activated by setting MODED:DIM2-0=001.
An access request to the TIC bus may either be generated by software (µP access to the C/I channel) or by the IPAC itself (transmission of an HDLC frame in the D-channel). A software access request to the bus is performed by setting CIX0:BAC=1 bit which has the effect that the BAC bit on the DU line (bit 5 of last octet of Ch2, **see figure 67**) is tied to "0" (i.e. "TIC bus is occupied").

In the case of an access request, the IPAC checks the Bus Accessed-bit BAC on DU for the status "bus free", which is indicated by a logical "1". If the bus is free, the IPAC transmits its individual TIC bus address programmed in the STCR register. The IPAC sends its TIC bus address TAD and compares it bit by bit with the value on DU. If a sent bit set to ’1’ is read back as ’0’ because of the access of another D-channel source with a lower TAD, the IPAC withdraws immediately from the TIC bus. The TIC bus is occupied by the device which sends its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address values wins. This one will set BAC=0 on TIC bus and starts D-channel transmission.

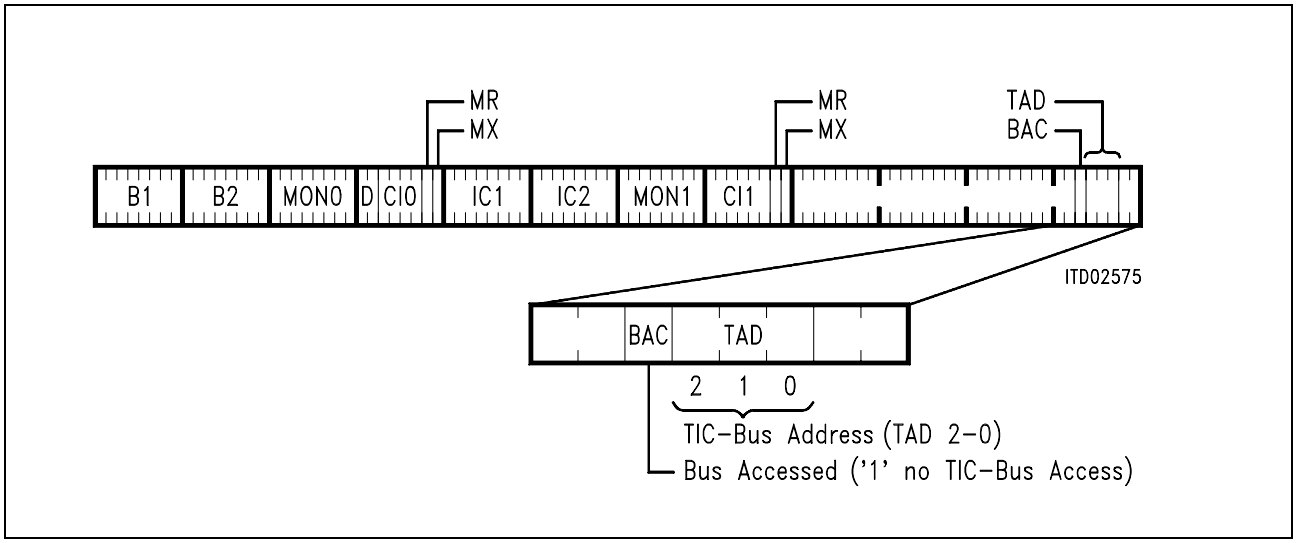


Figure 67 Structure of Last Octet of Ch2 on DU

When the TIC bus is seized by the IPAC, the bus is identified to other devices as occupied via the DU Ch2 Bus Accessed-bit state "0" until the access request is

withdrawn. After a successful bus access, the IPAC is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM interface request access to the D and C/I channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

Note: Bit BAC (CIX0 register) should be reset by the µP when access to the C/I channels is no more requested, to grant other devices access to the D and C/I channels.

The availability of the S/T interface D channel is indicated in bit 5 "Stop/Go" (S/G) of the DD last octet of Ch2 channel (**figure 68**).

S/G = 1 : stop
S/G = 0 : go

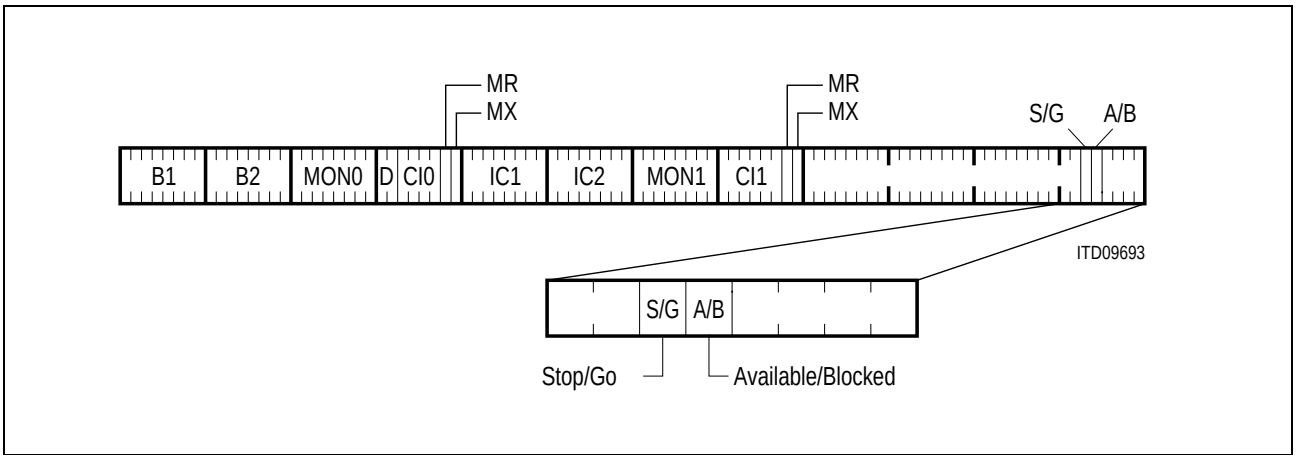


Figure 68 Structure of Last Octet of Ch2 on DD

The Stop/Go bit is available to other layer-2 devices connected to the IOM to determine if they can access the S/T bus D channel.

The A/B bit is used by the exchange (controlled by layer 1) to temporarily prohibit D-channel transmission (A/B = ’0’) when only a single D-channel controller on the linecard handles more lines (ELIC concept). For most applications D-channel transmission is usually permitted (A/B = ’1’).

2.8 Auxiliary Interface

2.8.1 Mode Dependent Functions

The AUX interface provides for various functions, which depend on the operation mode (TE, LT-T or LT-S mode) selected by pins MODE0 and MODE1/$\overline{\text{EAW}}$ (see **table 15**). After reset all pins except DRQTA and DRQRA (pins AUX0 and AUX1 in TE mode) are switched as inputs until further configuration is done by the host.

Table 15 AUX Pin Functions

Pin	TE mode	LT-T mode	LT-S mode
AUX0	DRQTA	CH0	CH0
AUX1	DRQRA	CH1	CH1
AUX2	AUX2 / INT	CH2	CH2
AUX3	AUX3	AUX3 / FBOUT	AUX3 / FBOUT
AUX4	AUX4	AUX4 / PCMIN	AUX4 / PCMIN
AUX5	AUX5	AUX5 / PCMOUT	AUX5 / PCMOUT
AUX6	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$
AUX7	$\overline{\text{INT1}}$	$\overline{\text{INT1}}$ / SGOUT	$\overline{\text{INT1}}$

AUX2-5 (TE mode), AUX3-5 (LT modes)

These pins can be used as programmable I/O lines. In LT modes this function is multiplexed with the PCM interface, i.e. the host can select either PCM functionality (PCFG:PLD=0) or standard I/O characteristic on AUX3-5 (PCFG:PLD=1).

As inputs (AOE:OEx=1) the state at the pin is latched in when the host performes read operation to register ARX. A certain setup and hold time must be ensured for proper operation (see **figure 69**).

As outputs (AOE:OEx=0) the value in register ATX is driven on the pins with a minimum delay after the write operation to this register is performed. They can be configured as open drain (ACFG:ODx=0) or push/pull outputs (ACFG:ODx=1). The status (’1’ or ’0’) at output pins can be read back from register ARX, which may be different from the ATX value, e.g. if another device drives a different level.

AUX2 / INT (TE mode, output)

If configured as output, pin AUX2 provides the high active interrupt output signal. If configured as input it can be used as a general purpose input pin as described above (also see **chapter 2.6.4**).

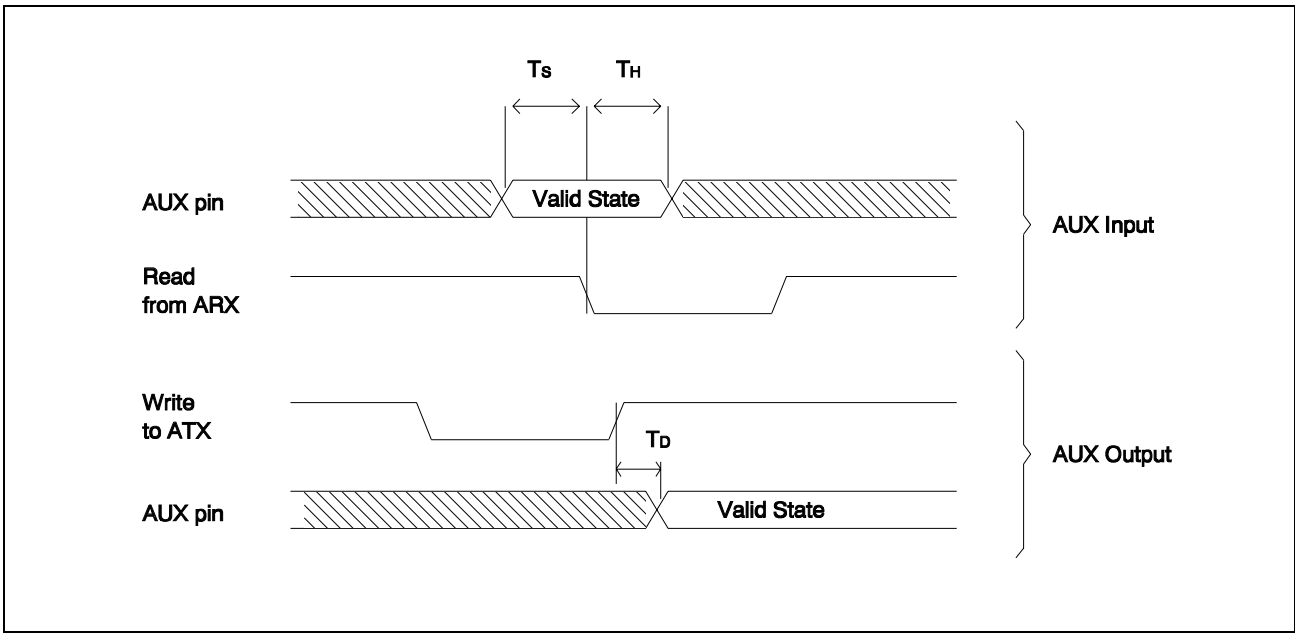


Figure 69 Input/Output Characteristic of AUX Pins

$\overline{\text{INT0}}$, $\overline{\text{INT1}}$ (all modes), $\overline{\text{INT1}}$/SGOUT (LT-T mode)

For all modes two pins can be used as programmable I/O with optional interrupt input capability (default after reset, i.e. both interrupts masked).

The $\overline{\text{INT0/1}}$ pins are general input or output pins like AUX2-5 (see description above). In addition to that, as inputs they can generate an interrupt to the host (ISTA:INT0/1) which is maskable in MASK:INT0/1. The interrupt input is either edge or level triggered (ACFG:EL0/1).
As outputs both pins are able to sink I_{OL}= 5 mA which allows for direct connection of LEDs in standalone applications for example.

In LT-T mode pin AUX7 provides the additional capability to output the S/G bit from the IOM-2 interface by setting CONF:SGO=1. This may be used for test purposes.

DRQTA, DRQRA (TE mode)

For B-channel B DMA pins are always available, whereas for channel A the availability depends on the mode of operation.

In TE mode DRQTA and DRQRA are additionally available for the DMA interface, so both B-channels can be operated in DMA mode.
In LT-T and LT-S mode only B-channel B can be operated by DMA data transfer.

Data transfer by DMA is described in detail in chapter **2.6.5 DMA Interface**.

CH0, CH1, CH2

In linecard mode one FSC frame is a multiplex of eight IOM-2 channels, each of them consisting of B1-, B2-, MONITOR-, D- and C/I-channel and MR- and MX-bits.
So in LT-T and LT-S mode one of eight channels on the IOM-2 interface is selected by CH0-2. These pins must be strapped to VDD or VSS according to **table 4**.

Table 16 IOM-2 Channel Selection

CH2	CH1	CH0	Channel on IOM-2
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

For DCL = 1.536 MHz one of the IOM-2 channels 0 - 2 can be selected, for DCL = 4.096 MHz any of the eight IOM-2 channels can be selected.

PCMIN, PCMOUT

PCMIN and PCMOUT are receive and transmit lines of the general PCM interface. If enabled, the B-channels on the IOM-2 interface can flexibly be switched to any timeslot of the PCM interface.

If the PCM Interface is not used (PCFG:PLD=1), these pins serve as general I/O pins.

FBOUT (FSC/BCL Output)

In LT-T and LT-S mode this pin can be programmed to one of two functions:

- FSC Output (PCFG:FBS=0):
  An FSC clock is output which is derived from the DCL input (SCLK provides a 1.536 MHz output in LT-T mode) divided by 192. This is especially suitable for multiline applications, where one of several IPACs generates the common FSC.
- BCL Output (PCFG:FBS=1):
  This pin can output a single bit clock (DCL input divided by 2) equal to the IOM-2 data rate, especially to serve non IOM-2 compatible peripheral devices on the PCM interface.

If the PCM Interface is not used (PCFG:PLD=1), this pin serves as a general I/O pin.

2.8.2 PCM Interface

In LT-S and LT-T mode the IPAC provides a PCM interface (PCFG:PLD=0, default) that can be disabled (PCFG:PLD=1), so that the PCM pins can be used as general I/O pins (see previous **chapter 2.8.1**).

2.8.2.1 PCM Lines

Through its standard PCM interface the IPAC can be connected to devices in general TDM (time division multiplex) systems. In this way data controllers, which are not IOM-2 compatible, can indirectly be connected to the IOM-2 interface, since the programmed PCM timeslots are reflected in the corresponding IOM-2 B-channel timeslots.

The data and signal lines to be used with the PCM interface depend on the mode of operation and the type of interface of the external device:

PCMIN	Receive Data: The IPAC receives data from a peripheral device on PCMIN. The received data is then mapped to a B-channel on the IOM-2 interface.
PCMOUT	Transmit Data: The IPAC transmits data to a peripheral device on PCMOUT. This data is originated from a B-channel on the IOM-2 interface.
FSC	Frame Sync: FSC is used on the IOM-2 interface to indicate the beginning of a new IOM-2 frame. It is also used for the PCM interface to mark the beginning of new frame.
DCL	Bit Clock (double rate): DCL is the reference clock according to which data is written to PCMOUT and read from PCMIN. For peripheral devices supporting double rate bit clock, the clock signal is directly provided by SCLK (LT-T mode) or by the system (LT-S mode). DCL is the same clock as used for the IOM-2 interface.

BCL (FBOUT)	Bit Clock (single rate): For peripheral devices supporting single rate bit clock, the clock signal is provided at FBOUT. It is derived from SCLK (LT-T mode) or from a system clock (LT-S mode) by an internal divider (division by 2). See **chapter 2.8.2.2**.
FSC (FBOUT)	Frame Sync: The frame sync signal is multiplexed with BCL (see above) and output at FBOUT. It is derived from SCLK (LT-T mode) or from a system clock (LT-S mode) by an internal divider (division by 192). See **chapter 2.8.2.2**.

The frame sync signal FSC and the data clock DCL which are used on the IOM-2 interface also serve as the reference clocks on the PCM interface.

The rising edge of FSC marks the beginning of a new frame that consists of several timeslots each of which is 8 bits long (see **figure 70**). Depending on the frequency of the DCL clock the host can select one of up to 32 possible timeslots (DCL = 4.096 MHz) on the PCM interface from which B-channel data is read from (PCMIN) and written to (PCMOUT).

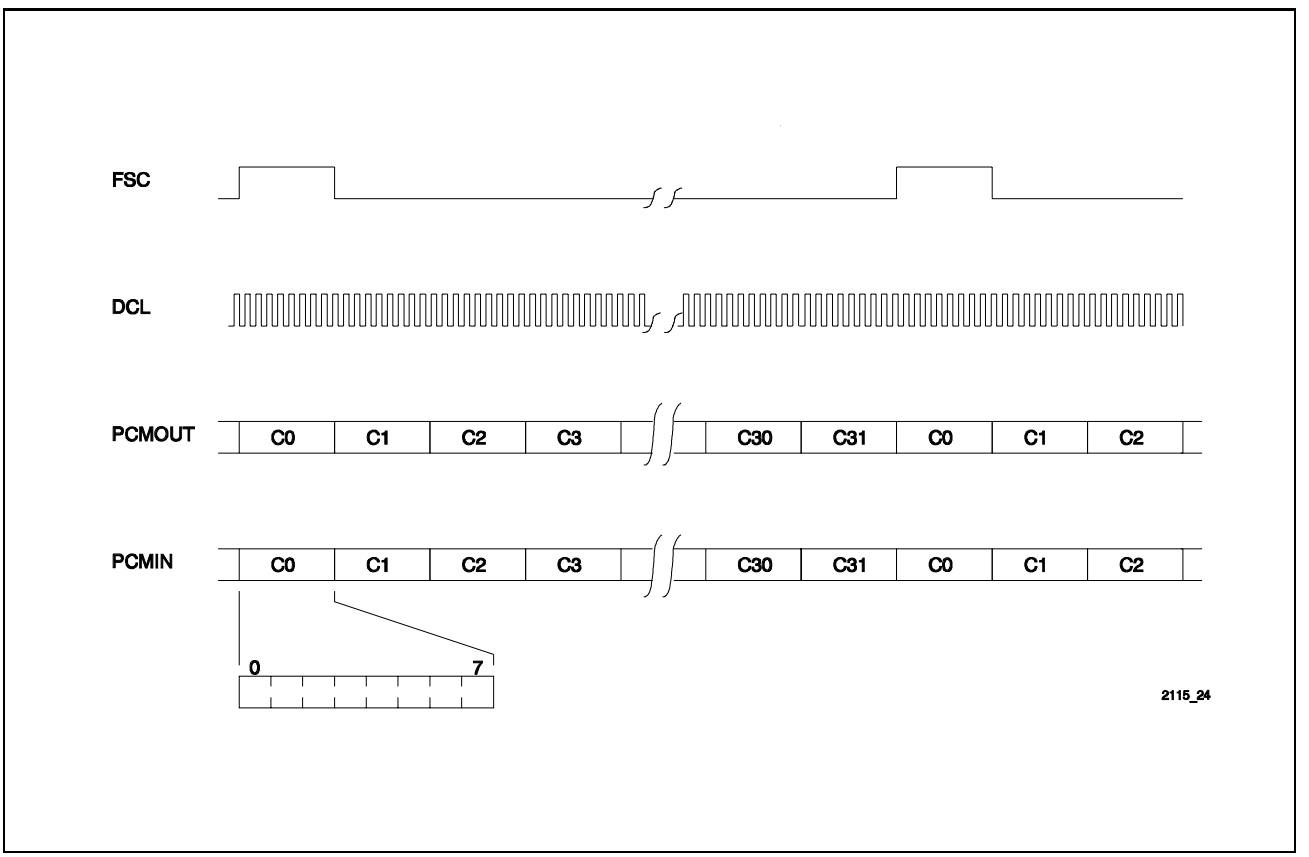


Figure 70 PCM Frame Alignment

Similar as on the IOM-2 interface, PCM data is written to PCMOUT with the first rising edge of DCL and latched in from PCMIN with the second falling edge of DCL (see **figure 71**).
BCL is derived from the DCL clock by an internal devider (refer to **chapter 2.8.2.2**).

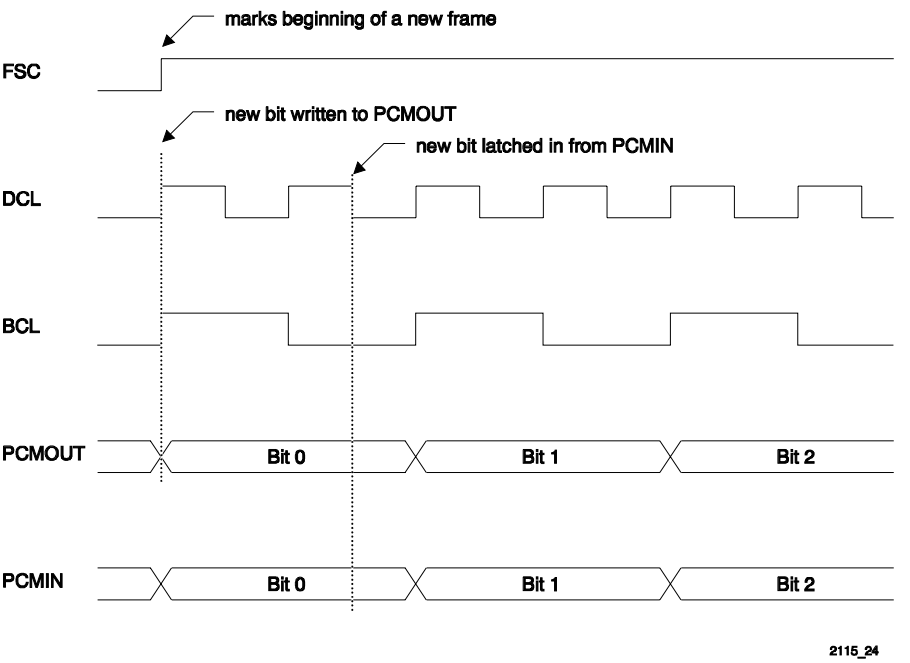


Figure 71 PCM Bit Alignment

The PCM interface can be used to build a connection between non IOM-2 compatible voice/data controllers and the IOM-2 interface in order to transfer B-channel data from/ to the external device. Receive data on the DD line can be mapped to any timeslot on the PCMOUT line. Data received from the external device on any timeslot on PCMIN can be mapped to the DU line (see **figure 72**).
Data which is received on PCMIN is forwarded to the DU line with the next IOM-2 frame. Similar for the opposite direction, data on DD is forwarded to the PCMOUT line with the next FSC frame.
For test purposes data on PCMIN can be mapped to DD and B-channel data on DU can be mapped to PCMOUT (refer to **chapter 2.8.2.3**).

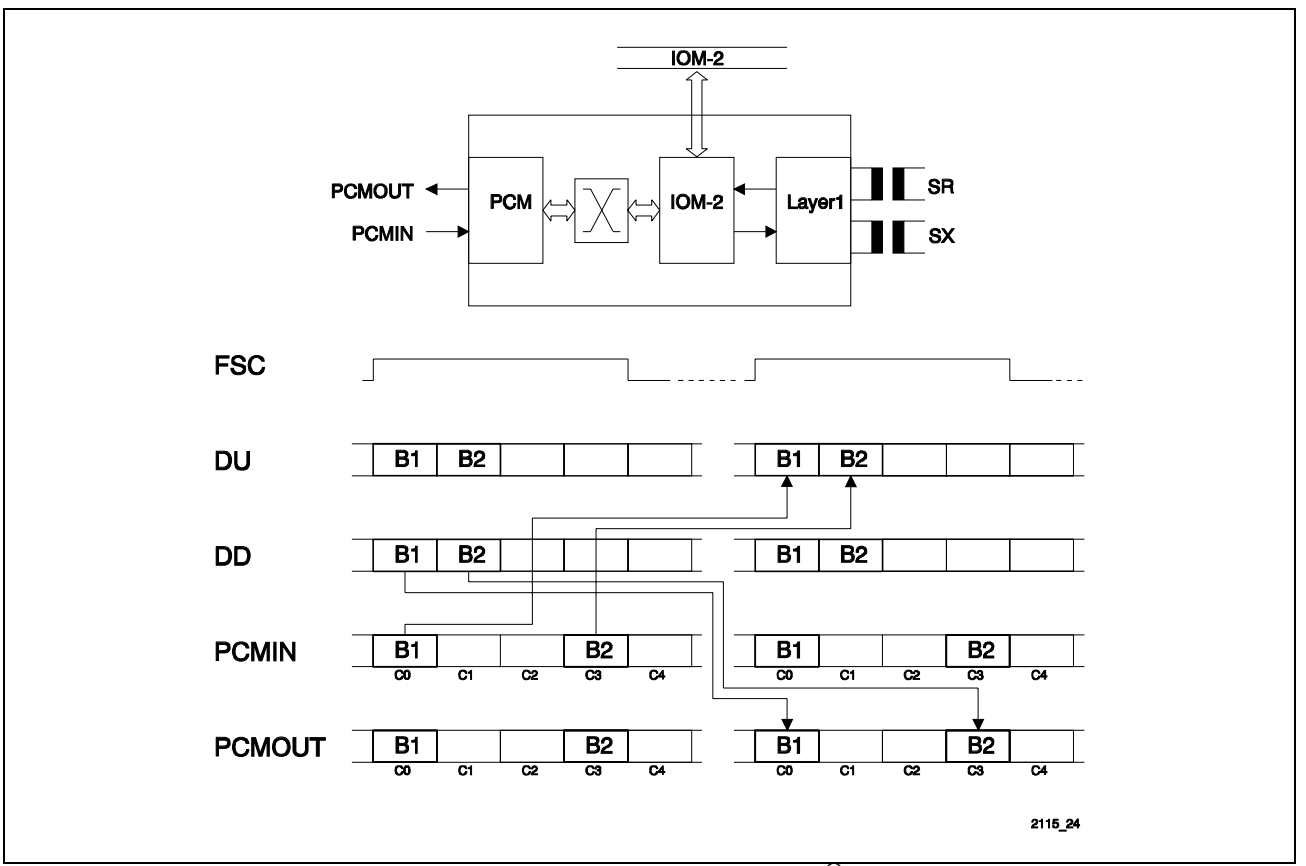


Figure 72 Switching Data between PCM and IOM®-2

Data transfer from/to the host is performed via the 64-byte FIFOs. The paragraphs above describe the procedures when data is tranferred between FIFO and IOM-2 interface while the corresponding data is mapped from IOM-2 to the PCM interface.
In a similar way data can be transferred directly between FIFO and PCM interface while the corrsponding PCM timeslots are mapped to the IOM-2 interface (**figure 73**). The programming of timeslots on PCM (timeslot position and length) is the same as for IOM-2, the only difference is that the data path is switched from FIFO ↔ IOM-2 (DPS = 0) to FIFO ↔ PCM (DPS = 1), the timeslot switching between PCM and IOM-2 also remains the same.

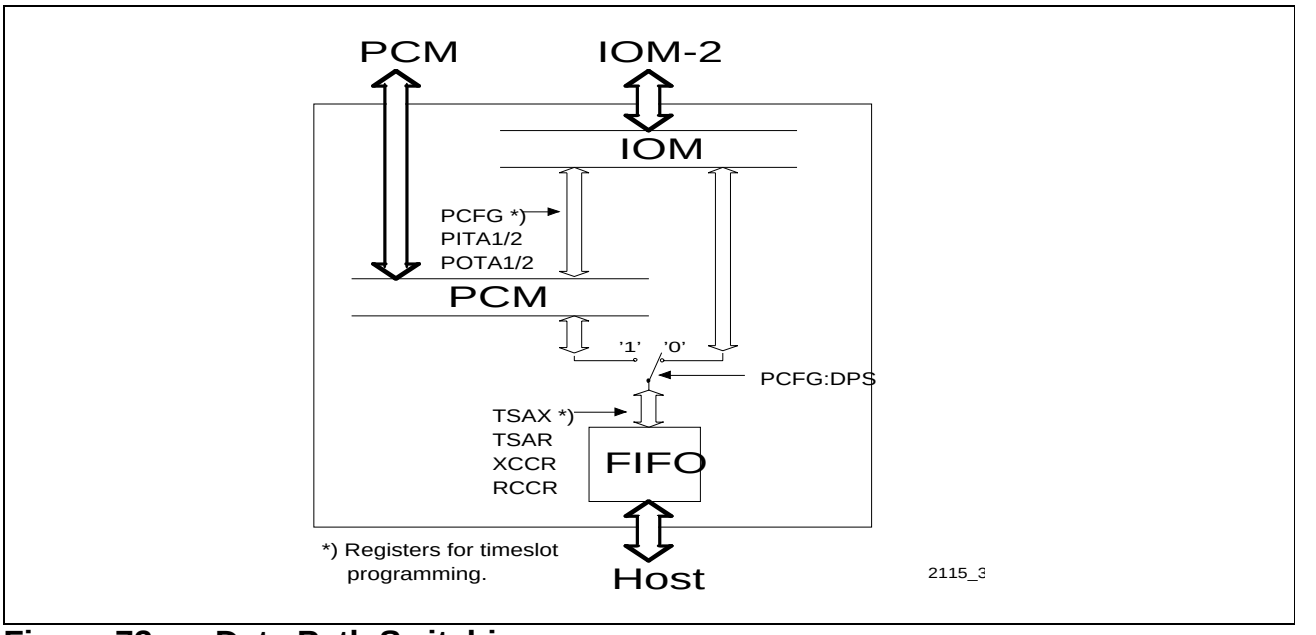


Figure 73 Data Path Switching

2.8.2.2 Clock Generation

In LT-T mode a 1.536 MHz clock synchronous to the S interface is provided via pin SCLK, which can be connected to the DCL input and used as the bit clock (double rate!) for the IOM-2 interface. An internal divider derives from the DCL input either a common FSC (division by 192) or a single bit clock (division by 2) which is suitable for external devices that don't support double rate (**figure 74**). The host can select whether FSC (PCFG:FBS=0) or BCL (PCFG:FBS=1) is provided on FBOUT.

In LT-S mode the 1.536 MHz clock is to be provided by the system. In a similar way it can be used as the DCL input for FSC/BCL generation.

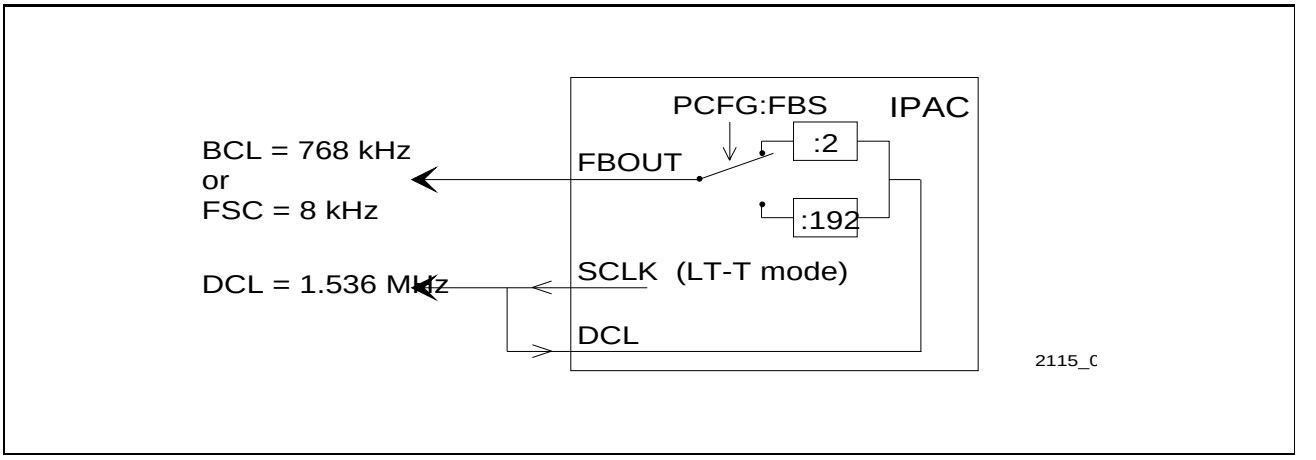


Figure 74 Generation of FSC and BCL in LT-T mode

Therefore in multiline applications where two or three IPACs are connected across one IOM-2 interface, one IPAC may generate the FSC signal for all IPACs, while another one generates the BCL, if necessary, for peripheral devices (**figure 75**).

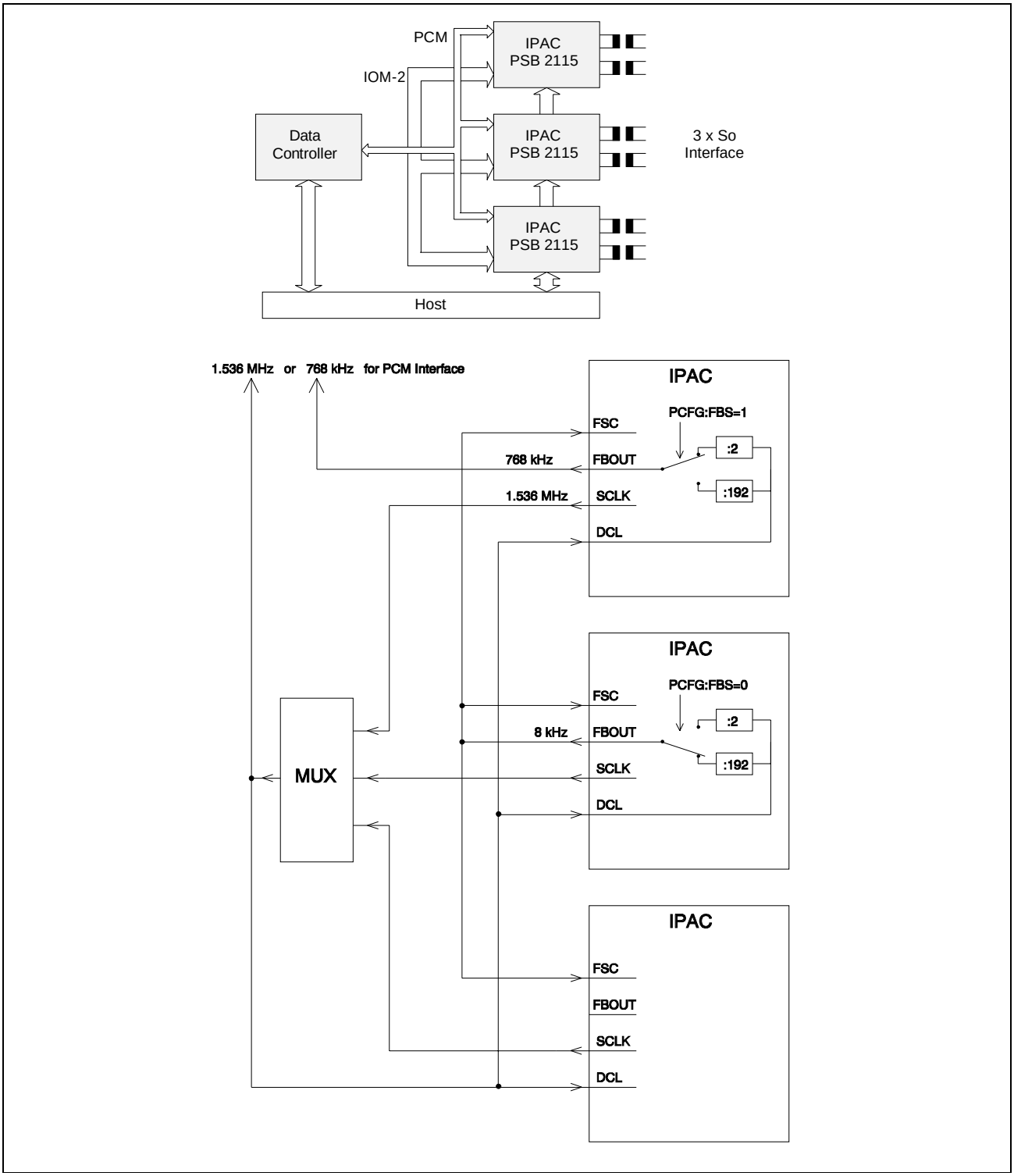


Figure 75 Multiline Application

2.8.2.3 Switching of Timeslots

Figure 76 shows as an example, the switching of timeslots from the PCM lines to the data upstream and data downstream lines of IOM-2 channel B1.
The datapath switching of channel B2 to the PCM interface is done in a similar way.

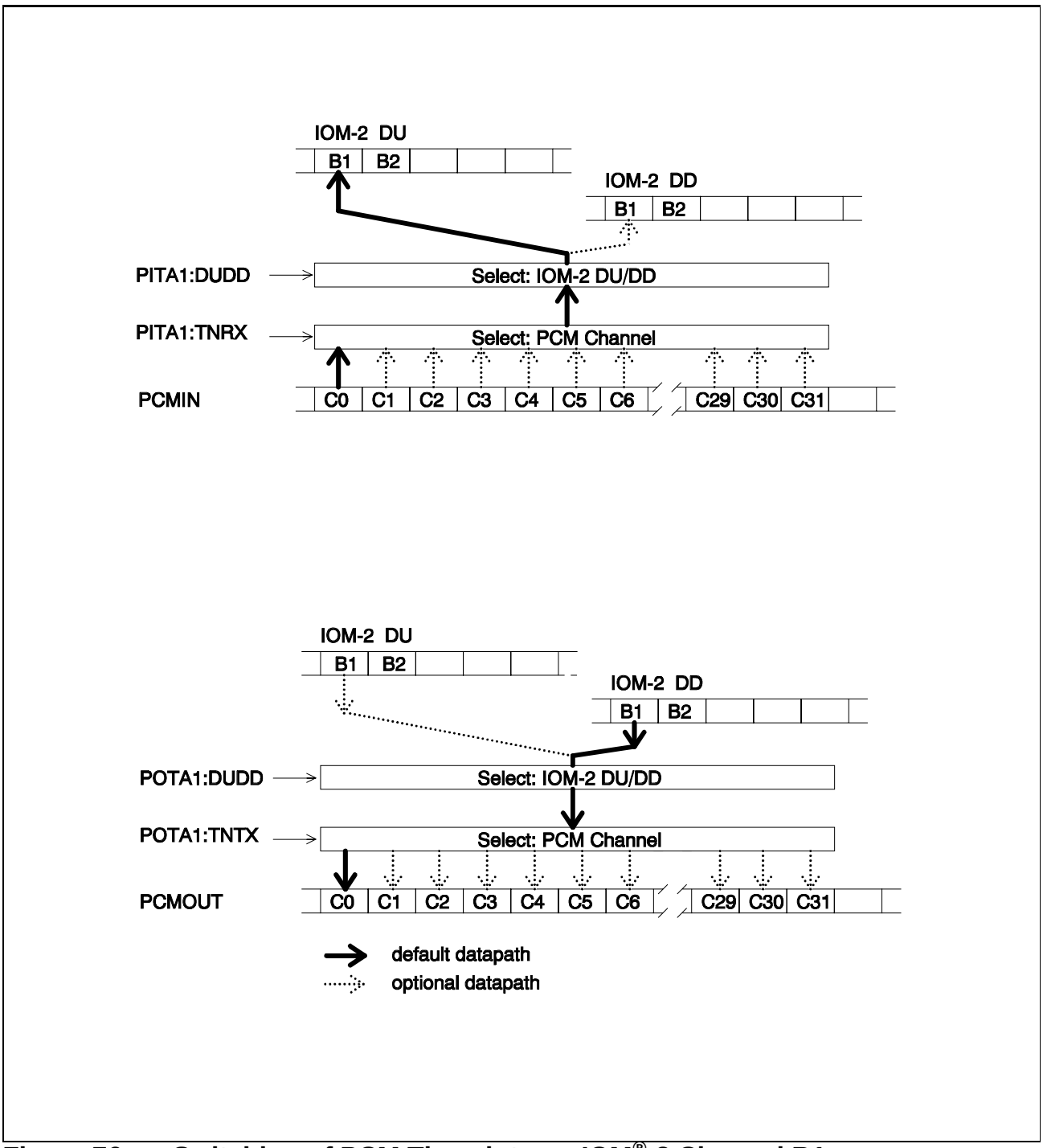


Figure 76 Switching of PCM Timeslots on IOM®-2 Channel B1

PCM Transmit Line - PCMOUT

By default the B-channel from the DD line (POTA1/2:DUDD=0) is connected to the PCM transmit line PCMOUT, so 8-bit data which is received by the IPAC from the S interface on DD (LT-T mode), is transmitted to an external device via the PCM interface.

The B-channel from the DU line (POTA1/2:DUDD=1) can also be switched to the transmit line of the PCM interface PCMOUT. This is necessary in LT-S mode where the direction of IOM-2 data lines is inverted (see **chapter 2.7.2**) or it may be used for test purposes.

B-channel data from DD (default) or DU (optional) is mapped to one of up to 32 (DCL = 4.096 MHz) or 12 (DCL = 1.536 MHz) programmable timeslots (POTA1/2:TNTX) on PCMOUT.

PCM Receive Line - PCMIN

By default the B-channel from the DU line (PITA1/2:DUDD=0) is connected to the PCM receive line PCMIN, so 8-bit data which is received on the PCM interface from an external device is transmitted by the IPAC to the S interface on DU (LT-T mode).

The B-channel from the DD line (PITA1/2:DUDD=0) can also be switched to the receive line of the PCM interface PCMIN. As described above this is used in LT-S mode or for test purposes.

Data from one of up to 32 (DCL = 4.096 MHz) or 12 (DCL = 1.536 MHz) programmable timeslots (PITA1/2:TNRX) on PCMIN is mapped to the B-channel timeslot on DU (default) or DD (optional).

2.9 Oscillator Circuit

The IPAC derives its system clocks from an external clock connected to XTAL1 (while XTAL2 is not connected) or from a 7.68 MHz crystal connected across XTAL1 and XTAL2.

At pin C768 a buffered 7.68 MHz output clock is provided to drive further devices, which is suitable in multiline applications for example (see **figure 77**). This clock is not synchronized to the S-interface.

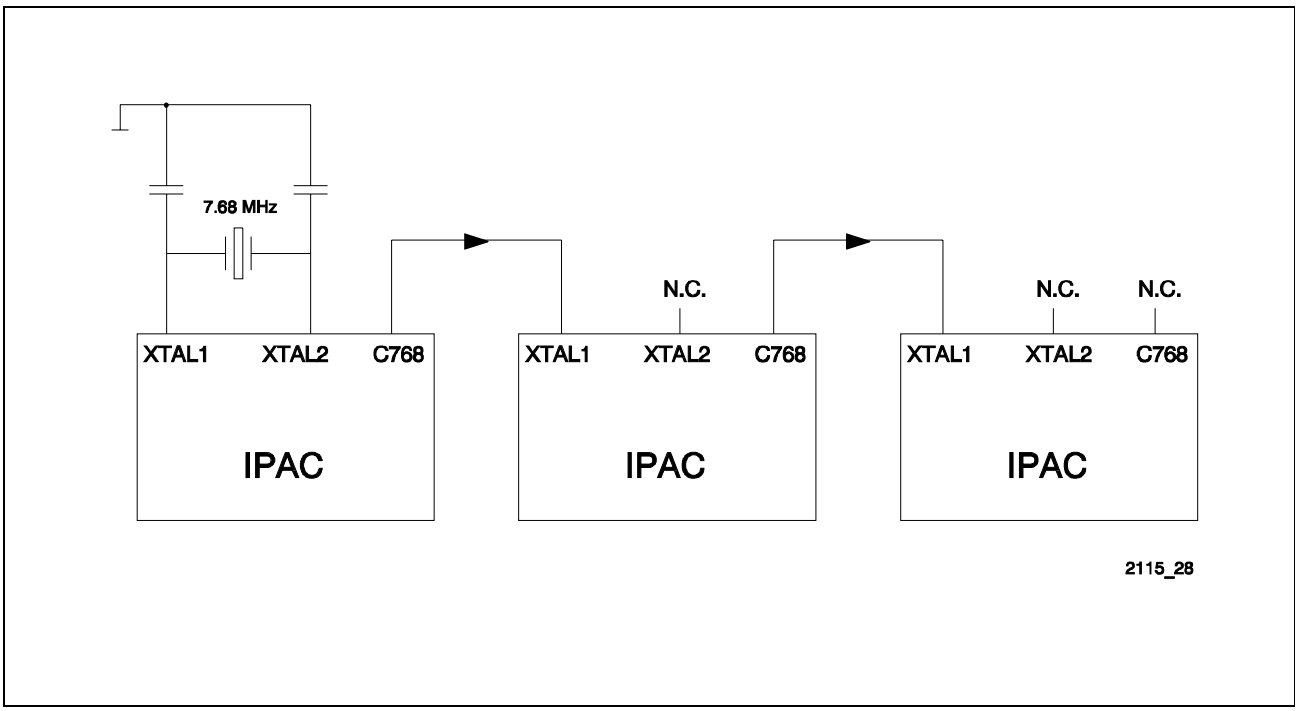


Figure 77 Buffered Oscillator Clock Output

3 Operational Description

3.1 RESET

After a reset the IPAC is in an idle state and its registers are loaded with specific values.

B-Channel registers

The B-Channel related registers are located in the address range 00h - 73h. Their reset values are described in **table 17**.

Table 17 RESET Values for B-Channel Registers

Register	Value after Reset (hex)	Meaning
CCR1	00	– Power down mode – Serial port configuration: NRZ coding – Interframe time fill: idle (’1’) are output on DU
CCR2	00	– Special output control: TX on DU, RX on DD – Transmit data enabled – Receive frame start interrupt enable: RFS disabled
MODEB	00	– Mode select: reserved mode – Address mode: 1 byte address field – Receivers inactive – Continuous frame transmission: delayed XPR interrupt – Receiver active: HDLC receiver inactive – Test loop disabled
STARB	48	– XFIFO write enable – Receive line inactive – No commands executing – Transmitter inactive
ISTAB MASKB EXIRB	00	– No interrupt pending – All interrupts enabled
CMDRB	00	– No commands
XBCH RBCHB	00	– Interrupt controlled data transfer – Transmit continuously disabled
XCCR RCCR	00	– 1-bit time-slot

D-Channel registers

The D-Channel registers are located in the address range 80h - BAh. The important reset values are summarized in **table 18**.

Table 18 RESET Values for D-Channel Registers

Register	Value after Reset (hex)	Meaning
ISTAD	00	– no interrupts
MASKD	00	– all interrupts enabled
EXIRD	00	– no interrupts
STARD	48	– XFIFOD is ready to be written to – RFIFOD is ready to receive at least 16 octets of a new message
CMDRD	00	– no command
MODED	00	– auto mode – 1-octet address field – external timer mode – receiver inactive
RBCLD RBCHD	00 $XXX00000_2$	– no frame bytes received
SPCR	00	– DU pin = “High” – IOM interface test loop deactivated
CIR0	7C	– another device occupies the D and C/I channels – received C/I code = “1111” – no C/I code change
CIX0	3F	– TIC bus is not requested for transmitting a C/I code – transmitted C/I code = “1111”
STCR	00	– terminal specific functions disabled – TIC bus address = “0000” – no synchronous transfer
ADF1	00	– inter-frame time fill = continuous “1”

General IPAC registers

The IPAC registers for general functions are located in the address range C0h - CCh. The reset values are summarized in **table 18**.

Table 19 RESET Values for General IPAC Registers

Register	Value after Reset (hex)	Meaning
CONF	00	– transformer ratio 2:1 – Test mode disabled – D-Channel priority handler disabled – Pin AUX7 is general I/O – DU/DD are open drain – IOM is operational
ISTA	00	– No interrupts
MASK	C0	– INT0/1 masked – All other interrupts enabled
ACFG	00	– AUX2-7 are open drain (as outputs) – $\overline{\text{INT0,1}}$ are negative level triggered (as INT inputs)
AOE	FC	– AUX2-7 are inputs
ATX	00	– Output value for AUX2-7 is 0
PITA1/2	00	– PCMIN line is disabled – RX data from PCMIN mapped to DU line – Selected PCM timeslot is channel 0
POTA1/2	00	– PCMOUT line is disabled – TX data on PCMOUT derived from DD line – Selected PCM timeslot is channel 0
PCFG	00	– $\overline{\text{ACL}}$ will indicate S-bus activation status – AUX3-5 are used for PCM interface (LT modes) – FSC (derived from DCL in) is output on AUX3 (LT modes) – IOM Channel 0 selected for PCM interface (LT modes)
SCFG	00	– 8 bit timeslot length – SDS active during timeslot 0
TIMR2	00	– Count down timer mode – Timer is disabled

3.2 Initialization

After reset the CPU has to write a minimum set of registers and an optionally set dependent on the required features and operating modes.

The CPU may switch the IPAC between power-up and power-down mode, which has no influence upon the contents of the registers, i.e. the internal state remains stored.

In power-down mode however, all internal clocks are disabled, no interrupts are forwarded to the CPU.

This state can be used as standby mode, when the IPAC is temporarily not used, thus minimizing the power consumption.

The individual operating mode must be defined writing the individual MODE register (MODE, MODEB and MODED).

The need for programming further registers depends on the selected features (operating mode, address mode, user demands) according to the following tables:

B-Channel registers

Clock Mode	Register
5 (Time Slot Mode)	CCR2, TSAR, TSAX, XCCR, RCCR

Note: The clock mode 5 is well known from the HSCX-TE PSB 21525, other clock modes are not supported.

Table 20 Register Setup

Address Mode / Operating Mode	2 Byte Address Field (MODEB: ADM = 1)	1 Byte Address Field (MODEB: ADM = 0)
Non Auto	RAH1 RAH2 RAL1 RAL2	RAH1 set to 00_H RAH2 set to 00_H RAL1 RAL2
Transparent	RAH1 RAH2	–

Table 21 User Demand Registers

User Demand	Register
RFS Interrupt Provided	CCR2
Selective Interrupts Should be Masked	MASKB
DMA Controlled Data Transfer	XBCH
Receive Length Check Feature	RLCR
Extended (modulo 128) Counting	RAH2

D-Channel registers

Register	Bit	Effect	Application
SPCR	SPU	Pull DU low (to request clocking from layer-1 device).	TE
	SDL	Switch Data Line IOM-2 data port DU/DD direction control	
	SPM	0 Terminal timing mode 1 Non-terminal timing mode	TE LT
	TLP	IOM-2 interface test loop	
	C2C1-0 C1C1-0	B/IC channel connect	
MODED	DIM2-0	IOM interface configuration for D + C/I channel arbitration Stop/Go bit monitoring for HDLC transmission yes/no	
	MDS2-0	HDLC message transfer mode 2 octet/(1 octet) address	
	TMD	Timer mode external/internal	Auto mode only
ADF1	CSEL2-0	IOM channel select (Time slot)	non-TE

Register	Bit	Effect	Application
CIX0	RSS	Hardware reset generated by either subscriber/exchange awake or watchdog timer	TE specific functions (TSF = 1)
STCR	TSF TBA2-0	Terminal specific function enable TIC bus address	 Bus configuration for D+C/I (TIC)
TIMR	CNT VALUE	N1 and T1 in internal timer mode (TMD = 1) T2 in external timer mode	
XAD1 XAD2		SAPI, TEI Transmit frame address	Auto mode only
SAPI1/2 TEI1/2		Receive SAPI, TEI address values for internal address recognition	

General IPAC registers

Register	Bit	Effect	Application
CONF	ODS	DU/DD output driver selection (open drain or push pull)	
	IOF	IOM interface off or operational	
	IDH	Enable/disable IOM-2 D-Channel priority handler	LT-S mode (intelligent NT)
	CFS	Clock relations and recovery on S/T interface	
	AMP	Transformer ratio	
	TEM	Tests mode (disable layer-1 function)	
	PDS	Select phase deviation of the S-interface.	TE and LT-T mode
	SGO	S/G bit output on pin AUX7	LT-S and LT-T mode
PCFG	PLD	PCM interface enable/disable	LT modes
	CSL2-0	IOM Channel Select for PCM interface	LT modes
	FBS	FSC or BCL output on pin AUX3	LT modes
	ACL	Pin $\overline{\text{ACL}}$ as indication for S-bus activation or as programmable output	all modes
	LED	Output value on $\overline{\text{ACL}}$ (if enabled)	all modes
PITA1/2	ENA	Enable PCMIN channel	PCM interface (LT modes)
	DUDD	Map data on DU/DD	
	TNRX	Timeslot number select	

Register	Bit	Effect	Application
POTA1/2	ENA	Enable PCMOUT channel	PCM interface (LT modes)
	DUDD	Map data on DU/DD	
	TNTX	Timeslot number select	
SCFG	PRI	Priority selection for IOM-2 D-channel priority handler	Data strobe signal
	TLEN	Timeslot length 8/16 bit	
	TSLT	Timeslot position	
TIMR2	TMD	Timer mode (count down or periodic)	Timer 2
	CNT	Timer Count (timer off or 1...63 ms)	
ACFG	OD7-2	Output driver select for AUX7-2 (open drain or push pull)	Aux-interface
	EL1,0	Trigger mode (edge/level) for interrupt input $\overline{\text{INT0,1}}$	
AOE	OE7-2	Switch AUX7-2 as input/output	Aux-interface

3.3 Interrupt Structure and Logic

Special events in the IPAC are indicated by means of a single interrupt output, which requests the host to read status information from the IPAC or transfer data from/to the IPAC.

Since only one $\overline{\text{INT}}$ request output is provided, the cause of an interrupt must be determined by the host reading the IPAC's interrupt status registers.

The structure of the interrupt status registers is shown in **figure 78**.

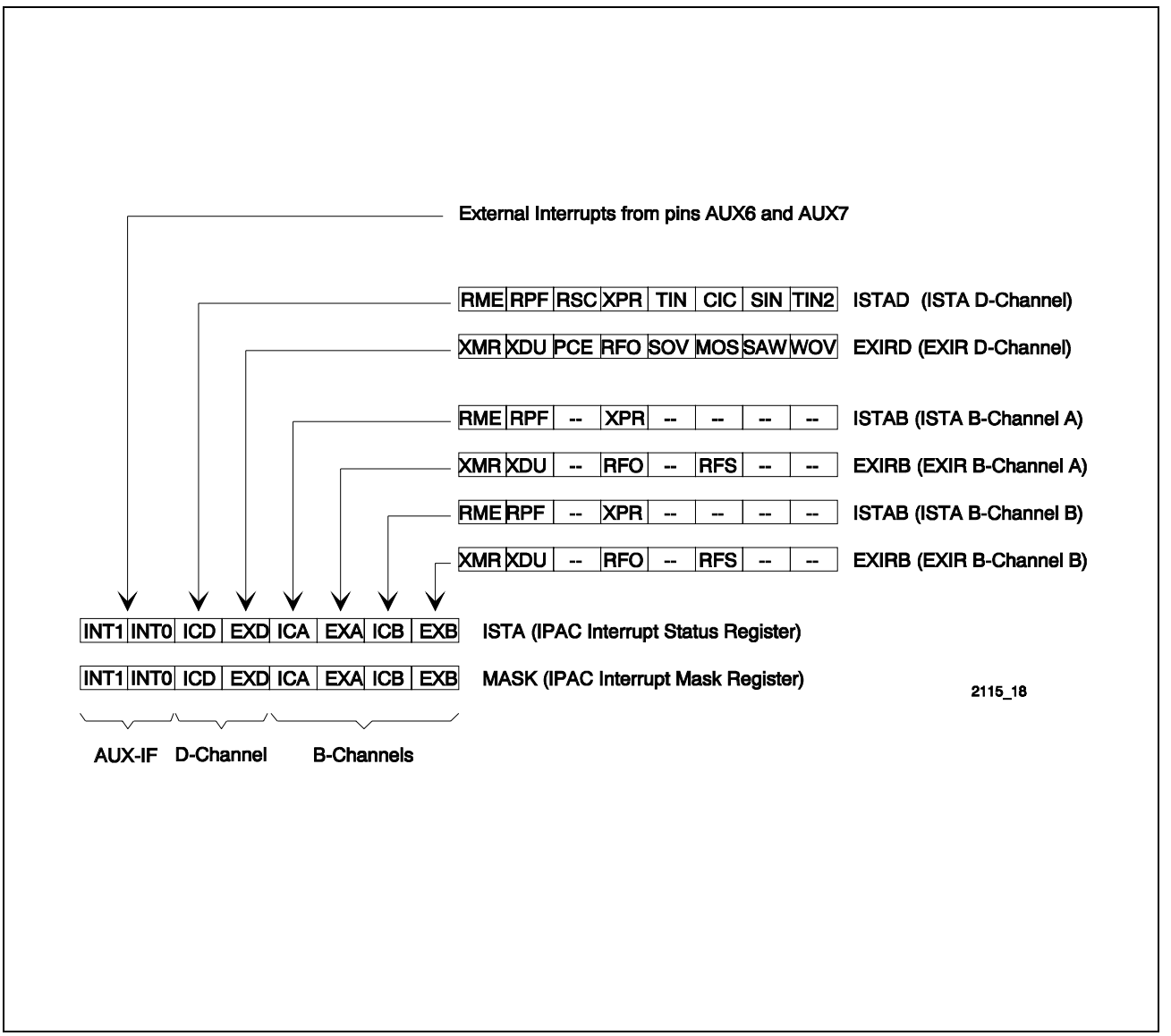


Figure 78 IPAC Interrupt Status Registers

Two interrupt indications can be read directly from the ISTA register and another six interrupt indications from separate interrupt status registers and extended interrupt registers for the B-channels (ISTAB, EXIRB, each for B-Channel A and B) and the D-channel (ISTAD, EXIRD).

After the IPAC has requested an interrupt by setting its $\overline{\text{INT}}$ pin to low, the host must first read the IPAC interrupt status register (ISTA) in the associated interrupt service routine. The six lowest order bits (bit 5-0) of ISTA (IDC, EXD, ICA, EXA, ICB, EXB) point to those registers in which the actual interrupt source is indicated. It is possible that several interrupt sources are indicated referring to one interrupt request (e.g. if the ICA bit is set, at least one interrupt is indicated in the ISTA register of channel A).

An interrupt source from the general I/O pins AUX6 and AUX7 of the auxiliary interface is directly indicated in bits 6 and 7 of the ISTA register, therefore these bits must always be checked (see **chapter 3.3.3**).

Two bits indicate an interrupt source from the D-channel (see **chapter 3.3.2**) and for each of the channels A and B another two bits indicate a source from ISTAB or EXIRB (see **chapter 3.3.1**).

The $\overline{\text{INT}}$ pin of the IPAC remains active until all interrupt sources are cleared by reading the corresponding interrupt register. Therefore it is possible that the $\overline{\text{INT}}$ pin is still active when the interrupt service routine is finished.

For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF_H into the MASK register) and write back the old mask to the MASK register.

Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register.

The ISTA register represents the combined interrupt status from all the individual interrupt status registers (ISTAD, EXIRD, ISTAB, EXIRB). If a specific interrupt source (e.g. ISTAD:RME) is acknowledged by the host the interrupt indication in the ISTA register (in this case ISTA:ICD) is reset, it does not need to be acknowledged by reading ISTA.
In other words, the host does not need to read the ISTA register if it uses some other mechanism to determine the interrupt source. This may be suitable for the adaptation of driver software based on HSCX-TE PSB 21525 and ISAC-S TE PSB 2186 which already implements the subsequent check of all B-channel and D-channel interrupt registers.

3.3.1 B-Channel Interrupts

The B-Channel related interrupt sources can be logically grouped into

– receive interrupts,
– transmit interrupts and
– special condition interrupts.

Each interrupt indication of the ISTAB registers can be selectively masked by setting the respective bit in the MASKB registers.

The following tables give a complete overview of the individual interrupt indications and the cause of their activation as well as specific restrictions (marked with '*').

Table 22 Receive Interrupts

RPF	Receive Pool Full (ISTAB)	Activated as soon as 64-bytes are stored in the RFIFOB but the message is not yet completed.
RME	Receive Message End (ISTAB)	Activated if either one message up to 64 bytes or the last part of a message with more than 64 bytes is stored in the RFIFOB, i.e. after the reception of the CRC and closing flag sequence.
RFO	Receive Frame Overflow (EXIRB)	Activated if a complete frame could not be stored due to occupied RFIFOB, i.e. the RFIFOB is full and the IPAC has detected the start of a new frame.
RFS	Receive Frame Start (EXIRB)	*Only activated if enabled by setting the RIE bit in CCR2 register. Activated after the **start** of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes. After an RFS interrupt, the contents of – RHCRB – RAL1 – RSTAB – bit 3-0 are valid and can be read by the CPU.

Table 23 Transmit Interrupts

XPR	Transmit Pool Ready (ISTAB)	Activated whenever a 64-byte FIFO pool is empty and accessible to the CPU, i.e. – following a XRES command via CMDRB. Repeatedly during frame transmission started by XTF command, and no end of message indication (XME command) has been issued yet by the CPU, – after the end-of-message indication when frame transmission of a transparent frame is completed (i.e. CRC and closing flag sequence are shifted out).
XMR	Transmit Message Repeat (EXIRB)	Transmission of the last frame has to be repeated.
XDU	Transmit Data Underrun (EXIRB)	Activated if the XFIFOB holds no further data, i.e. all data has been shifted out via the serial DU pin, but no End Of Message (EOM) indication has been detected by the IPAC. The EOM indication is supplied by a XME command from the CPU.

3.3.2 D-Channel Interrupts

The cause of an interrupt related to the D-Channel is determined by the microprocessor by reading the Interrupt Status Register ISTAD and the Extended Interrupt Status Register EXIRD.

A read of the ISTAD register clears all bits except CIC. CIC is cleared by reading CIR0. A read of EXIRD clears the EXD bit in ISTA as well as the EXIRD register itself.

Each interrupt source in ISTAD register can be selectively masked by setting to “1” the corresponding bit in MASKD. Masked interrupt status bits are not indicated when ISTAD is read. Instead, they remain internally stored and pending, until the mask bit is reset to zero. Reading the ISTAD while a mask bit is active has no effect on the pending interrupt.

In the event of an extended interrupt EXIRD, EXD is not set when the corresponding mask bit in MASK is active and no interrupt ($\overline{INT}$) is generated. In the event of a C/I channel interrupt CIC is set, even when the corresponding mask bit in MASKD is active, but no interrupt ($\overline{INT}$) is generated.

Except for CIC and MOS all interrupt sources are directly determined by a read of ISTAD and EXIRD.

The FIFO logic, which consists of a 2×32 byte receive FIFO (RFIFOD) and a 2×32 byte transmit FIFO (XFIFOD), as well as an intelligent FIFO controller, builds a flexible interface to the upper protocol layers implemented in the microcontroller.

The interrupt sources from the D-Channel HDLC controller are listed in **table 24**.

Table 24 Interrupts from D-Channel HDLC Controller

Mnemonic	Register	Meaning	Reaction
Layer-2 Receive			
RPF	ISTAD	Receive Pool Full. Request to read received octets of an uncompleted HDLC frame from RFIFOD.	Read 32 octets from RFIFOD and acknowledge with RMC.
RME	ISTAD	Receive Message End. Request to read received octets of a complete HDLC frame (or the last part of a frame) from RFIFOD.	Read RFIFOD (number of octets given by RBCL4-0) and status information and acknowledge with RMC.
RFO	EXIRD	Receive Frame Overflow. A complete frame has been lost because storage space in RFIFOD was not available.	Error report for statistical purposes. Possible cause: deficiency in software.
PCE	EXIRD	Protocol Error. S or I frame with incorrect N(R) or S frame with I field received (in auto mode only).	Link re-establishment. Indication to layer 3.
Layer-2 Transmit			
XPR	ISTAD	Transmit Pool Ready. Further octets of an HDLC frame can be written to XFIFOD. If XIF&XME was issued (auto mode), indicates that the message was successfully acknowledged with S frame.	Write data bytes in the XFIFOD if the frame currently being transmitted is not finished or a new frame is to be transmitted, and issue an XIF, XIF&XME, XTF or XTF&XME command.

Table 24 Interrupts from D-Channel HDLC Controller (cont'd)

Mnemonic	Register	Meaning	Reaction
XMR	EXIRD	Transmit Message Repeat. Frame must be repeated because of a transmission error (all HDLC message transfer modes) or a received negative acknowledgment (auto mode only) from peer station.	Transmission of the frame must be repeated. No indication to layer 3.
XDU	EXIRD	Transmit Data Underrun. Frame has been aborted because the XFIFOD holds no further data and XME (i.e. XIF&XME or XTF&XME) was not issued.	Transmission of the frame must be repeated. Possible cause: excessively long software reaction times.
RSC	ISTAD	Receive Status Change. A status change from peer station has been received (RR or RNR frame), auto mode only.	Stop sending new I frames.
TIN	ISTAD	Timer Interrupt. External timer expired or, in auto mode, internal timer (T200) and repeat counter (N200) both expired.	Link re-established. Indication to layer 3. (Auto mode)
TIN2	ISTAD	Timer Interrupt 2. Timer 2 expired (single interrupt or continuous interrupts with timer period).	No acknowledge necessary. Restart timer if required.

Figure 79 shows the CIC and MOS interrupt logic.

CIC Interrupt Logic

A CIC interrupt may originate

– from a change in received C/I channel (0) code (CIC0)

or (in the case of IOM-2 terminal mode only)

– from a change in received C/I channel 1 code (CIC 1).

The two corresponding status bits CIC0 and CIC1 are read in CIR0 register. CIC1 can be individually disabled by clearing the enable bit CI1E (ADF1 register). In this case the occurrence of a code change in CIR1 will not be displayed by CIC1 until the corresponding enable bit has been set to one.

Bits CIC0 and CIC1 are cleared by a read of CIR0.

An interrupt status is indicated every time a valid new code is loaded in CIR0 or CIR1. But in the case of a code change, the new code is not loaded until the previous contents have been read. When this is done and a second code change has already occurred, a new interrupt is immediately generated and the new code replaces the previous one in the register. The code registers are buffered with a FIFO size of two. Thus, if several consecutive codes are detected, only the first and the last code is obtained at the first and second register read, respectively.

MOS Interrupt Logic

In the case of IOM-2 non-terminal timing modes only one MONITOR channel is handled and MOR1 and MOX1 are unused.

The interrupt logic is different for MONITOR channel 0 and channel 1:

- MONITOR channel 0

The MONITOR Data Receive **MDR0** and the MONITOR channel End of Reception **MER0** interrupt status have two enable bits, MONITOR Receive interrupt Enable (**MRE0**) and MR bit Control (**MRC0**).
The MONITOR channel Data Acknowledged **MDA0** and MONITOR channel Data Abort **MAB0** interrupt status bits have a common enable bit MONITOR Interrupt Enable **MIE0**.

MRE0 prevents the occurrence of **MDR0** status, including when the first byte of a packet is received. When **MRE0** is active (1) but **MRC0** is inactive, the **MDR0** interrupt status is generated only for the first byte of a receive packet. When both **MRE0** and **MRC0** are active, **MDR** is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored. (Additionally, an active **MRC0** enables the control of the MR handshake bit according to the MONITOR channel protocol.)

- MONITOR channel 1

The MONITOR Data Receive interrupt status **MDR1** has two enable bits, MONITOR Receive interrupt Enable (**MRE1**) and MR bit Control (**MRC1**). The MONITOR channel End of Reception **MER1**, MONITOR channel Data Acknowledged **MDA1** and MONITOR channel Data Abort **MAB1** interrupt status bits have a common enable bit MONITOR Interrupt Enable **MIE1**.

MRE1 prevents the occurrence of **MDR1** status, including when the first byte of a packet is received. When **MRE1** is active (1) but **MRC1** is inactive, the **MDR1** interrupt status is generated only for the first byte of a receive packet. When both **MRE1** and **MRC1** are active, **MDR1** is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored. (Additionally, an active **MRC1** enables the control of the MR handshake bit according to the MONITOR channel protocol.)

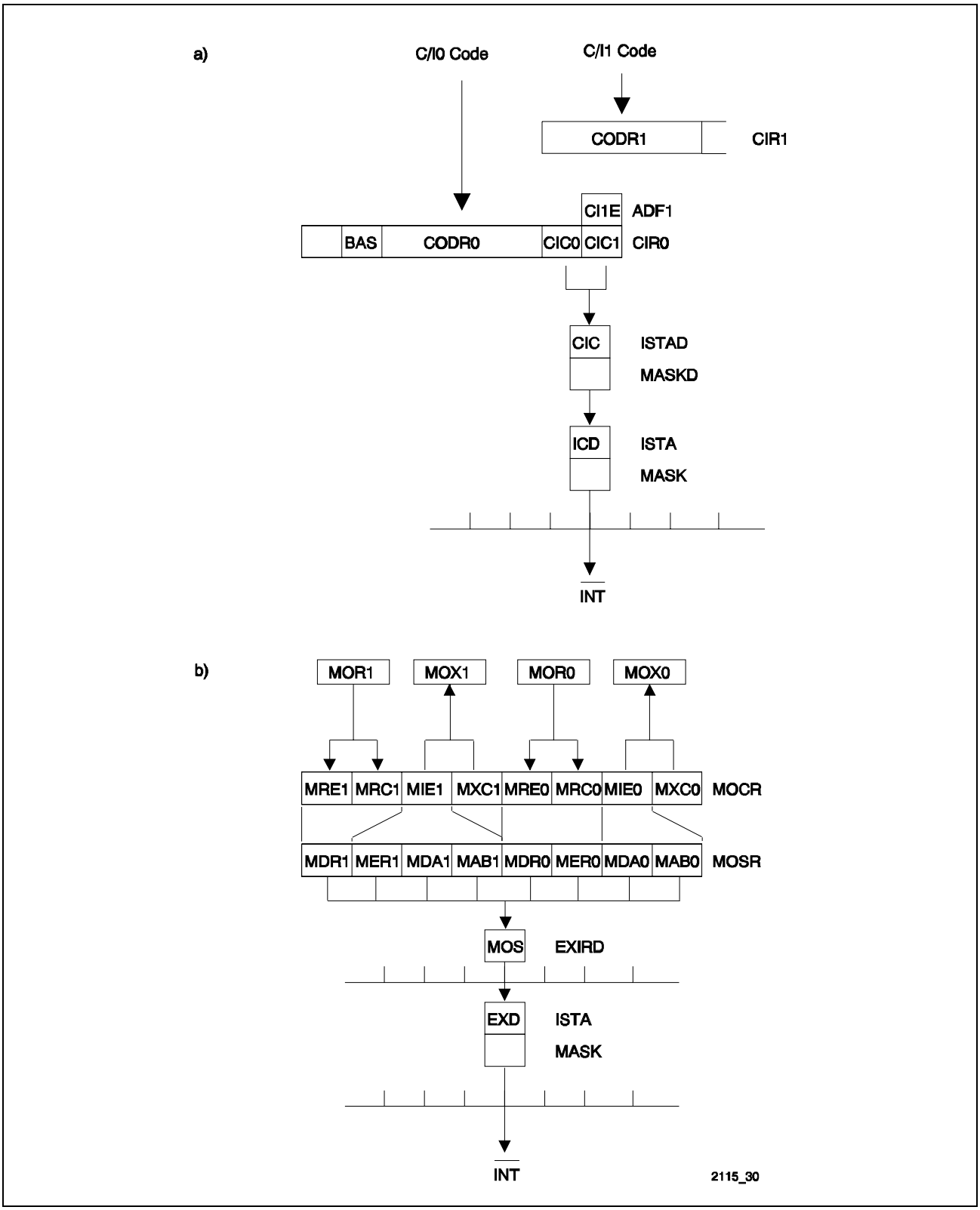


Figure 79 **a) CIC Interrupt Structure**
b) MOS Interrupt Structure

3.3.3 Auxiliary Interface

Interrupts from external devices can be indicated in the Interrupt Status Register (ISTA) of the IPAC.

The auxiliary pins AUX6 and 7 can be configured as general I/O pins and as inputs they can generate a maskable interrupt to the host (INT0, 1). The host can configure whether the interrupt on these pins is edge or level triggered.

In contrast to all other interrupt sources in the ISTA register, INT0 and INT1 are masked (MASK register) after reset.

Table 25 Auxiliary Interface Interrupts

Mnemonic	Register	Meaning	Reaction
INT0/1	ISTA	External Interrupt 0/1 Activated if a negative edge or level (programmable in ACFG:EL0/1) is detected on auxiliary pins AUX6/7.	Service interrupt from external device(s).

3.4 B-Channel Data Transfer

Initially, the CPU should bring the transmitter and receiver to a defined state by issuing a XRES (transmitter reset) and RHR (receiver reset) command via the CMDRB register. If data reception should be performed, the receiver must be activated by setting the RAC bit in MODEB to 1.

After having performed the initialization, the CPU switches each individual B-channel of the IPAC into operational phase by setting the PU bit in the CCR1 register (power-up).

Now the IPAC is ready to transmit and receive B-Channel data. The control of the data transfer phase is mainly done by commands from CPU to IPAC via the CMDRB register, and by interrupt indications from IPAC to CPU.

Additional status information, which does not trigger an interrupt, is available in the STARB register.

3.4.1 Data Transmission

Interrupt Mode

In transmit direction 2×64 byte FIFO buffers (transmit pools) are provided for each channel. After checking the XFIFOB status by polling the Transmit FIFO Write Enable bit (XFW in STARB register) or after a Transmit Pool Ready (XPR) interrupt, up to 64 bytes may be entered by the CPU to the XFIFOB.

The transmission of a frame can then be started issuing a XTF command via the CMDRB register. If the transmit command does not include an end of message indication (CMDRB : XME), the IPAC will repeatedly request for the next data block by means of a XPR interrupt as soon as no more than 64 bytes are stored in the XFIFOB, i.e. a 64-byte pool is accessible to the CPU.

This process will be repeated until the CPU indicates the end of message per command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence.

In case no more data is available in the XFIFOB prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt (EXIRB : XDU). The frame may also be aborted per software (CMDRB : XRES).

The data transmission sequence, from the CPU's point of view, is outlined in **figure 80**.

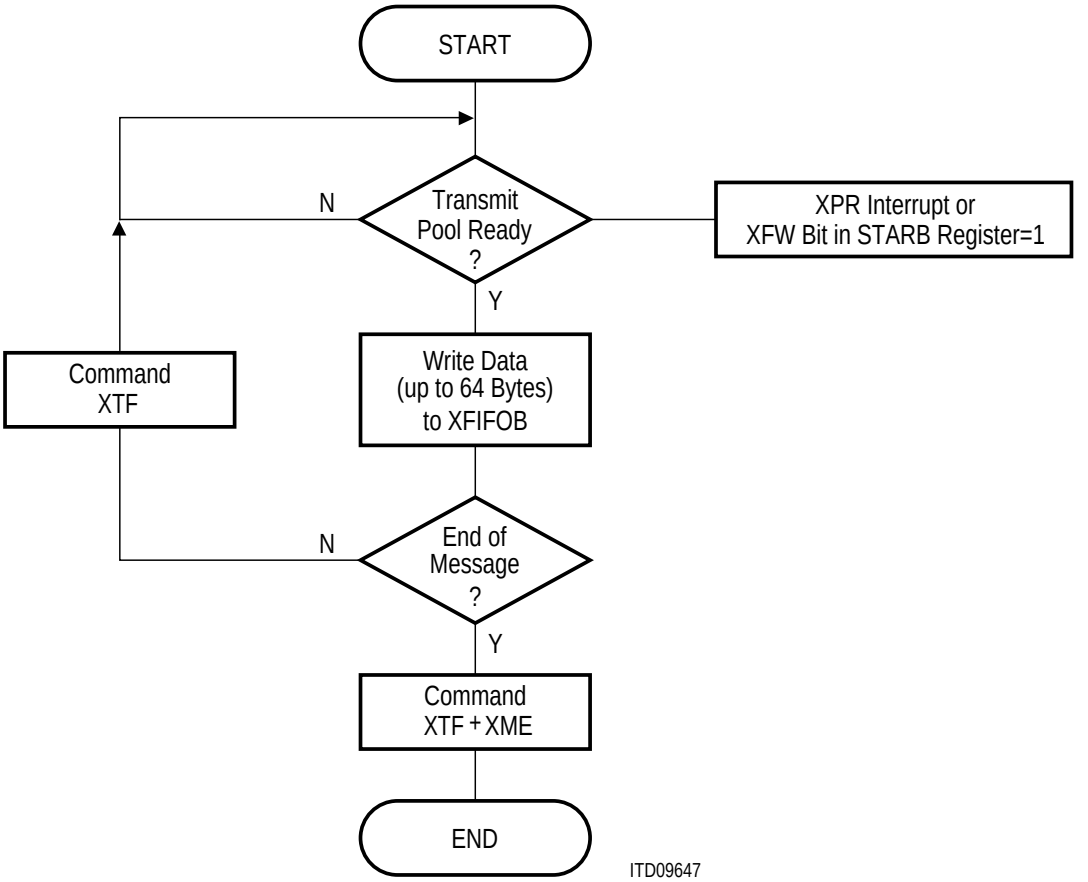


Figure 80 Interrupt Driven Data Transmission (Flow Diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 140 bytes) is shown in **figure 81**.

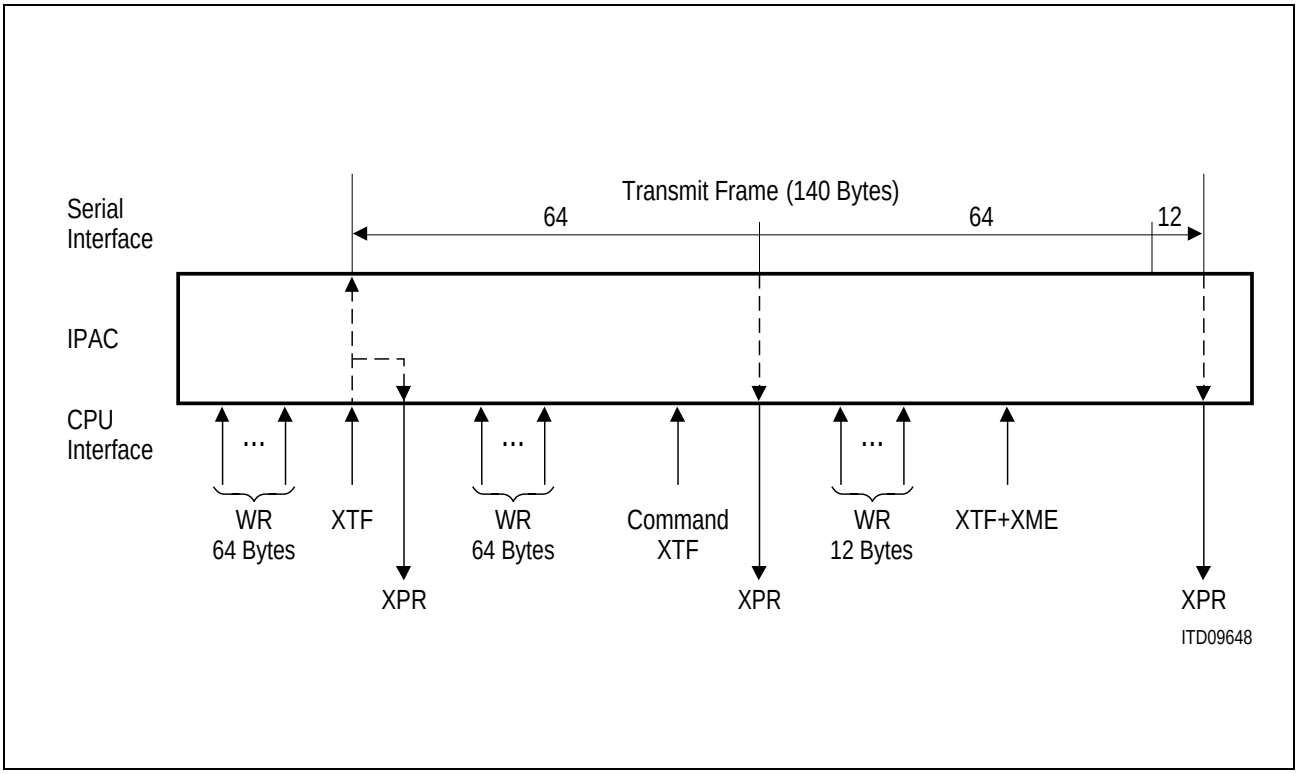


Figure 81 Interrupt Driven Transmission Sequence Example

Back to Back Frames

If two or more frames should be transmitted in a high speed sequence without interframe time fill, the transmission sequence according **figure 82** has to be used.

This means that the closing flag will be immediately followed by an opening flag. The IPAC receiver, however, is capable of receiving frames separated by only one (shared) flag.

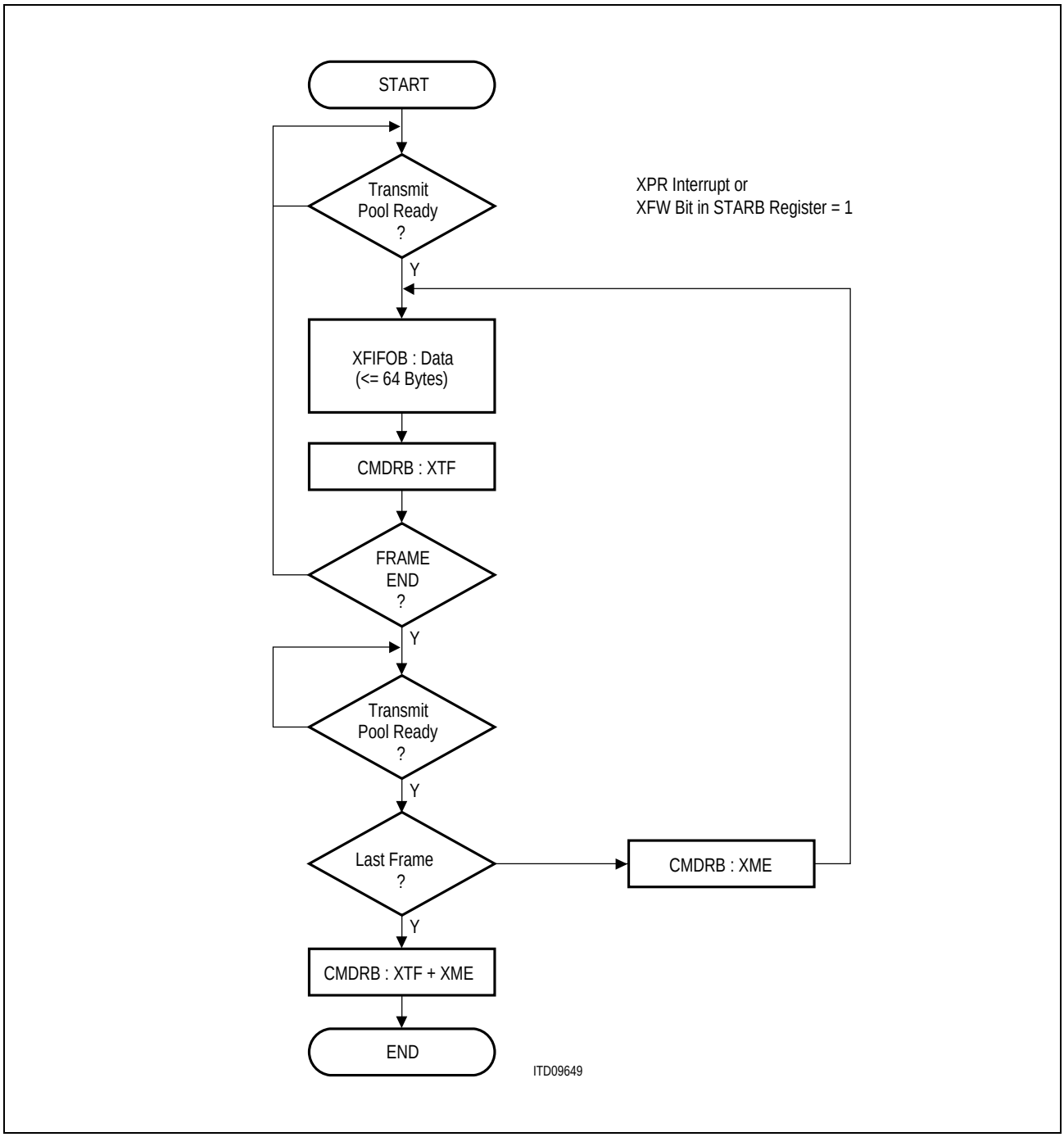


Figure 82 Continuous Frames Transmission (Flow Diagram)

The activities during frame transmission (supposed two frames, 36 bytes and 104 bytes) is shown in **figure 83**.

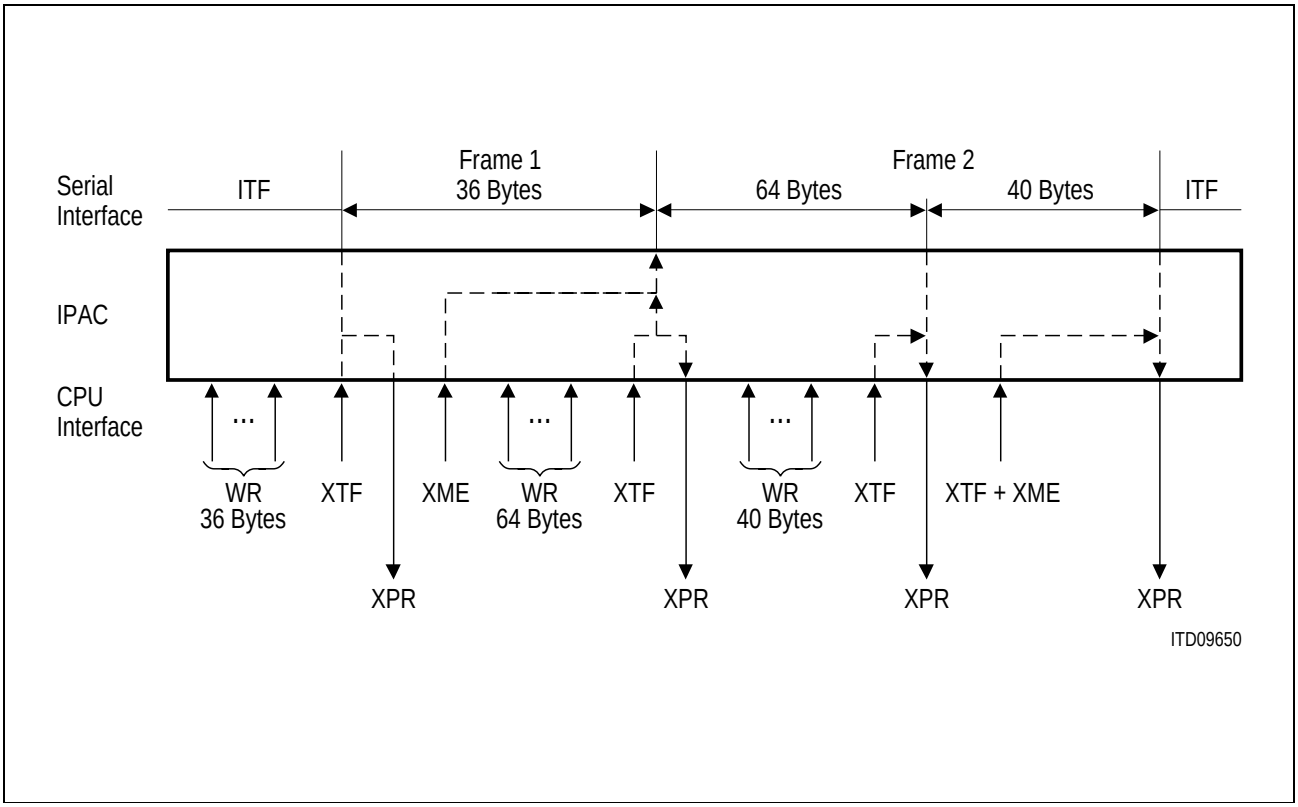


Figure 83 Continuous Frames Transmission Sequence Example

DMA Mode

Prior to data transmission, the length of the next frame to be transmitted must be programmed via the Transmit Byte Count Registers (XBCH, XBCL). The resulting byte count equals the programmed value plus one byte, i.e. since 12 bits are provided via XBCH, XBCL (XBC11. . .XBC0) a frame length of 1 up to 4096 bytes (4 Kbytes) can be selected.

After this, data transmission can be initiated by command (XTF). The IPAC will then autonomously request the correct amount of write bus cycles by activating the DRQTA/B line. Depending on the programmed frame length, block data transfers of

$n \times$ 64-bytes + remainder (n = 0, 1,…64)

are requested everytime a 64-byte FIFO half (transmit pool) is empty and accessible to the DMA controller.

The following figure gives an example of a DMA driven transmission sequence with a supposed frame length of 140 bytes, i.e. programmed transmit byte count (XCNT) equal 139 bytes.

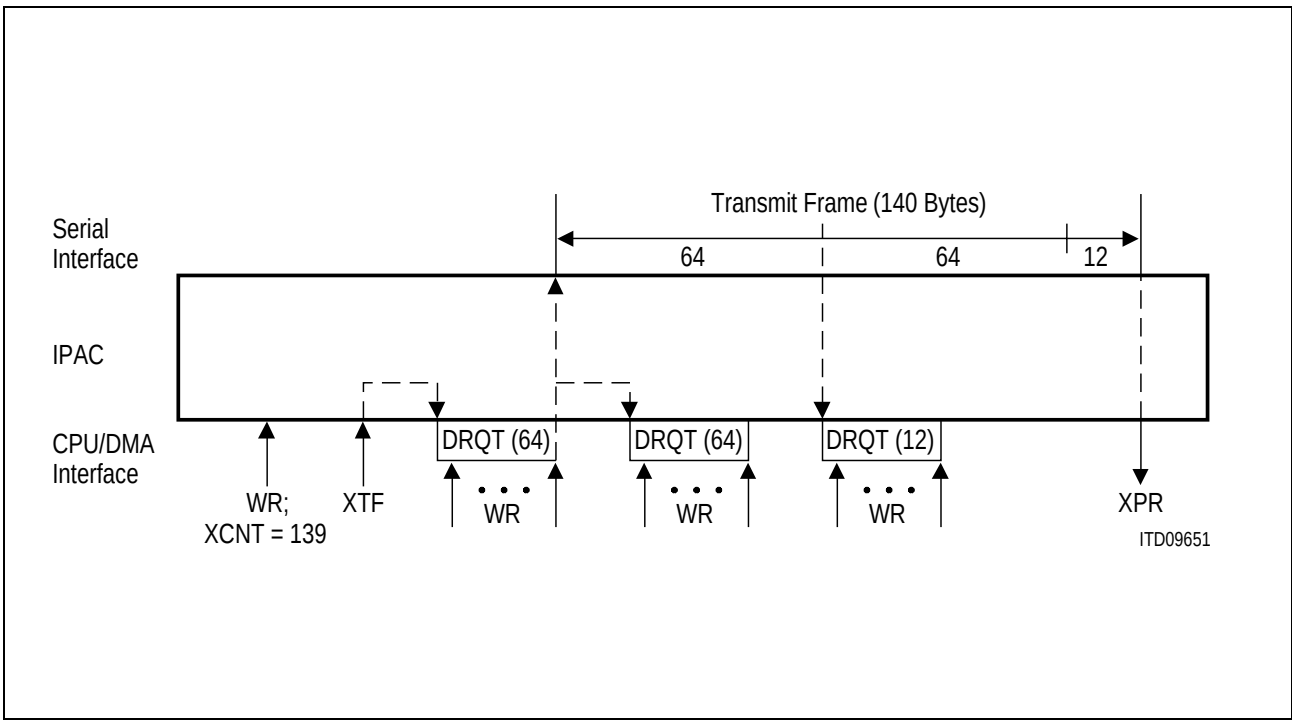


Figure 84 DMA Driven Transmission Sequence Example

3.4.2 Data Reception

Interrupt Mode

Also 2 × 64 byte FIFO buffers (receive pools) are provided for each channel in receive direction.

There are two different interrupt indications concerned with the reception of data:

- RPF (Receive Pool Full) interrupt, indicating that a 64 byte block of data can be read from the RFIFOB and the received message is not yet complete.
- RME (Receive Message End) interrupt, indicating that the reception of one message is completed, i.e. either
  - one message with less than 64 bytes, or the
  - last part of a message with more than 64 bytes

is stored in the RFIFOB.

After an interrupt has been processed, i.e. the received data has been read from the RFIFOB, this must be explicitly acknowledged by the CPU issuing a RMC (Receive Message Complete) command.

The CPU has to handle the RPF interrupt before additional 64 bytes are received via the serial interface which would cause a ‘Receive Data Overflow’ condition.

In addition to the message end (RME) interrupt, the following information about the received frame is stored by the IPAC in special registers and/or RFIFOB:

Table 26 Status Information after RME Interrupt

Length of message (bytes) →	RBCHB, RBCLB	Register
Address combination and/or →	RSTAB	RFIFOB: last byte
Address field →	RAL1	RFIFOB
Control field →	RHCRB	RFIFOB
Type of frame (COMMAND/RESPONSE) →	RSTAB	RFIFOB: last byte
CRC result (good/bad) →	RSTAB	RFIFOB: last byte
Valid frame (yes/no) →	RSTAB	RFIFOB: last byte
ABORT sequence recognized (yes/no) →	RSTAB	RFIFOB: last byte
Data overflow →	RSTAB	RFIFOB: last byte

The following figure gives an example of an interrupt controlled reception sequence, supposed that a long frame (132 bytes) followed by two short frames (12 bytes each) are received.

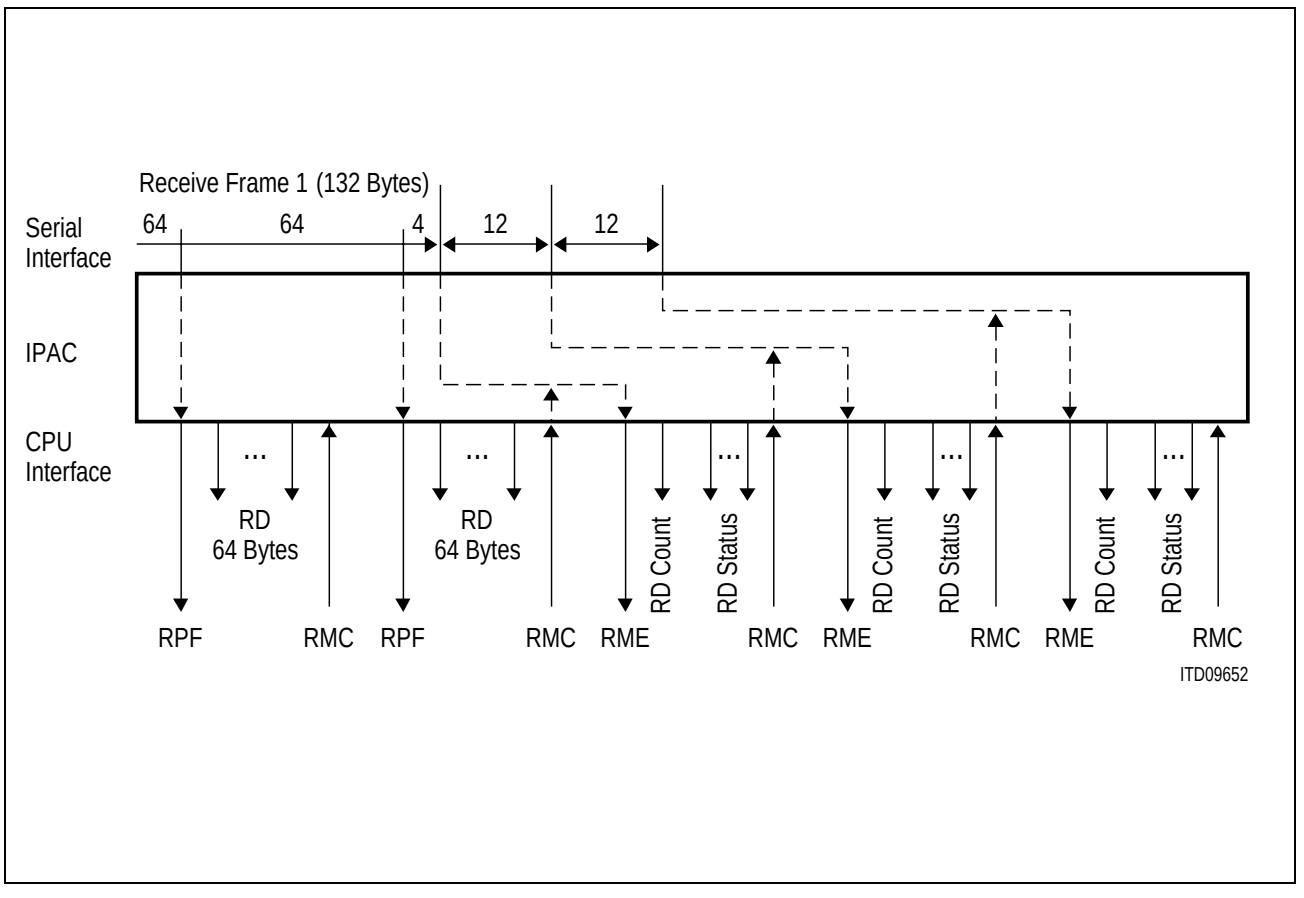


Figure 85 Interrupt Driven Reception Sequence Example

DMA Mode

If the RFIFOB contains 64 bytes, the IPAC autonomously requests a block data transfer by DMA activating the DRQRA/B line as long as the start of the 64th read cycle. This forces the DMA controller to continuously perform bus cycles till 64 bytes are transferred from the IPAC to the system memory.

If the RFIFOB contains less than 64 bytes (one short frame or the last part of a long frame) the IPAC requests a block data transfer depending on the contents of the RFIFOB according to the following table:

RFIFOB Contents (No. of bytes)	DMA Request (No. of Bytes)
1, 2, 3	4
4 - 7	8
8 - 15	16
16 - 31	32
32 - 64	64

Note: All available status informations after RME are summarized in ***table 11.***

After the DMA controller has been set up for the reception of the next frame, the CPU must be issue a RMC command to acknowledge the completion of the receive frame processing.

The IPAC will not initiate further DMA cycles by activating the DRQRA/B line prior to the reception of RMC.

Note: It's also possible to set up the DMA controller immediately after the start of a frame has been detected using the IPAC's RFS (Receive Frame Start) interrupt option.

The following figure gives an example of a DMA controlled reception sequence, supposed that a long frame (132 bytes) followed by one short frame (12 bytes) is received.

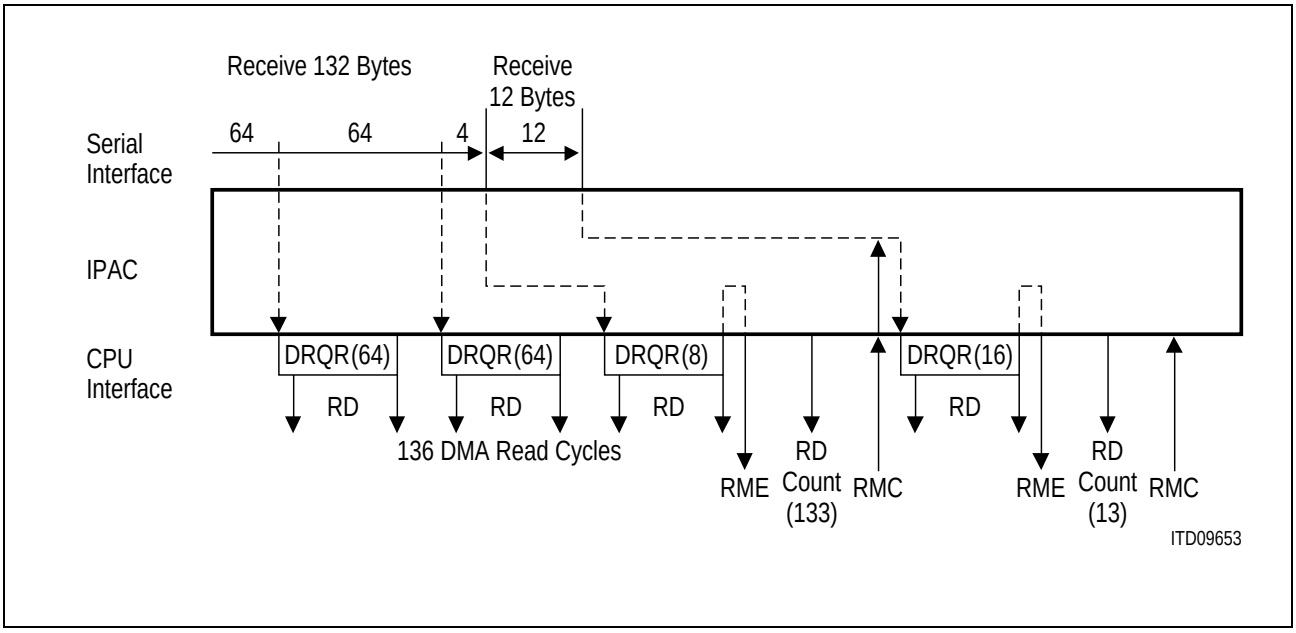


Figure 86 DMA Driven Reception Sequence Example

3.5 D-Channel Data Transfer

3.5.1 HDLC Frame Transmission

After the XFIFOD status has been checked by polling the Transmit FIFO Write Enable (XFW) bit or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be entered in XFIFOD. Transmission of an HDLC frame is started when a transmit command is issued. The opening flag is generated automatically. In the case of an auto mode transmission (XIF or XIFC), the control field is also generated by the IPAC, and the contents of register XAD1 (and XAD2 for LAPD) are transmitted as the address, as shown in **figure 87**.

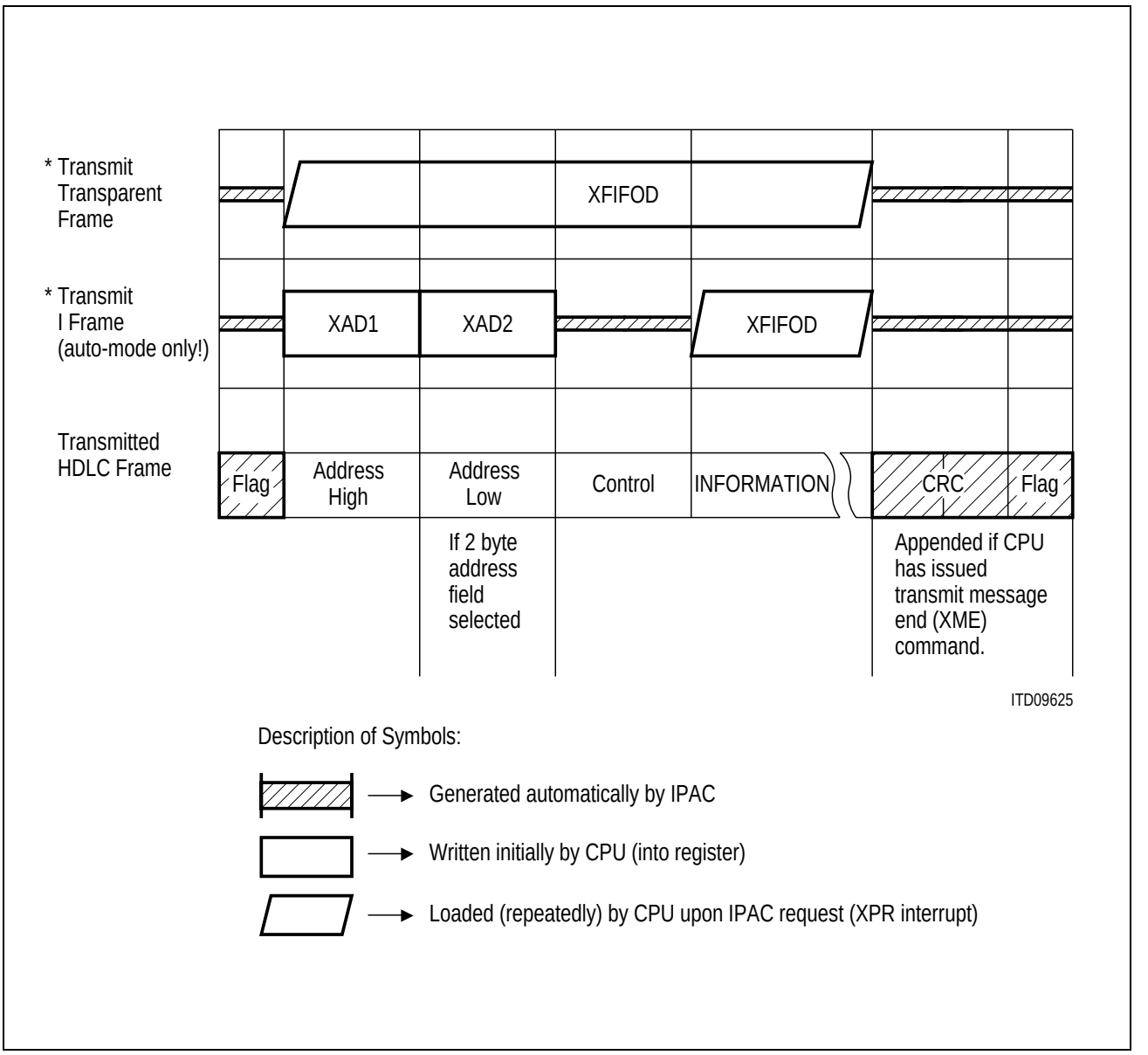


Figure 87 Transmit Data Flow

The HDLC controller will request another data block by an XPR interrupt if there are no more than 32 bytes in XFIFOD and the frame close command bit (Transmit Message End XME) has not been set. To this the microcontroller responds by writing another pool of data and re-issuing a transmit command for that pool. When XME is set, all remaining bytes in XFIFOD are transmitted, the CRC field and the closing flag of the HDLC frame are appended and the controller generates a new XPR interrupt.

The microcontroller does not necessarily have to transfer a frame in blocks of 32 bytes. As a matter of fact, the sub-blocks issued by the microcontroller and separated by a transmit command, can be between 0 and 32 bytes long.

If the XFIFOD runs out of data and the XME command bit has not been set, the frame will be terminated with an abort sequence (seven 1’s) followed by inter-frame time fill, and the microcontroller will be advised by a Transmit Data Underrun (XDU) interrupt. An HDLC frame may also be aborted by setting the Transmitter Reset (XRES) command bit.

3.5.2 HDLC Frame Reception

Assuming a normal running communication link (layer 1 activated, layer 2 link established), **figure 88** illustrates the transfer of an I frame. The transmitter is shown on the left and the receiver on the right, with the interaction between the microcontroller system and the IPAC in terms of interrupt and command stimuli.

When the frame (excluding the CRC field) is not longer than 32 bytes, the whole frame is transferred in one block. The reception of the frame is reported via the Receive Message End (RME) interrupt. The number of bytes stored in RFIFOD can be read out from RBCLD. The Receive Status Register (RSTAD) includes information about the frame, such as frame aborted yes/no or CRC valid yes/no and, if complete or partial address recognition is selected, the identification of the frame address.

Depending on the HDLC message transfer mode, the address and control field of the frame can be read from auxiliary registers (SAPR and RHCRD), as shown in **figure 89**.

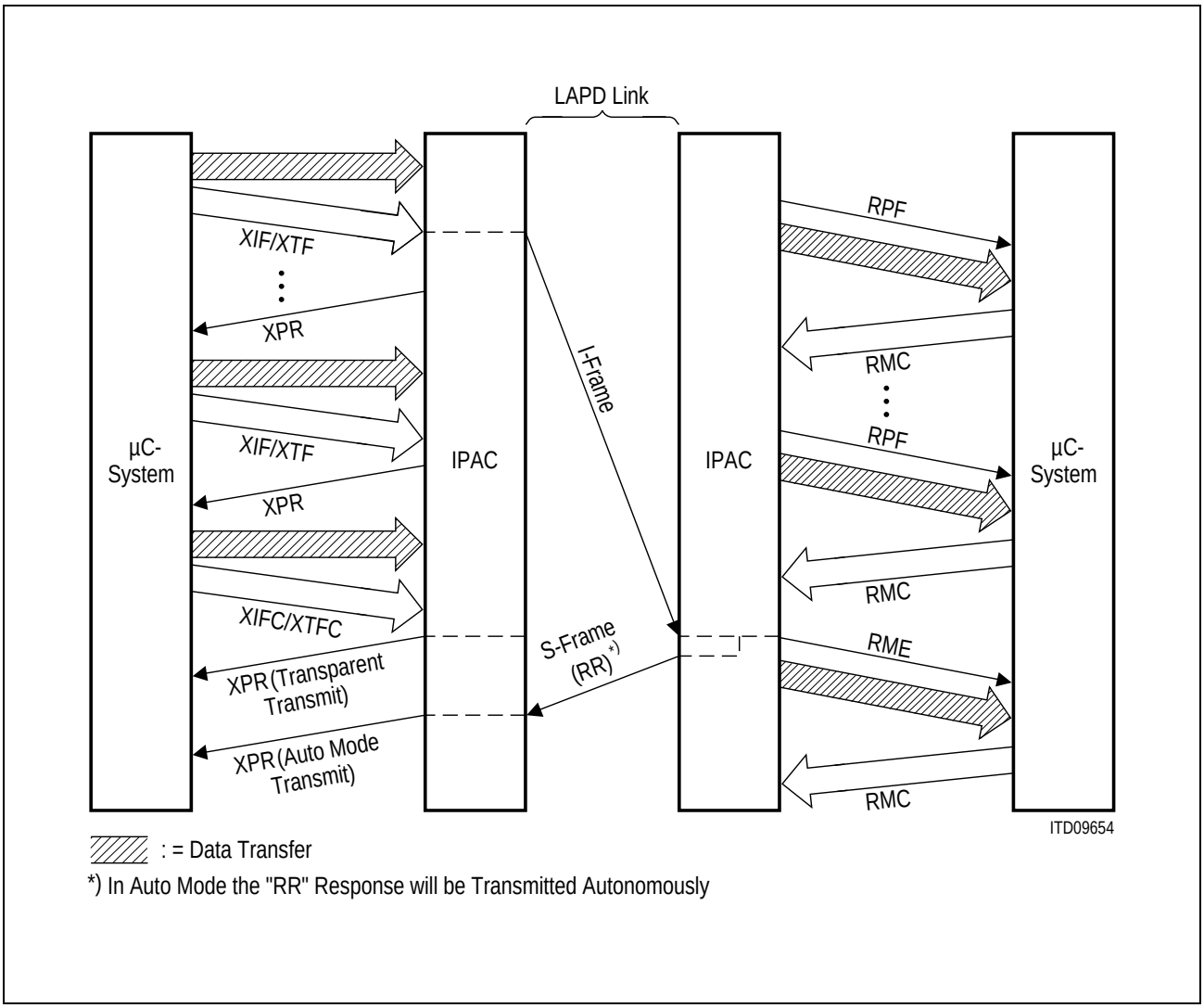


Figure 88 Transmission of an I Frame in the D Channel (Subscriber to Exchange)

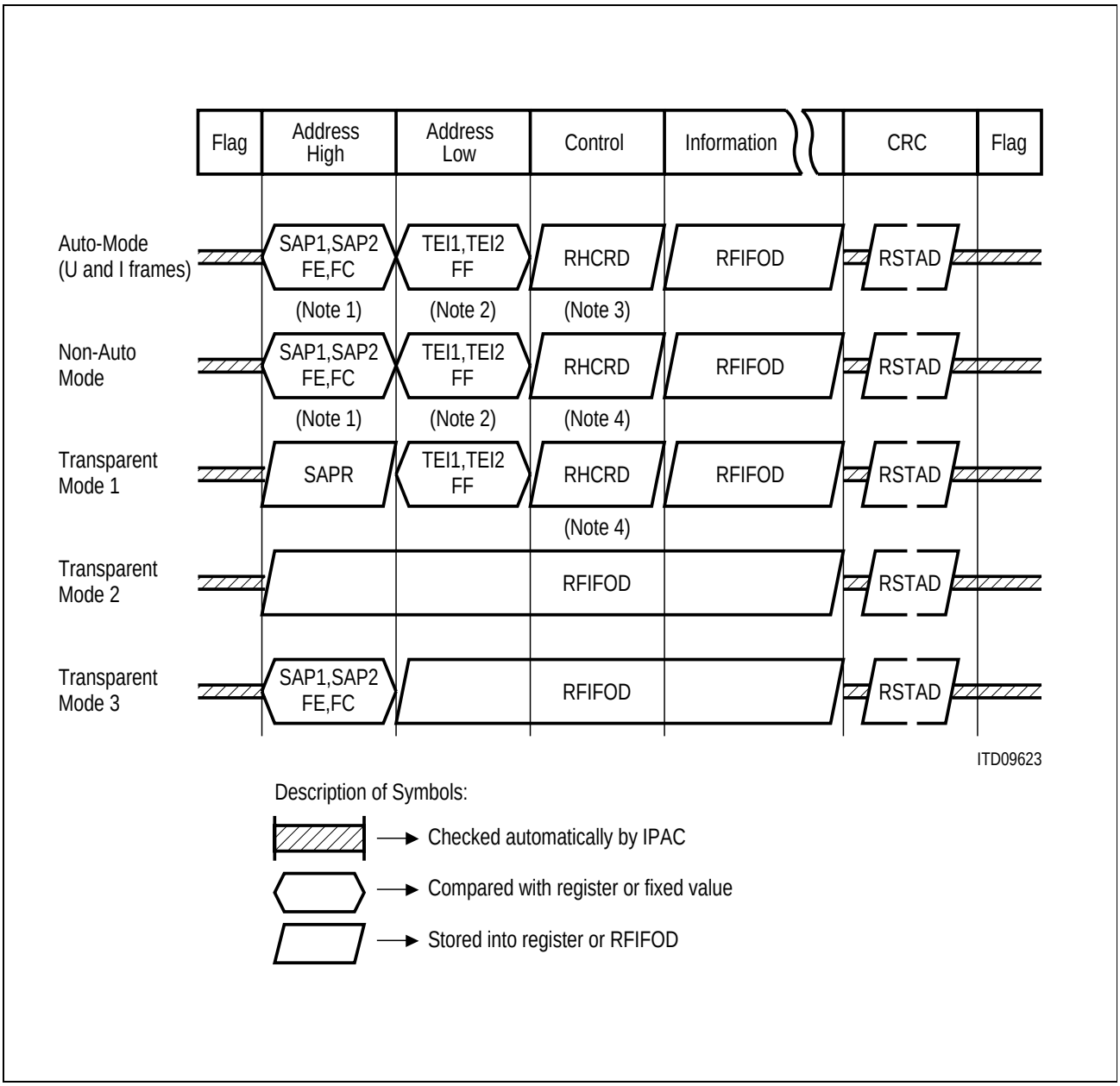


Figure 89 Receive Data Flow

Note 1: Only if a 2-byte address field is defined (MDS0 = 1 in MODED register).

Note 2: Comparison with group TEI (FFH) is only made if a 2-byte address field is defined MDS0 = 1 in MODED register).

Note 3: In the case of an extended, modulo 128 control field format (MCS = 1 in SAP2 register) the control field is stored in RHCRD in compressed form (I frames).

Note 4: In the case of extended control field, only the first byte is stored in RHCRD, the second in RFIFOD.

A frame longer than 32 bytes is transferred to the microcontroller in blocks of 32 bytes plus one remainder of length 1 to 32 bytes. The reception of a 32-byte block is reported by a Receive Pool Full (RPF) interrupt and the data in RFIFOD remains valid until this interrupt is acknowledged (RMC). This process is repeated until the reception of the remainder block is completed, as reported by RME (**figure 88**). If the second RFIFOD pool has been filled or an end-of frame is received while a previous RPF or RME interrupt is not yet acknowledged by RMC, the corresponding interrupt will be generated only when RMC has been issued. When RME has been indicated, bits 0-4 of the RBCLD register represent the number of bytes stored in the RFIFOD. Bits 7 to 5 of RBCLD and bits 0 to 3 of RBCHD indicate the total number of 32-byte blocks which where stored until the reception of the remainder block. When the total frame length exceeds 4095 bytes, bit OV (RBCHD) is set but the counter is not blocked.

The contents of RBCLD, RBCHD and RSTAD registers are valid only after the occurrence of the RME interrupt, and remain valid until the microprocessor issues an acknowledgment (RMC). The contents of RHCRD and/or SAPR, also remain valid until acknowledgment.

If a frame could not be stored due to a full RFIFOD, the microcontroller is informed of this via the Receive Frame Overflow interrupt (RFO).

3.6 Control of Layer-1

3.6.1 Activation/Deactivation of IOM®-2 Interface

In LT-T and LT-S applications the IOM interface should be kept active, i.e. the clock DCL and the frame sync FSC (inputs) should always be supplied by the system.

In TE applications the IOM-2 interface can be switched off in the inactive state, reducing power consumption to a minimum. In this deactivated state the clock line is low and the data lines are high.

In TE mode the IOM-2 interface can be kept active while the S interface is deactivated by setting the CFS bit to "0" (CONF register). This is the case after a hardware reset. If the IOM-2 interface should be switched off while the S interface is deactivated, the CFS bit should be set to "1". In this case the internal oscillator is disabled when no signal (info 0) is present on the S bus and the C/I command is ’1111’ = DIU (refer to **chapter 3.6.2**). If the TE wants to activate the line, it has first to activate the IOM-2 interface either by using the "Software Power Up" function (SPCR:SPU bit) or by setting the CFS bit to "0" again.

For the TE case the deactivation procedure is shown in **figure 90**. After detecting the code DIU (Deactivate Indication Upstream) the layer 1 of the IPAC responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I (C/I0) channel bit of the fourth frame.

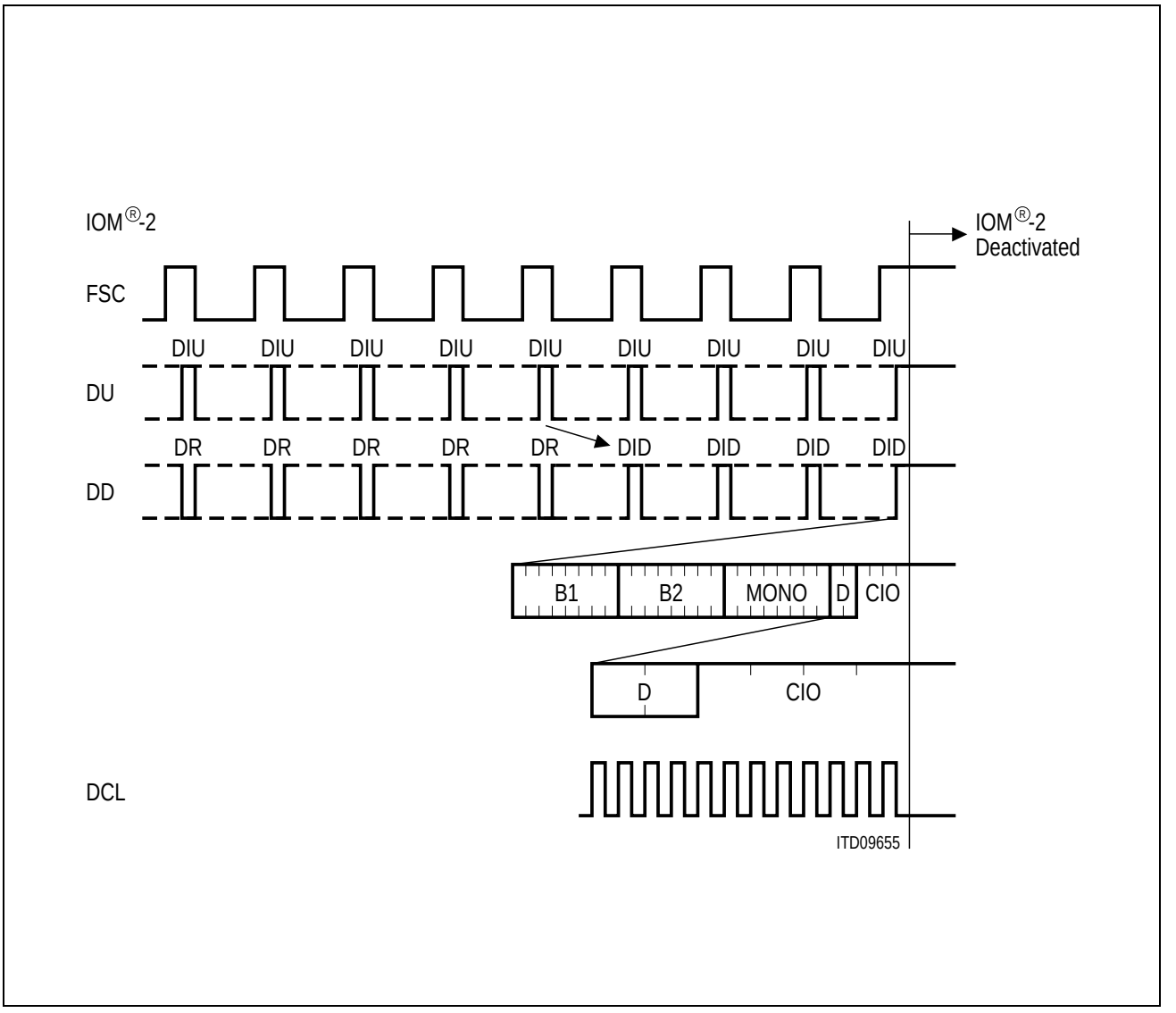


Figure 90 Deactivation of the IOM® Interface

The clock pulses will be enabled again when the DU line is pulled low (bit SPU, SPCR register) i.e. the C/I command TIM = "0000" is received by layer 1, or when a non-zero level on the S-line interface is detected. The clocks are turned on after approximately 0.2 to 4 ms depending on the capacitances on XTAL 1/2.

DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I (C/I0) channel.

After the clocks have been enabled this is indicated by the PU code in the C/I channel and, consequently, by a CIC interrupt. The DU line may be released by resetting the Software Power Up bit SPCR:SPU=0, and the C/I code written to CIX0 before (e.g. TIM or AR8) is output on DU.

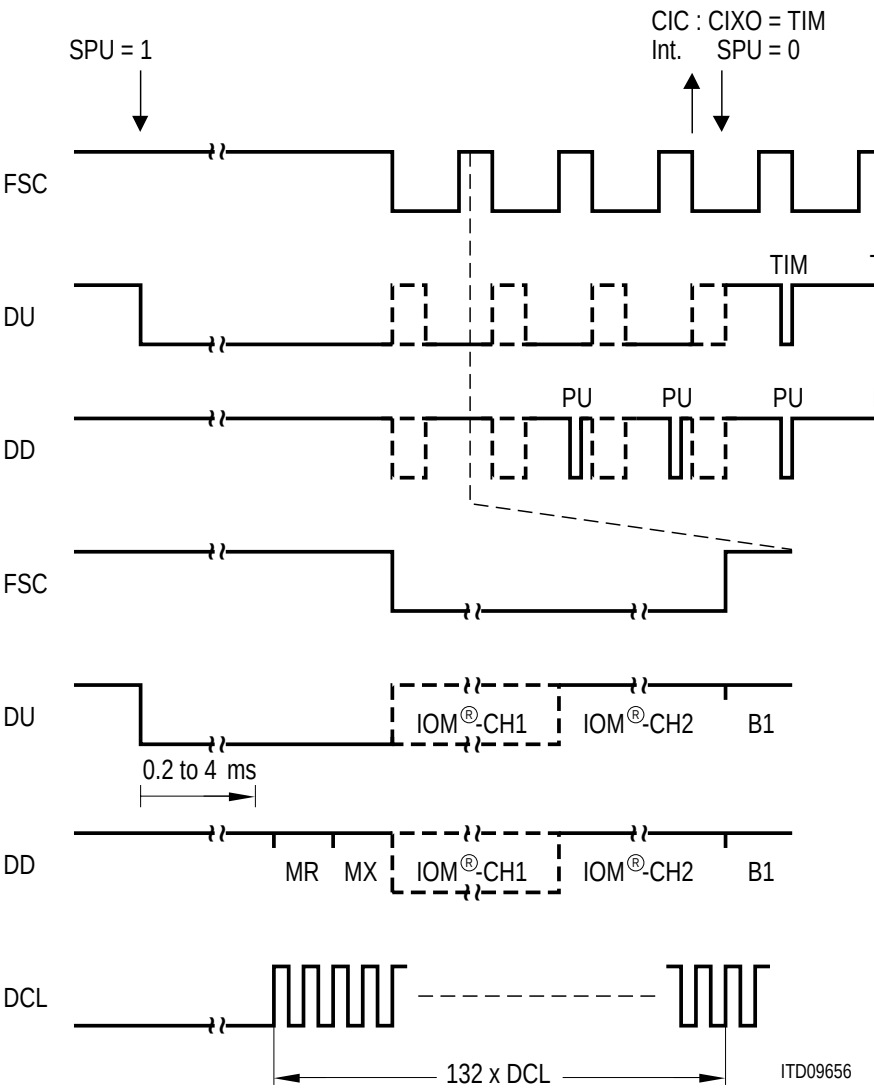


Figure 91 Activation of the IOM® interface

The IPAC supplies IOM timing signals as long as there is no DIU command in the C/I (C/I0) channel. If timing signals are no longer required and activation is not yet requested, this is indicated by programming DIU in the CIX0 register.

As an alternative to activation via DU, the IOM interface can be activated by setting the CFS bit to "0". The activation of FSC and DCL in this case is similar to **figure 91**. Note that the IOM interface can be deactivated through DIU (power-down state, **figure 90**) only if CFS is set to logical "1".

3.6.2 Activation/Deactivation of S/T Interface

Assuming the IPAC has been initialized with the required features of the application, it is now ready to transmit and receive messages in the D channel (LAPD support).

But as a prerequisite, the layer 1 has to be activated.

The layer-1 functions are controlled by commands issued via the CIX0 register. These commands, sent over the IOM C/I channel 0 to layer 1, trigger certain procedures, such as activation/deactivation, switching of test loops and transmission of special pulse patterns. These are governed by layer-1 state diagrams in accordance with ITU I.430. Responses from layer 1 are obtained by reading the CIR0 register after a CIC interrupt (ISTAD).

The state diagrams are shown in the following figures. The activation/deactivation implemented by the IPAC in its different operating modes agrees with the requirements set forth in ITU recommendations. State identifiers F1-F8 (TE/LT-T) and G1-4 (LT-S) are in accordance with ITU I.430.

State machines are the key to understanding the IPAC in different operational modes. They include all information relevant to the user and enable him to understand and predict the behaviour of the IPAC. The informations contained in the state diagrams are:

– state name (based on ITU I.430)
– S/T signal transmitted
– C/I code received
– C/I code transmitted
– transition criteria

The coding of the C/I commands and indications are described in detail in **chapter 3.6.6**.

It is essential to be able to interpret the state diagrams.

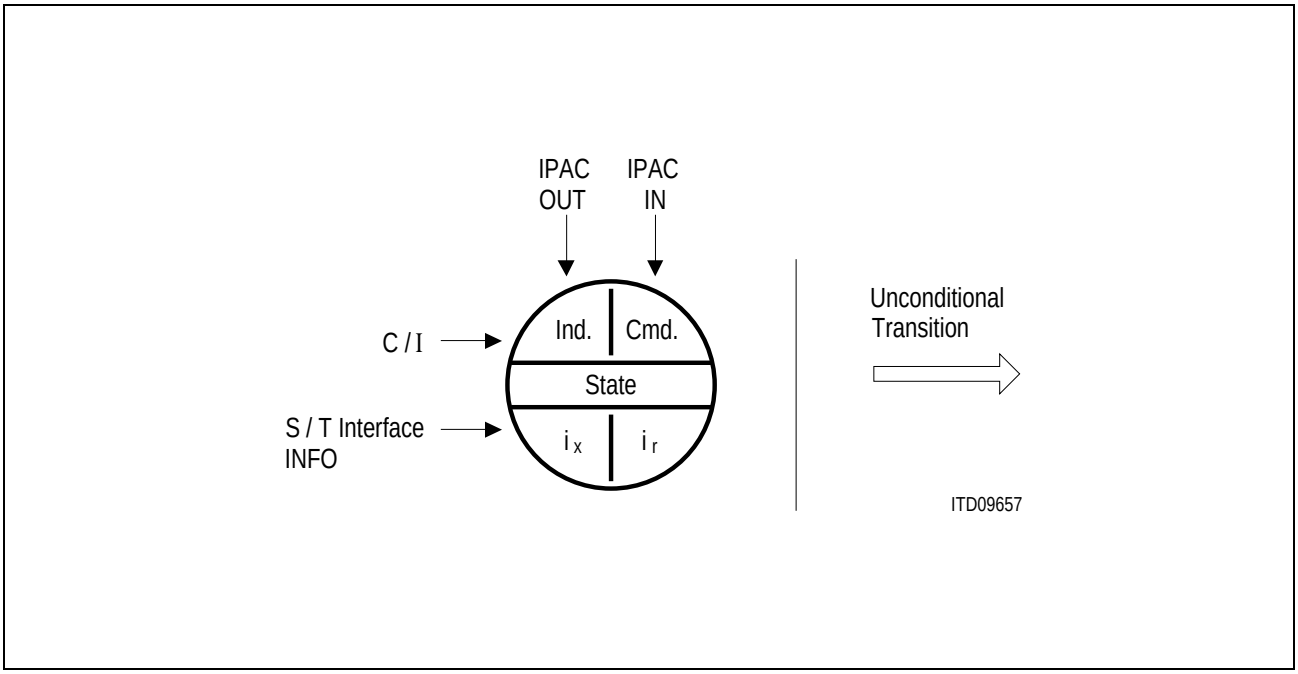


Figure 92 State Diagram Notation

The following example illustrates the use of a state diagram with an extract of the TE state diagram. The state explained is “F3 power down”.

The state may be entered by either of two methods:

– from state “test mode i” after the C/I command “DI” has been received.
– from state “F3 pending deactivation”, “F3 power up” or “F4 pending activation” after the C/I command “DI” has been received.

The following informations are transmitted:

– INFO 0 (no signal) is sent on the S/T-interface.
– C/I message “DC” is issued on the IOM-2 interface.

The state may be left by either of the following methods:

– Leave for the state “F3 power up” after synchronous or asynchronous “TIM” code has been received on IOM.
– Leave for state “F5/8 unsynchron” after any kind of signal (not INFO 0) has been recognized on the S/T-interface.
– Leave for state “F4 pending activation” in case C/I = AR8 or AR10 is received.

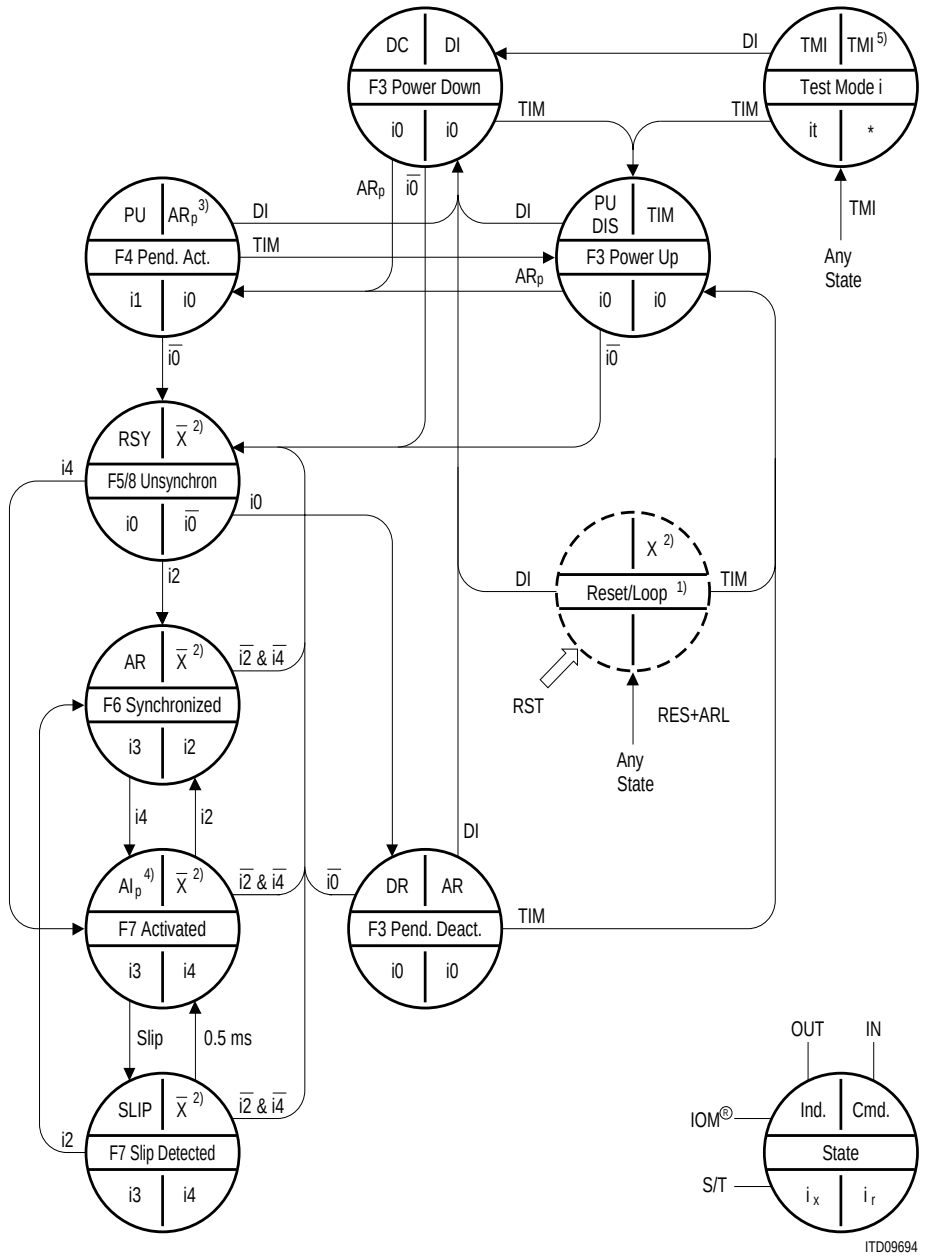
As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A “&” stands for a logical AND combination. An “or” indicates a logical OR combination.

The sections following the state diagram contain detailed information on all states and signals used. These details are mode dependent and may differ for identically named signals/states. They are therefore listed for each mode.

3.6.3 State Machine TE/LT-T Modes

This section is applicable for both TE and LT-T operational modes.

3.6.3.1 TE/LT-T Modes State Diagram

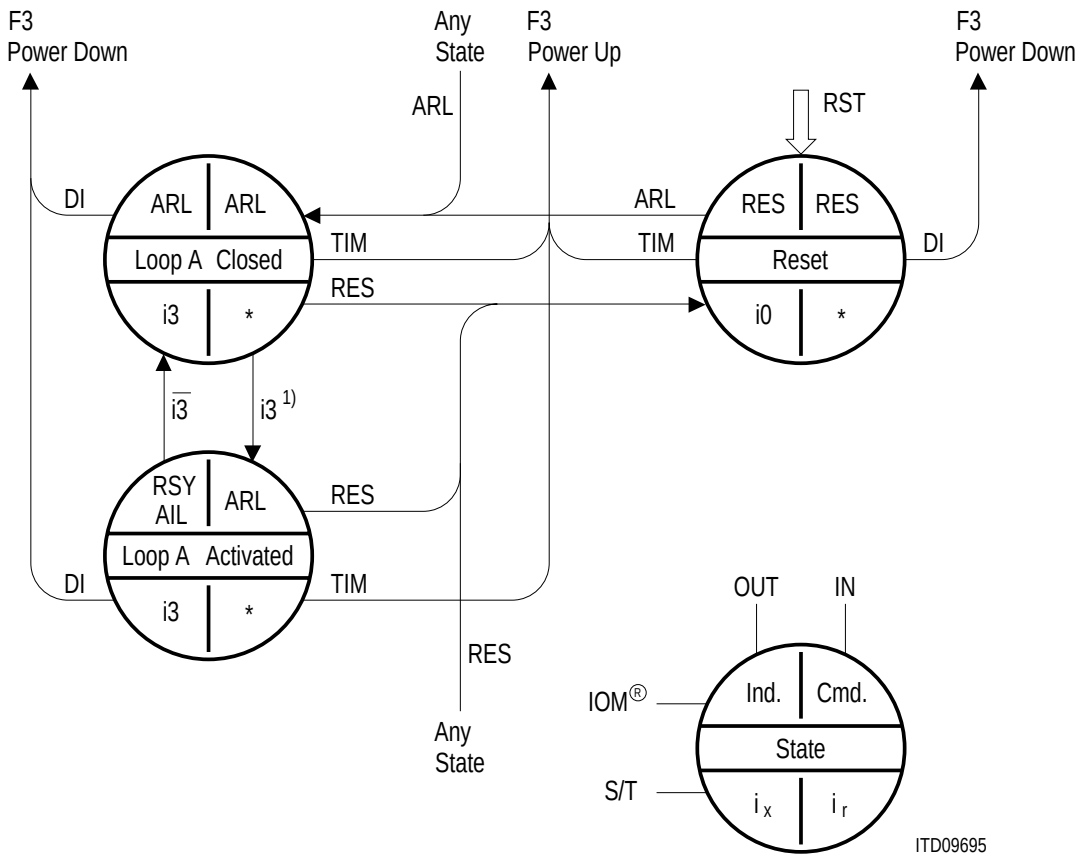


Notes:

1. See state diagram for unconditional transitions for details
2. x = TM1 or TM 2 or RES or ARL
   $\overline{x}$ = $\overline{TM1}$ & $\overline{TM2}$ & $\overline{RES}$ & $\overline{ARL}$
3. AR_P = AR8 or AR10
4. AI_P = AI8 or AI10
5. TMI = TM1 or TM2

B- and D-channel on SX transparent if the command equals to AR8 or AR10.

Figure 93 State Transition Diagram in TE/LT-T Modes



Note:

1. In state “loop A activated” I3 is the internal signal, the external signal is I0.

Figure 94 State Diagram of the TE/LT-T Modes, Unconditional Transitions

3.6.3.2 TE/LT-T Modes Transition Criteria

The transition criteria used by the IPAC are described in the following sections. They are grouped into:

– C/I commands
– Pin states
– Events related to the S/T-interface

C/I Commands

AR8 Activation Request with priority 8 for D-channel transmission. This command is used to start a TE initiated activation. D-channel priority 8 is the highest priority. It should be used to request signaling information transfer.

AR10 Activation request with priority 10 for D-channel transmission. This command is used to start a TE initiated activation. D-channel priority 10 is the lower priority. It should be used to request packet data transfer.

ARL Activation request loop. The IPAC is requested to operate an analog loop-back close to the S/T-interface. ARL is an unconditional command.

DI Deactivation indication. This command transfers the IPAC into “F3 power down” mode and disables the IOM-2 clocks.

RES Reset of state machine. Transmission of Info 0. No reaction to incoming infos. RES is an unconditional command.

TIM Timing Request. Requests the IPAC to change into power-up state and provide timing signals on IOM-2.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command.

Pin States

Pin-RES Pin-Reset. Corresponds to a high level at pin RST. At power up, a reset pulse (RST high active) of minimum 2 DCL clock cycles should be applied to bring the IPAC to the state “reset”. After that the IPAC may be operated according to the state diagrams. In NT mode the DCL is needed during the hardware reset (RES = 1) for initialization. The function of this pin is identical to the C/I code RES concerning the state machine.

S/T-Interface Events

I0 INFO 0 detected

$\overline{I0}$ A signal different to INFO 0 was detected

I2 INFO 2 detected

I4 INFO 4 detected

SLIP SLIP detected (applicable in LT-T mode only) IOM-2 interface framing and S/T-interface framing differences have exceeded the specified limit. It is likely that data will be lost to enable a resynchronization.

Transmitted Signals and Indications in TE/LT-T Modes

The following signals and indications are issued on the IOM-2 and S/T-interface.

C/I Indications

Abbreviation	Indication	Remark
DR	Deactivate Request	Deactivation request via S/T-interface
RES	Reset	Reset acknowledge
TM1	Test mode 1	TM1 acknowledge
TM2	Test mode 2	TM2 acknowledge
SLIP	Slip detected (LT-T only)	Wander is larger than 50 µs peak-to-peak (or 25 µs peak-to-peak if programmed, refer to the C/W/P-bit of the MON-8 Configuration Register)
RSY	Resynchronization during level detect	Signal received, receiver not synchronous
PU	Power up	IOM-2 interface clocking is provided
AR	Activate request	Info 2 received
ARL	Activate request loop	Loop A closed
CVR	Far-end-code-violation	After each multi-frame the receipt of at least one illegal code violation is indicated six times. This function must be enabled by setting the RCVE-bit in the MON-8 Configuration Register.
AIL	Activate indication loop	Loop A activated
AI8	Activate indication with priority class 8	Info 4 received, D-channel priority is 8 or 9.
AI10	Activate indication with priority class 10	Info 4 received, D-channel priority is 10 or 11.
DC	Deactivate confirmation	Clocks will be disabled, (in TE), quiescent state

S/T-Interface Signals

I0	INFO 0
I1	INFO 1
I3	INFO 3
It	Pseudo-ternary pulses at 2 kHz frequency (alternating, TM1) Pseudo-ternary pulses at 96 kHz frequency (alternating, TM2)

States TE/LT-T Mode

F3 power down

This is the deactivated state of the physical protocol. The received line awake unit is active. In TE mode, clocks are disabled if the CFS bit of the IPAC Configuration Register is set to “1“.

F3 power up

This state is similar to “F3 power down”. The state is invoked by a C/I command TIM = “0000” (or DU static low). After the subsequent activation of the clocks the “Power Up” message is output.

F3 pending deactivation

The IPAC reaches this state after receiving INFO0 (from states F5 to F8) from F6 and F7 via F5/8. From this state an activation is only possible from the line (transition “F3 pend. deact.” to “F5 unsynchronized”). The power down state may be reached only after receiving DI.

F4 pending activation

Activation has been requested from the terminal, INFO 1 is transmitted, INFO 0 is still received, “Power Up” is transmitted in the C/I channel. This state is stable: timer T3 (I.430) is to be implemented in software.

F5/8 unsynchronized

At the reception of any signal from the NT, the IPAC ceases to transmit INFO 1, adapts its receiver circuit, and awaits identification of INFO 2 or INFO 4. This state is also reached after the IPAC has lost synchronism in the states F6 or F7 respectively.

F6 synchronized

When the IPAC receives an activation signal (INFO 2), it responds with INFO 3 and waits for normal frames (INFO 4).

F7 activated

This is the normal active state with the layer 1 protocol activated in both directions. From state “F6 synchronized”, state F7 is reached almost 0.5 ms after reception of INFO 4.

F7 slip detected

When a slip is detected between the S/T-interface clocking system and the IOM-2 interface clocks (phase wander greater than 50 µs, data may be disturbed, or 25 µs if programmed in the MON-8 Configuration Register) the IPAC enters this state, synchronizing again the internal buffer. After 0.5 ms this state is left again (only possible in LT-T mode).

Unconditional States TE/LT-T Mode

Loop A closed

On Activate Request Loop command, INFO 3 is sent by the line transmitter internally to the line receiver (INFO0 is transmitted to the line). The receiver is not yet synchronized.

Loop A activated

The receiver is synchronized on INFO 3 which is looped back internally from the transmitter. Data may be sent. The indication “AIL” is output to indicate the activated state. When the S/T line awake detector, which is switched to the line, detects an incoming signal, this is indicated by “RSY”.

Test mode 1

Single alternating pulses are sent on the S/T-interface (2 kHz repetition rate)

Test mode 2

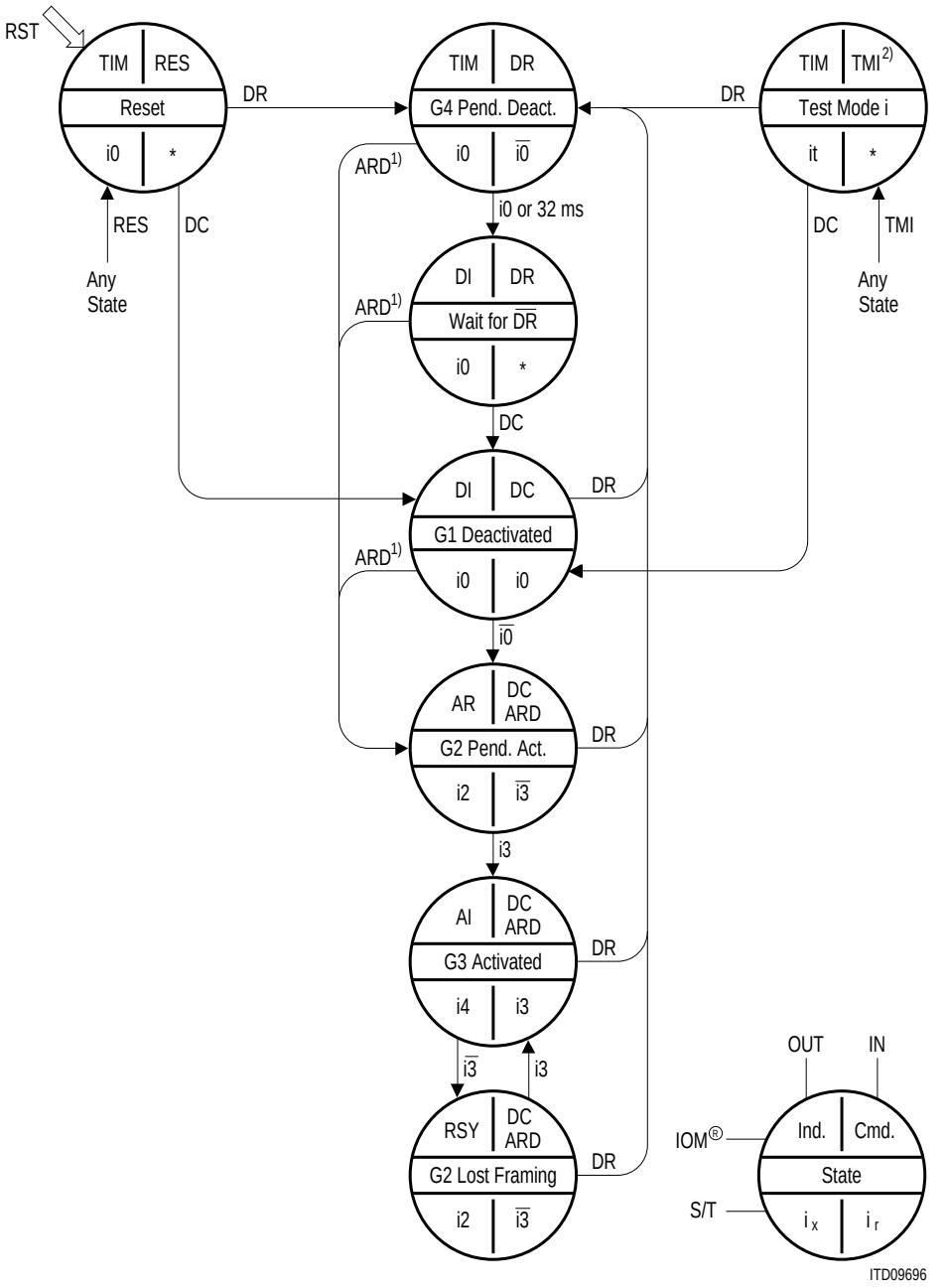
Continuous alternating pulses are sent on the S/T-interface (96 kHz)

Reset state

A hardware or software reset (RES) forces the IPAC to an idle state where the analog components are disabled (transmission of INFO0) and the S/T line awake detector is inactive. Thus activation from the NT is not possible. Clocks are still supplied and the outputs are in a low impedance state.

3.6.4 State Machine LT-S Mode

3.6.4.1 LT-S Mode State Diagram



Notes:
1. ARD stands for AR or ARL
2. TMI = TM1 or TM2

Figure 95 State Transition Diagram in LT-S Mode

3.6.4.2 LT-S Mode Transition Criteria

The transition criteria used by the IPAC are described in the following sections. They are grouped into:

– C/I commands
– Pin states
– Events on the S/T-interface.

C/I Commands

AR Activation Request. This command is used to start an exchange initiated activation.

ARL Activation request loop. The IPAC is requested to operate an analog loop-back close to the S/T-interface.

DC Deactivation Confirmation. Transfers the LT-S into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

DR Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command.

RES Please refer to **section 3.6.3.2** (C/I command description) for details.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command.

Pin States

Pin-$\overline{\text{RES}}$ Pin Reset. Please refer to **section 3.6.3.2** (pin states).

S/T-Interface Events

I0 INFO 0 detected

$\overline{\text{I0}}$ Level detected (signal different to I0)

I3 INFO 3 detected

$\overline{\text{I3}}$ Any INFO other than INFO 3

3.6.4.3 Transmitted Signals and Indications in LT-S Mode

The following signals and indications are issued on the IOM-2 and S/T-interface.

C/I Indications

Abbreviation	Indication (upstream) LT-S mode	Remark
TIM	Timing	Interim indication during deactivation procedure
RSY	Resynchronizing	Receiver is not synchronous
AR	Activate request	$\overline{\text{INFO 0}}$ received from terminal. Activation proceeds.
CVR	Far-end-code-violation	After the receipt of at least one illegal code violation CVR is indicated six times. This function must be enabled by setting the RCVE-bit in the MON-8 configuration register.
AI	Activate indication	Synchronous receiver, i.e. activation completed.
DI	Deactivate indication	Timer (32 ms) expired or INFO 0 received after deactivation request

S/T-Interface Signals

I0 INFO 0

I2 INFO 2

I4 INFO 4

It Pseudo ternary pulses at 2-kHz frequency (TM1).
Pseudo ternary pulses at 96-kHz frequency (TM2).

3.6.4.4 States LT-S Mode

G1 deactivated

The IPAC is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel.

G2 pending activation

As a result of an $\overline{\text{INFO 0}}$ detected on the S/T line or an ARD command, the IPAC begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.

G3 activated

Normal state where INFO 4 is transmitted to the S/T-interface. The IPAC remains in this state as long as neither a deactivation nor a test mode is requested, nor the receiver loses synchronism.

When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter keeps on sending INFO 4.

G2 lost framing

This state is reached when the IPAC has lost synchronism in the state G3 activated.

G4 pending deactivation

This state is triggered by a deactivation request DR. It is an unstable state: indication DI (state “G4 wait for DR.”) is issued by the IPAC when:

either INFO0 is received,

or an internal timer of 32 ms expires.

G4 wait for DR

Final state after a deactivation request. The IPAC remains in this state until a response to DI (in other words DC) is issued.

Test mode 1

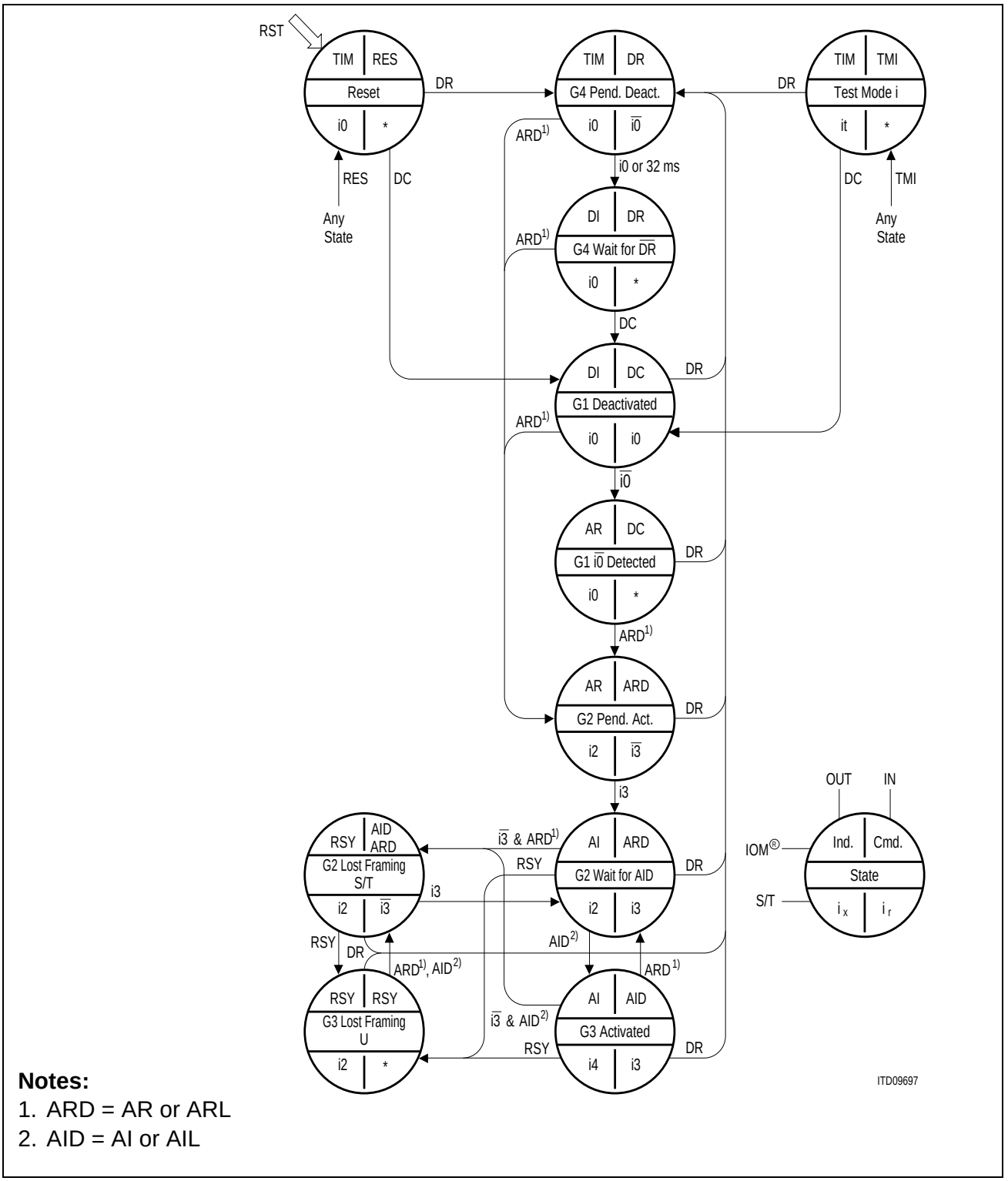
Single alternating pulses are sent on the S/T-interface (2-kHz repetition rate).

Test mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz).

3.6.5 State Machine Intelligent NT Mode

3.6.5.1 Intelligent NT Mode State Diagram



Notes:
1. ARD = AR or ARL
2. AID = AI or AIL

Figure 96 NT Mode State Diagram

3.6.5.2 Intelligent NT Mode Transition Criteria

The transition criteria used by the IPAC are described in the following sections. They are grouped into:

–C/I commands
–Pin states
–Events or the S/T-interface.

C/I Commands

AR Activation Request. This command is used to start an exchange initiated activation.

ARL Activation request loop. The IPAC is requested to operate an analog loop-back close to the S/T-interface.

AI Activation Indication. Confirms that the U-interface is fully transparent, on D-channel data transfer is allowed.

AIL Activation Indication loop.

DC Deactivation Confirmation. Transfers the NT into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

DR Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command.

RES Please refer to **section 3.6.3.2** (C/I commands) for details.

RSY Resynchronizing. The U-interface has not obtained or lost synchronization. INFO 2 is transmitted consequently by the IPAC.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command.

Pin States

Pin-$\overline{\text{RES}}$ Pin Reset. Please refer to **section 3.6.3.2** (pin states) for details.

S/T-Interface Events

I0 INFO 0 detected

$\overline{\text{I0}}$ Level detected (any signal different to I0)

I3 INFO 3 detected

$\overline{\text{I3}}$ Any INFO other than INFO 3.

3.6.5.3 Transmitted Signals and Indications in Intelligent NT Mode

The following signals and indications are issued on the IOM-2 and S/T-interface.

C/I Indications

Abbreviation	Indication (upstream) NT Mode	Remark
TIM	Timing	S transceiver requires clock pulses
RSY	Resynchronizing	Receiver is not synchronous
AR	Activate request	$\overline{\text{INFO 0}}$ received
CVR	Far-end-code-violation	After each multi-frame the receipt of at least one illegal code violation is indicated six times. This function must be enabled by setting the RCVE-bit in the MON-8 configuration register.
AI	Activate indication	Synchronous receiver
DI	Deactivate indication	Timer (32 ms) expired or INFO 0 received after deactivation request

S/T-Interface Signals

I0 INFO 0

I2 INFO 2

I4 INFO 4

It Pseudo ternary pulses at 2-kHz frequency (TM1).
Pseudo ternary pulses at 96-kHz frequency (TM2).

3.6.5.4 States Intelligent NT Mode

G1 Deactivated

The IPAC is not transmitting. No signal is detected on the S/T-interface, and no activation command is received in C/I channel. DI is output in the normal deactivated state, and TIM is output as a first step when an activation is requested from the S/T-interface.

G1 $\overline{\text{I0}}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The IPAC is waiting for an AR command, which normally indicates that the transmission line upstream (usually a two-wire U interface) is synchronized.

G2 Pending Activation

As a result of the ARD command, and INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the IPAC waits for a “switch-through” command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the IPAC has lost synchronism in the state G3 activated.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the two-wire U interface, the IPAC transmits INFO 2.

G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for DR”) is issued by the IPAC when:

either INFO0 is received

or an internal timer of 32 ms expires.

G4 wait for DR

Final state after a deactivation request. The IPAC remains in this state until an “acknowledgment” to DI (DC) is issued.

Test Mode 1

Single alternating pulses are sent on the S/T-interface (2-kHz repetition rate).

Test Mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz).

3.6.6 Command/Indicate Channel

Structure

4 bit wide, located at bit positions 26-29 in each time-slot (assuming that bit 0 is the first bit).

Verification

Double last-look criterion. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames.

Codes

Both commands and indications depend on the IPAC mode and the data direction. The table below presents all defined C/I codes. A command needs to be applied continuously until the desired action has been initiated. Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

C/I Codes

Code	LT-S		NT		TE/LT-T	
	IN	OUT	IN	OUT	IN	OUT
0 0 0 0	DR	TIM	DR	TIM	TIM	DR
0 0 0 1	RES	–	RES	–	RES	RES
0 0 1 0	TM1	–	TM1	–	TM1	TM1
0 0 1 1	TM2	–	TM2	–	TM2	TM2 SLIP [1]
0 1 0 0	–	RSY	RSY	RSY	–	RSY
0 1 0 1	–	–	–	–	–	–
0 1 1 0	–	–	–	–	–	–
0 1 1 1	–	–	–	–	–	PU
1 0 0 0	AR	AR	AR	AR	AR8	AR
1 0 0 1	–	–	–	–	AR10	–
1 0 1 0	ARL	–	ARL	–	ARL	ARL
1 0 1 1	–	CVR	–	CVR	–	CVR
1 1 0 0	–	AI	AI	AI	–	AI8
1 1 0 1	–	–	–	–	–	AI10
1 1 1 0	–	–	AIL	–	–	AIL
1 1 1 1	DC	DI	DC	DI	DI	DC

1) In LT-T mode only

AI	Activation Indication	DI	Deactivation Indication
AI8	Activation Indication with high priority	DR	Deactivation Request
AI10	Activation Indication with low priority	PU	Power-Up
AIL	Activation Indication Loop	RES	Reset
AR	Activation Request	RSY	Resynchronizing
AR8	Activation Request with high priority	SLIP	IOM Frame Slip
AR10	Activation Request with low priority	TIM	Timer
ARL	Activation Request Loop	TM1	Test Mode 1 (2-kHz signal)
CVR	Code Violation Received	TM2	Test Mode 2 (96-kHz signal)
DC	Deactivation Confirmation		

3.6.7 Example of Activation/Deactivation

An example of an activation/deactivation of the S interface, with the time relationships mentioned in the previous chapters, is shown in **figure 97**, in the case of an IPAC in TE and LT-S modes.

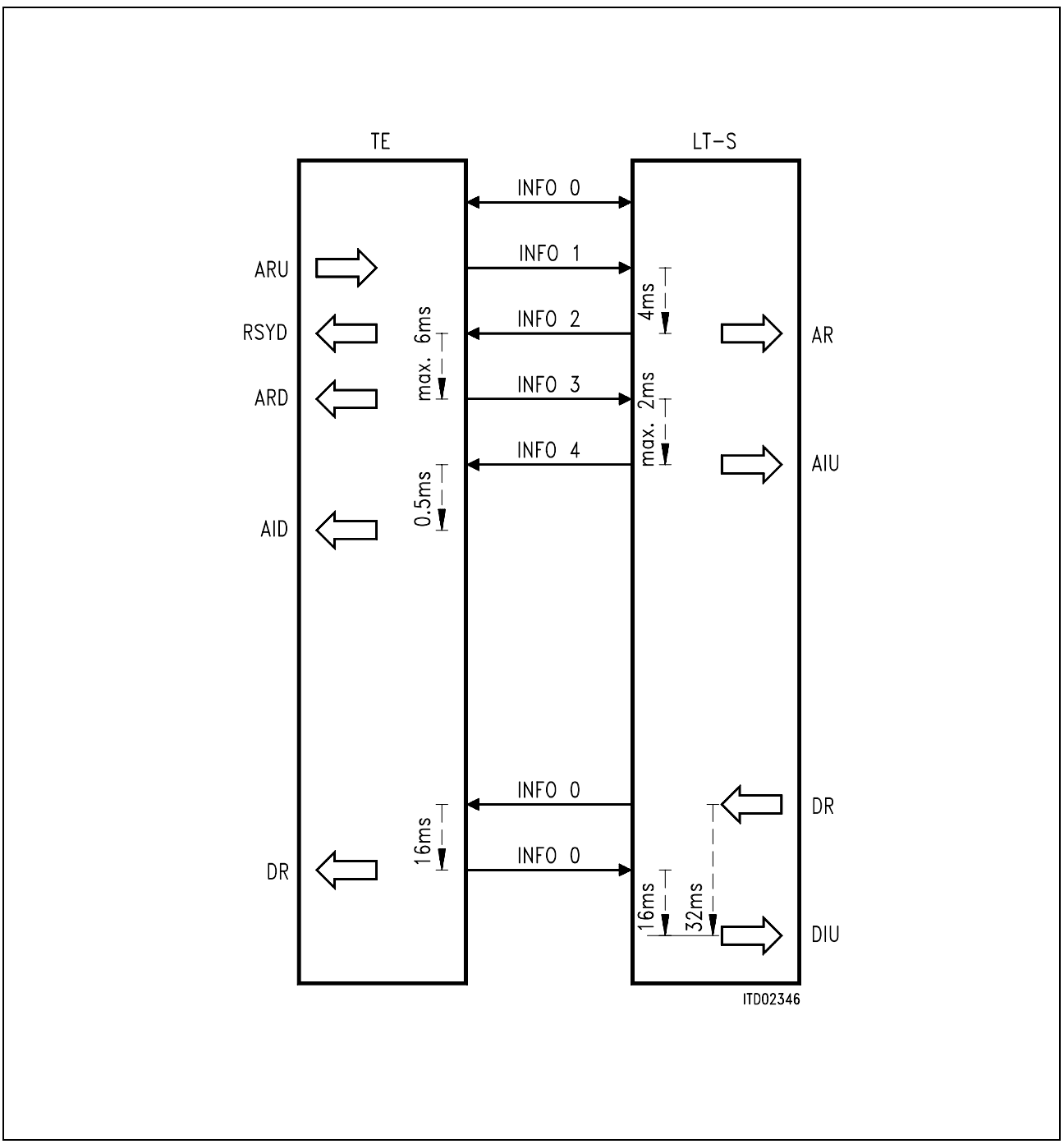


Figure 97 Example of Activation/Deactivation

4 Detailed Register Description

4.1 Register Address Arrangement

The IPAC comprises the basic functionality of the ISAC-S PEB 2086 and of the HSCX-TE PSB 21525 with additional DMA capability. Therefore the IPAC register set is very similar to these two devices, which allows for easy adaptation of existing host software.

As shown in **figure 98** the B-Channel registers are located in the range from 00h to 73h whereas the D-Channel specific registers are available from 80h to BAh. As some of the registers provide similar functionality for B-Channel and D-Channel operation, the nomenclature indicates to which functional block the register is related to
(e.g. RFIFOB = receive FIFO B-Channel, RFIFOD = receive FIFO D-Channel).

The IPAC specific registers for configuration, interrupt handling, PCM and Auxiliary interface are located at the upper address range starting at C0h.

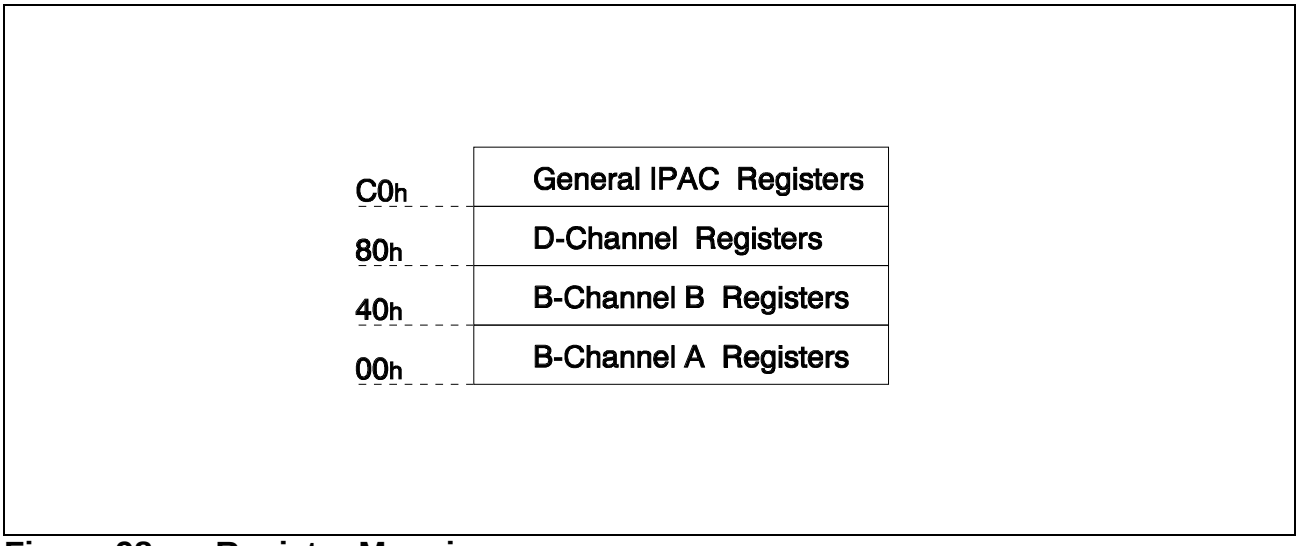


Figure 98 Register Mapping

	7	6	5	4	3	2	1	0	
B-Channel Registers									
RFIFOB	B-Channel Receive FIFO								RD (00-1F/40-5F)
XFIFOB	B-Channel Transmit FIFO								WR (00-1F/40-5F)
ISTAB	RME	RPF	0	XPR	0	0	0	0	RD (20/60)
MASKB	RME	RPF	0	XPR	0	0	0	0	WR (20/60)
STARB	XDOV	XFW	XREP	RFR	RLI	CEC	XAC	AFI	RD (21/61)
CMDRB	RMC	RHR	XREP	0	XTF	0	XME	XRES	WR (21/61)
MODEB	MDS1	MDS0	ADM	CFT	RAC	0	0	TLP	RD/WR (22/62)
reserved									RD/WR (23/63)
EXIRB	XMR	XDU EXE	0	RFO	0	RFS	0	0	RD (24/64)
RBCLB	RBC7							RBC0	RD (25/65)
RAH1	RAH1						0	0	WR (26/66)
RAH2	RAH2						0	0	WR (27/67)
RSTAB	VFR	RDO	CRC	RAB	HA1	HA0	C/R	LA	RD (27/67)
RAL1	RAL1								RD/WR (28/68)
RAL2	RAL2								WR (29/69)
RHCRB	RHCR								RD (29/69)
XBCL	XBC7							XBC0	WR (2A/6A)
reserved									RD/WR (2B/6B)
CCR2	SOC	0	XCS0	RCS0	TXD	0	RIE	DIV	RD/WR (2C/6C)
RBCHB	DMA	0	0	OV	RBC11			RBC8	RD (2D/6D)

	7	6	5	4	3	2	1	0	
XBCH	DMA	0	0	XC	XBC11			XBC8	WR (2D/6D)
reserved									RD (2E/6E)
RLCR	RC	0	RL5					RL0	WR (2E/6E)
CCR1	PU	SC	0	0	ITF	0	1	0	RD/WR (2F/6F)
TSAX	TSNX						XCS2	XCS1	WR (30/70)
TSAR	TSNR						RCS2	RCS1	WR (31/71)
XCCR	XBC7							XBC0	WR (32/72)
RCCR	RBC7							RBC0	WR (33/73)

D-Channel Registers

RFIFOD	D-Channel Receive FIFO								RD (80 - 9F)
XFIFOD	D-Channel Transmit FIFO								WR (80 - 9F)
ISTAD	RME	RPF	RSC	XPR	TIN	CIC	SIN	TIN2	RD (A0)
MASKD	RME	RPF	RSC	XPR	TIN	CIC	SIN	TIN2	WR (A0)
STARD	XDOV	XFW	XRNR	RRNR	MBR	MAC1	--	MAC0	RD (A1)
CMDRD	RMC	RRES	RNR	STI	XTF	XIF	XME	XRES	WR (A1)
MODED	MDS2	MDS1	MDS0	TMD	RAC	DIM2	DIM1	DIM0	RD/WR (A2)
TIMR1	CNT			VALUE					RD/WR (A3)
EXIRD	XMR	XDU	PCE	RFO	SOV	MOS	SAW	WOV	RD (A4)
XAD1									WR (A4)
XAD2									WR (A5)
RBCLD	RBC7							RBC0	RD (A5)
SAPR									RD (A6)
SAP1	SAPI1						CRI	0	WR (A6)

	7	6	5	4	3	2	1	0	
SAP2	SAPI2						MCS	0	WR (A7)
RSTAD	RDA	RDO	CRC	RAB	SA1	SA0	C/R	TA	RD (A7)
TEI1	TEI1							EA	WR (A8)
TEI2	TEI2							EA	WR (A9)
RHCRD									RD (A9)
RBCHD	XAC	--	--	OV	RBC11			RBC8	RD (AA)
STAR2	0	0	0	0	WFA	0	TREC	SDET	RD (AB)
SPCR	SPU	SDL	SPM	TLP	C1C1	C1C0	C2C1	C2C0	RD/WR (B0)
CIR0	0	BAS	CODR0				CIC0	CIC1	RD (B1)
CIX0	RSS	BAC	CODX0				1	1	WR (B1)
MOR0									RD (B2)
MOX0									WR (B2)
CIR1	CODR1						MR1	MX1	RD (B3)
CIX1	CODX1						1	1	WR (B3)
MOR1									RD (B4)
MOX1									WR (B4)
C1R									RD/WR (B5)
C2R									RD/WR (B6)
STCR	TSF	TBA2	TBA1	TBA0	ST1	ST0	SC1	SC0	WR (B7)
B1CR									RD (B7)
B2CR									RD (B8)
ADF1	WTC1	WTC2	CI1E	0	CSEL2	CSEL1	CSEL0	ITF	WR (B8)
reserved	1	0	0	0	0	0	0	0	RD/WR (B9)

	7	6	5	4	3	2	1	0	
MOSR	MDR1	MER1	MDA1	MAB1	MDR0	MER0	MDA0	MAB0	RD (BA)
MOCR	MRE1	MRC1	MIE1	MXC1	MRE0	MRC0	MIE0	MXC0	WR (BA)

General IPAC Registers

CONF	AMP	CFS	TEM	PDS	IDH	SGO	ODS	IOF	RD/WR (C0)
ISTA	INT1	INT0	ICD	EXD	ICA	EXA	ICB	EXB	RD (C1)
MASK	INT1	INT0	ICD	EXD	ICA	EXA	ICB	EXB	WR (C1)
ID									RD (C2)
ACFG	OD7	OD6	OD5	OD4	OD3	OD2	EL1	EL0	RD/WR (C3)
AOE	OE7	OE6	OE5	OE4	OE3	OE2	0	0	RD/WR (C4)
ARX	AR7	AR6	AR5	AR4	AR3	AR2	0	0	RD (C5)
ATX	AT7	AT6	AT5	AT4	AT3	AT2	0	0	WR (C5)
PITA1	ENA	DUDD	0	TNRX					RD/WR (C6)
PITA2	ENA	DUDD	0	TNRX					RD/WR (C7)
POTA1	ENA	DUDD	0	TNTX					RD/WR (C8)
POTA2	ENA	DUDD	SRES	TNTX					RD/WR (C9)
PCFG	DPS	ACL	LED	PLD	FBS	CSL2	CSL1	CSL0	RD/WR (CA)
SCFG	PRI	TXD	TLEN	TSLT					RD/WR (CB)
TIMR2	TMD	0	CNT						RD/WR (CC)

Note: The MON-8 registers for layer 1 are not directly accessible to the host but they are controlled via the MONITOR channel.
*These registers are described in **chapter 2.4.4**.*

4.2 B-Channel Registers

4.2.1 RFIFOB - Receive FIFO B-Channel (Read))

	7						0	
RFIFOB	Receive data							(00-1F/40-5F)

Interrupt Controlled Data Transfer (Interrupt Mode, selected by XBCH:DMA=0):

Up to 64 bytes of receive data can be read from the RFIFOB following an RPF or an RME interrupt.

RPF Interrupt: Exactly 64 bytes to be read.
RME Interrupt: Number of bytes to be determined by reading the RBCLB, RBCHB registers.

Although the address range covers only 32 byte (similar to HSCX-TE) the FIFO depth is 64 byte as the read address does not need to be reprogrammed. Addresses within the address space of the FIFO's are interpreted equally, i.e. the actual data byte can be accessed with any address within the valid scope.

DMA Controlled Data Transfer (DMA Mode, selected by XBCH:DMA=1):

If the RFIFOB contains 64 bytes, the IPAC autonomously requests a block data transfer by activating the DRQRA/B-line until the 63rd read cycle is finished. This forces the DMA-controller to continuously perform bus cycles until 64 bytes are transferred from the IPAC to the system memory (DMA controller mode: demand transfer, level triggered).

If the RFIFOB contains less than 64 bytes (one short frame or the last bytes of a long frame) the IPAC requests a block data transfer depending on the contents of the RFIFOB according to the following table:

RFIFOB Contents (bytes)	DMA Transfer (bytes)
(1), 2, 3	4
4 - 7	8
8 - 15	16
16 - 31	32
32 - 64	64

Additionally an RME interrupt is issued after the last byte has been transferred. As a result, the DMA-controller may transfer more bytes than actually valid in the current

received frame. The valid byte count must therefore be determined by reading the registers RBCHB, RBCLB following the RME interrupt.

The corresponding DRQRA/B pin remains 'high' as long as the RFIFOB requires data transfers. It is deactivated upon the rising edge of the 63rd DMA transfer or, if n < 64 or n is the remainder of a long frame, upon the falling edge of the last DMA transfer.

If n ≥ 64 and the DMA controller does not perform the 64th DMA cycle, the DRQRA/B line will go high again as soon as $\overline{CS}$ goes high, thus indicating further bytes to fetch.

4.2.2 XFIFOB - Transmit FIFO B-Channel (WRITE))

	7		0	
XFIFOB	Transmit data			(00-1F/40-5F)

Interrupt Controlled Data Transfer (Interrupt Mode, selected by XBCH:DMA=0):

Up to 64 bytes of transmit data can be written to the XFIFOB following an XPR interrupt.

DMA Controlled Data Transfer (DMA Mode, selected by XBCH:DMA=1):

Prior to any data transfer, the actual byte count of the frame to be transmitted must be written to the XBCH, XBCL registers by the user.

1 byte:	XBCL = 0
n bytes:	XBCL = n - 1

If data transfer is then initiated via the CMDRB register (command XTF or XIF), the IPAC autonomously requests the correct amount of block data transfers (n × 64 + remainder, n = 0, 1, …).
The corresponding DRQTA/B pin remains 'high' as long as the XFIFOB requires data transfers. It is deactivated upon the rising edge of $\overline{WR}$ in the DMA transfer 63 or n-1 respectively. The DMA controller must take care to perform the last DMA transfer. If it is missing, the DRQTA/B line will go active again when $\overline{CS}$ is raised.

Although the address range covers only 32 byte (similar to HSCX-TE) the FIFO depth is 64 byte as the read address does not need to be reprogrammed. Addresses within the address space of the FIFO's are interpreted equally, i.e. the actual data byte can be accessed with any address within the valid scope.

4.2.3 ISTAB - Interrupt Status Register for B-Channel (READ)

Value after reset: 00_H

	7							0	
ISTAB	RME	RPF	0	XPR	0	0	0	0	(20/60)

RME … Receive Message End

One message up to 64 bytes or the last part of a message greater then 64 bytes has been received and is now available in the RFIFOB. The message is complete! The actual message length can be determined reading the RBCHB, RBCLB registers. Additional information is available in the RSTAB register.

RPF … Receive Pool Full

A block of 64 bytes of a message is stored in the RFIFOB. The message is not yet completed!

Note: This interrupt is only generated in interrupt mode, not in DMA mode.

XPR … Transmit Pool Ready

A data block of up to 64 bytes can be written to the transmit FIFO.

To generate edges at the $\overline{INT}$ pin it is necessary to mask all interrupts at the end of the interrupt service routine and write back the old mask to the mask register.

4.2.4 MASKB - Mask Register for B-Channel (WRITE)

Value after reset: 00_H (all interrupts enabled)

	7							0	
MASKB	RME	RPF	0	XPR	0	0	0	0	(20/60)

Each interrupt source can be selectively masked by setting the respective bit in MASKB (bit positions corresponding to ISTAB register). Masked interrupts are not indicated when reading ISTAB. Instead, they remain internally stored and will be indicated after the respective MASKB bit is reset.

4.2.5 STARB - Status Register for B-Channel (READ)

Value after reset: 48_H

	7							0	
STARB	XDOV	XFW	XREP	RFR	RLI	CEC	XAC	AFI	(21/61)

XDOV … Transmit Data Overflow

More than 64 bytes have been written to the XFIFOB.

XFW … Transmit FIFO Write Enable

Data can be written to the XFIFOB.

Note: XFW is valid if CEC = 0 only!

XREP … Transmission Repeat

Contains the read back value of the corresponding command bit CMDRB:XREP.

RFR … Receive FIFO read enable

A ’1’ indicates, that valid data is in the RFIFOB and read access is enabled. RFR is set with the RME- or RPF-interrupt and reset when executing the RMC-command.

RLI … Receive Line Inactive

Neither FLAGs as interframe time fill nor frames are received via the receive line.

CEC … Command Executing

0 … no command is currently executed, the CMDRB register can be written to.
1 … a command (written previously to CMDRB) is currently executed, no further command can be temporarily written via CMDRB register.

Note: CEC will be active at most 2.5 transmit clock periods. If the IPAC is in power down mode CEC will stay active.

XAC … Transmitter Active

A ’1’ indicates, that the transmitter is currently active. In bus mode the transmitter is considered active also when it waits for bus access.

AFI … Additional Frame Indication

A ’1’ indicates, that one or more completely received frames or the last part of a frame are in the CPU inaccessible part of the RFIFOB. In combination with the bit STARB:RFR multiple frames can be read out of the RFIFOB without interrupt control.

4.2.6 CMDRB - Command Register for B-Channel (WRITE)

Value after reset: 00_H

	7							0	
CMDRB	RMC	RHR	XREP	0	XTF	0	XME	XRES	(21/61)

Note: The maximum time between writing to the CMDRB register and the execution of the command is 2.5 clock cycles. Therefore, if the CPU operates with a very high clock in comparison with the IPAC’s clock, it’s recommended that the CEC bit of the STARB register is checked before writing to the CMDRB register to avoid any loss of commands.

RMC … Receive Message Complete

Confirmation from CPU to IPAC, that the actual frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFOB can be released.

Note: In DMA mode this command is only issued once after an RME interrupt. The IPAC does not generate further DMA requests prior to the reception of this command.

RHR … Reset HDLC Receiver

All data in the RFIFOB and the HDLC receiver is deleted.

XREP … Transmission Repeat

In extended transparent mode 0, 1 :

Together with XTF and XME set (write 2 A_H to CMDRB), the IPAC repeatedly transmits the contents of the XFIFOB (1 … 64 bytes) without HDLC framing fully transparent, i.e. without FLAG, CRC insertion, bit stuffing.

The cyclic transmission continues until the command XRES is executed or the bit XREP is reset. The interframe timefill pattern is issued afterwards. When resetting XREP, data transmission is stopped after the next XFIFOB-cycle is completed, the XRES command terminates data transmission immediately .

Note: MODEB:CFT must be set to '0' when using cyclic transmission.

XTF … Transmit Transparent Frame

After having written up to 64 bytes to the XFIFOB, this command initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the IPAC (only in non-automode, transparent mode 0,1).
No opening flag sequence is generated in extended transparent mode 0, 1.

XME … Transmit Message End (used in interrupt mode only!)

Indicates, that the data block written last to the transmit FIFO completes the actual frame. The IPAC can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

Note: In DMA mode the XME must not be used.

XRES … Transmit Reset

The content of the XFIFOB is deleted and IDLE is transmitted. This command can be used by the CPU to abort a frame currently in transmission. After setting XRES an XPR interrupt is generated in every case.

4.2.7 MODEB - Mode Register for B-Channel (READ/WRITE)

Value after reset: 00_H

	7							0	
MODEB	MDS1	MDS0	ADM	CFT	RAC	0	0	TLP	(22/62)

MDS1, MDS0 … Mode Select

The operating mode of the HDLC controller is selected.

01 … non-auto mode
10 … transparent mode
11 … extended transparent mode

ADM … Address Mode

The meaning of this bit varies depending on the selected operating mode:

- Non-auto mode

  Defines the length of the HDLC address field.
  0 … 8-bit address field
  1 … 16-bit address field

In transparent modes, this bit differentiates between two sub-modes:

- Transparent mode

  0 … transparent mode 0; no address recognition.
  1 … transparent mode 1; high byte address recognition.

- Extended transparent mode; without HDLC framing.

  0 … extended transparent mode 0; received data in RAL1.
  1 … extended transparent mode 1; received data in RFIFOB and RAL1.

Note: In extended transparent modes, the RAC bit must set to '0' to enable fully transparent reception!

CFT … Continuous Frame Transmission

1… When CFT is set, the XPR interrupt is generated immediately after the CPU accessible part of XFIFOB is copied into the transmitter section.
0… Otherwise the XPR interrupt is delayed until the transmission is completed (D-Channel arbiter).

RAC … Receiver Active

Via RAC the HDLC receiver can be activated/deactivated.

0 … HDLC receiver inactive
1 … HDLC receiver active

In extended transparent modes this bit must be reset to enable fully transparent reception!

TLP … Test Loop

When TLP is set, input and output of the HDLC controller are internally connected, i.e.

transmitter channel A to receiver channel A and

transmitter channel B to receiver channel B.

The receive B-channels on DD are disabled (data is ignored) and the transmit B-channels on DU remain active (data is transmitted).

4.2.8 EXIRB - Extended Interrupt Register for B-Channel (READ)

Value after reset: 00_H

	7							0	
EXIRB	XMR	XDU EXE	0	RFO	0	RFS	0	0	(24/64)

XMR … Transmit Message Repeat

The transmission of the last message has to be repeated.

XDU/EXE … Transmit Data Underrun/Extended Transmission End

The actual frame has been aborted with IDLE, because the XFIFOB holds no further data, but the frame is not yet complete!

In extended transparent mode, this bit indicates the transmission-end condition.

Note: It is not possible to send transparent-frames when a XMR or XDU interrupt is indicated.

RFO … Receive Frame Overflow

One frame could not be stored due to occupied RFIFOB (i.e. whole frame has been lost). This interrupt can be used for statistical purposes and indicates, that the CPU does not respond quickly enough to an incoming RPF, or RME interrupt.

RFS … Receive Frame Start

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes.

After an RFS interrupt, the contents of

- RHCRB
- RAL1
- RSTAB – bit 3-0

are valid and can be read by the CPU.
This interrupt must be enabled setting the RIE bit in CCR2.

4.2.9 RBCLB - Receive Byte Count Low for B-Channel (READ)

Value after reset: (not defined)

	7						0	
RBCLB	RBC7						RBC0	(25/65)

Together with RBCHB (bits RBC11 – RBC8), the length of the actual received frame (1 … 4095 bytes) can be determined. These registers must be read by the CPU following an RME interrupt.

4.2.10 RAH1 - Receive Address Byte High Register 1 (WRITE)

Value after reset: (not defined)

	7						0	
RAH1	RAH1					0	0	(26/66)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individual programmable values in RAH1, or RAH2.

4.2.11 RAH2 - Receive Address Byte High Register 2 (WRITE)

Value after reset: (not defined)

	7					1	0	
RAH2	RAH2					0	0	(27/67)

RAH2 … Value of second individual programmable high address byte.

Note: RAH1, RAH2 registers are used in non-auto operating mode when a 2-byte address field has been selected (MODEB.ADM = 1) and in the transparent mode 1.
If a 1-byte address field is selected, RAH1 and RAH2 must be set to 00_H.

4.2.12 RSTAB - Receive Status Register for B-Channel (READ)

Value after reset: (not defined)

	7							0	
RSTAB	VFR	RDO	CRC	RAB	HA1	HA0	C/R	LA	(27/67)

VFR … Valid Frame

Determines whether a valid frame has been received.

1 … Valid
0 … Invalid

An invalid frame is either

- a frame which is not an integer multiple of 8 bits (n × 8 bits) in length (e.g. 25 bit), or
- a frame which is too short depending on the selected operation mode via MODEB (MDS1, MDS0, ADM) as follows:
  – Non-auto mode (16-bit address): 4 bytes
  – Non-auto mode (8-bit address): 3 bytes
  – Transparent mode 1:3 bytes.
  – Transparent mode 0:2 bytes.

Note: Shorter frames are not reported.

RDO … Receive Data Overflow

A data overflow has occurred within the actual frame.
Caution: Data loss because the CPU did not serve RME or RPF interrupt in time.

CRC … CRC compare/check

0 … CRC check failed; received frame contains errors.
1 … CRC check o.k.; received frame is error-free.

RAB … Receive Message Aborted

The received frame was aborted from the transmitting station.
According to the HDLC protocol, this frame must be discarded by the CPU.

HA1, HA0 … High Byte Address Compare; significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the IPAC compares the high byte of a 2-bytes address with the contents of two individual programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (group address).

Depending on the result of this comparison, the following bit combinations are possible:

10 … RAH1 has been recognized
00 … RAH2 has been recognized
01 … group address has been recognized

Note: If RAH1, RAH2 contain the identical values, the combination 00 will be omitted.

C/R … Command/Response; significant only, if 2-byte address mode has been selected.

Value of the C/R bit (bit of high address byte) in the received frame.

0 ... response received
1 ... command received

LA … Low Byte Address Compare; not significant in transparent and extended transparent operating modes.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two programmable registers (RAL1, RAL2)
0 … RAL2 has been recognized
1 … RAL1 has been recognized
According to the X.25 LAPB protocol, RAL1 is interpreted as COMMAND and RAL2 interpreted as RESPONSE.

Note: RSTAB corresponds to the last received HDLC frame; it is duplicated into RFIFOB for every frame (last byte of frame).
If several frames are contained in the RFIFO the corresponding status information for each frame should be evaluated from the FIFO contents (last byte) as RSTAB only refers to last frame in the FIFO.

4.2.13 RAL1 - Receive Address Byte Low Register 1 (READ/WRITE)

Value after reset: (not defined)

	7						0	
RAL1	RAL1							(28/68)

The general function (READ/WRITE) and the meaning or contents of this register depends on the selected operating mode:

– Non-auto mode (16-bit address) – **WRITE only**:
  RAL1 can be programmed with the value of the first individual low address byte.
– Non-auto mode (8-bit address) – **WRITE only**:
  According to X.25 LAPB protocol, the address in RAL1 is recognized as COMMAND address.
– Transparent mode 1 (high byte address recognition) – **READ only**:
  RAL1 contains the byte following the high byte of the address in the receive frame (i.e. the second byte after the opening flag).
– Transparent mode 0 (no address recognition) – **READ only**:
  RAL1 contains the first byte after the opening flag (first byte of received frame).
– Extended transparent modes 0, 1 – **READ only**:
  RAL1 contains the actual data byte currently assembled at the DD pin, bypassing the HDLC receiver (fully transparent reception without HDLC framing).

4.2.14 RAL2 - Receive Address Byte Low Register 2 (WRITE)

Value after reset: (not defined)

	7						0	
RAL2	RAL2							(29/69)

Value of the second individual programmable low address byte. If a one byte address field is selected, RAL2 is recognized as RESPONSE according to X.25 LAPB protocol.

4.2.15 RHCRB - Receive HDLC Control Register for B-Channel (READ)

Value after reset: (not defined)

	7						0	
RHCRB	RHCR							(29/69)

Value of the HDLC control field corresponds to the last received frame.

Note: RHCRB is duplicated into RFIFOB for every frame.

Mode	Contents of RHCR
Non-auto mode, 1-byte address	2nd byte after flag
Non-auto mode, 2-byte address	3rd byte after flag
Transparent mode 1	3rd byte after flag
Transparent mode 0	2nd byte after flag

4.2.16 XBCL - Transmit Byte Count Low (WRITE)

Value after reset: (not defined)

	7						0	
XBCL	XBC7						XBC0	(2A/6A)

Together with XBCH (bits XBC11 ... XBC8) this register is used in DMA mode only, to program the length (1 ... 4095 bytes) of the next frame to be transmitted.

This allows the IPAC to request the correct amount of DMA cycles after an XTF command via CMDRB.

4.2.17 CCR2 - Channel Configuration Register 2 (READ/WRITE)

Value after reset: 00_H

	7							0	
CCR2	SOC	0	XCS0	RCS0	TXD	0	RIE	DIV	(2C/6C)

SOC … Special Output Control

0 … B-Channel data is transmitted on DU, received on DD pin (normal case)
1 … B-Channel data is transmitted on DD, received on DU pin

XCS0, RCS0 … Transmit/Receive Clock Shift, Bit 0

Together with bits XCS2, XCS1 (RCS2, RCS1) in TSAX (TSAR) the clock shift relative to the frame synchronization signal of the transmit (receive) time-slot can be adjusted. A clock shift of 0 … 7 bits is programmable.

TXD … Transmitter Disable

0 ... DU pin is enabled during the programmed timeslot
1 ... DU pin is disabled (high impedant) during the programmed timeslot

Note: This mode can be used to deactivate the B-channel timeslot in push-pull configuration.

RIE … Receive Frame Start Interrupt Enable

When RIE is set, the RFS interrupt (via EXIRB) is enabled.

DIV … Data Inversion

If enabled (DIV=1), data is transmitted and received inverted. This feature is described in detail in **chapter 2.1.12**.

Note: This option is only valid if NRZ data encoding is selected (CCR1:SC=0).

4.2.18 RBCHB - Received Byte Count High for B-Channel (READ)

Value after reset: 000xxxxx

	7				3	0	
RBCHB	DMA	0	0	OV	RBC11	RBC8	(2D/6D)

DMA … DMA Mode

Contains the read back value from register XBCH, which selects between interrupt or DMA mode.

OV … Counter Overflow

More than 4095 bytes received!
The received frame exceeded the byte count in RBC11 … RBC0.

RBC11 … RBC8 … Receive Byte Count (most significant bits)

Together with RBCLB (bits RBC7 … RBC0) the length of the received frame can be determined.

4.2.19 XBCH - Transmit Byte Count High (WRITE)

Value after reset: 0000xxxx

	7				3	0	
XBCH	DMA	0	0	XC	XBC11	XBC8	(2D/6D)

DMA … DMA Mode

Selects the data transfer mode between the IPAC and the host system.
0 ... Interrupt controlled data transfer (interrupt mode)
1 ... DMA controlled data transfer (DMA mode)

XC … Transmit Continuously

Only valid if DMA mode is selected (DMA=1):
If the XC bit is set, the IPAC continuously requests for transmit data ignoring the transmit byte count programmed via XBCH and XBCL.

XBC11-8 … Transmit Byte Count (most significant bits)

Only valid if DMA mode is selected (DMA=1):
Together with XBC7-0 the length of the next frame to be transmitted in DMA mode is determined (1 ... 4096 bytes).

4.2.20 RLCR - Receive Length Check Register (WRITE)

Value after reset: (not defined)

	7			0	
RLCR	RC	0	RL5	RL0	(2E/6E)

RC … Receive Check (on/off)

0 … receive length check feature disabled
1 … receive length check feature enabled

Note: All bytes stored in the RFIFOB are relevant for the receive length check feature including the receiver status byte.

RL … Receive Length

The maximum receive length after which data reception is suspended can be programmed here. Depending on the value RL programmed via RL5 … RL0, the receive length is (RL + 1) $\times$ 64 bytes! A frame exceeding this length is treated as if it was aborted by the opposite station (RME Interrupt, RAB bit set).

In this case, the Receive Byte Count (RBCHB, RBCLB) is greater than the programmed receive length.

4.2.21 CCR1 - Channel Configuration Register 1 (READ/WRITE)

Value after reset: 02_H

	7							0	
CCR1	PU	SC	0	0	ITF	0	1	0	(2F/6F)

PU … Switches between Power Up and Power Down mode

0 … power down (standby)
1 … power up (active)

Note: In order to switch the IPAC in power down mode it is necessary to program ITF=0 together with PU=0.

SC ... Serial Port Configuration

0 … NRZ data encoding
1 … NRZI data encoding

ITF … Interframe Time Fill

ITF determines the idle state (= no data to send) of the transmit data pin (DU)

0 … Continuous IDLE sequences are output (DU pin remains in the '1' state)
1 … Continuous FLAG sequences are output ('01111110' bit patterns)

Note: ITF must be set to '0' for power down mode.

4.2.22 TSAX - Time-Slot Assignment Register Transmit (WRITE)

Value after reset: (not defined)

	7						2	1	0	
TSAX	TSNX							XCS2	XCS1	(30/70)

TSNX … Time-Slot Number Transmit

Selects one of up 64 possible time-slots (00_H – $3F_H$) in which data is transmitted. The number of bits per time-slot can be programmed via XCCR.

XCS2, XCS1 … Transmit Clock Shift, Bit 2-1

Together with the XCS0 in CCR2, the transmit clock shift can be adjusted.

4.2.23 TSAR - Time-Slot Assignment Register Receive (WRITE)

Value after reset: (not defined)

	7			0	
TSAR	TSNR		RCS2	RCS1	(31/71)

TSNR … Time-Slot Number Receive

Defines one of up to 64 possible time-slots (00_H – $3F_H$) in which data is received. The number of bits per time-slot can be programmed via RCCR.

RCS2, RCS1 … Receive Clock Shift, Bit 2-1

Together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

4.2.24 XCCR - Transmit Channel Capacity Register (WRITE)

Value after reset: 00_H

	7		0	
XCCR	XBC7		XBC0	(32/72)

XBC7 … XBC0 … Transmit Bit Count, Bit 7-0

Defines the number of bits to be transmitted with a time-slot:
Number of bits = XBC + 1. (1 … 256 bits/time-slot)

4.2.25 RCCR - Receive Channel Capacity Register (WRITE)

Value after reset: 00_H

	7		0	
RCCR	RBC7		RBC0	(33/73)

RBC7 … RBC0 … Receive Bit Count, Bit 7-0

Defines the number of bits to be transmitted with a time-slot:
Number of bits = RBC + 1. (1 … 256 bits/time-slot)

4.3 D-Channel Registers

4.3.1 RFIFOD - Receive FIFO D-Channel (Read)

	7						0	
RFIFOD	Receive data							(80-9F)

A read access to any address within the range 80h-9Fh gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each read access. This allows for the use of efficient “moving string” type commands by the processor.

The RFIFOD contains up to 32 bytes of received frame.

After an ISTAD:RPF interrupt, exactly 32 bytes are available.

After an ISTAD:RME interrupt, the number of bytes available can be obtained by reading the RBCLD register.

4.3.2 XFIFOD - Transmit FIFO D-Channel (Write)

	7						0	
XFIFOD	Transmit data							(80-9F)

A write access to any address within the range 00-1F$_H$ gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each write access. This allows for the use of efficient “move string” type commands by the processor.

Up to 32 bytes of transmit data can be written to the XFIFOD following an ISTAD:XPR interrupt.

4.3.3 ISTAD - Interrupt Status Register D-Channel (Read)

Value after reset: 00_H

	7							0	
ISTAD	RME	RPF	RSC	XPR	TIN	CIC	SIN	TIN2	(A0)

RME ... Receive Message End

One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes has been received. The contents are available in the RFIFOD. The message length and additional information may be obtained from RBCHD and RBCLD and the RSTAD register.

RPF ... Receive Pool Full

A 32-byte block of a frame longer than 32 bytes has been received and is available in the RFIFOD. The frame is not yet complete.

RSC ... Receive Status Change. Used in auto mode only

A status change in the receiver of the remote station - Receiver Ready/Receiver Not Ready - has been detected (RR or RNR S-frame). The actual status of the remote station can be read from the STARD register (RRNR bit).

XPR ... Transmit Pool Ready

A data block of up to 32 bytes can be written to the XFIFOD.

An XPR interrupt will be generated in the following cases:

- after an XTF or XIF command, when one transmit pool is emptied and the frame is not yet complete
- after an XTF together with an XME command is issued, when the whole transparent frame has been transmitted
- after an XIF together with an XME command is issued, when the whole I frame has been transmitted and a positive acknowledgment from the remote station has been received (auto mode).

TIN ... Timer Interrupt

The internal timer and repeat counter has expired (see TIMR1 register).

CIC ... C/I Channel Change

A change in C/I channel 0 or C/I channel 1 (only TE mode) has been recognized. The actual value can be read from CIR0 or CIR1.

SIN ... Synchronous Transfer Interrupt

When programmed (STCR register), this interrupt is generated to enable the processor to lock on to the IOM timing, for synchronous transfers.

TIN2 ... Timer Interrupt 2

The internal timer 2 counter has expired (see TIMR2 register).

Note: A read of the ISTAD register clears all bits except CIC. CIC is cleared by reading CIR0.

4.3.4 MASKD - Mask Register D-Channel (Write)

Value after reset: 00_H (all interrupts enabled)

	7							0	
MASKD	RME	RPF	RSC	XPR	TIN	CIC	SIN	TIN2	(A0)

Each interrupt source in the ISTAD register can be selectively masked by setting to “1” the corresponding bit in MASKD. Masked interrupt status bits are not indicated when ISTAD is read. Instead, they remain internally stored and pending, until the mask bit is reset to “0”.

Note: In the event of a C/I channel change, CIC is set in ISTAD even if the corresponding mask bit in MASKD is active, but no interrupt is generated.

4.3.5 STARD - Status Register D-Channel (Read)

Value after reset: 48_H

	7							0	
STARD	XDOV	XFW	XRNR	RRNR	MBR	MAC1	--	MAC0	(A1)

XDOV ... Transmit Data Overflow

More than 32 bytes have been written in one pool of the XFIFOD, i.e. data has been overwritten.

XFW ... Transmit FIFO Write Enable

Data can be written in the XFIFOD. This bit may be polled instead of (or in addition to) using the XPR interrupt.

XRNR ... Transmit RNR. Used in auto mode only

In auto mode, this bit indicates whether the IPAC receiver is in the “ready” (0) or “not ready” (1) state. When “not ready”, the IPAC sends an RNR S-frame autonomously to the remote station when an I frame or an S frame is received.

RRNR ... Receive RNR. Used in auto mode only

In the auto mode, this bit indicates whether the IPAC has received an RR or an RNR frame, this being an indication of the current state of the remote station: receiver ready (0) or receiver not ready (1).

MBR ... Message Buffer Ready

This bit signifies that temporary storage is available in the RFIFOD to receive at least the first 16 bytes of a new message.

MAC1 ... MONITOR Transmit Channel 1 Active (IOM-2 terminal mode only)

Data transmission is in progress in MONITOR channel 1.

MAC0 ... MONITOR Transmit Channel 0 Active

Data transmission is in progress in MONITOR channel 0.

4.3.6 CMDRD - Command Register (Write)

Value after reset: 00_H

	7							0	
CMDRD	RMC	RRES	RNR	STI	XTF	XIF	XME	XRES	(A1)

RMC ... Receive Message Complete

Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the processor confirms that it has fetched the data, and indicates that the corresponding space in the RFIFOD may be released.

RRES ... Receiver Reset

HDLC receiver is reset, the RFIFOD is cleared of any data. In addition, in auto mode, the transmit and receive counters (V(S), V(R)) are reset.

RNR ... Receiver Not Ready. Used in auto mode only.

Determines the state of the IPAC HDLC receiver.

When RNR = “0”, a received I or S-frame is acknowledged by an RR supervisory frame, otherwise by an RNR supervisory frame.

STI ... Start Timer

The IPAC hardware timer is started when STI is set to one. In the internal timer mode (TMD bit, MODED register) an S Command (RR, RNR) with poll bit set is transmitted in addition. The timer may be stopped by a write to the TIMR1 register.

XTF ... Transmit Transparent Frame

After having written up to 32 bytes in the XFIFOD, the processor initiates the transmission of a transparent frame by setting this bit to “1”. The opening flag is automatically added to the message by the IPAC.

XIF ... Transmit I Frame. Used in auto mode only

After having written up to 32 bytes in the XFIFOD, the processor initiates the transmission of an I frame by setting this bit to “1”. The opening flag, the address and the control field are automatically added by the IPAC.

XME ... Transmit Message End

By setting this bit to “1” the processor indicates that the data block written last in the XFIFOD completes the corresponding frame. The IPAC terminates the transmission by appending the CRC and the closing flag sequence to the data.

XRES ... Transmitter Reset

HDLC transmitter is reset and the XFIFOD is cleared of any data. This command can be used by the processor to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDRD register and the execution of the command is 2.5 DCL clock cycles. During this time no further commands should be written to the CMDRD register to avoid any loss of commands.

After an XPR interrupt further data has to be written to the XFIFOD and the appropriate Transmit Command (XTF or XIF) has to be written to the CMDRD register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTAD).

During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically.

4.3.7 MODED - Mode Register (Read/Write)

Value after reset: 00_H

	7							0	
MODED	MDS2	MDS1	MDS0	TMD	RAC	DIM2	DIM1	DIM0	(A2)

MDS2-0 ... Mode Select

Determines the message transfer mode of the HDLC controller, as follows:

MDS2-0	Mode	Number of Address Bytes	Address Comparison		Remark
			1.Byte	2.Byte	
0 0 0	Auto mode	1	TEI1,TEI2	–	One-byte address compare. HDLC protocol handling for frames with address TEI1
0 0 1	Auto mode	2	SAP1,SAP2,SAPG	TEI1,TEI2,TEIG	Two-byte address compare. LAPD protocol handling for frames with address SAP1 + TEI1
0 1 0	Non-Auto mode	1	TEI1,TEI2	–	One-byte address compare.
0 1 1	Non-Auto mode	2	SAP1,SAP2,SAPG	TEI1,TEI2,TEIG	Two-byte address compare.
1 0 0	Reserved				
1 0 1	Transparent mode 1	> 1	–	TEI1,TEI2,TEIG	Low-byte address compare.
1 1 0	Transparent mode 2	–	–	–	No address compare. All frames accepted.
1 1 1	Transparent mode 3	> 1	SAP1,SAP2,SAPG	–	High-byte address compare.

Note: SAP1, SAP2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte);
SAPG = fixed value FC / FE_H.
TEI1, TEI2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte; TEIG = fixed value FF_H

TMD ...Timer Mode

Sets the operating mode of the IPAC timer 1. In the external mode (0) the timer is controlled by the processor. It is started by setting the STI bit in CMDRD and it is stopped by a write of the TIMR1 register. In the internal mode (1) the timer is used internally by the IPAC for timeout and retry conditions (handling of LAPD/HDLC protocol in auto mode).

RAC ... Receiver Active

The HDLC receiver is activated when this bit is set to “1”.

DIM2-0 ... Digital Interface Modes

These bits define the characteristics of the IOM Data Ports (DU, DD) according to following table:

Table 27 IOM®-2 Modes

Characteristics DIM2, DIM1, DIM0	000	001	010	011	100...111
Last octet of IOM channel 2 used for TIC bus access	x	x			
Stop/go bit evaluated for D-channel access handling		x		x	
Reserved					x
Applications					
TE mode		x		x	
LT-T mode with D-channel collision resolution				x	
LT-T, LT-S modes with transparent D-channel			x		

4.3.8 TIMR1 - Timer 1 Register (Read/Write)

Value after reset: (not defined, previous value)

	7 5	4 0	
TIMR1	CNT	VALUE	(A3)

CNT ... The meaning depends on the selected timer mode (MODED:TMD):

• Internal Timer Mode (TMD=1)

CNT indicates the maximum number of S commands “N1” which are transmitted autonomously by the IPAC after expiration of time period T1 (retry, according to HDLC).

The internal procedure will be **started** in automode:

- after start of an I-frame transmission or
- after an ’RNR’ S-frame has been received

After the last retry a timer interrupt (TIN-bit in ISTAD) is generated.

The timer procedure will be **stopped** when

- a TIN interrupt is generated. The time between the start of an I-frame transmission or reception of an ’RNR’ S-frame and the generation of a TIN interrupt is equal to:

  (**CNT + 1) x T1**

- or the TIMR1 is written
- or a positive or negative acknowledgment has been received.

Note: The maximum value of CNT can be 6. If CNT is set to 7, the number of retries is unlimited.

• External Timer Mode (TMD=0)

CNT together with VALUE determine the time period T2 after which a TIN interrupt will be generated in the normal case:

T2 = CNT x 2.048 sec + T1 with **T1 = (VALUE+1) x 0.064 sec**

When TLP=1 (test loop activated, SPCR register):

T2 = 16348 x CNT x DCL + T1 with **T1 = 512 x (VALUE+1) x DCL**

DCL denotes the period of the DCL clock.

The timer can be started by setting the STI-bit in CMDRD and will be stopped when a TIN interrupt is generated or the TIMR1 register is written.

Note: If CNT is set to 7, a TIN interrupt is indefinitely generated after every expiration of T1.

VALUE ... Determines the time period T1

T1 = (VALUE + 1) x 0.064 sec (SPCR:TLP = 0, normal mode)
T1 = 512 x (VALUE + 1) x DCL (SPCR:TLP = 1, test mode)

4.3.9 EXIRD - Extended Interrupt Register (Read)

Value after reset: 00_H.

	7							0	
EXIRD	XMR	XDU	PCE	RFO	SOV	MOS	SAW	WOV	(A4)

XMR ... Transmit Message Repeat

The transmission of the last frame has to be repeated because:

– the IPAC has received a negative acknowledgment to an I frame in auto mode (according to HDLC/LAPD)
– or a collision on the S bus has been detected after the 32nd data byte of a transmit frame.

XDU ... Transmit Data Underrun

The current transmission of a frame is aborted by transmitting seven “1’s” because the XFIFOD holds no further data. This interrupt occurs whenever the processor has failed to respond to an XPR interrupt (ISTAD register) quickly enough, after having initiated a transmission and the message to be transmitted is not yet complete.

When a XMR or an XDU interrupt is generated, it is not possible to send transparent frames or I frames until the interrupt has been acknowledged by reading EXIR.

PCE ... Protocol Error (Used in auto mode only)

A protocol error has been detected in auto mode due to a received

– S or I frame with an incorrect sequence number N (R) or
– S frame containing an I field or
– I frame which is not a command or
– S-frame with an undefined control field.

RFO ... Receive Frame Overflow

The received data of a frame could not be stored, because the RFIFOD is occupied. The whole message is lost.

This interrupt can be used for statistical purposes and indicates that the processor does not respond quickly enough to an RPF or RME interrupt (ISTAD).

SOV ... Synchronous Transfer Overflow

The synchronous transfer programmed in STCR has not been acknowledged in time via the SC0/SC1 bit.

MOS ... MONITOR Status

A change in the MONITOR Status Register (MOSR) has occured.

SAW ... Subscriber Awake

Used only in TE mode (MODE0=0) and if terminal specific functions are enabled (STCR:TSF=1).

Indicates that a falling edge on $\overline{\text{EAW}}$ line has been detected.

WOV ... Watchdog Timer Overflow

Used only if terminal specific functions are enabled (STCR:TSF=1).

Signals the expiration of the watchdog timer, which means that the processor has failed to set the watchdog timer control bits WTC1 and WTC2 (ADF1 register) in the correct manner. A reset pulse has been generated by the IPAC.

4.3.10 XAD1 - Transmit Address 1 (Write)

Value after reset: (not defined)

	7						0	
XAD1								(A4)

Used in auto mode only.

XAD1 contains a programmable address byte which is appended automatically to the frame by the IPAC in auto mode. Depending on the selected address mode XAD1 is interpreted as follows:

2-Byte Address Field

XAD1 is the high byte (SAPI in the ISDN) of the 2-byte address field. Bit 1 is interpreted as the command/response bit “C/R”. It is automatically generated by the IPAC following the rules of ISDN LAPD protocol and the CRI bit value in SAP1 register. Bit 1 has to be set to “0”.

C/R Bit			
Command	**Response**	**Transmitting End**	**CRI Bit**
0	1	subscriber	0
1	0	network	0

In the ISDN LAPD the address field extension bit “EA”, i.e. bit 0 of XAD1 has to be set to “0”.

or

1-Byte Address Field

According to the X.25 LAPB protocol, XAD1 is the address of a command frame.

Note: In standard ISDN applications only 2-byte address fields are used.

4.3.11 XAD2 - Transmit Address 1 (Write)

Value after reset: (not defined)

	7						0	
XAD2								(A5)

Used in auto mode only.

XAD2 contains the second programmable address byte, whose function depends on the selected address mode:

2-Byte Address Field

XAD2 is the low byte (TEI in the ISDN) of the 2-byte address field.

or

1-Byte Address Field

According to the X.25 LAPB protocol, XAD2 is the address of a response frame.

Note: See note to XAD1 register description.

4.3.12 RBCLD - Receive Frame Byte Count Low for D-Channel (Read)

Value after reset: 00_H

	7						0	
RBCLD	RBC7						RBC0	(A5)

RBC7-0 ... Receive Byte Count

Eight least significant bits of the total number of bytes in a received message. Bits RBC4-0 indicate the length of a data block currently available in the RFIFOD, the other bits (together with RBCHD) indicate the number of whole 32-byte blocks received.

If exactly 32 bytes are received RBCLD holds the value 20_H.

4.3.13 SAPR - Received SAPI Register (Read)

Value after reset: (not defined)

	7						0	
SAPR								(A6)

When transparent mode 1 is selected SAPR contains the value of the first address byte of a receive frame.

4.3.14 SAP1 - SAPI1 Register (Write)

Value after reset: (not defined)

	7						0	
SAP1	SAPI1					CRI	0	(A6)

SAPI1 ... SAPI1 value

Value of the first programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD protocol.

CRI ... Command/Response Interpretation

CRI defines the end of the ISDN user-network interface the IPAC is used on, for the correct identification of “Command” and “Response” frames. Depending on the value of CRI the C/R-bit will be interpreted by the IPAC, when receiving frames in auto mode, as follows:

		C/R Bit	
CRI Bit	**Receiving End**	**Command**	**Response**
0	subscriber	1	0
1	network	0	1

For transmitting frames in auto mode, the C/R-bit manipulation will also be done automatically, depending on the value of the CRI-bit (refer to XAD1 register description).

In message transfer modes with SAPI address recognition the first received address byte is compared with the programmable values in SAP1, SAP2 and the fixed group SAPI.

In 1-byte address mode, the CRI-bit is to be set to “0”.

4.3.15 SAP2 - SAPI2 Register (Write)

Value after reset: (not defined)

	7			0	
SAP2	SAPI2		MCS	0	(A7)

SAPI2 ... SAPI2 value

Value of the second programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD-protocol.

MCS ... Modulo Count Select. Used in auto-mode only.

This bit determines the HDLC-control field format as follows:

0: One-byte control field (modulo 8)
1: Two-byte control field (modulo 128)

4.3.16 RSTAD - Receive Status Register (Read)

Value after reset: (not defined)

	7							0	
RSTAD	RDA	RDO	CRC	RAB	SA1	SA0	C/R	TA	(A7)

RDA ... Receive Data

A “1” indicates that data is available in the RFIFOD. After an RME-interrupt, a “0” in this bit means that data is available in the internal registers RHCRD or SAPR only (e.g. S-frame). See also RHCRD-register description table.

RDO ... Receive Data Overflow

If RDO=1, at least one byte of the frame has been lost, because it could not be stored in RFIFOD.

CRC ... CRC Check

The CRC is correct (1) or incorrect (0).

RAB ... Receive Message Aborted

The receive message was aborted by the remote station (1), i.e. a sequence of seven 1’s was detected before a closing flag.

SA1-0 ... SAPI Address Identification
TA ... TEI Address Identification

SA1-0 are significant in auto-mode and non-auto-mode with a two-byte address field, as well as in transparent mode 3. TA is significant in all modes except in transparent modes 2 and 3.

Two programmable SAPI values (SAP1, SAP2) plus a fixed group SAPI (SAPG of value FC/FE_H), and two programmable TEI values (TEI1, TEI2) plus a fixed group TEI (TEIG of value FF_H), are available for address comparison.

The result of the address comparison is given by SA1-0 and TA, as follows:

				Address Match with	
	SA1	**SA0**	**TA**	**1st Byte**	**2nd Byte**
Number of Address Bytes = 1	x x	x x	0 1	TEI2 TEI1	- -
Number of address Bytes=2	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 x	SAP2 SAP2 SAPG SAPG SAP1 SAP1 reserved	TEIG TEI2 TEIG TEI1 or TEI2 TEIG TEI1

Note: If the SAPI values programmed to SAP1 and SAP2 are identical the reception of a frame with SAP2/TEI2 results in the indication SA1=1, SA0=0, TA=1. Normally RSTAD should be read by the processor after an RME-interrupt in order to determine the status of the received frame. The contents of RSTAD are valid only after an RME-interrupt, and remain so until the frame is acknowledged via the RMC-bit.

C/R ... Command/Response

The C/R-bit identifies a receive frame as either a command or a response, according to the LAPD-rules:

Command	**Response**	**Direction**
0	1	Subscriber to network
1	0	Network to subscriber

4.3.17 TEI1 - TEI1 Register 1 (Write)

Value after reset: (not defined)

	7		0	
TEI1	TEI1		EA	(A8)

TEI1 ... Terminal Endpoint Identifier
EA ... Address field Extension bit

This bit is set to “1” according to HDLC/LAPD.

In all message transfer modes except in transparent modes 2 and 3,

TEI1 is used by the IPAC for address recognition. In the case of a two-byte address field, it contains the value of the first programmable Terminal Endpoint Identifier according to the ISDN LAPD-protocol.

In the auto-mode with a two-byte address field, numbered frames with the address SAPI1-TEI1 are handled autonomously by the IPAC according to the LAPD-protocol.

Note: If the value FF_H is programmed in TEI1, received numbered frames with address SAPI1-TEI1 (SAPI1-TEIG) are not handled autonomously by the IPAC.

In auto and non-auto-modes with one-byte address field, TEI1 is a command address, according to X.25 LAPB.

4.3.18 TEI2 - TEI2 Register (Write)

Value after reset: (not defined)

	7		0	
TEI2	TEI2		EA	(A9)

TEI2 ... Terminal Endpoint Identifier
EA ... Address field Extension bit

This bit is to be set to “1” according to HDLC/LAPD.

In all message transfer modes except in transparent modes 2 and 3, TEI2 is used by the IPAC for address recognition. In the case of a two-byte address field, it contains the value of the second programmable Terminal Endpoint Identifier according of the ISDN LAPD-protocol.

In auto and non-auto-modes with one-byte address field, TEI2 is a response address, according to X.25 LAPD.

4.3.19 RHCRD - Receive HDLC Control Register for D-Channel (Read)

Value after reset: (not defined)

	7						0	
RHCRD								(A9)

In all modes except transparent modes 2 and 3, this register contains the control field of a received HDLC-frame. In transparent modes 2 and 3, the register is not used.

	Contents of RHCRD		
Mode	**Modulo 8 (MCS=0)**	**Modulo 128 (MCS=1)**	**Contents of RFIFOD**
Auto-mode, 1-byte address (U/I frames) [1]	Control field	U-frames only: Control field [2]	From 3rd byte after flag [3]
Auto-mode, 2-byte address (U/I frames) [1]	Control field	U-frames only: Control field [2]	From 4th byte after flag [3]
Auto-mode, 1-byte address (I frames)		Control field compressed form [4]	From 4th byte after flag [3]
Auto-mode, 2-byte address (I frames)		Control field in compressed form [4]	From 5th byte after flag [3]
Non-auto-mode, 1-byte address	2nd byte after flag		From 3rd byte after flag
Non-auto-mode, 2-byte address	3rd byte after flag		From 4th byte after flag
Transparent mode 1	3rd byte after flag		From 4th byte after flag
Transparent mode 2	–		From 1st byte after flag
Transparent mode 3	–		From 2nd byte after flag

[1] S-frames are handled automatically and are not transferred to the microprocessor**.**

[2] For U-frames (bit 0 of RHCRD = 1) the control field is as: in the modulo 8 case.

[3] I-field.

[4] For I-frames (bit 0 of RHCRD = 0) the compressed control field has the same format as in the modulo 8 case, but only the three LSB's of the receive and transmit counters are visible:

7						0
N(R)	2-0	P	N(S)	2-0	0

4.3.20 RBCHD - Receive Frame Byte Count High for D-Channel (Read)

Value after reset: $0XXX0000_2$.

	7					0	
RBCHD	XAC	--	--	OV	RBC11	RBC8	(AA)

XAC ... Transmitter Active

The HDLC-transmitter is active when XAC = 1. This bit may be polled. The XAC-bit is active when:

– either an XTF/XIF-command is issued and the frame has not been completely transmitted
– or the transmission of an S-frame is internally initiated and not yet completed.

OV ... Overflow

A “1” in this bit position indicates a message longer than 4095 bytes.

RBC8-11 ... Receive Byte Count

Four most significant bits of the total number of bytes in a received message.

Note: Normally RBCHD and RBCLD should be read by the processor after an RME-interrupt in order to determine the number of bytes to be read from the RFIFOD, and the total message length. The contents of the registers are valid only after an RME-interrupt, and remain so until the frame is acknowledged via the RMC-bit.

4.3.21 STAR2 - Status Register 2 (Read)

Value after reset: (not defined)

	7							0	
STAR2	0	0	0	0	WFA	0	TREC	SDET	(AB)

WFA ... Waiting for Acknowledge

This bit shows, if the last transmitted I-frame was acknowledged, i.e.
V(A) = V(S) (=> WFA= 0) or was not yet acknowledged, i.e. V(A) < V(S) (=> WFA = 1).

TREC ... Timer recovery status

0: The device is not in the Timer Recovery state.
1: The device is in the Timer Recovery state.

SDET ... S-frame detected

This bit is set to “1” by the first received correct I-frame or S-command with p = 1.

It is reset by reading the STAR2 register or by a HW reset.

4.3.22 SPCR - Serial Port Control Register (Read/Write)

Value after reset: $00x00000_B$

	7							0	
SPCR	SPU	SDL	SPM	TLP	C1C1	C1C0	C2C1	C2C0	(B0)

SPU ... Software Power UP. (Used in TE-mode only)

Setting this bit to 1 will pull the DU-line to low. This will enforce connected layer 1 devices to deliver IOM-clocking.

After power down in TE-mode the SPU-bit has to be set to “1” and then cleared again.

After a subsequent CIC-interrupt (C/I-code change; ISTAD) and reception of the C/I-code “PU” (Power Up indication in TE-mode) the reaction of the processor would be:

- to write an Activate Request or TIM command as C/I-code in the CIX0-register.
- to reset the SPU bit and wait for the following CIC-interrupt.

SDL ... Switch Data Line

The switching of receive and transmit data of the D-channel controller to the IOM-2 interface is programmable by the SDL bit.

0: Transmit data is forwarded to the DU line, receive data comes from the DD line.
1: Transmit data is forwarded to the DD line, receive data comes from the DU line.

SPM ... Serial Port Timing Mode

Depending on the interface mode, the following timing options for the D-channel controller are provided.

0: Terminal Mode	All three channels of the IOM-2 interface are used (Typical applications: TE mode, LT-S in intelligent NT).
1: Non Terminal Mode	The selected IOM-2 channel (ADF1:CSEL2-0) is used (Typical applications: LT-T, LT-S modes, 8 channel structure on IOM-2)

*Note: The reset value for SPM is determined by pin MODE0 strapped to VDD or VSS (see **chapter 2.4.1**), however after reset the host can reconfigure the serial port timing mode for the D-channel controller.*

TLP ... Test Loop

When set to 1 the DU and DD-lines are internally connected together, and the times T1 and T2 are reduced (see TIMR1 register). Data coming from the layer 1 controller will not be forwarded to the layer 2 controller (see **chapter 2.5.9.2**).

C1C1, C1C0 ... Channel 1 Connect

Determines which of the two channels B1 or IC1 is connected to register C1R and/or B1CR, for monitoring, test-looping and switching data to/from the processor.

		C1R		B1CR	
C1C1	**C1C0**	**Read**	**Write**	**Read**	**Application(s)**
0	0	IC1	–	B1	B1-monitoring + IC1-monitoring
0	1	IC1	IC1	B1	B1-monitoring + IC1-looping from/to IOM
1	0	–	B1	B1	B1-access from/to S; transmission of a constant value in B1-channel to S.
1	1	B1	B1	–	B1-looping from S; transmission of a variable pattern in B1-channel to S.

C2C1, C2C0 ... Channel 2 Connect

Determines which of the two channels B2 or IC2 is connected to register C2R and/or B2CR, for monitoring, test-looping and switching data to/from the processor.

		C2R		B2CR	
C2C1	**C2C0**	**Read**	**Write**	**Read**	**Application(s)**
0	0	IC2	–	B2	B2-monitoring + IC2-monitoring
0	1	IC2	IC2	B2	B2-monitoring + IC2-looping from/to IOM
1	0	–	B2	B2	B2-access from/to S; transmission of a constant value in B2-channel to S.
1	1	B2	B2	–	B2-looping from S; transmission of a variable pattern in B2-channel to S.

Note: B-channel access is only possible in TE-mode.

4.3.23 CIR0 - Command/Indication Receive 0 (Read)

Value after reset: $7C_H$

	7				0	
CIR0	0	BAS	CODR0	CIC0	CIC1	(B1)

BAS ... Bus Access Status

Indicates the state of the TIC-bus:

0: the IPAC itself occupies the D- and C/I-channel
1: another device occupies the D- and C/I-channel

CODR0 ... C/I Code 0 Receive

Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

CIC0 ... C/I Code 0 Change

A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

CIC1 ... C/I Code 1 Change

A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.

CIC1 is only used if Terminal Mode is selected.

Note: The BAS and CODR0 bits are updated every time a new C/I-code is detected in two consecutive IOM-frames. If several consecutive valid new codes are detected and CIR0 is not read, only the first and the last C/I code (and BAS bit) is made available in CIR0 at the first and second read of that register, respectively.

4.3.24 CIX0 - Command/Indication Transmit 0 (Write)

Value after reset: $3F_H$

	7				0	
CIX0	RSS	BAC	CODX0	1	1	(B1)

RSS ... Reset Source Select

Only valid if the terminal specific functions are activated (STCR:TSF).

0 → **Subscriber or Exchange Awake**

As reset source serves:

– a falling edge on the $\overline{\text{EAW}}$-line (External Subscriber Awake)

– a C/I code change (Exchange Awake).

A logical zero on the $\overline{\text{EAW}}$-line activates also the IOM-interface clock and frame signal, just as the SPU-bit (SPCR) does.

1 → **Watchdog Timer**

The expiration of the watchdog timer generates a reset pulse. The watchdog timer will be reset and restarted, when two specific bit combinations are written in the ADF1-register within the time period of 128 ms (see also ADF1 register description).

After a reset pulse generated by the IPAC and the corresponding interrupt (WOV, SAW or CIC) the actual reset source can be read from the ISTAD and EXIRD-register.

Note: 'External Awake' is only available in TE mode.

BAC ... Bus Access Control

Only valid if the TIC-bus feature is enabled (MODED:DIM2-0).

If this bit is set, the IPAC will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.

Note: Access is always granted by default to the IPAC with TIC-Bus Address (TBA2-0, STCR register) "7", which has the lowest priority in a bus configuration.

CODX0 ... C/I-Code 0 Transmit

Code to be transmitted in the C/I-channel / C/I-channel 0.

4.3.25 MOR0 - MONITOR Receive Channel 0 (Read)

Value after reset: (not defined)

	7						0	
MOR0								(B2)

Contains the MONITOR data received in IOM-2 MONITOR Channel 0 according to the MONITOR channel protocol.

4.3.26 MOX0 - MONITOR Transmit Channel 0 (Write)

Value after reset: (not defined)

	7						0	
MOX0								(B2)

Contains the MONITOR data transmitted in IOM-2 MONITOR Channel 0 according to the MONITOR channel protocol.

4.3.27 CIR1 - Command/Indication Receive 1 (Read)

Value after reset: (not defined)

	7						0	
CIR1	CODR1					MR1	MX1	(B3)

CODR1 ... C/I-Code 1 Receive (only valid in terminal mode)

MR1 ... MR bit

Bit 1 of C/I channel 1

MX1 ... MX bit

Bit 0 of C/I/channel 1

4.3.28 CIX1 - Command/Indication Transmit 1 (Write)

Value after reset: FF_H

	7			0	
CIX1	CODX1		1	1	(B3)

CODX1 ... C/I-Code 1 Transmit (significant only in terminal mode)

Bits 7-2 of C/I-channel 1

4.3.29 MOR1 - MONITOR Receive Channel 1 (Read)

Value after reset: (not defined)

	7			0	
MOR1					(B4)

Used only in terminal mode.

Contains the MONITOR data received in IOM MONITOR channel 1 according to the MONITOR channel protocol.

4.3.30 MOX1 - MONITOR Transmit Channel 1 (Write)

Value after reset: (not defined)

	7			0	
MOX1					(B4)

Used only in terminal mode.

Contains the MONITOR data to be transmitted in IOM MONITOR channel 1 according to the MONITOR channel protocol.

4.3.31 C1R - Channel Register 1 (Read/Write)

Value after reset: (not defined)

	7						0	
C1R								(B5)

Used only in terminal mode.

Contains the value received/transmitted in IOM-channel B1 or IC1, as the case may be (cf. C1C1, C1C0, SPCR-register).

4.3.32 C2R - Channel Register 2 (Read/Write)

Value after reset: (not defined)

	7						0	
C2R								(B6)

Used only in terminal mode.

Contains the value received/transmitted in IOM-channel B2 or IC2, as the case may be (cf. C2C1, C2C0, SPCR-register).

4.3.33 STCR - Synchronous Transfer Control Register (Write)

Value after reset: 00_H

	7							0	
STCR	TSF	TBA2	TBA1	TBA0	ST1	ST0	SC1	SC0	(B7)

TSF ... Terminal Specific Functions (only in TE mode)

0 → No terminal specific functions

1 → The terminal specific functions are activated, such as

– Watchdog Timer

– Subscriber/Exchange Awake (**$\overline{\text{EAW}}$**).

In this case the **$\overline{\text{EAW}}$**-line is always an input signal which can serve as a request signal from the subscriber to initiate the awake function in a terminal.

A falling edge on the $\overline{\text{EAW}}$-line generates an SAW-interrupt (EXIRD). When the RSS-bit in the CIX0-register is zero, a falling edge on the $\overline{\text{EAW}}$-line (Subscriber Awake) or a C/I-code change (Exchange Awake) initiates a reset pulse.

When the RSS-bit is set to one a reset pulse is triggered only by the expiration of the watchdog timer (see also CIX0-register description).

Note: The TSF-bit will be cleared only by a hardware reset.
The 'Exchange Awake' functionality is only available in TE mode.

TBA2-0 ... TIC Bus Address

Defines the individual address for the IPAC on the IOM-bus.

This address is used to access the C/I- and D-channel on the IOM.

Note: One device liable to transmit in C/I- and D-fields on the IOM should always be given the address value "7".

ST1 ... Synchronous Transfer 1

When set, causes the IPAC to generate a SIN-interrupt status (ISTAD-register) at the beginning of an IOM-frame.

ST0 ... Synchronous Transfer 0

When set, causes the IPAC to generate a SIN-interrupt status (ISTAD-register) at the middle of an IOM-frame.

SC1 ... Synchronous Transfer 1 Completed

After a SIN interrupt the processor has to acknowledge the interrupt by setting the SC1 bit before the middle of the IOM frame, if the interrupt was originated from a Synchronous Transfer 1 (ST1).
Otherwise a SOV interrupt (EXIRD register) will be generated.

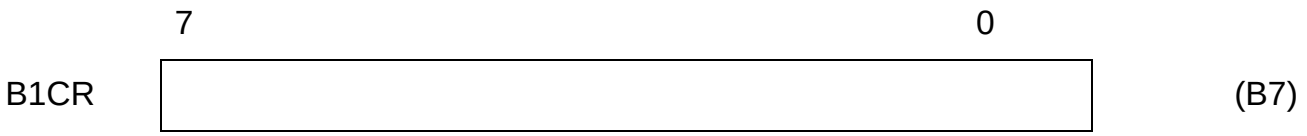
SC0 ... Synchronous Transfer 0 Completed

After a SIN interrupt the processor has to acknowledge the interrupt by setting the SC0 bit before the end of the IOM frame, if the interrupt was originated from a Synchronous Transfer 0 (ST0).
Otherwise a SOV interrupt (EXIRD register) will be generated.

Note: ST0/1 and SC0/1 are useful for synchronizing processor accesses and receive/ transmit operations.

4.3.34 B1CR - B1 Channel Register (Read)

Value after reset: (not defined)

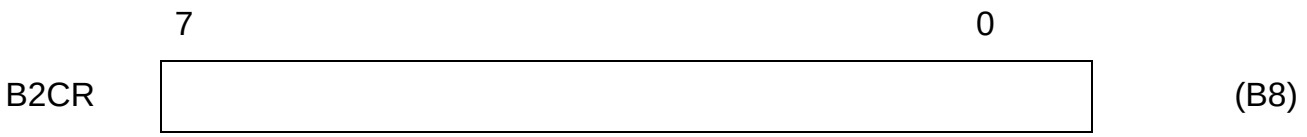


Used only in terminal mode.

Contains the value received in IOM-channel B1, if programmed
(cf. C1C1, C1C0, SPCR-register).

4.3.35 B2CR - B2 Channel Register (Read)

Value after reset: (not defined)



Used only in terminal mode.

Contains the value received in the IOM-channel B2, if programmed
(cf. C2C1, C2C0, SPCR-register).

4.3.36 ADF1 - Additional Feature Register 1 (Write)

Value after reset: $0000xxx0_2$

	7							0	
ADF1	WTC1	WTC2	CI1E	0	CSEL2	CSEL1	CSEL0	ITF	(B8)

WTC1, 2 ... Watchdog Timer Control 1, 2

After the watchdog timer mode has been selected (STCR:TSF = CIX0:RSS = 1) the watchdog timer is started.

During every time period of 128 ms the processor has to program the WTC1- and WTC2-bit in the following sequence:

	WTC1	**WTC2**
1.	1	0
2.	0	1

to reset and restart the watchdog timer.
If not, the timer expires and a WOV-interrupt (EXIRD) together with a reset pulse is generated.

CI1E ... C/I-channel 1 interrupt enable

Interrupt generation ISTAD:CIC of CIR0:CIC1 is enabled (1) or masked (0).

CSEL2-0 ... IOM-2 Channel Select (in LT modes only)

Select one IOM-channel out of 8, where the IPAC is to receive/transmit B-Channel data.

“000” channel 0 (first channel in IOM-frame)
“001” channel 1

...

“111” channel 7 (last channel in IOM-frame)

The reset value for CSEL2-0 is determined by the pins CH2-0 strapped to VDD or VSS. After reset the selected channel can be reconfigured by the host and the setting of pins CH2-0 has no further effect.

ITF ... Inter-Frame Time Fill

Selects the inter-frame time fill signal which is transmitted between HDLC-frames.

0: idle (continuous 1 s),

1: flags (sequence of patterns: “0111 1110”)

Note: In TE- and LT-T-applications with D-channel access handling (collision resolution), the only possible inter-frame time fill signal is idle (continuous 1s). Otherwise the D-channel on the S/ T-bus cannot be accessed.

4.3.37 MOSR - MONITOR Status Register (Read)

Value after reset: 00_H

	7							0	
MOSR	MDR1	MER1	MDA1	MAB1	MDR0	MER0	MDA0	MAB0	(BA)

MDR1 ... MONITOR channel 1 Data Received

MER1 ... MONITOR channel 1 End of Reception

MDA1 ... MONITOR channel 1 Data Acknowledged

The remote end has acknowledged the MONITOR byte being transmitted.

MAB1 ... MONITOR channel 1 Data Abort

MDR0 ... MONITOR channel 0 Data Received

MER0 ... MONITOR channel 0 End of Reception

MDA0 ... MONITOR channel 0 Data Acknowledged

The remote end has acknowledged the MONITOR byte being transmitted.

MAB0 ... MONITOR channel 0 Data Abort

4.3.38 MOCR - MONITOR Control Register (Write)

Value after reset: 00_H

	7							0	
MOCR	MRE1	MRC1	MIE1	MXC1	MRE0	MRC0	MIE0	MXC0	(BA)

MRE1 ... MONITOR receive interrupt enable (IOM-channel 1)

MONITOR interrupt status MDR1 generation is enabled (1) or masked (0).

MRE0 ... MONITOR receive interrupt enable (IOM-channel 0)

MONITOR interrupt status MDR0, MER0 generation is enabled (1) or masked (0).

MRC1, 0 ... Determines the value of the MR-bit:

0: Determines the value of the MR-bit: MR always “1”. In addition, the MDR1/MDR0 interrupt is blocked, except for the first byte of a packet (if MRE 1/0=1).

1: MR internally controlled by the IPAC according to MONITOR channel protocol. In addition, the MDR1/MDR0-interrupt is enabled for all received bytes according to the MONITOR channel protocol (if MRE1,0=1).

MIE1 ... MONITOR interrupt enable (IOM-channel 1)

MONITOR interrupt status MER1, MDA1, MAB1 generation is enabled (1) or masked (0).

MIE0 ... MONITOR interrupt enable (IOM-channel 0)

MONITOR interrupt status MDA0, MAB0 generation is enabled (1) or masked (0).

MXC1, 0 ... MX Bit Control (IOM-channel 1,0)

Determines the value of the MX-bit:

0.. MX always “1”.

1.. MX internally controlled by the IPAC according to MONITOR channel protocol.

4.4 General IPAC Registers

4.4.1 CONF - IPAC Configuration Register (Read/Write)

Value after reset: 00_H

	7							0	
CONF	AMP	CFS	TEM	PDS	IDH	SGO	ODS	IOF	(C0)

AMP ... Amplification of S/T receiver

0: an external transformer of ratio 2:1 is connected to the receive lines.

1: an external transformer of ratio 1:1 is connected to the receive lines.

CFS ... Configuration Select

This bit determines clock relations and recovery on S/T and IOM interfaces.

- TE and LT-T Modes

  0: The IOM interface clock and frame signals are always active, "Power Down" state included.

  The states "Power Down" and "Power Up" are thus functionally identical except for the indication: PD = 1111 and PU = 0111.

  With the C/I command Timing (TIM) the processor can enforce the "Power Up" state.

  With C/I command Deactivation Indication (DIU) the "Power Down" state is reached again.

  However, it is also possible to activate the S-Interface directly with the C/I command Activate Request (AR 8/10/L) without the TIM command.

  1: The IOM interface clock and frame signals are normally inactive ("Power Down").

  For activating the IOM-2 clocks the "Power Up" state can be induced by software (SPU-bit in SPCR register) or by resetting again CFS.

  After that the S-interface can be activated with the C/I command Activate Request (AR 8/10/L). The "Power Down" state can be reached again with the C/I command Deactivation Indication (DIU).

  Note: After reset the IOM interface is always active. To reach the "Power Down" state the CFS-bit has to be set.

- LT-S Mode

  CFS has to be set to "0" always.

TEM ... Test Mode

In test mode (TEM=1) all layer-1 functions are disabled and the IPAC behaves like a D-Channel HDLC controller (e.g. ICC PEB 2070) with a two channel HDLC communications controller (e.g. HSCX-TE PSB 21525).

PDS ... Phase Deviation Select

Defines the phase deviation of the S-transceiver in TE or LT-T mode.
0: the phase deviation is two S-bits plus analog delay plus delay of the external circuitry.
1: the above phase deviation is reduced by 2 oscillator clocks (= 260 ns).

IDH ... IOM D-Channel Priority Handler

The state machine for D-channel priority handling on IOM-2 is

0: disabled

1: enabled

Note: This mode is used in intelligent NT applications.
The priority 8 or 10 is selected via bit SCFG:PRI.

SGO ... Stop/Go Bit Output (LT-T mode)

In LT-T mode the S/G bit can be output on pin AUX7. This may be used for test purposes in order to observe the Stop/Go indications.

0: Pin AUX7 has default I/O functionality.

1: The S/G bit is output on pin AUX7.

ODS ... Output Driver Selection

Defines the output driver of the IOM-2 interface:

0: open drain

1: push pull

IOF ... IOM OFF

0: IOM interface is operational

1: IOM interface is switched off (DU, DD, FSC, DCL, BCL/SCLK, SDS high impedant).

IOF should be set to ’1’ if external devices connected to the IOM interface should be “disconnected“ e.g. for power saving purposes or for not disturbing the internal IOM connection between layer 1 and layer 2. However, the IPAC internal operation between S-transceiver, B-channel and D-channel controller is independent of the IOF bit.

In Non-TE mode FSC and DCL (both input) are not switched off from the IOM-2 interface.

4.4.2 ISTA - IPAC Interrupt Status Register (Read)

Value after reset: 00_H

	7							0	
ISTA	INT1	INT0	ICD	EXD	ICA	EXA	ICB	EXB	(C1)

INT1, INT0 ... Interrupt 1/0 from external devices

A low level or negative state transition (programmable in ACFG: EL1, EL0) was detected at pin AUX6 or AUX7 respectively.

ICD ... Interrupt from D-Channel

An interrupt is caused by the D-channel, its source can be read in the interrupt status register of the D-Channel (ISTAD).

EXD ... Extended Interrupt from D-Channel

An extended interrupt is caused by the D-channel, its source can be read in the extended interrupt status register of the D-Channel (EXIRD).

ICA, ICB ... Interrupt from B-Channel A, B

An interrupt is caused by the B-channel A, B. Its source can be read in the interrupt status register of the B-Channel A or B, respectively (ISTAB).

EXA, EXB ... Extended Interrupt from B-Channel A, B

An extended interrupt is caused by the B-channel A, B. Its source can be read in the extended interrupt status register of the B-Channel A or B, respectively (EXIRB).

4.4.3 MASK - IPAC Mask Register (Write)

Value after reset: $C0_H$

	7							0	
MASK	INT1	INT0	ICD	EXD	ICA	EXA	ICB	EXB	(C1)

Each interrupt source can selectively be masked by setting the respective bit in MASK (bit positions corresponding to ISTA register). Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the respective MASK bit is reset.

Note: In the event of an extended interrupt, no interrupt request will be generated with a masked ICD, EXD, ICA, EXA, ICB, EXB bit, although a bit is set in ISTAD, EXIRD, ISTAB or EXIRB.
After Reset all interrupts are enabled except INT1 and INT0.

4.4.4 ID - Identification Register (Read)

Value after reset: 01_H

	7							0	
ID									(C2)

ID ... Identification Number

The version number of the IPAC can be read from ID

01_H: Version 1.1

4.4.5 ACFG - Auxiliary Interface Configuration (Read/Write)

Value after reset: 00_H

	7							0	
ACFG	OD7	OD6	OD5	OD4	OD3	OD2	EL1	EL0	(C3)

OD7 - OD2 ... Output Driver Select for AUX7 - AUX2

0: output is open drain

1: output is push/pull

Note: The ODx configuration is only valid, if the corresponding output is enabled in the AOE register.
AUX2 is only available in TE mode and not in LT modes.
In LT modes AUX 3-5 is only available if the PCM interface is disabled (PCFG:PLD=1).
In TE mode the host must set PCFG:PLD=1 before the output driver is selected.

EL1, EL0 ... Edge / Level Triggered Interrupt Input for $\overline{\text{INT1}}$, $\overline{\text{INT0}}$

0: a negative level ...

1: a negative edge ... on $\overline{\text{INT1/0}}$ (pins AUX7/6) generates an interrupt to the IPAC.

An interrupt is only generated to the IPAC, if the corresponding mask bit in MASK is reset.

Note: This configuration is only valid, if the corresponding output enable bit in AOE is disabled.

4.4.6 AOE - Auxiliary Output Enable (Read/Write)

Value after reset: FC_H

	7							0	
AOE	OE7	OE6	OE5	OE4	OE3	OE2	0	0	(C4)

OE7 - OE2 ... Output Enable for AUX7-2

0: Pin AUX7-2 is configured as output. The value of the corresponding bit in the ATX register is driven on AUX7-2.

1: Pin AUX7-2 is configured as input. The value of the corresponding bit can be read from the ARX register.

Note: If pins AUX7, AUX6 are to be used as interrupt input, OE7,OE6 must be set to 1.
Pin AUX2 is only available in TE mode and not in LT modes.
In LT modes the pins AUX 3-5 are only available if the PCM interface is disabled (PCFG:PLD=1).
The general purpose I/O pins are input after reset (OEx=1).

4.4.7 ARX - Auxiliary Interface Receive Register (Read)

Value after reset: (not defined)

	7							0	
ARX	AR7	AR6	AR5	AR4	AR3	AR2	0	0	(C5)

AR7-AR2 ... Auxiliary Receive

The value of AR7-AR2 reflects the level at pin AUX7-AUX2 at that time when ARX is read by the host. If the mask bit for AUX7,6 is set in the MASK register, no interrupt is generated to the IPAC, however, the current state at pin AUX7,6 can be read from AR7,6.

Note: Pin AUX2 is only available in TE mode and not in LT modes.
In LT modes the pins AUX 3-5 are only available if the PCM interface is disabled (PCFG:PLD=1).

4.4.8 ATX - Auxiliary Interface Transmit Register (Write)

Value after reset: 00_H

	7							0	
ATX	AT7	AT6	AT5	AT4	AT3	AT2	0	0	(C5)

AT7-AT2 ... Auxiliary Transmit

A ’0’ or ’1’ in AT7-AT2 will drive a low or high level at pin AUX7-AUX2, if the corresponding output is enabled in the AOE register.

Note: AUX2 is only available in TE mode and not in LT modes.
In LT modes AUX 3-5 is only available if the PCM interface is disabled (PCFG:PLD=1).

4.4.9 PITA1/2 - PCM Input Time Slot Assignment B1/B2 (Read/Write)

Value after reset: 00_H

	7				0	
PITA1/ PITA2	ENA	DUDD	0	TNRX		(C6/C7)

PITA1 refers to the B1-channel and PITA2 to the B2-channel of the IOM channel which is selected by PCFG:CSL2-0.

ENA ... Enable PCMIN channel

0: Disables...

1: Enables ... reception of data in from the PCM interface line PCMIN.

Note: Data from an external controller is received on the PCM interface by the IPAC. This data is then mapped to the corresponding B1/B2 channel of the IOM-2 DU line (default) or DD line.

DUDD ... Switch on IOM-2 DU/DD line

The selected PCM timeslot on the PCMIN line is mapped to the

0: DU-line (default)

1: DD-line ... of the IOM-2 interface.

TNRX ... Time Slot Number Receive

Selects one of up to 32 possible timeslots (00h-1Fh) in which data is received from the PCM interface.

Note: The configuration of the PCM timeslots is equal for B1 and B2-channel.

4.4.10 POTA1/2 - PCM Output Time Slot Assignment B1/B2 (Read/Write)

Value after reset: 00_H

	7				0	
POTA1	ENA	DUDD	0	TNTX		(C8)

	7				0	
POTA2	ENA	DUDD	SRES	TNTX		(C9)

POTA1 refers to the B1-channel and POTA2 to the B2-channel of the IOM channel which is selected by PCFG:CSL2-0.

ENA ... Enable PCMOUT channel

0: Disables...

1: Enables ... transmission of data on the PCM interface line PCMOUT.

Note: Data is transmitted by the IPAC on the PCM interface to an external device. This data may be originated from the B1/B2 channel of the IOM-2 DD-line (default) or DU-line.

DUDD ... Switch on IOM-2 DU/DD line

The selected PCM timeslot on the PCM interface is mapped to the

0: DD-line (default)

1: DU-line ... of the IOM-2 interface.

SRES... Software Reset

0: Deactivates ...

1: Activates ... the internal RESET state of the IPAC.

The RESET state is activated to the internal blocks of the IPAC when a ’1’ is written to SRES and it is active until the SRES-bit is set to ’0’ again, i.e. the host must ensure the required RESET timing of the IPAC which is 4 ms.

TNTX ... Time Slot Number Transmit

Selects one of up to 32 possible timeslots (00h-1Fh) in which data is transmitted to the PCM interface.

Note: The configuration of the PCM timeslots is equal for B1 and B2-channel.

4.4.11 PCFG - PCM Configuration Register (Read/Write)

Value after reset: 00_H

	7							0	
PCFG	DPS	ACL	LED	PLD	FBS	CSL2	CSL1	CSL0	(CA)

DPS ... Data Path Select

Data from the B-channel FIFOs is exchanged with the

0: IOM-2 interface

1: PCM interface

ACL ... ACL Function Select

0: pin ACL indicates the S-bus activation status by a LOW level

1: the state at pin ACL is programmable by the host via bit LED.

LED ... LED Control

If enabled (ACL=1) the LED connected to pin ACL is switched

0: Off

1: On

Note: The state (log. high/low) on pin ACL is derived from the inverted state of PCFG:LED. For ACL=0 the state of PCFG:LED has no effect.

PLD ... PCM Lines Disable (LT-S and LT-T modes)

0: AUX3-5 are used for PCM interface (default)

1: AUX3-5 are used as normal I/O lines (PCM interface disabled)

Note: In TE mode PLD must be set to '1' before AUX3-5 are used as I/O lines.

FBS ... FSC/BCL Output Select (LT-S and LT-T modes)

0: FSC is output on AUX3, which is derived from the DCL input by division of 192.

1: BCL single bit clock is output on AUX3. It is derived from the DCL input by division of 2.

Note: SCLK output provides 1.536 MHz in LT-T mode. This may be used for the DCL input. This bit is ignored in TE mode.

CSL2-0 ... IOM-2 Channel Selection for PCM (LT-S and LT-T modes)

Selects one of eight IOM channels to which the PCM interface is connected to.

000: channel 0
001: channel 1
: :
111: channel 7

Note: These bits are ignored in TE mode.

4.4.12 SCFG - SDS Configuration Register (Read/Write)

Value after reset: 00_H

	7				0	
SCFG	PRI	TXD	TLEN	TSLT		(CB)

PRI ... Priority for D-channel Handler (only in LT-S mode in intelligent NT)

Determines the priority of D-channel access on IOM-2 for the D-channel controller on the IPAC and for external D-channel sources connected to the IOM-2 interface. The state machine for D-channel handling controls the S/G bit according to the setting of PRI and enables the access of internal or external D-channel sources.

0: Priority = 8

1: Priority = 10

Note: The read back value of PRI only contains the programmed value as soon as the state machine has switched to the selected priority.
The D-channel handler can be enabled/disabled via bit CONF:IDH.

TXD ... S-transmitter Disable

The transmitter of the S-transceiver can be disabled by setting TXD to “1“. This can be used to reduce power consumption (see **chapter 2.5.4**).

TLEN ... Timeslot Length

0: 8 bit

1: 16 bit

TSLT ... Timeslot Position

Selects one of 32 timeslots on the IOM-2 interface (with respect to FSC) during which SDS is active high. The data strobe signal allows standard data devices to access a programmable channel.

4.4.13 TIMR2 - Timer 2 Register (Read/Write)

Value after reset: 00_H

	7			0	
TIMR2	TMD	0	CNT		(CC)

TMD ... Timer Mode

Timer 2 can be used in two different modes of operation.

0: Count down timer. An interrupt is generated only once after a time period of 1 ... 63 ms.

1: Periodic timer. An interrupt is periodically generated every 1 ... 63 ms (see CNT).

CNT ... Timer Count

0: Timer off

1 ... 63: Timer length = 1 ... 63 ms

By writing ’0’ to CNT, the timer is immediately stopped. A value different from that determines the time period after which an interrupt will be generated.

If the timer is already started with a certain CNT value and is written again before an interrupt has been released, the timer will be reset to the new value and restarted again.

An interrupt is indicated to the host in ISTAD:TIN2.

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 150	°C
Maximum voltage on V_{DD}	V_{DD}	7	V

Note: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device.
Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.
This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse (**figure 99**).

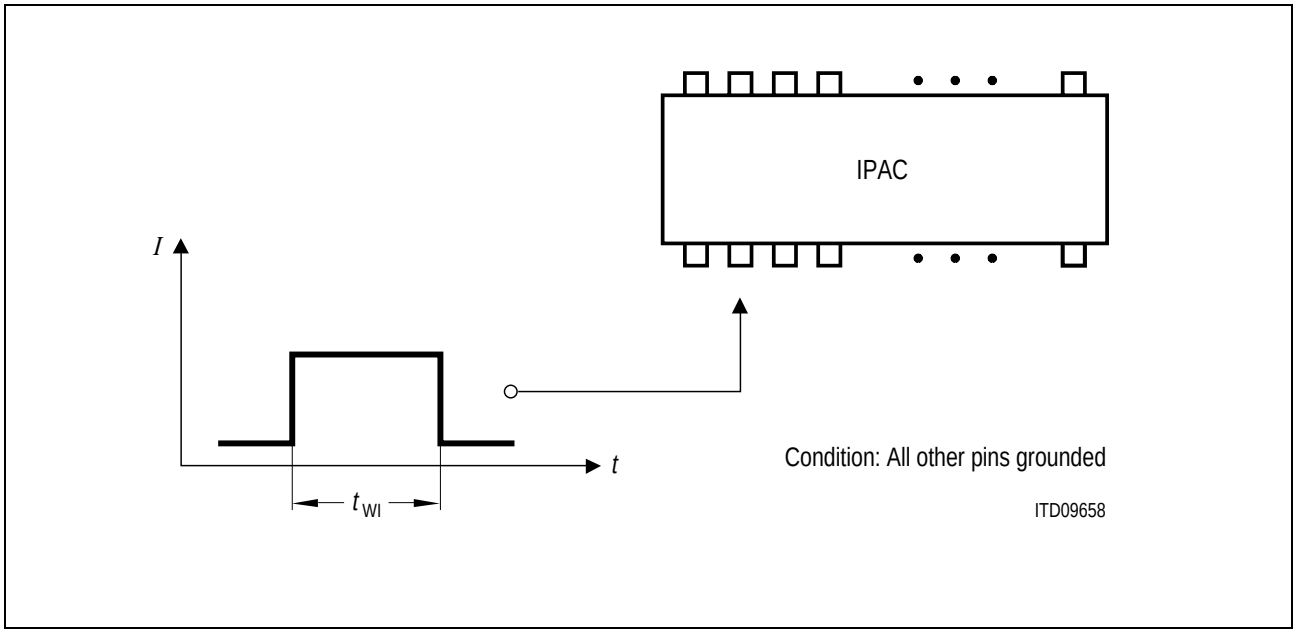


Figure 99 Test Condition for Maximum Input Current

Line Input Current

The destruction limits are given in **figure 100**.

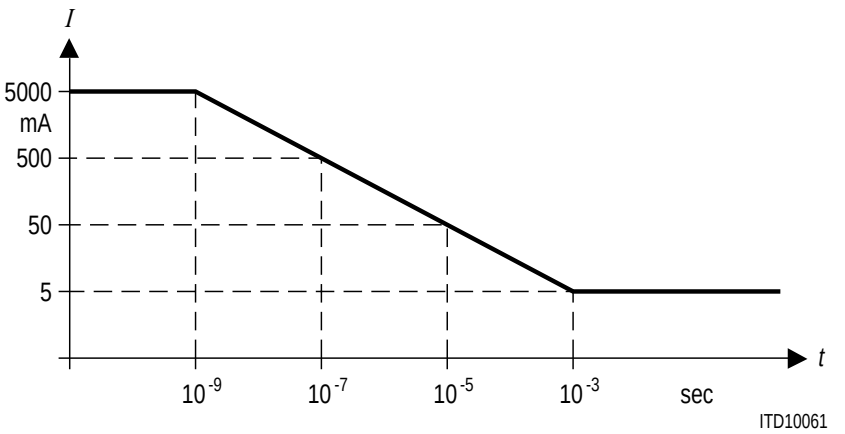


Figure 100 Maximum Line Input Current

DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{DDA} = 5 V ± 5 %, V_{SS} = 0 V, V_{SSA} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition		Remarks
		min	max				
L-input voltage	V_{IL}	– 0.3	0.8	V			All pins except SX1,2, SR1,2 XTAL1/2
H-input voltage	V_{IH}	2.0	V_{DD} + 0.3	V			
L-output voltage	V_{OL}		0.45	V	I_{OL} = 7 mA (DU, DD, C768) I_{OL} = 5 mA ($\overline{ACL}$, AUX6,7, AD0-7) I_{OL} = 2 mA (all others)		
H-output voltage	V_{OH}	2.4		V	I_{OH} = – 5 mA (AD0-7) I_{OH} = – 400 µA (all others)		
H-output voltage	V_{OH}	V_{DD} – 0.5		V	I_{OH} = – 100 µA		
Power supply current - power down	I_{CC}		3	mA		V_{DD} = 5 V Inputs at V_{SS} / V_{DD} No output loads	
Power supply current - operational			20	mA	DCL=1536 kHz (96 kHz test pulse)	V_{DD} = 5 V Inputs at V_{SS} / V_{DD} No output loads (including SX1, 2)	
			20	mA	DCL=1536 kHz ($B1=B2=FF_H$, D=1)		
			25	mA	DCL=4096 kHz ($B1=B2=FF_H$, D=1)		

DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{DDA} = 5 V ± 5 %, V_{SS} = 0 V, V_{SSA} = 0 V (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition	Remarks
		min	max			
Input leakage current	I_{LI}		1	µA	0 V < V_{IN} < V_{DD}	All pins except SX1,2, SR1,2 XTAL1/2, AUX7/6
Output leakage current	I_{LO}		1	µA	0 V < V_{OUT} < V_{DD}	
Input leakage current internal pull-up	I_{LIPU}	50	200	µA	0 V < V_{IN} < V_{DD}	AUX7/6
Absolute value of output pulse amplitude (VSX2 – VSX1)	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω R_L = 400 Ω	SX1,2
Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω	
Transmitter output impedance	Z_X	10 0		kΩ Ω	Inactive or during binary one during binary zero R_L = 50 Ω	
Receiver input impedance	Z_R	30		kΩ	V_{DD} = 5 V	SR1,2

Note: Due to the transformer, the load resistance seen by the circuit is four times R_L.

Capacitances

T_A = 25 °C, V_{DD} = 5 V ± 5 %, V_{SSA} = 0 V, V_{SSD} = 0 V, f_c = 1 MHz, unmeasured pins grounded.

Table 28 Capacitances

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input Capacitance I/O Capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	All pins except SX1,2 and XTAL1,2
Output Capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Load Capacitance	C_L		50	pF	XTAL1,2

Recommended Oscillator Circuits

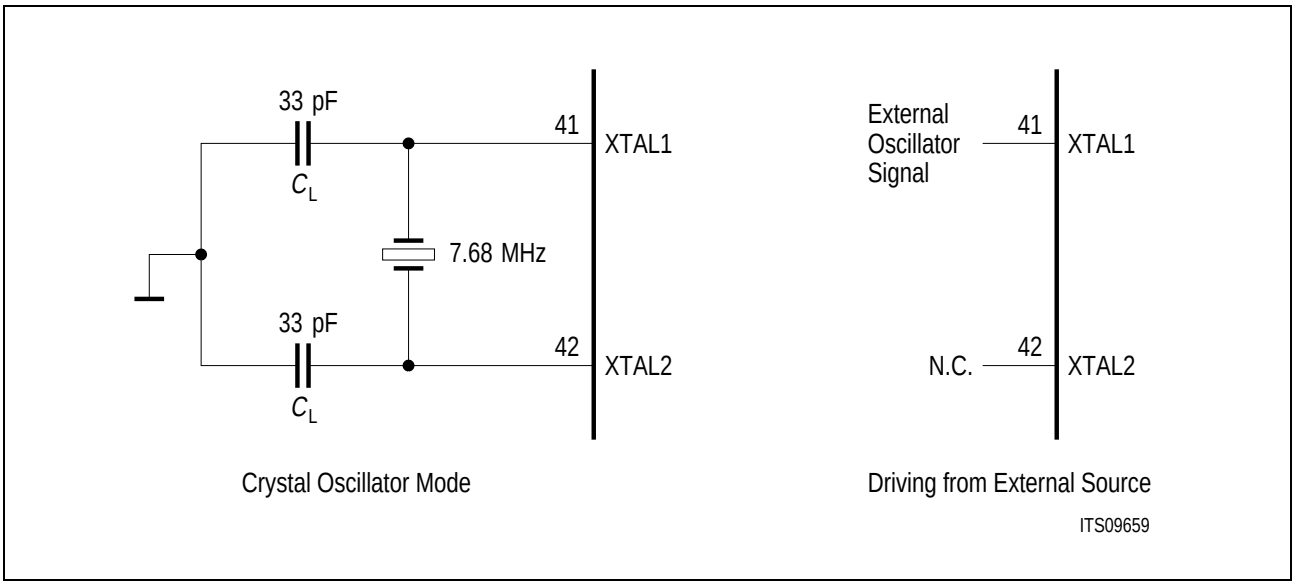


Figure 101 Oscillator Circuits

Crystal Specification

Parameter	Symbol	Limit Values	Unit
Frequency	f	7.680	MHz
Frequency calibration tolerance		max. 100	ppm
Load capacitance	C_L	max. 50	pF
Oscillator mode		fundamental	

Note: The load capacitance C_L depends on the recommendation of the crystal specification. Typical values for C_L are 22 ... 33 pF.

XTAL1 Clock Characteristics (external oscillator input)

Parameter	Limit Values	
	min.	max.
Duty cycle	1:2	2:1

AC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.45 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **figure 102.**

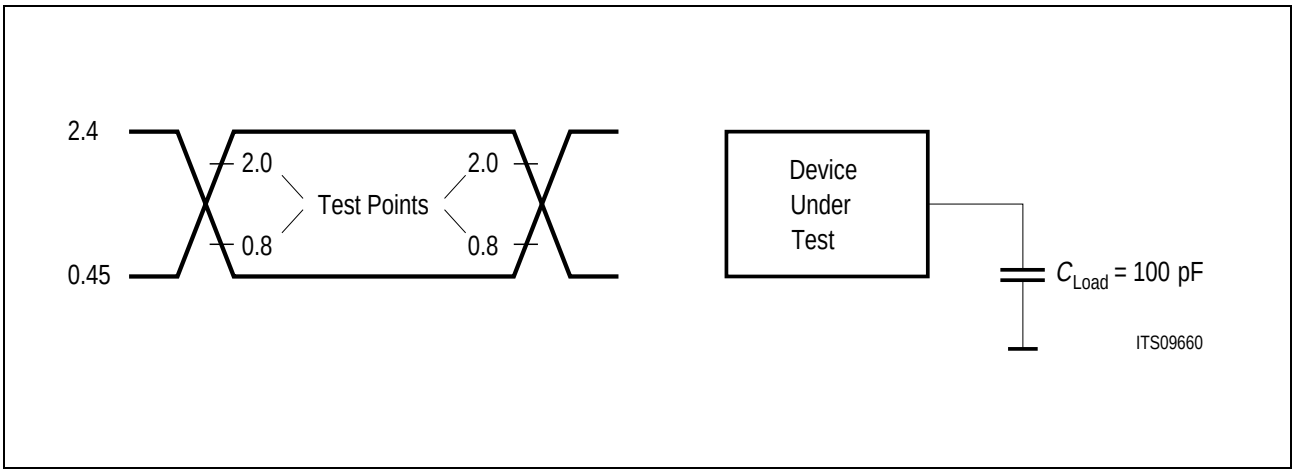


Figure 102 Input/Output Waveform for AC Tests

Microprocessor Interface Timing

Siemens/Intel Bus Mode

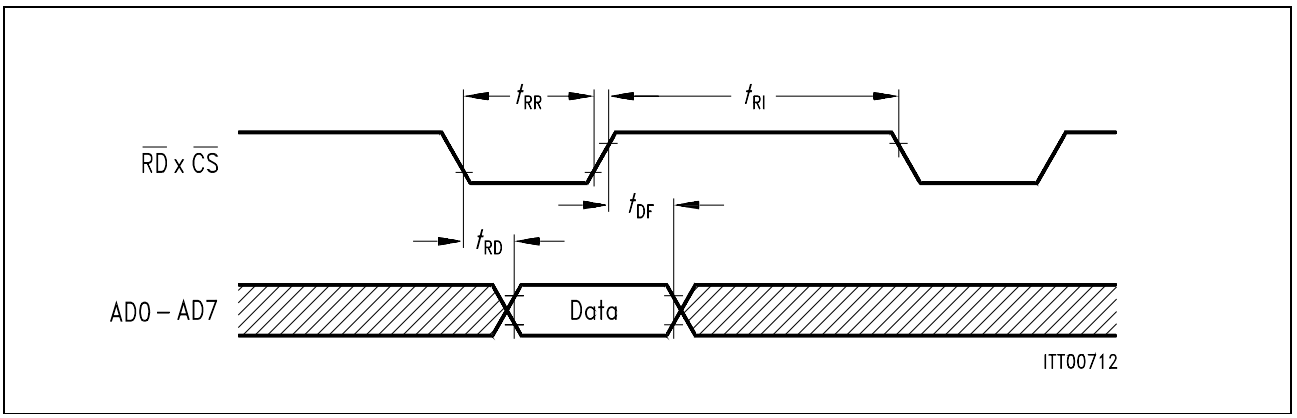


Figure 103 Microprocessor Read Cycle

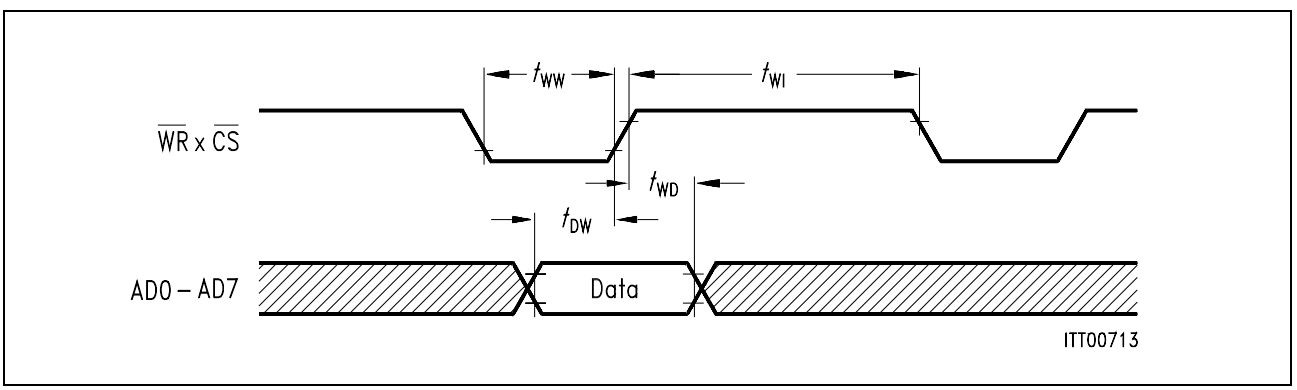


Figure 104 Microprocessor Write Cycle

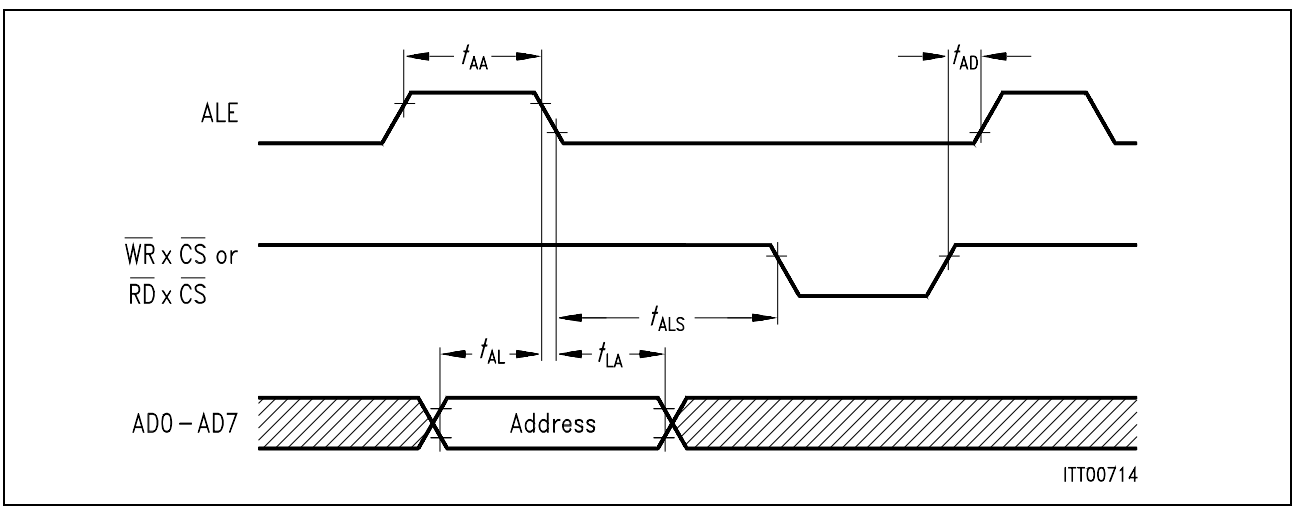


Figure 105 Multiplexed Address Timing

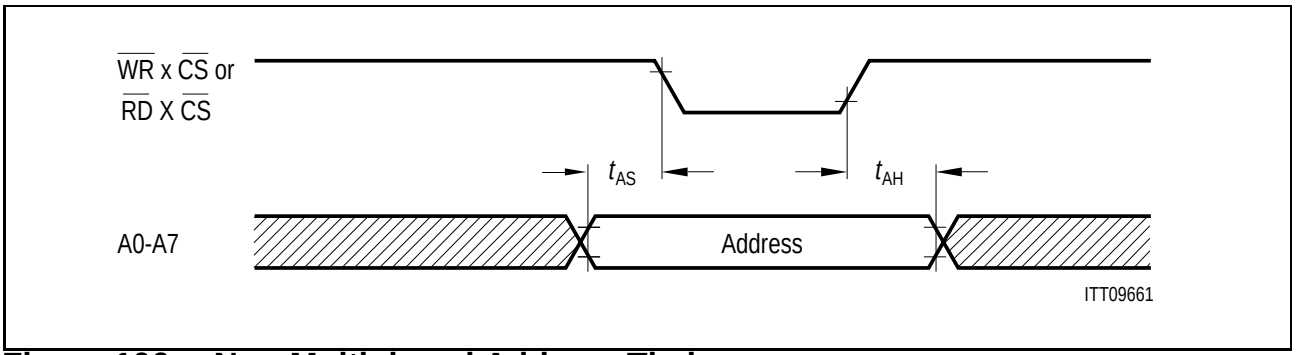


Figure 106 Non-Multiplexed Address Timing

Motorola Bus Mode

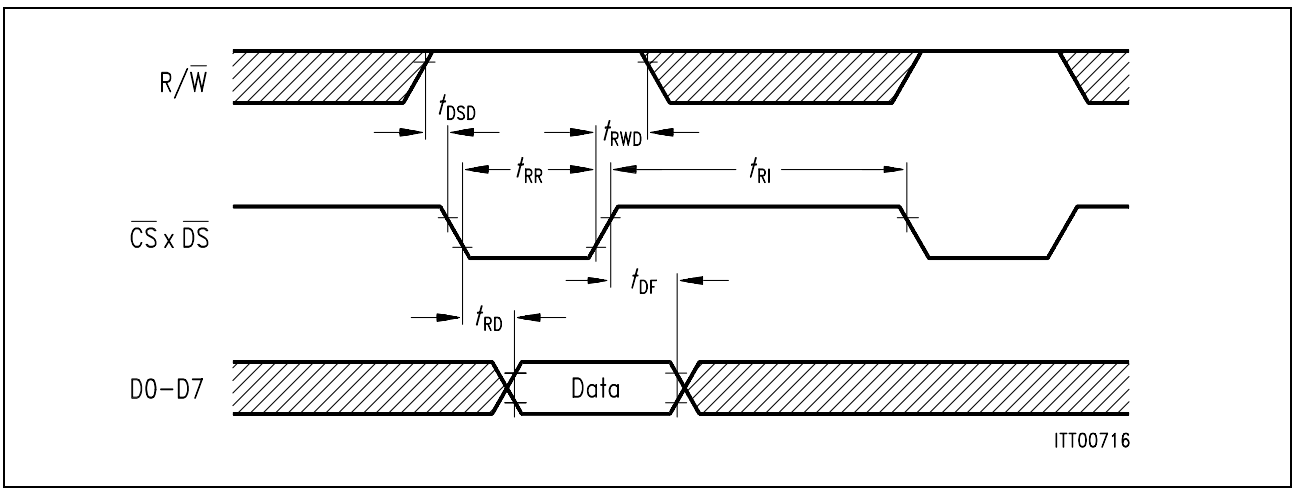


Figure 107 Microprocessor Read Timing

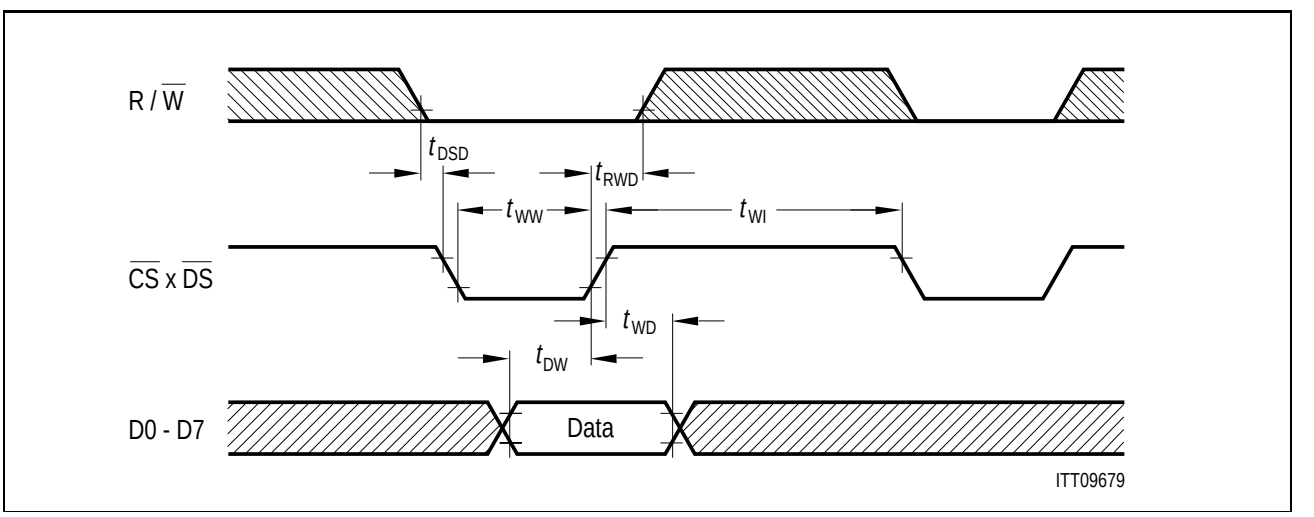


Figure 108 Microprocessor Write Cycle

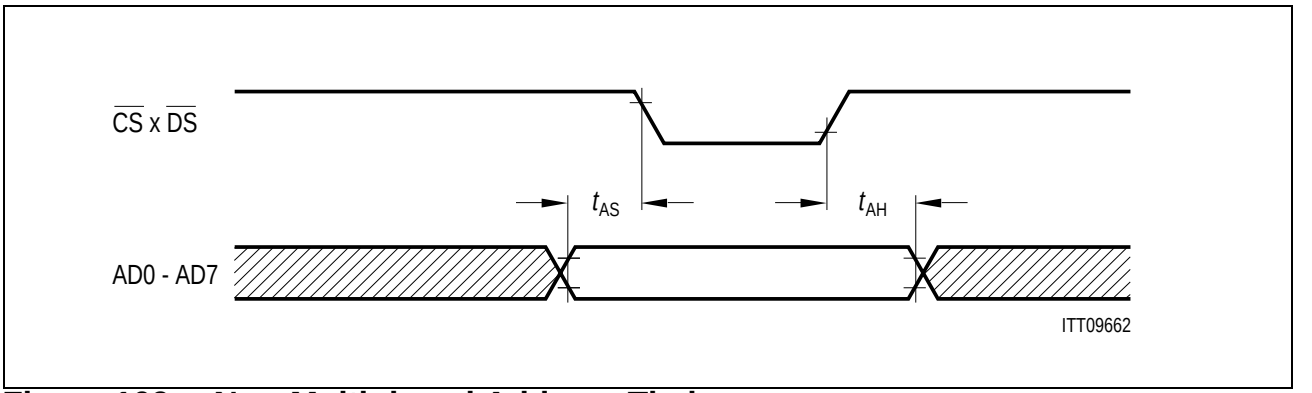


Figure 109 Non-Multiplexed Address Timing

Microprocessor Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time	t_{AS}	25		ns
Address hold time	t_{AH}	10		ns
ALE guard time	t_{AD}	15		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{W}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	35		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{W}$ control interval	t_{WI}	70		ns
R/$\overline{W}$ hold from $\overline{CS}$ x $\overline{DS}$ inactive	t_{RWD}	tbd		ns

Serial Interface Timing

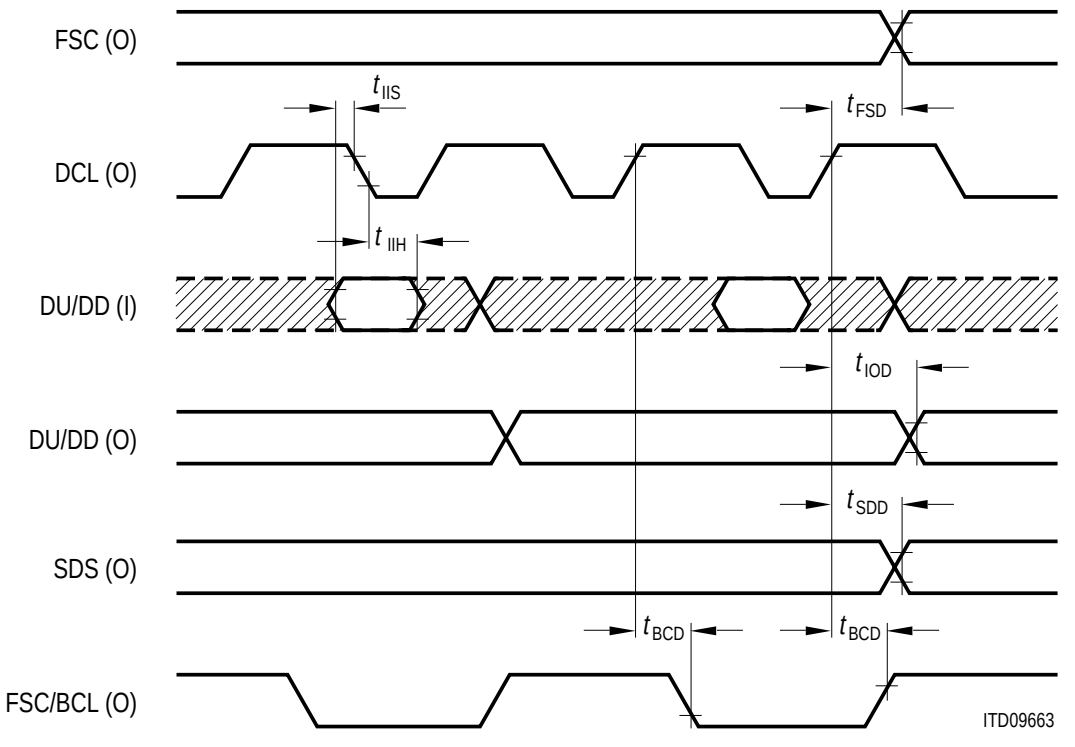


Figure 110 IOM® Timing (TE mode)

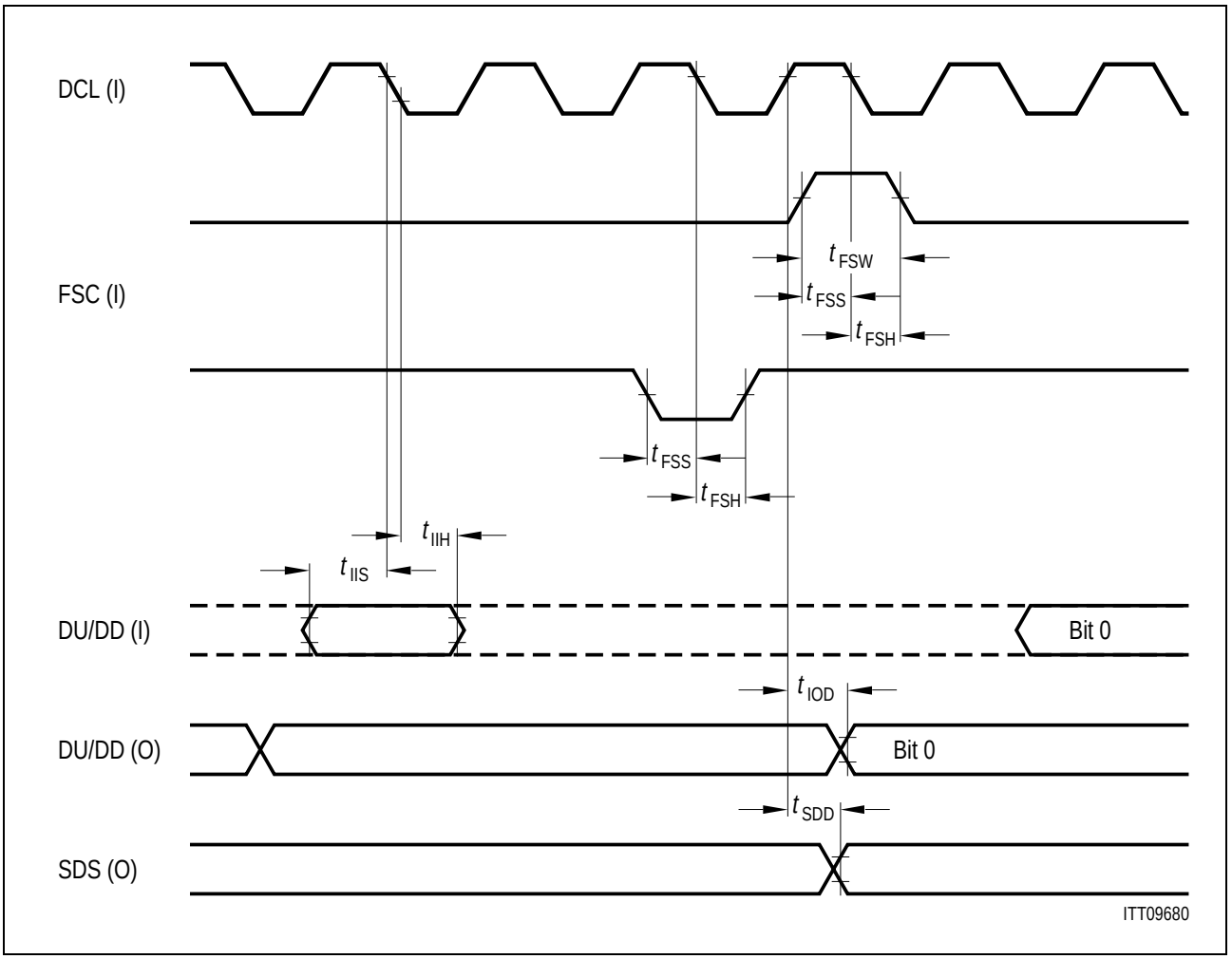


Figure 111 IOM® Timing (LT-S, LT-T mode)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
IOM output data delay	t_{IOD}		100	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	20		ns
FSC strobe delay	t_{FSD}	-100	20	ns
Strobe signal delay	t_{SDD}		120	ns
BCL / FSC delay	t_{BCD}		100	ns
Frame sync setup	t_{FSS}	50		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

PCM Interface Timing

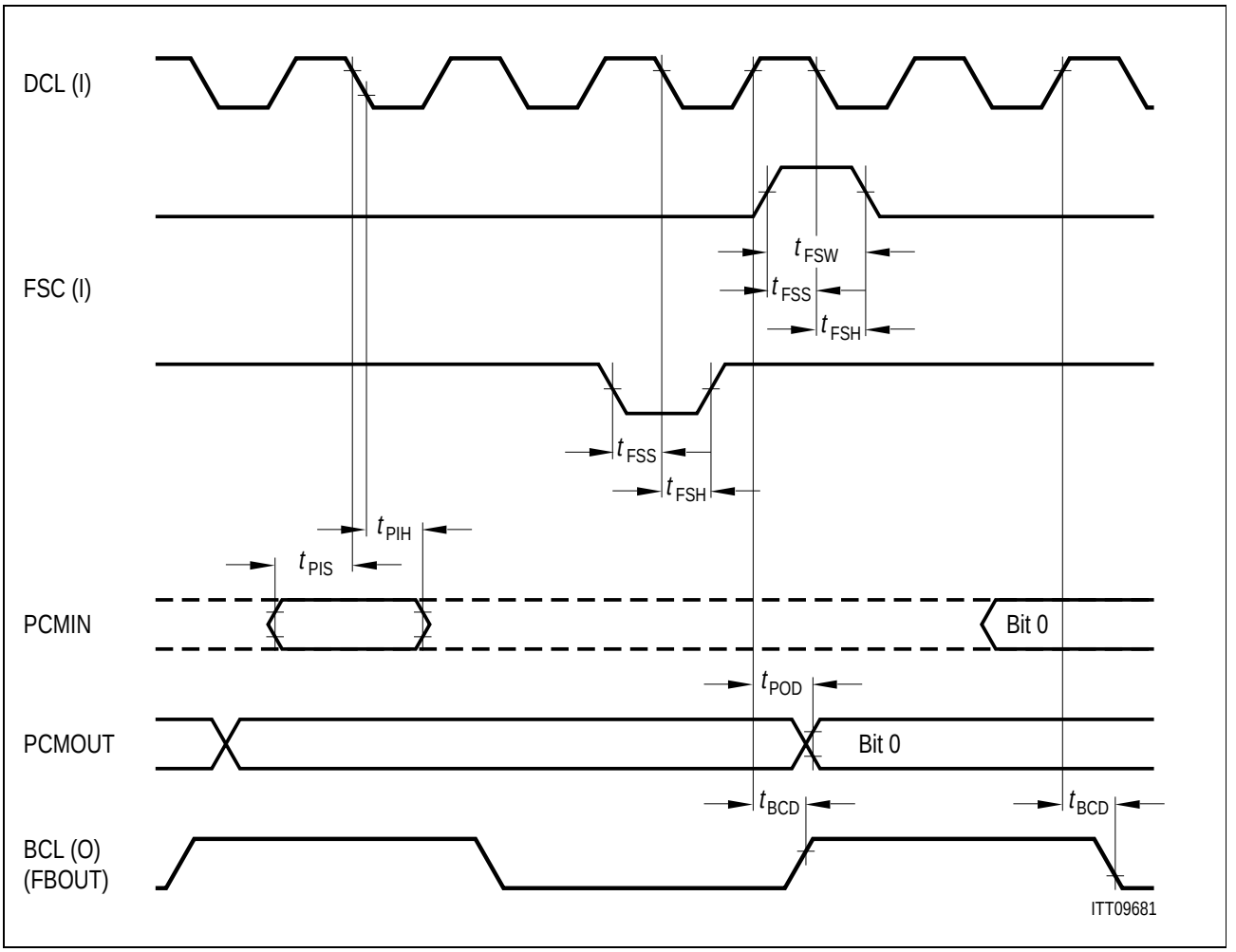


Figure 112 PCM Interface Timing (LT-S, LT-T mode)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM output data delay	t_{POD}		100	ns
PCM input data setup	t_{PIS}	20		ns
PCM input data hold	t_{PIH}	50		ns
BCL delay	t_{BCD}		100	ns
Frame sync setup	t_{FSS}	50		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

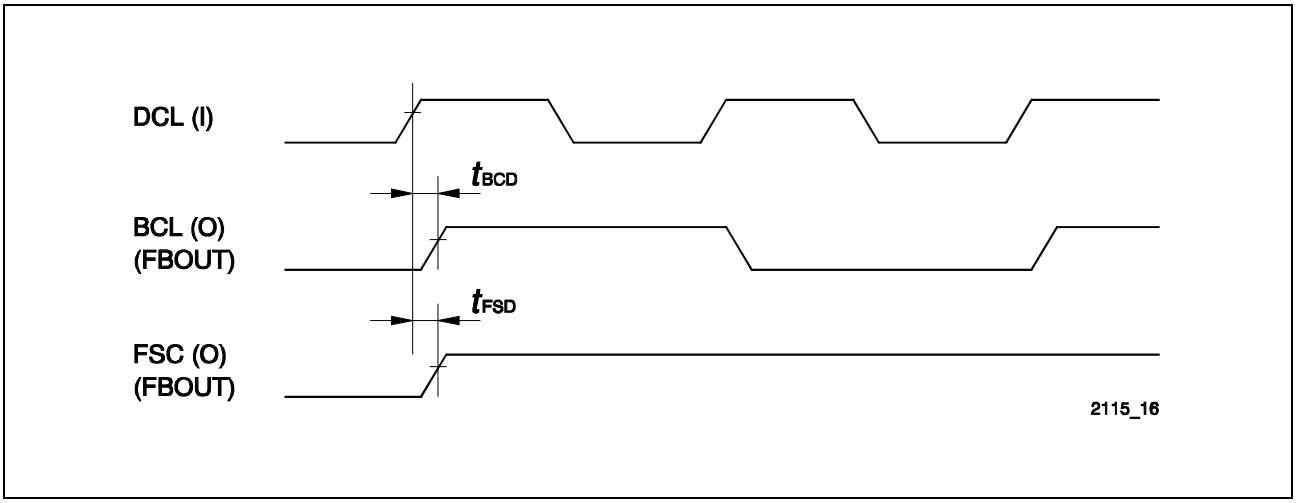


Figure 113 BCL, FSC Output Delay

Parameter	Symbol	Limit Values		Unit
		min.	max.	
BCL delay from DCL	t_{BCD}		100	ns
FSC delay from DCL	t_{FSD}		100	ns

Auxiliary Interface Timing

Certain pins from the auxiliary interface can be used as standard I/O pins (see **chapter 2.8**). Their timing conditions either as input or as output is shown in **figure 114**. The read and write signals indicate the corresponding access to the IPAC register, they are not control signals on the auxilliary interface.

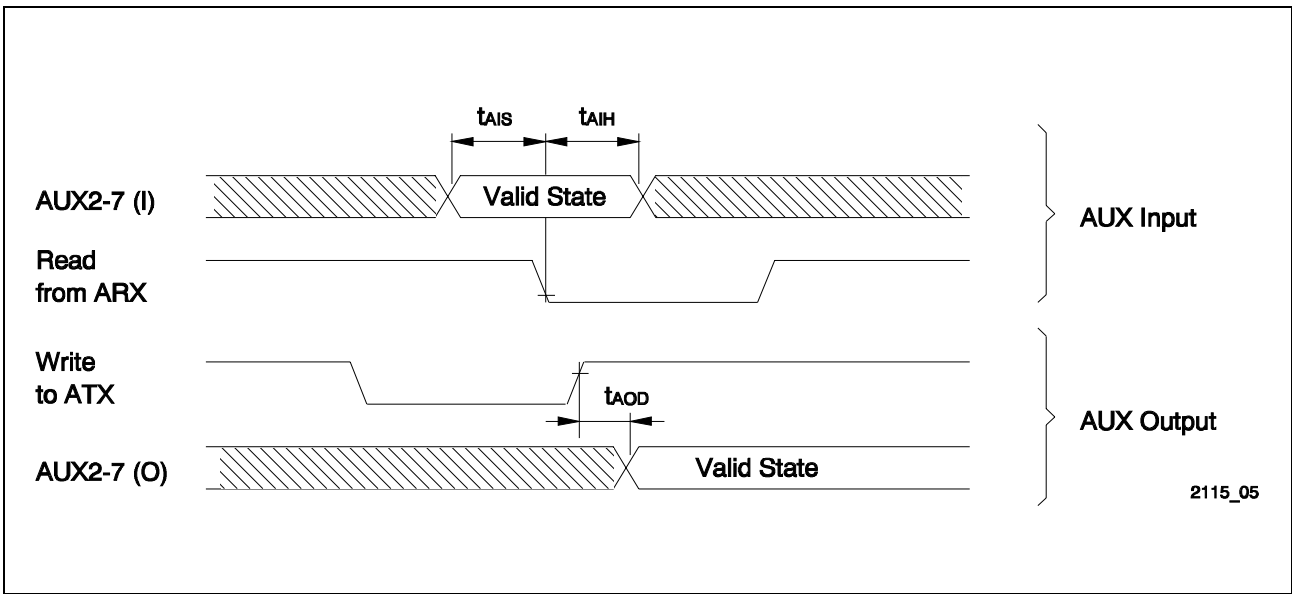


Figure 114 AUX Interface I/O Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Auxiliary input data setup	t_{AIS}	30		ns
Auxiliary input data hold	t_{AIH}	30		ns
Auxiliary output data delay	t_{AOD}		200	ns

Clock Timing

The clocks in the different operating modes are summarized in table below with the respective duty ratios.

Application	M0 M1	DCL	FSC	BCL / SCLK
TE	0 X	o: 1536 kHz 1:1	o: 8kHz 1:2	o: 768 kHz 1:1
LT-T	1 1	i: 4096 kHz (max.)	i: 8 kHz	o: 1536 kHz 1:1
LT-S	1 0	i: 4096 kHz (max.)	i: 8 kHz	o: DCL/2

Note: M0 and M1 denote the pins MODE0 and MODE1/$\overline{EAW}$, respectively.
In TE mode MODE 1 is don't care (used as $\overline{EAW}$ pin).
All output clocks are synchronous to the S-receiver.
BCL/SCLK output in LT-S mode is derived from the DCL input clock.

The 1536-kHz clock (TE mode) is phase-locked to the receive S signal, and derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal.

A phase tracking with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the "high" state of the 1536-kHz clock may be either reduced or extended by half of one 7.68-MHz period (duty ratio 4:5 or 5:4 instead of 5:5) once every 250 µs. Since the other signals are derived from this clock (TE mode), the "high" or "low" states may likewise be reduced or extended by the same amount once every 250 µs.

The phase relationships of the clocks are shown in **figure 115.**

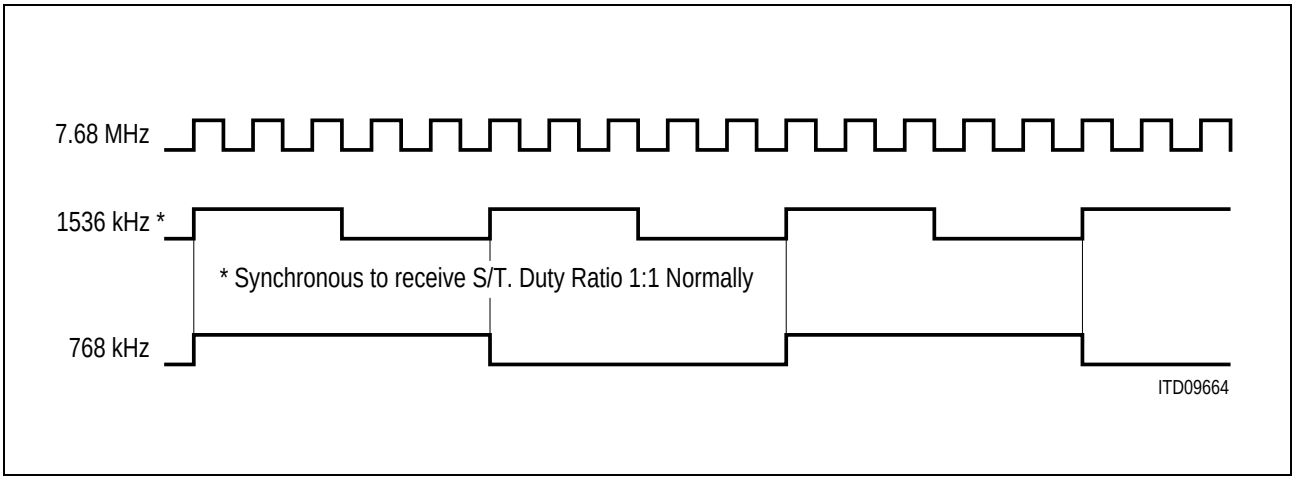


Figure 115 Phase Relationships of IPAC Clock Signals

The following tables give the timing characteristics of the clocks.

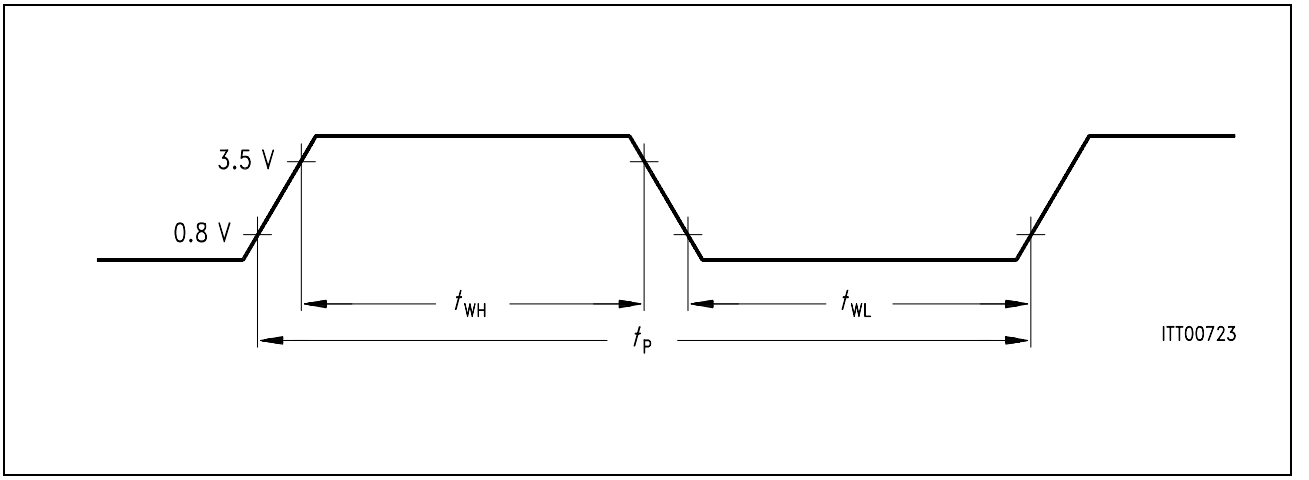


Figure 116 Definition of Clock Period and Width

DCL Clock Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
(TE) 1536 kHz	t_{PO}	585	651	717	ns	osc ± 100 ppm
	t_{WHO}	235	315	405	ns	osc ± 100 ppm
	t_{WLO}	300	315	350	ns	osc ± 100 ppm
(LT-S, LT-T) 4096 kHz	t_{PI}	240	244		ns	
	t_{WHI}	100			ns	
	t_{WLI}	100			ns	

Jitter

In TE mode, the timing extraction jitter of the IPAC conforms to CCITT Recommendation I.430 (– 7% to + 7% of the S-interface bit period).

In the LT-S applications, the clock input FSC is used as reference clock to provide the 192-kHz clock for the S-line interface. In the case of a plesiochronous 7.68-MHz clock generated by an oscillator, the clock FSC should have a jitter less than 100 ns peak-to-peak. (In the case of a zero input jitter on FSC the IPAC generates at most 65 ns "self-jitter" on the S interface.)

In the case of a synchronous (fixed divider ratio between XTAL1 and DCL) 7.68-MHz clock (input XTAL1), the IPAC transfers the input jitter of XTAL1, DCL and FSC to the S interface. The maximum jitter of the LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

Description of the Transmit PLL (XPLL) of the IPAC

Function of the XPLL

The XPLL generates a 1.536-MHz clock synchronized to the FSC 8-kHz clock by modification of the counter's divider ratio. The 1.536-MHz clock is then divided to 192 kHz and 8 kHz. The 8 kHz is used as the looped back clock and compared to the FSC 8-kHz in the phase detector.

Jitter considerations in case of a synchronous 7.68-MHz clock

After the XPLL has locked once, no more tracking steps are performed because there is a fixed divider ratio of 960 between 7.68 MHz and FSC. Therefore the input jitter at FSC and 7.68 MHz is transferred transparently to the S/T interface (192 kHz).

Jitter considerations in case of a plesiochronous 7.68-MHz clock (crystal)

Each tracking step of the XPLL produces an output jitter of 130 ns pp. In case of non-zero input jitter at DCL, this input jitter is increased by 130 ns pp. That means that the output jitter will not exceed 130 ns pp.

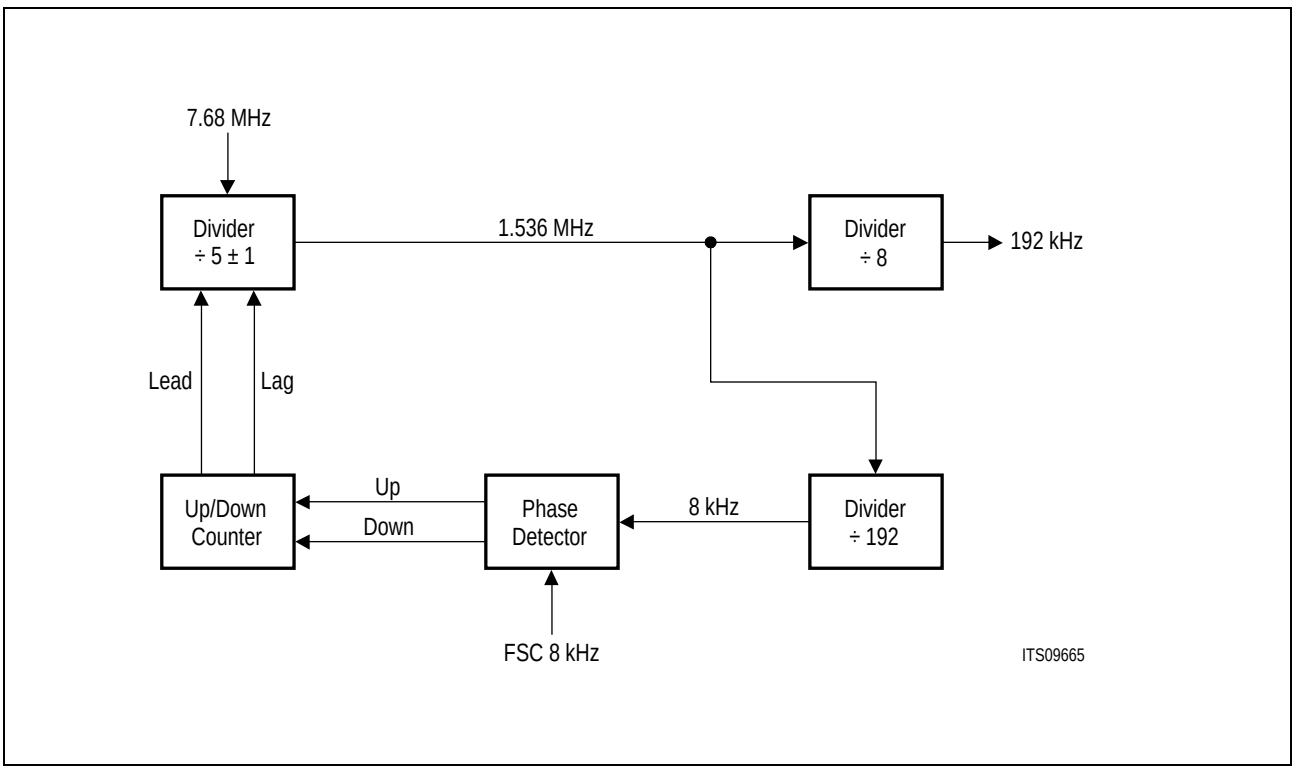


Figure 117 Block Diagram of XPLL

Description of the receive PLL (RPLL) of the IPAC

The receive PLL performs phase tracking each 250 µs after detecting the phase between the F/L transition of the receive signal and the recovered clock. Phase adjustment is done by adding or subtracting 65 ns to or from a 1.536-MHz clock cycle. The 1.536-MHz clock is than used to generate any other clock synchronized to the line.

During (re)synchronization an internal reset condition may effect the 1.536-MHz clock to have high or low times as short as 130 ns. After the S/T interface frame has achieved the synchronized state (after three consecutive valid pairs of code violations) the FSC output in TE mode is set to a specific phase relationship, thus causing once an irregular FSC timing.

Reset

Table 29 Reset Signal Characteristics

Parameter	Symbol	Limit Values	Unit	Test Conditions
		min.		
Length of active high state	t_{RST}	4	ms	Power On/Power Down to Power Up (Standby)
		2 x DCL clock cycles		During Power Up (Standby)

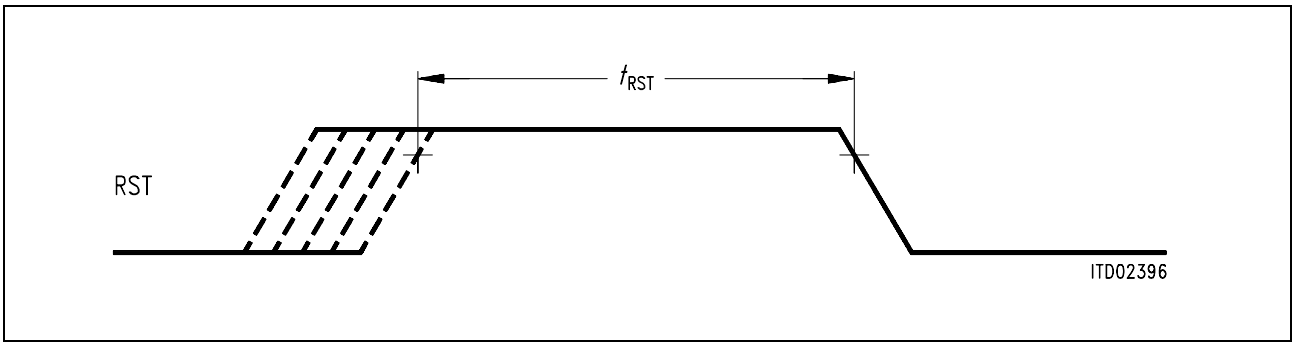
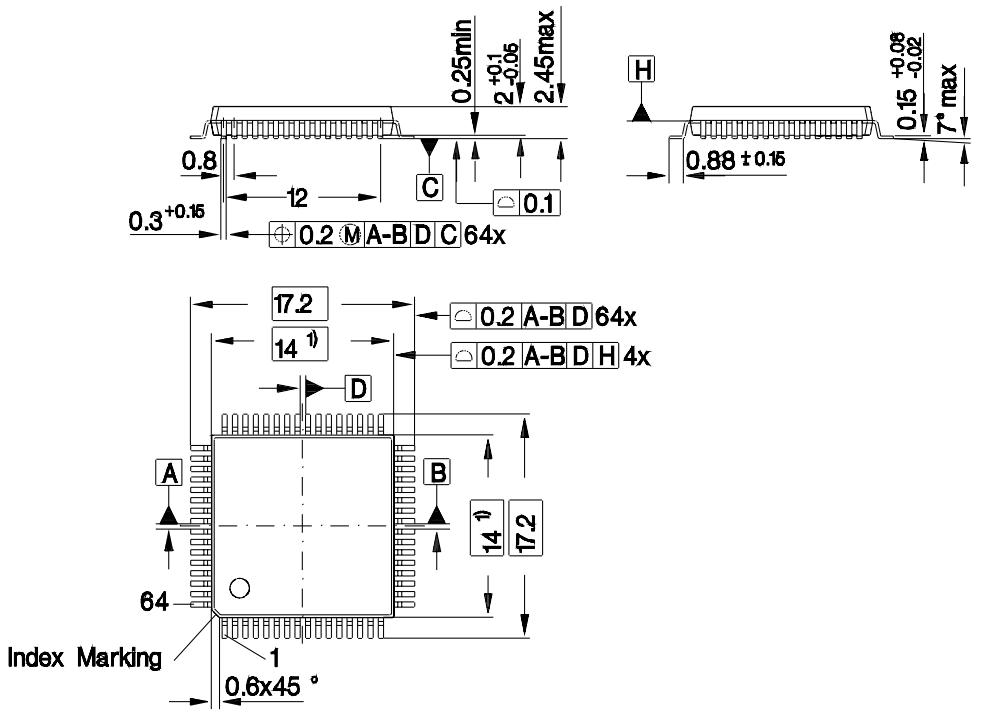


Figure 118 Reset Signal

6 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)

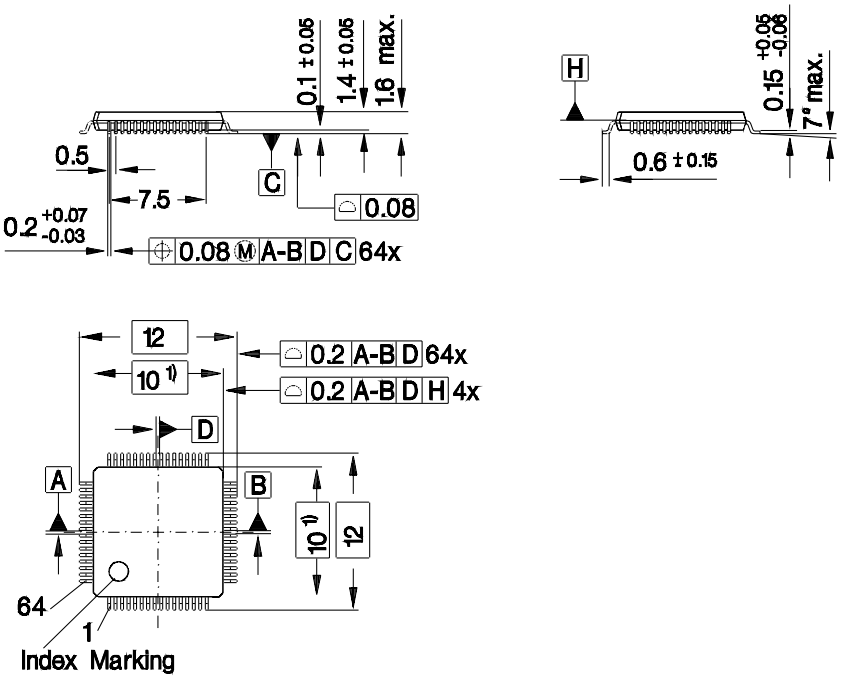


Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-64
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05613

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

7 Appendix

The following chapters contain a quick reference guide.

7.1 MON-8 Registers

MON-8 Configuration Register

In the configuration register the user programs the IPAC for different operational modes, and selects required S-bus features.

The following paragraphs describe the application relevance of all individual configuration register bits.

Address: 1h	MFD	0	FSMM	LP	SQM	RCVE	C/W/P	0	RD/WR

Value after Reset: 00_H

MFD	Multi-Frame-Disable. Selects whether multiframe generation (LT-S) or synchronization (TE, LT-T) is prohibited (MFD=1) or allowed (MFD=0). Enable multiframing if S/Q channel data transfer is desired. If MFD=1 no S/Q MONITOR messages are released. When reading this register the bit indicates whether multiframe synchronization has been established (MFD=1) or not (MFD=0).
FSMM	Finite State Machine Mode. By programming this bit the user has the possibility to exchange the state machines of LT-S and NT, i.e. an IPAC pin strapped for LT-S operates with a NT state machine. All other operation mode specific characteristics are retained. This function is used in intelligent NT configurations where the IPAC needs to be pin-strapped to LT-S mode but the state machine of an NT is desirable.
LP	Loop Transparency. In case analog loop-backs are closed with C/I = ARL or bit SC in the loop-back register, the user may determine with this bit, whether the data is forwarded to the S/T-interface outputs (transparent) or not. The default setting depends on the operational mode. TE/LT-T modes:0 =non transparent 1 =transparent ext. loop LT-S mode:0 =transparent 1 = non transparent In LT-S by default transparency is selected (LP=0), for LT-T and TE non-transparency is standard (LP=0).

SQM	Selects the SQ channel handling mode. In non-auto mode operation, the IPAC issues S1 and Q messages in the IOM-2 monitor channel only after a change has been detected. The S2 channel is not available in non-auto mode. In transparent mode monitor messages containing the S1, S2 and Q data are forwarded to IOM-2 once per multiframe (5 ms), regardless of the data content. Programming the SQM bit is only relevant if multiframing on S/T is selected (bit MFD configuration register). See also MON-1 and MON-2 monitor messages.
RCVE	Receive Code Violation Errors. The user has the option to issue a C/I error code (CVR) everytime an illegal code violation has been detected. The implementation is realized according to ANSI T1.605.
C/W/P	This bit has three different meanings depending on the operational mode of the IPAC: In **LT-S** mode the S/T bus configuration is programmed. For point-to-point or extended passive bus configurations an adaptive timing recovery must be chosen. This allows the IPAC to adapt to cable length dependent round trip delays. In **LT-T** mode the user selects the amount of permissible wander before a C/I code warning will be issued by the IPAC. The warning may be sent after 25 µs (C/W/P=1) or 50 µs (C/W/P=0). **Note:** The C/I indication SLIP which will be issued if the specified wander has been exceeded, is only a warning. Data has not been lost at this stage. In **TE** mode this bit is not used

MON-8 Loop-Back Register

The loop-back register controls all analog (S/T-interface) and digital (IOM-2 interface) loop-backs. Additionally the wake-up mode can be programmed.

Address: 2h	AST	SB1	SB2	SC	IB1	IB2	1	IB12	RD/WR

Value after Reset: 02_H

.

AST	Asynchronous Timing. Defines the length of the Timing signal (DU = 0) on IOM-2. If synchronous timing is selected (AST=0) the IPAC in LT-S mode will issue the timing request only in the C/I channel of the selected timeslot (C/I = 0000b). This mode is useful for applications where IOM-2 clock signals are not switched off. Here the IPAC can pass the TE initiated activation via C/I = 0000b in IOM-2 cannel 0 upstream to the U-interface device. In case IOM-2 clocks can be turned off during power-down or the LT-S IPAC is pin-strapped to a different timeslot than the U-interface device, synchronous timing signals will not succeed in waking the U-interface device. Under these circumstances asynchronous timing needs to be programmed (AST=1). Here the line DU is set to ZERO for a period long enough to wake any U-interface device, independent of timeslot or clocks. Typically asynchronous timing is programmed for intelligent NT applications (IPAC pin-strapped to LT-S with NT state machine). **Note:** The asynchronous timing option is restricted to configurations with the IPAC operating with NT state machine (i.e., LT-S pin-strap & FSMM bit programmed).
SB1	Closes the loop-back for B1 channel data close to the activated S/T-interface (i.e., loop-back IOM-2 data) in LT-S mode.
SB2	Closes the loop-back for B2 channel data close to the activated S/T-interface (i.e., loop-back IOM-2 data) in LT-S mode.
SC	Close complete analog loop-back (2B+D) close to the S/T-interface. Corresponds to C/I = ARL. Transparency is optional. Operational in LT-S mode.
IB1	Close the loop-back for B1 channel close to the IOM-2 interface (i.e. loop-back S/T data). Transparent. IB1 and IB2 may be closed simultaneously.

IB2	Close the loop-back for B2 channel close to the IOM-2 interface (i.e. loop-back S/T data). Transparent. IB1 and IB2 may be closed simultaneously.
IB12	Exchange B1 and B2 channels. IB1 and/or IB2 need to be programmed also. Loops back data received from S/T and interchanges it, i.e. B1 input (S/T) $\rightarrow$ B2 output (S/T) and vice versa.

MON-8 IOM®-2 Channel Register

The features accessible via the IOM-2 Channel register allow to implement simple switching functions. These make the IPAC the ideal device for intelligent NT applications. Please refer also to the section “IOM-2 channel switching”. Two types of manipulation are possible: the transfer from the pin-strapped IOM-2 channel (0 … 7) into IOM-2 channel 0 and a change of the B1, B2 and D data source.

Address: 3h	B1L	B1D	B2L	B2D	DL	0	CIL	CIH	RD/WR

Value after Reset: 00_H

B1L	Transfers the B1 channel from its pin-strapped location into IOM-2 channel 0.
B1D	Direction of the B1 channel. The normal direction (input/output) of DU and DD depends on the mode and is shown in **table 30** below. By setting B1D the direction for the B1 data channel is inverted.
B2L	Transfers the B2 channel from its pin-strapped location into IOM-2 channel 0.
B2D	Direction of the B2 channel. The normal direction (input/output) of DU and DD depends on the mode and is shown in **table 30** below. By setting B2D the direction for the B2 data channel is inverted.
DL	Transfers the D-channel from its pin-strapped location into IOM-2 channel 0.
CIL	C/I Channel location: The timeslot position of the C/I Channel can be programmed as “normal“ (LT-S and LT-T modes: pin strapped IOM-2 channel, TE mode: IOM-2 channel 0) or “fixed“ to IOM-2 channel 0 (regardless the selected mode).
CIH	C/I Channel handling: Normally the C/I commands are read from the pin-strapped IOM-2 channel. With this bit programmed C/I channel access is only possible via the SM/CI register.

Table 30 DU/DD Direction

	MODE0	**MODE1 /$\overline{\text{EAW}}$**	**Transmit data on S**	**Receive data on S**
TE-mode	0	$\overline{\text{EAW}}$	DU (input)	DD (output)
LT-T mode	1	1	DU (input)	DD (output)
LT-S mode	1	0	DD (input)	DU (output)

MON-8 SM/CI Register

This multifeature register allows access to the C/I channel and controls the monitor time-out.

Address: 4h	CI3	CI2	CI1	CI0	TOD	0	0	0	RD/WR

Value after Reset: $X0_H$ (X contains the C/I code)

C/I	Allows the user to access the C/I channel if the CIH bit in the IOM-2 register has been set previously. If the CIH bit was not programmed the content of the CI bits will be ignored and the IPAC will access the IOM-2 C/I channel. When reading the SM/CI register these bits will always return the current C/I indication (independent of CIH bit).
TOD	Time Out Disable. Allows the user to disable the monitor time-out function. Refer to section “Monitor Timeout” for details.

7.2 Register Address Arrangement

	7	6	5	4	3	2	1	0	
B-Channel Registers									
RFIFOB	B-Channel Receive FIFO								RD (00-1F/40-5F)
XFIFOB	B-Channel Transmit FIFO								WR (00-1F/40-5F)
ISTAB	RME	RPF	0	XPR	0	0	0	0	RD (20/60)
MASKB	RME	RPF	0	XPR	0	0	0	0	WR (20/60)
STARB	XDOV	XFW	XREP	RFR	RLI	CEC	XAC	AFI	RD (21/61)
CMDRB	RMC	RHR	XREP	0	XTF	0	XME	XRES	WR (21/61)
MODEB	MDS1	MDS0	ADM	CFT	RAC	0	0	TLP	RD/WR (22/62)
reserved									RD/WR (23/63)
EXIRB	XMR	XDU EXE	0	RFO	0	RFS	0	0	RD (24/64)
RBCLB	RBC7							RBC0	RD (25/65)
RAH1	RAH1						0	0	WR (26/66)
RAH2	RAH2						0	0	WR (27/67)
RSTAB	VFR	RDO	CRC	RAB	HA1	HA0	C/R	LA	RD (27/67)
RAL1	RAL1								RD/WR (28/68)
RAL2	RAL2								WR (29/69)
RHCRB	RHCR								RD (29/69)
XBCL	XBC7							XBC0	WR (2A/6A)
reserved									RD/WR (2B/6B)
CCR2	SOC	0	XCS0	RCS0	TXD	0	RIE	DIV	RD/WR (2C/6C)

	7	6	5	4	3	2	1	0	
RBCHB	DMA	0	0	OV	RBC11			RBC8	RD (2D/6D)
XBCH	DMA	0	0	XC	XBC11			XBC8	WR (2D/6D)
reserved									RD (2E/6E)
RLCR	RC	0	RL5					RL0	WR (2E/6E)
CCR1	PU	SC	0	0	ITF	0	1	0	RD/WR (2F/6F)
TSAX	TSNX						XCS2	XCS1	WR (30/70)
TSAR	TSNR						RCS2	RCS1	WR (31/71)
XCCR	XBC7							XBC0	WR (32/72)
RCCR	RBC7							RBC0	WR (33/73)

D-Channel Registers

RFIFOD	D-Channel Receive FIFO								RD (80 - 9F)
XFIFOD	D-Channel Transmit FIFO								WR (80 - 9F)
ISTAD	RME	RPF	RSC	XPR	TIN	CIC	SIN	TIN2	RD (A0)
MASKD	RME	RPF	RSC	XPR	TIN	CIC	SIN	TIN2	WR (A0)
STARD	XDOV	XFW	XRNR	RRNR	MBR	MAC1	--	MAC0	RD (A1)
CMDRD	RMC	RRES	RNR	STI	XTF	XIF	XME	XRES	WR (A1)
MODED	MDS2	MDS1	MDS0	TMD	RAC	DIM2	DIM1	DIM0	RD/WR (A2)
TIMR1	CNT			VALUE					RD/WR (A3)
EXIRD	XMR	XDU	PCE	RFO	SOV	MOS	SAW	WOV	RD (A4)
XAD1									WR (A4)
XAD2									WR (A5)
RBCLD	RBC7							RBC0	RD (A5)
SAPR									RD (A6)

	7	6	5	4	3	2	1	0	
SAP1	SAPI1						CRI	0	WR (A6)
SAP2	SAPI2						MCS	0	WR (A7)
RSTAD	RDA	RDO	CRC	RAB	SA1	SA0	C/R	TA	RD (A7)
TEI1	TEI1							EA	WR (A8)
TEI2	TEI2							EA	WR (A9)
RHCRD									RD (A9)
RBCHD	XAC	--	--	OV	RBC11			RBC8	RD (AA)
STAR2	0	0	0	0	WFA	0	TREC	SDET	RD (AB)
SPCR	SPU	SDL	SPM	TLP	C1C1	C1C0	C2C1	C2C0	RD/WR (B0)
CIR0	0	BAS	CODR0				CIC0	CIC1	RD (B1)
CIX0	RSS	BAC	CODX0				1	1	WR (B1)
MOR0									RD (B2)
MOX0									WR (B2)
CIR1	CODR1						MR1	MX1	RD (B3)
CIX1	CODX1						1	1	WR (B3)
MOR1									RD (B4)
MOX1									WR (B4)
C1R									RD/WR (B5)
C2R									RD/WR (B6)
STCR	TSF	TBA2	TBA1	TBA0	ST1	ST0	SC1	SC0	WR (B7)
B1CR									RD (B7)
B2CR									RD (B8)
ADF1	WTC1	WTC2	CI1E	0	CSEL2	CSEL1	CSEL0	ITF	WR (B8)

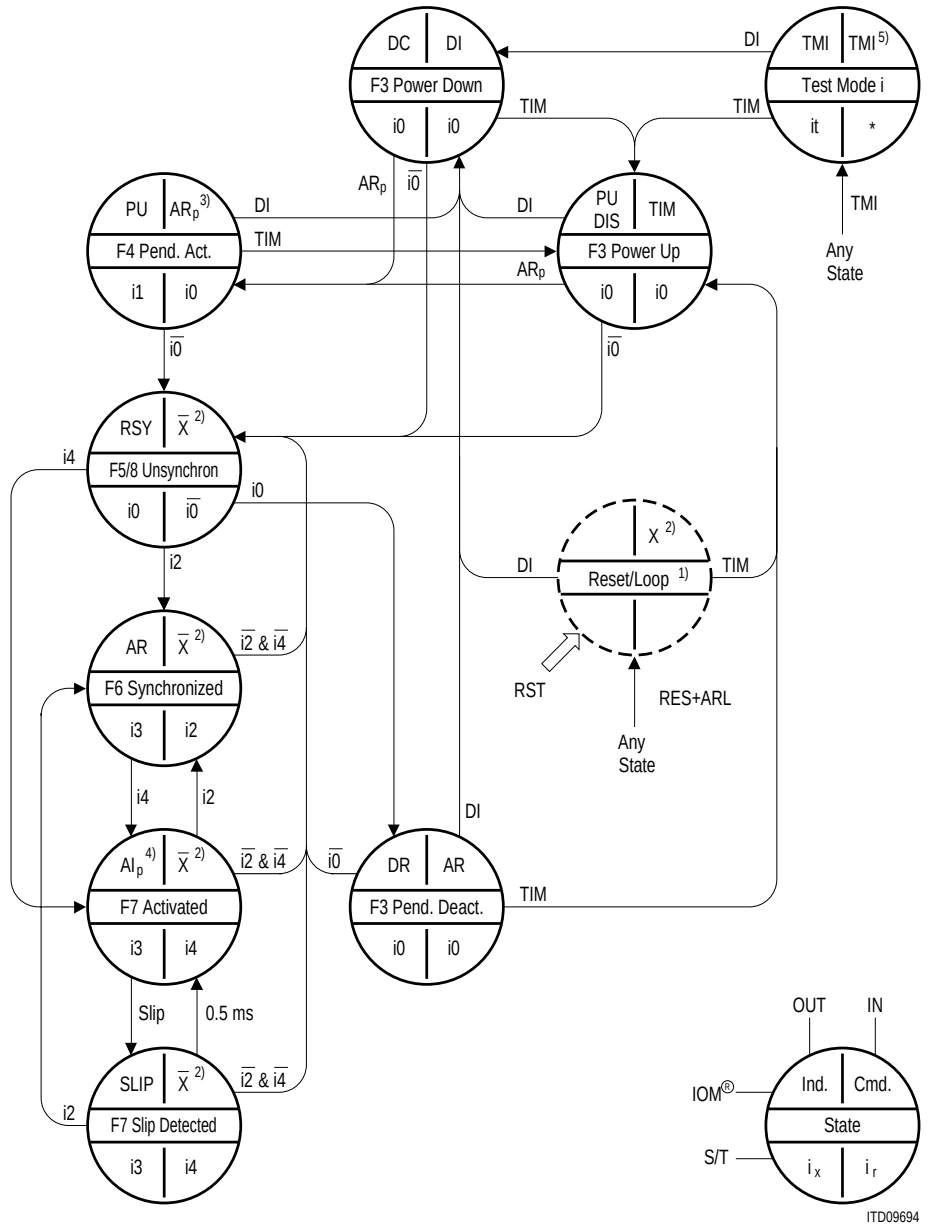
	7	6	5	4	3	2	1	0	
reserved	1	0	0	0	0	0	0	0	RD/WR (B9)
MOSR	MDR1	MER1	MDA1	MAB1	MDR0	MER0	MDA0	MAB0	RD (BA)
MOCR	MRE1	MRC1	MIE1	MXC1	MRE0	MRC0	MIE0	MXC0	WR (BA)

General IPAC Registers

CONF	AMP	CFS	TEM	PDS	IDH	SGO	ODS	IOF	RD/WR (C0)
ISTA	INT1	INT0	ICD	EXD	ICA	EXA	ICB	EXB	RD (C1)
MASK	INT1	INT0	ICD	EXD	ICA	EXA	ICB	EXB	WR (C1)
ID									RD (C2)
ACFG	OD7	OD6	OD5	OD4	OD3	OD2	EL1	EL0	RD/WR (C3)
AOE	OE7	OE6	OE5	OE4	OE3	OE2	0	0	RD/WR (C4)
ARX	AR7	AR6	AR5	AR4	AR3	AR2	0	0	RD (C5)
ATX	AT7	AT6	AT5	AT4	AT3	AT2	0	0	WR (C5)
PITA1	ENA	DUDD	0	TNRX					RD/WR (C6)
PITA2	ENA	DUDD	0	TNRX					RD/WR (C7)
POTA1	ENA	DUDD	0	TNTX					RD/WR (C8)
POTA2	ENA	DUDD	SRES	TNTX					RD/WR (C9)
PCFG	DPS	ACL	LED	PLD	FBS	CSL2	CSL1	CSL0	RD/WR (CA)
SCFG	PRI	TXD	TLEN	TSLT					RD/WR (CB)
TIMR2	TMD	0	CNT						RD/WR (CC)

7.3 State Diagrams

TE/LT-T Modes State Diagram

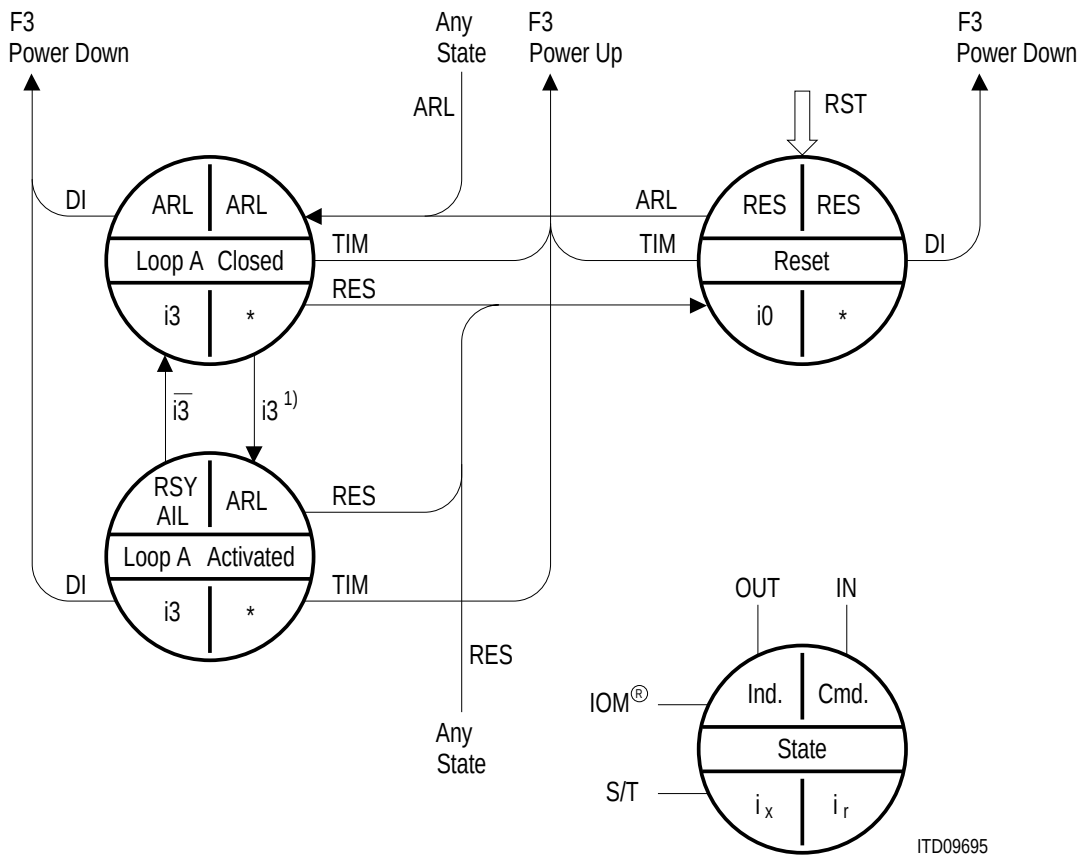


Notes:

1. See state diagram for unconditional transitions for details
2. x = TM1 or TM 2 or RES or ARL
   $\overline{x}$ = $\overline{TM1}$ & $\overline{TM2}$ & $\overline{RES}$ & $\overline{ARL}$
3. AR_P = AR8 or AR10
4. AI_P = AI8 or AI10
5. TMI = TM1 or TM2

B- and D-channel on SX transparent if the command equals to AR8 or AR10.

Figure 119 State Transition Diagram in TE/LT-T Modes

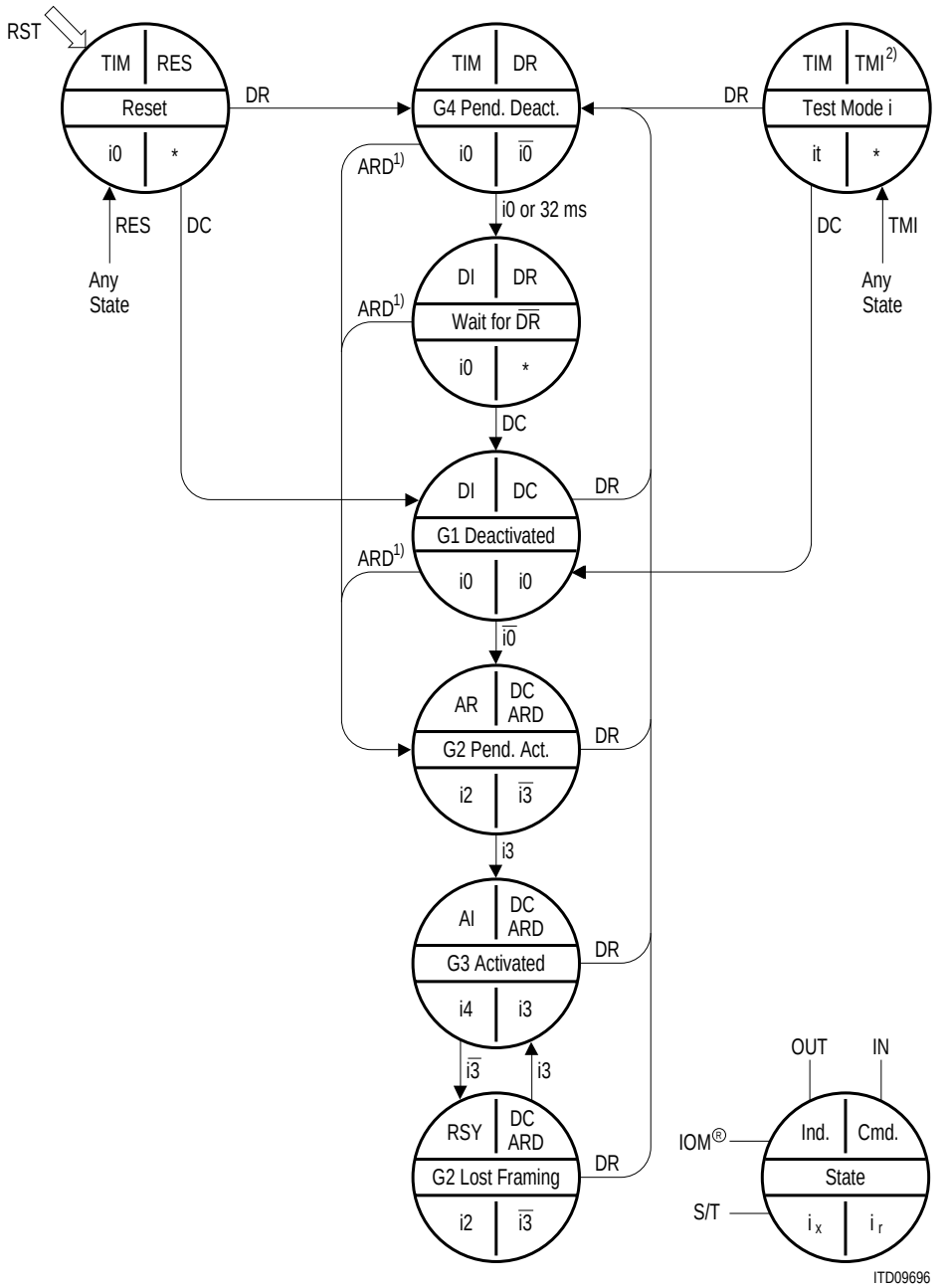


Note:

1. In state “loop A activated” I3 is the internal signal, the external signal is I0.

Figure 120 State Diagram of the TE/LT-T Modes, Unconditional Transitions

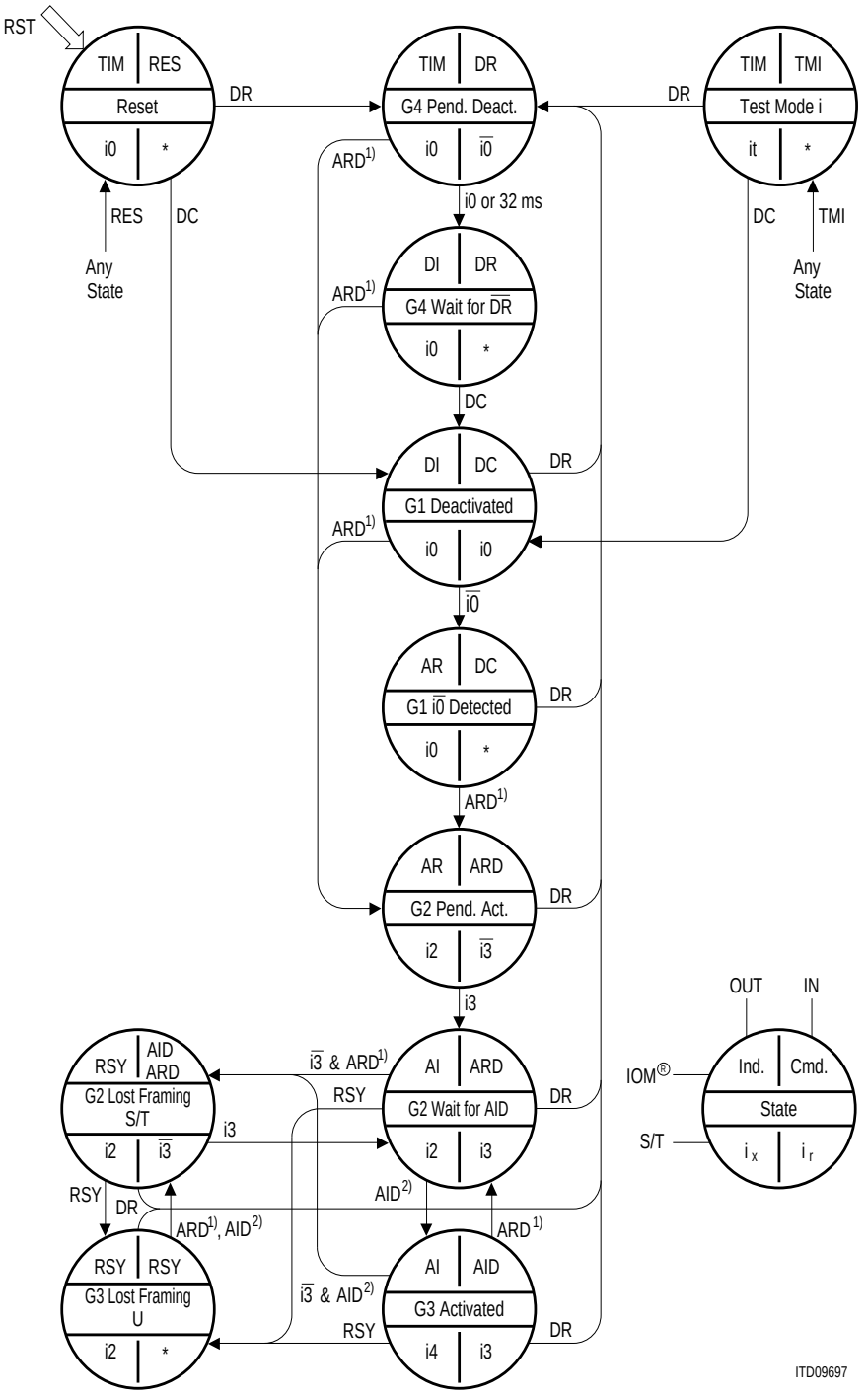
LT-S Mode State Diagram



Notes:
1. ARD stands for AR or ARL
2. TMI = TM1 or TM2

Figure 121 State Transition Diagram in LT-S Mode

Intelligent NT Mode State Diagram



Notes:
1. ARD = AR or ARL
2. AID = AI or AIL

Figure 122 NT Mode State Diagram

7.4 C/I Codes

Code	LT-S		NT		TE/LT-T	
	IN	OUT	IN	OUT	IN	OUT
0 0 0 0	DR	TIM	DR	TIM	TIM	DR
0 0 0 1	RES	–	RES	–	RES	RES
0 0 1 0	TM1	–	TM1	–	TM1	TM1
0 0 1 1	TM2	–	TM2	–	TM2	TM2 SLIP [1]
0 1 0 0	–	RSY	RSY	RSY	–	RSY
0 1 0 1	–	–	–	–	–	–
0 1 1 0	–	–	–	–	–	–
0 1 1 1	–	–	–	–	–	PU
1 0 0 0	AR	AR	AR	AR	AR8	AR
1 0 0 1	–	–	–	–	AR10	–
1 0 1 0	ARL	–	ARL	–	ARL	ARL
1 0 1 1	–	CVR	–	CVR	–	CVR
1 1 0 0	–	AI	AI	AI	–	AI8
1 1 0 1	–	–	–	–	–	AI10
1 1 1 0	–	–	AIL	–	–	AIL
1 1 1 1	DC	DI	DC	DI	DI	DC

1) In LT-T mode only

AI	Activation Indication
AI8	Activation Indication with high priority
AI10	Activation Indication with low priority
AIL	Activation Indication Loop
AR	Activation Request
AR8	Activation Request with high priority
AR10	Activation Request with low priority
ARL	Activation Request Loop
CVR	Code Violation Received
DC	Deactivation Confirmation
DI	Deactivation Indication
DR	Deactivation Request
PU	Power-Up
RES	Reset
RSY	Resynchronizing
SLIP	IOM Frame Slip
TIM	Timer
TIM1	Test Mode 1 (2-kHz signal)
TM2	Test Mode 2 (96-kHz signal)

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