6Ch, 24bit, 192kHz Digital Audio Processor for Full Digital Amplifier

Introduction

The PS9702B is a highly integrated system-on-chip solution for multi-channel AV systems. The PS9702B is 6 channel PCM to PWM modulator with sample rate converter and pre-amplifier functions. It features six 24-bit audio digital-to-digital converters and over-sampling digital filters, a sample rate converter, an audio DSP that functions as an on-chip pre-amplifier with equalizer, volume control, bass management, and compressor functions. The PS9702B accepts industry-standard audio data formats with 16- to 24-bit audio data. Sampling rates of up to 192 kHz are supported.

Features

General

- 1 serial input port for 6Ch and 3 serial input ports for 2Ch (or 2 serial input ports for 6Ch)
- SPDIF receiver for 2Ch non-encoded PCM input
- Supports 16/18/20/24 bit Input
- Supports 32kHz~192kHz Input Sample Rate
- I^2C or SPI control bus
- 100 pin QFP Package
- 3.3V Single Power Supply

Digital Filter and Sample-rate-converter Section

- On chip Sample rate converter
- On chip Digital De-emphasis filter for CD input signal

Preamplifier Section

- Input mixing function
- Microphone mixing function
- Stereo REC output
- Parametric EQ (4 band, 1dB/step) per channel
- Tone control (±15dB, 1dB/step) per channel
- Bass management function
- Volume control (+24 ~ -70dB, 0.5dB/step) per channel
- Dynamic range compression function
- Soft and Hard Mute Functions

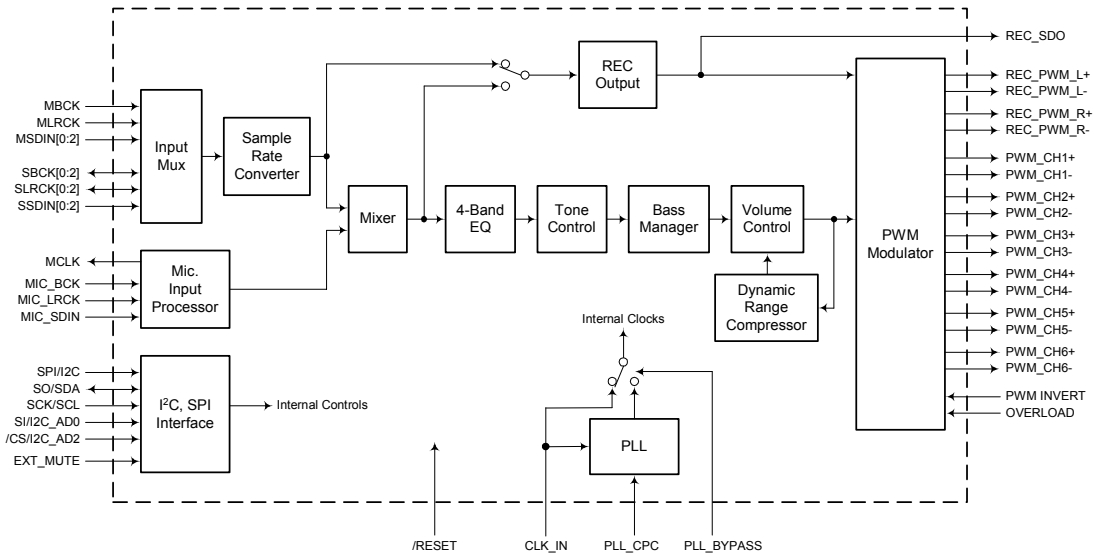
PCM-to-PWM modulator section

- 6 channel PWM Amplification output
- 95 dB Dynamic Range (typical)

Application

- DVD Receiver (DVD player plus 5.1ch Receiver)
- Integrated A/V Receiver
- HDTV sets
- Car A/V Systems
- DVD Add-On Cards for High-End PCs
- Digital Audio Workstations
- Other Multi-Channel Digital Audio Systems

Functional Block Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Power Supply Voltage (VDD to VSS)	V_{SS} – 0.3	4.0	V
Input Current, (Any pin except Supply)	-	±10	mA
Output Current (/Pin)	-	±30	mA
Input Voltage	V_{SS} – 0.5	+7.0	V
Storage Temperature	-65	+150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

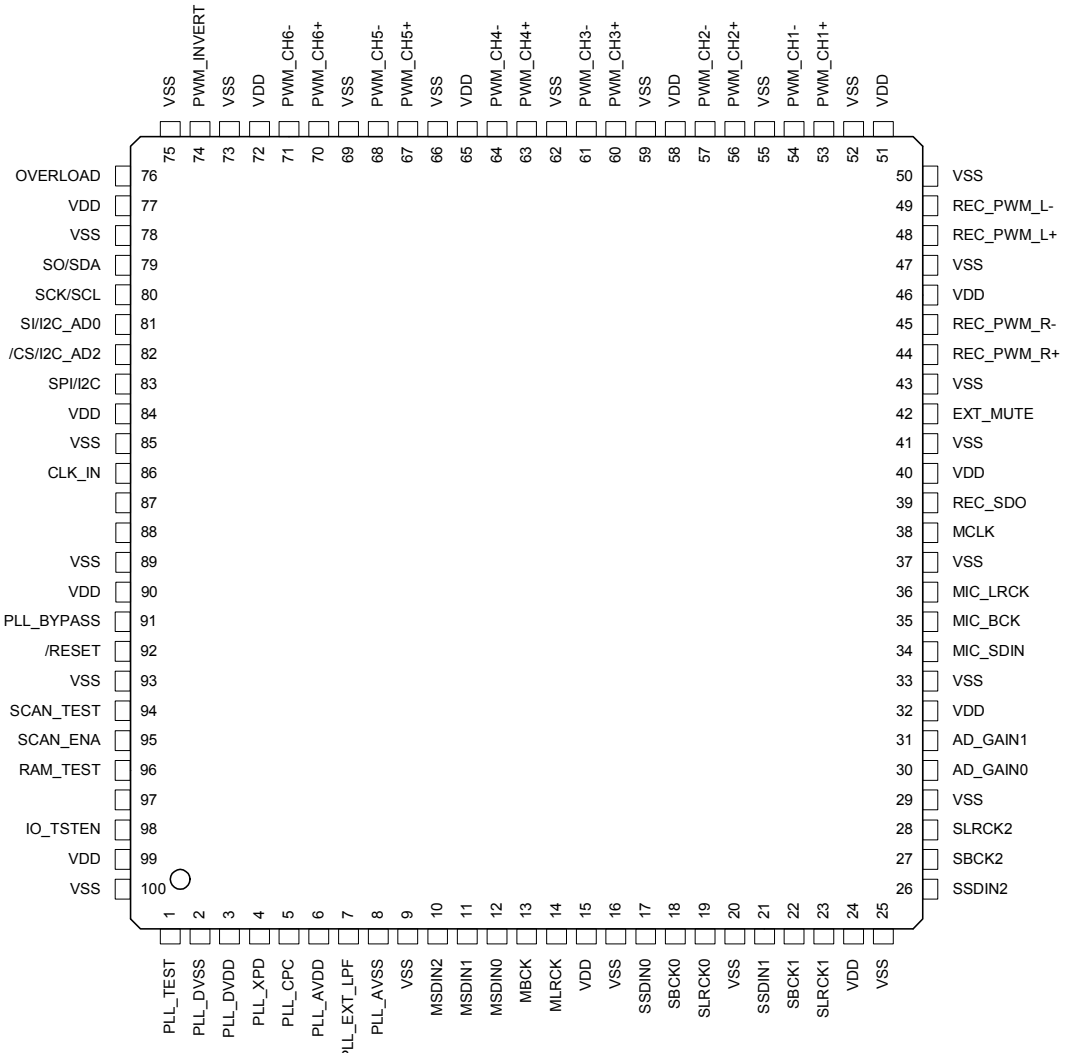
RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Power Supply Voltage (VDD to VSS)	3.0	3.3	3.6	V
Supply Current (VDD = 3.3V)	-	170	-	mA
Input Voltage	V_{SS} -0.5	-	5.5	V
Ambient Operating Temperature	-20	-	+75	°C

ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Input Leakage Current (except Pull-up, Pull-down Input)	-	-	30	µA
High-Level Input Voltage (except Schmitt Input)	2.0	-	-	V
Low-Level Input Voltage (except Schmitt Input)	-	-	0.8	V
High-Level Input Voltage (Schmitt Input)	1.39	-	2.06	V
Low-Level Input Voltage (Schmitt Input)	0.9	-	1.46	V
High-Level Output Voltage (I_O = 2mA)	V_{DD} – 0.4	-	-	V
Low-Level Output Voltage (I_O = 2mA)	-	-	0.4	V
Pull-up Resistance	20	50	100	kΩ
Pull-down Resistance	20	50	100	kΩ
Input Capacitance (f = 1MHz, V_{DD} = 0V)	-	-	10	pF
Output Capacitance (f = 1MHz, V_{DD} = 0V)	-	-	10	pF

Pin Assignment



PS9702B (100pin Plastic QFP, Top View)

Pin Descriptions

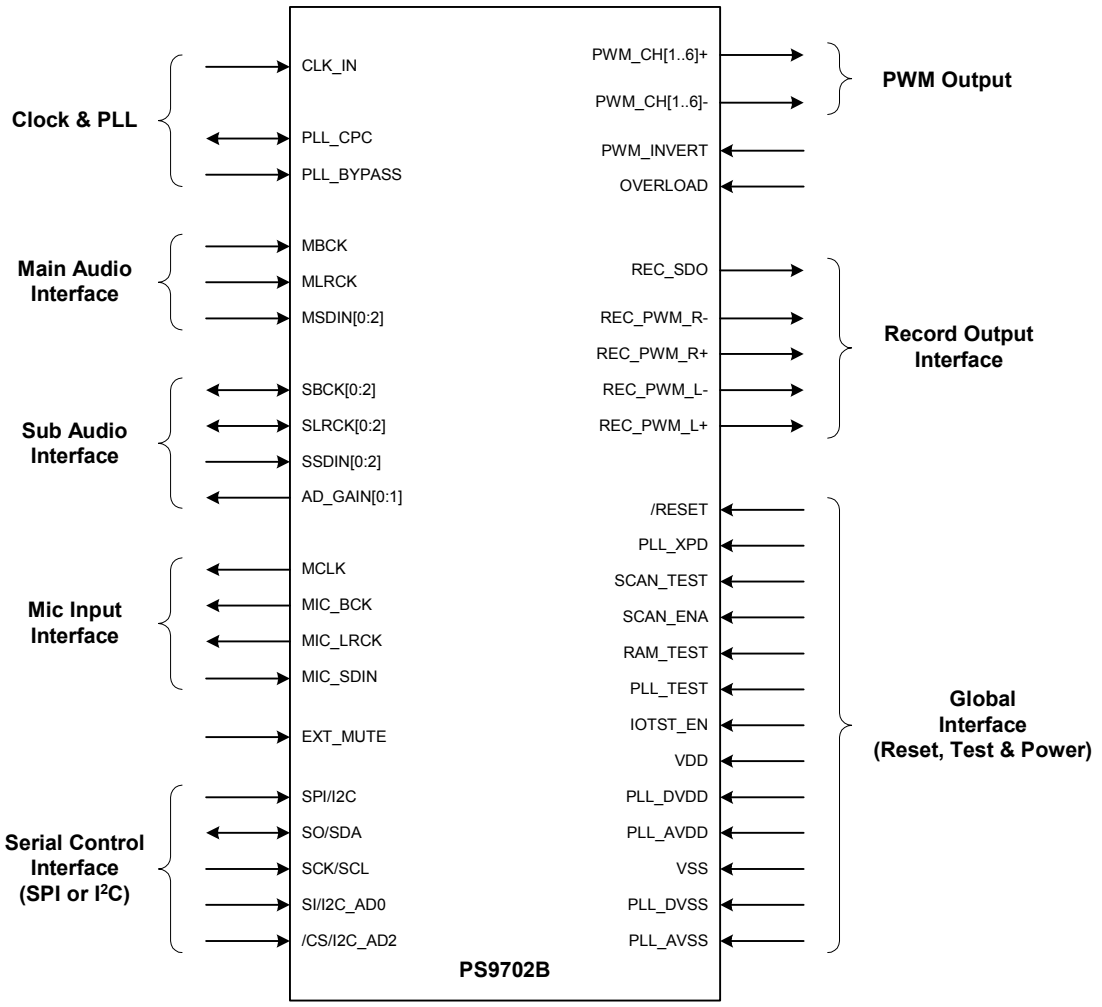
Name	Pin NO.	Type	Description
Power and Ground			
PLL_AVDD	6	Analog Power	PLL analog power supply. 3.3V supply voltage.
PLL_AVSS	8	Analog Ground	PLL analog ground.
PLL_DVDD	3	PLL Power	PLL peripheral digital power supply. 3.3V supply voltage.
PLL_DVSS	2	PLL Ground	PLL digital ground.
VDD	15, 24, 32, 40, 46, 51, 58, 65, 72, 77, 84, 90, 99	Power	Digital power supply. 3.3V supply voltage.
VSS	9, 16, 20, 25, 29, 33, 37, 41, 43, 47, 50, 52, 55, 59, 62, 66, 69, 73, 75, 78, 85, 89, 93, 100	Ground	Digital ground.
System Services			
/RESET	92	I	H/W reset signal. Active Low Schmitt-Trigger input. The Schmitt-Trigger input allows a slowly rising input to reset the chip reliably. The RESET signal must be asserted 'Low' during power up. De-assert 'High' for normal operation.
CLK_IN	86	I	External clock input. 12.288MHz is recommended. When the PLL_BYPASS is "LOW", the external clock input from CLK_IN is used as PLL reference clock source. The external oscillator generates 12.288MHz clock and the internal PLL generates 98.304MHz (12.288MHz x 8) system clock. When the PLL_BYPASS is "HIGH", the PS9702B directly uses the CLK_IN signal (98.304MHz clock) as system clock.
PLL_BYPASS	91	I	PLL bypass path selection input. Active High. *Internal pull-down resistor.*
PLL_XPD	4	I	Internal PLL Power Down. Active Low. Don't pull down "PLL_XPD" pin when PWM output is activated. *Internal pull-up resistor.*
PLL_CPC	5	I	Internal PLL Charge Pump Current Selection input. 'LOW' for 100uA, 'HIGH" for 50uA. *Internal pull-down resistor.*
PLL_EXT_LPF	7	Analog	External PLL low pass filter pin.
PCM Audio Input/Output Interface			
MBCK	13	I	PCM bit clock input of main six-channel audio. Schmitt-Trigger input.
MLRCK	14	I	PCM Word clock (left-right clock) input of main six-channel audio. Schmitt-Trigger input.
MSDIN[0:2]	12-10	I	PCM serial data input of main six-channel audio. Schmitt-Trigger input.
SBCK[0:2]	18, 22, 27	I/O	PCM bit clock input/output of sub-channel audio. User can select the master/slave mode of this signal.

Name	Pin NO.	Type	Description
SLRCK[0:2]	19, 23, 28	I/O	PCM Word clock (left-right clock) input/output of sub-channel audio.
SSDIN[0:2]	17, 21, 26	I	PCM serial data input of sub-channel audio. This sub-channel data can be treated as three two-channel audio or one six-channel audio. When it is used for six-channel audio, user can select the bit clock and word clock from SBCK[0:2] and SLRCK[0:2].
MCLK	38	O	Main clock for external A/DC or D/AC. Clock frequency is 12.288MHz (fixed).
MIC_BCK	35	O	PCM bit clock output of external MIC. Bit clock frequency is 3.072MHz (48KHz x 64, fixed)
MIC_LRCK	36	O	PCM Word clock (left-right clock) output of external MIC. Word clock rate is 48KHz (fixed).
MIC_SDIN	34	I	PCM serial data input of external MIC. Schmitt-Trigger input.
REC_SDO	39	O	PCM serial data output of record-out. This signal is synchronized to MIC_BCK and MIC_LRCK.
PWM Audio Output			
PWM_CH1+	53	O	Positive PWM output of channel 1. (default setting : front left channel)
PWM_CH1-	54	O	Negative PWM output of channel 1.
PWM_CH2+	56	O	Positive PWM output of channel 2. (default setting : front right channel)
PWM_CH2-	57	O	Negative PWM output of channel 2.
PWM_CH3+	60	O	Positive PWM output of channel 3. (default setting : rear left channel)
PWM_CH3-	61	O	Negative PWM output of channel 3.
PWM_CH4+	63	O	Positive PWM output of channel 4. (default setting : rear right channel)
PWM_CH4-	64	O	Negative PWM output of channel 4.
PWM_CH5+	67	O	Positive PWM output of channel 5. (default setting : center channel)
PWM_CH5-	68	O	Negative PWM output of channel 5.
PWM_CH6+	70	O	Positive PWM output of channel 6. (default setting: sub-woofer channel)
PWM_CH6-	71	O	Negative PWM output of channel 6.
REC_PWM_R+	44	O	Positive PWM output of Record-out left channel.
REC_PWM_R-	45	O	Negative PWM output of Record-out left channel.
REC_PWM_L+	48	O	Positive PWM output of Record-out right channel.
REC_PWM_L-	49	O	Negative PWM output of Record-out right channel.
System Control Interface			
SPI/I2C	83	I	Host interface mode (SPI or I2C) selector. Assert 'HIGH' for SPI mode. De-assert 'LOW' for I2C mode. *Internal pull-down resistor.*
SO/SDA	79	I/O	SO for SPI mode or SDA for I2C mode.
SCK/SCL	80	I	SCK for SPI mode or SCL for I2C mode. Schmitt-Trigger input.

Name	Pin NO.	Type	Description
SI/I2C_AD0	81	I	SI for SPI mode or Slave Address 0 for I2C mode. Schmitt-Trigger input. *Internal pull-down resistor.*
/CS/I2C_AD2	82	I	Chip selector (CS) for SPI mode or Slave Address 2 for I2C mode. Schmitt-Trigger input. *Internal pull-down resistor.*
Special Control Interface			
EXT_MUTE	42	I	External mute control input. Active High. Assert 'HIGH' to mute the output. *Internal pull-down resistor.*
PWM_INVERT	74	I	Inverting control input of the PWM output. Active High. Assert 'HIGH' to invert the PWM output. Default is non-inverting mode. *Internal pull-down resistor.*
OVERLOAD	76	I	Power stage overload indication input. Polarity is programmable. Schmitt-Trigger input. When OVERLOAD is asserted, all PWM audio outputs go to "LOW" (if PWM_INVERT pin is 'LOW"). *Internal pull-down resistor.*
AD_GAIN[0:1]	30, 31	O	External A/D converter's gain control output.
Test Mode			
PLL_TEST	1	I	Internal PLL test mode. Active High. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
SCAN_TEST	94	I	Scan test mode selector. Active High. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
SCAN_ENA	95	I	Scan enable. Active High. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
RAM_TEST	96	I	Internal SRAM test mode. Active High. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
IO_TSTEN	98	I	I/O Test pin. Active High. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
NC	87, 88, 97		Not connected pin. This pin should not be connected to any other signal.

※ All inputs and bi-directional inputs are 5 Volt tolerant. The corresponding pins can be connected to the buses that can swing between 0V and 5V. The output-only pins are not 5V tolerant and the buses they are connected to can swing only between 0V and 3.3V.

Signal Interface Diagram



Signal Descriptions

1. Clock and Reset

The PS9702B uses 98.304MHz (48KHz x 2048) system clock internally. The PS9702B uses external 12.288MHz clock source and has x8 PLL (Phase Locked Loop) for internal system clock generation. PS9702B can select the system clock between the internally generated clock and the external input clock (In this case the external input clock must be 98.304MHz).

2. PCM Audio Input Signals

PS9702B uses serial interface for PCM audio data input using ***BCK***, ***LRCK***, and ***DIN*** pins. It has one input port for six channel audio data (named as main channel) and has three sub-input port for two channel audio data (named as sub-channel). But the three sub-input ports can be used as one six-channel audio input port.

3. PWM Audio Output Signals

The PS9702B converts PCM audio data to PWM audio signal. It outputs one six-channel PWM signal for main audio, one two-channel PWM signal for record-out and one additional two-channel PCM signal for record-out. All PWM signal consist of the both positive and negative PWM signals.

4. Control Interface Signals

The PS9702B supports internal control register I/O using both SPI and I^2C. The pin ***SPI/I2C*** selects the control interface method. The control registers has 8-bit address space and 16-bit or 24-bit data length. All internal control registers are both readable and writable.

5. Special Control Signals

The PS9702B can generate only AD mode PWM signal. For more information about the Power stage driving method and BD/AD mode of PWM amplifier, refer the “PULSUS PWM Amplification application notes”.

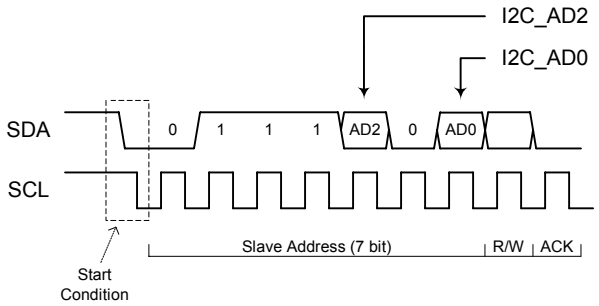
The PS9702B has Overload protection logic. When the pin ***OVERLOAD*** is “HIGH” (default setting, the polarity is programmable), the PS9702B goes to protection mode and all PWM outputs go to “LOW” (default setting).

Control Interface Protocol

1. I²C Control Interface

The pin ***SPI/I2C*** selects the control interface method. When the pin ***SPI/I2C*** is grounded, the control interface method is I²C interface.

The I²C slave address can be varied using two I²C slave address setting pin, ***I2C_AD0*** and ***I2C_AD2***. The base slave address is 0x38 with ***I2C_AD0*** and ***I2C_AD2*** pin grounded. Figure below shows you the configuration of slave address.

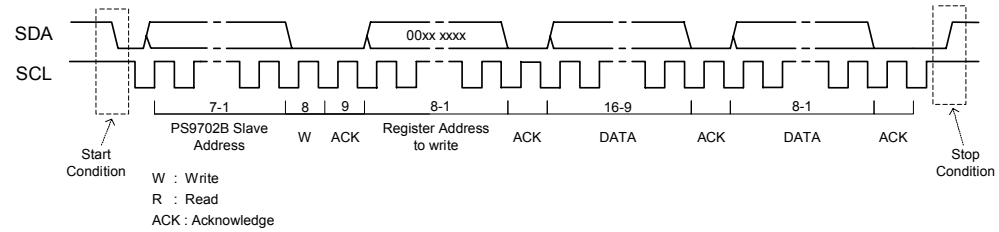


I2C_AD2	I2C_AD0	PS9702B Slave Address
0	0	0x38 (0b0111000)
0	1	0x39 (0b0111001)
1	0	0x3C (0b0111100)
1	1	0x3D (0b0111101)

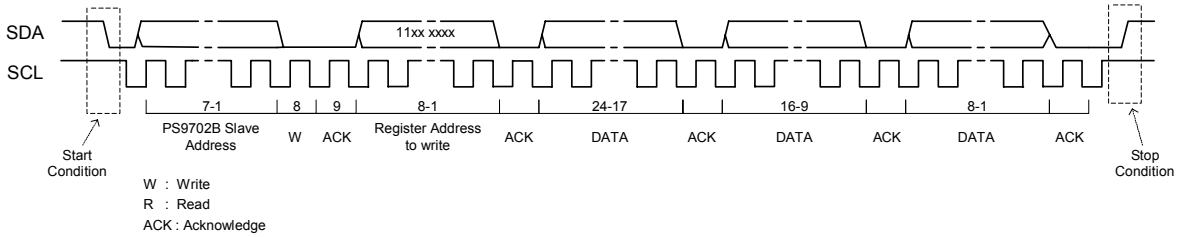
The control registers has 8-bit address space and 16-bit or 24-bit data length. If the upper two bits of register address are all HIGH, 11xx xxxx, then the data length will be three bytes (24 bits). The other case, the data length will be two bytes (16 bits).

The I²C control protocol diagram is in the next page.

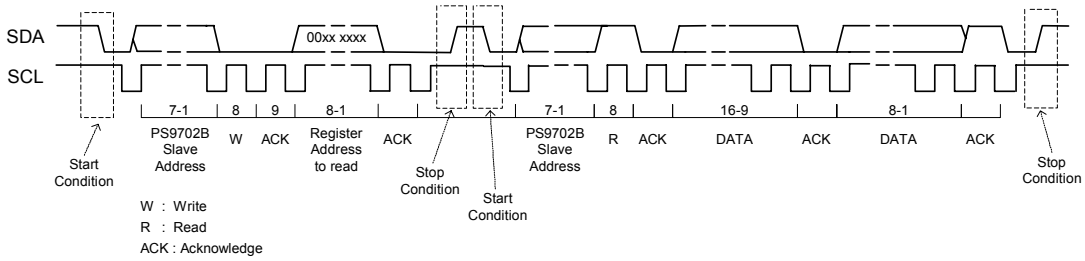
2Bytes Write Operation (I^2C interface)



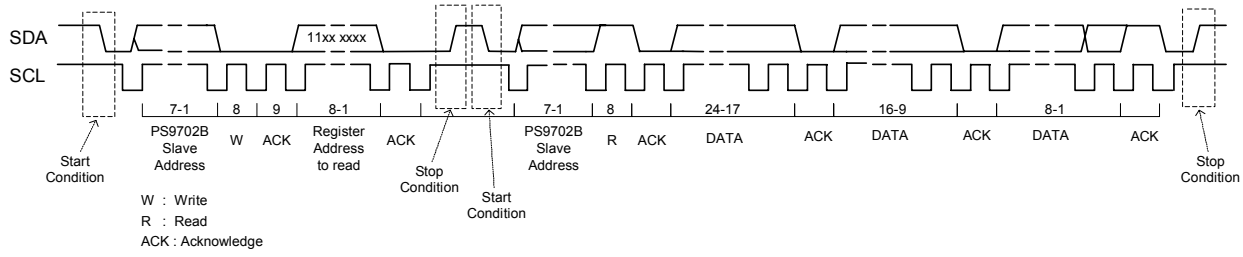
3Bytes Write Operation (I^2C interface)



2Bytes Read Operation (I^2C interface)



3Bytes Read Operation (I^2C interface)

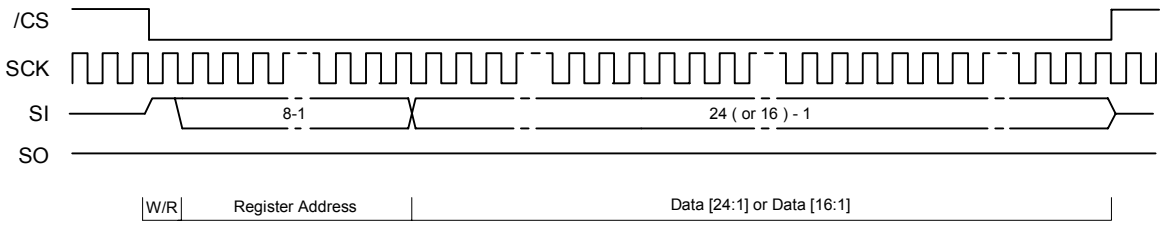


2. SPI Control Interface

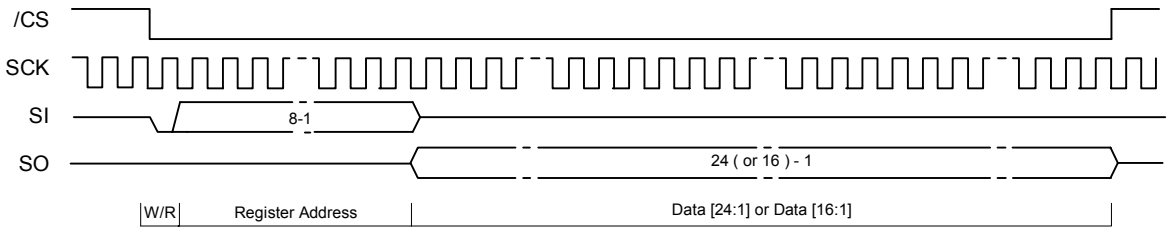
The pin ***SPI/I2C*** selects the control interface method. When the pin ***SPI/I2C*** is connected to VCC, the control interface method is SPI interface.

SPI control protocol diagram is below.

Write Operation (SPI interface)



Read Operation (SPI interface)



Control Register Descriptions

Register Name	Address	Word Length	Description
DDC Soft Reset Register			
DDC_RESET	0x00	2 Bytes	PWM output activation control register. [0]: PWM modulator Reset control. *Default = "1".* "0" = PWM On "1" = PWM Off [3:1]: *Reserved.* [4]: SRC (Sample Rate Converter) Lock indication. Active High. Read only. "0" = Unlock (or No signal) "1" = Lock [8:5]: Input sample rate indication. Read only. "0001" = 32KHz "0010" = 44.1KHz "0011" = 48KHz "0110" = 88.2KHz "0111" = 96KHz "1010" = 176.4KHz "1011" = 192KHz [15:9]: *Not Used.* *Default = 0x0XX1*
Input Interface Unit Configuration Registers			
IN_CONTROL	0x01	2 Bytes	Serial data input interface control register. [1:0]: BCK count. *Default = "10".* "00" = 16bit, "01" = 24bit, "10" = 32bit. [2]: BCK polarity. *Default = "1".* "0" = Valid data at Negative edge "1" = Valid data at Positive edge [3]: Data align. "0" = Right aligned, "1" = Left aligned. *Default = "1".* [4]: LRCK left high. *Default = "0".* "0" = Right data when LRCK is high. "1" = Left data when LRCK is high. [5]: Data MSB first. "0" = LSB first, "1" = MSB first. *Default = "1".* [7:6]: Data word length. *Default = "11".* "00" = 16bit, "01" = 18bit, "10" = 20bit, "11" = 24bit. [8]: I2S compatible. "1" = Compatible. *Default = "1".* [15:9]: *Not Used.* *Default = 0x01EE*

Register Name	Address	Word Length	Description
MIC_CONTROL	0x02	2 Bytes	MIC data input interface control register. This register is not changable and is fixed to default value. [8:0]: BCK count. *Default = "10".* "00" = 16bit, "10" = 32bit. [2]: BCK polarity. *Default = "1".* "0" = Valid data at Negative edge. "1" = Valid data at Positive edge. [3]: Data align. "0" = Right aligned. "1" = Left aligned. *Default = "1".* [4]: LRCK left high. *Default = "0".* "0" = Right data when LRCK is high. "1" = Left data when LRCK is high. [5]: Data MSB first. "0" = LSB first, "1" = MSB first. *Default = "1".* [7:6]: Data word length. *Default = "11".* "00" = 16bit, "01" = 18bit, "10" = 20bit, "11" = 24bit. [8]: I2S compatible. "1" = Compatible. *Default = "1".* [15:9]: *Not Used*. *Default = 0x01EE*
CHANNEL_CONFIGURE	0x03	2 Bytes	Register for serial input data port configuration. [2:0]: I2S Input port selector. *Default = "100".* "000" = Sub two-channel input mode using SDIN[0], SBCK[0], and SLRCK[0]. "001" = Sub two-channel input mode using SDIN[1], SBCK[1], and SLRCK[1]. "01x" = Sub two-channel input mode using SDIN[2], SBCK[2], and SLRCK[2]. "100" = Main six-channel input mode using MBCK and MLRCK. "101" = Sub six-channel input using SBCK[0] and SLRCK[0]. "110" = Sub six-channel input using SBCK[1] and SLRCK[1]. "111" = Sub six-channel input using SBCK[2] and SLRCK[2]. [4:3]: *Reserved*. [5]: Master-slave mode selector for SBCK[0] and SLRCK[0]. *Default = "0".* "0" = Slave mode, "1" = Master mode. [6]: Master-slave mode selector for SBCK[1] and SLRCK[1]. *Default = "0".* "0" = Slave mode, "1" = Master mode. [7]: Master-slave mode selector for SBCK[2] and SLRCK[2]. *Default = "0".* "0" = Slave mode, "1" = Master mode. [8]: I2S/SPDIF input selector. PS9702B can receive the both I2S and SPDIF input. "0" means the input is SPDIF input. "1" means the input is I2S input. *Default = "1".* [10:9]: SPDIF input port selector. *Default = "00".* "00" = SPDIF input from SDATA[0]. "01" = SPDIF input from SBCK[0]. "10" = SPDIF input from SLRCK[0]. "11" = SPDIF input from SDATA[0]. [15:11]: *Not Used*. *Default = 0x0104*

Register Name	Address	Word Length	Description
Volume Configuration Registers			
VOLUME1_CONTROL	0x05	2 Bytes	The PS9702B supports digital volume gain control with the resolution of 0.5dB/step. The maximum volume gain is +24dB and the minimum volume gain (except -∞dB) is -70dB. The each volume control register has 8-bit resolution. The register value 0x00 means +24dB, and the value 0xBC means -70dB. And the register value larger than 0xBC means sound mute. Table A-1 shows the relations between the register value and volume gain. [15:8]: PWM output Channel 1 volume. [7:0]: PWM output Channel 2 volume. *Default = 0xBDBD (Mute)*
VOLUME2_CONTROL	0x06	2 Bytes	Table A-1 shows the relations between the register value and volume gain. [15:8]: PWM output Channel 3 volume. [7:0]: PWM output Channel 4 volume. *Default = 0xBDBD (Mute)*
VOLUME3_CONTROL	0x07	2 Bytes	Table A-1 shows the relations between the register value and volume gain. [15:8]: PWM output Channel 5 volume. [7:0]: PWM output Channel 6 volume. *Default = 0xBDBD (Mute)*
VOLUME4_CONTROL	0x08	2 Bytes	Table A-1 shows the relations between the register value and volume gain. [15:8]: Record out left volume. [7:0]: Record out right volume. *Default = 0x3030 (0dB)*
Dynamic Range Compressor Configuration Registers			
THRESHOLD1_CONTROL	0x09	2 Bytes	Automatic gain control (AGC) threshold level. The AGC threshold level is controlled in dB magnitude and it has 0.5dB/step resolution. This register has 8-bit resolution and has the same meaning of volume control register. Table A-1 shows the relations between the register value and threshold level. [15:8]: AGC threshold of PWM output Channel 1 and Channel 2. [7:0]: *Reserved.* *Default = 0x3131 (-0.5dB)*
THRESHOLD2_CONTROL	0x0A	2 Bytes	Table A-1 shows the relations between the register value and threshold level. [15:8]: AGC threshold of PWM output Channel 3. [7:0]: AGC threshold of PWM output Channel 4. *Default = 0x3131 (-0.5dB)*
THRESHOLD3_CONTROL	0x0B	2 Bytes	Table A-1 shows the relations between the register value and threshold level. [15:8]: AGC threshold of PWM output Channel 5. [7:0]: AGC threshold of PWM output Channel 6. *Default = 0x3131 (-0.5dB)*

Register Name	Address	Word Length	Description
AGC_CONTROL	0x11	2 Bytes	AGC control register. [3:0]: AGC attack length control value. *Default = 0x6.* [6:4]: AGC attack height (in 0.5dB scale). *Default = 0x3.* [15:7]: AGC release length (x 0.6667msec). *Default = 0x180 (0.256 sec).* *Default = 0xC036*
PWM Modulator Configuration Register			
PWM_CONTROL1	0x13	2 Bytes	PWM modulator control register 1. [0]: Modulation index(PCM to PWM gain). *Default = "0".* "0" = 90.63% "1" = 93.75% [1]: Auto DC cut enable. Active high. *Default = "1".* [5:2]: *Reserved*. *Default = "0000"* [6]: Overload input signal polarity. *Default = "1"* "0" = Active Low, "1" = Active High. [11:7]: Overload sustained time. When overload condition is detected, all PWM outputs go to shutdown during assigned time. *Default = "10000" (2.73sec)* "00000" = No shutdown. "00001" ~ "11110" = multiple of 0.17sec. "11111" = No recovery. To recover PWM signal, set the DDC_RESET register (0x00) to "1" (PWM off) and then "0" (PWM on). [15:12]: *Reserved.* *Default = 0x0842*
PWM_CONTROL2	0x14	2 Bytes	PWM modulator control register 2. [0]: Interpolation method. "0" = Soft, "1" = Sharp. *Default = "0".* [1]: Dither enable. "0" = Dither disable, "1" = Dither enable. *Default = "0".* [2]: High S/N mode enable. "0" = Normal mode, "1" = High S/N mode. *Default = "0".* [3]: High bandwidth Noise shaping filter enable. *Default = "0".* "0" = Normal mode. "1'" = High bandwidth N/S filter enable. [7:4]: PWM Linearizer Coefficient. *Default = "0000".* [9:8]: Switching Frequency. *Default = "00".* "00", "11" = 384KHz "01" = 192KHz "10" = 96KHz. [11:10]: Dead time between positive and negative PWM signal. The unit is PWM clock (98.304MHz). *Default = "00".* [14:12]: Modulation limit. The unit is PWM clock (98.304MHz). *Default = "000".* [15]: *Reserved.* *Default = 0x0000*

<table>
<tr><th>Register Name</th><th>Address</th><th>Word Length</th><th>Description</th></tr>
<tr><td colspan="4">Status Monitoring Register</td></tr>
<tr><td>SPDIF_CONTROL</td><td>0x17</td><td>2 Bytes</td><td>SPDIF status register.
[4:0]: Reserved. Default = “00111”
[14:5]: SPDIF input status report register. Read only.
[5]: Pre-Emphasis flag. “0” = No emphasis, “1” = Emphasis.
[6]: Professional format flag. “0” = Consumer, “1” = Professional.
[7]: Copy enable flag. “0” = Copy inhibit, “1” = Copy enable.
[8]: Non-audio flag. “0” = Audio, “1” = Non-audio.
[9]: SPDIF detected flag. “1” means the PS9702B detects the SPDIF sync-word.
[10]: Parity error flag. “0” = Non error, “1” = Error.
[11]: Max word length 24 flag. “0” = Max 20-bit, “1” = Max 24-bit.
[14:12]: Word length.
<table><tr><td>Max 24</td><td>0</td><td>1</td></tr><tr><td>000</td><td>Default</td><td>Default</td></tr><tr><td>001</td><td>19</td><td>23</td></tr><tr><td>010</td><td>18</td><td>22</td></tr><tr><td>011</td><td>17</td><td>21</td></tr><tr><td>100</td><td>16</td><td>20</td></tr><tr><td>101</td><td>20</td><td>24</td></tr><tr><td>Others</td><td>Reserved</td><td>Reserved</td></tr></table>[15]: Not Used.
Default = 0x0007</td></tr>
<tr><td>OVERLOAD_STATE</td><td>0x18</td><td>2 Bytes</td><td>Overload status monitoring register.
[0]: Overload status. Read only.
“0” = Overload protection is not detected or output protection is ended.
“1” = Overload is detected and output protection is working.
[15:1]: Not Used.
Default = 0x0000</td></tr>
<tr><td colspan="4">Muting Control Register</td></tr>
<tr><td>SYS_SOFT_MUTE</td><td>0x3C</td><td>2 Bytes</td><td>System mute control register.
[0]: Mute. Active high. Default = “1”
[1]: Soft mute function enable. Active high. Default = “1”
[2]: Internal system mute monitoring bit. Read only.
[10:3]: Internal soft mute level counter. Read only.
[15:11]: Reserved.
Default = 0x0XX7</td></tr>
</table>

Register Name	Address	Word Length	Description
MIC Mixer Configuration Register			
MIC_MIX_LEVEL	0x81	2 Bytes	Mixing level of two microphone input. The each mixing level value consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and LS 7-bit is the mixing level coefficient. Table A-2 shows the relations between the register value and mixing level. [7..0]: MIC0 input into Mic mixer output mixing level. [15..8]: MIC1 input into Mic mixer output mixing level. *Default = 0x3030. (-6dB)*
De-Emphasis Control Register			
DE_EMPHASIS	0x82	2 Bytes	De-Emphasis control Register. [0]: De-Emphasis control of Front two channel. Active high. [15:1]: *Not Used.* *Default = 0x0000*
Input Channel Mapping Configuration Registers			
INPUT_CH_MAPPING1	0x83	2 Bytes	Input channel Mapping Register1. “0” : Input Channel 0 (left channel data from SDIN0) “1” : Input Channel 1 (right channel data from SDIN0) “2” : Input Channel 2 (left channel data from SDIN1) “3” : Input Channel 3 (right channel data from SDIN1) “4” : Input Channel 4 (left channel data from SDIN2) “5” : Input Channel 5 (right channel data from SDIN2) “6”, “7” : not used [2:0]: Input Channel number that is linked to Left Channel. [3]: *Not Used.* [6:4]: Input Channel number that is linked to Right Channel. [15:7]: *Not Used.* *Default = 0x0010*
INPUT_CH_MAPPING2	0x84	2 Bytes	Input channel Mapping Register2. [2:0]: Input Channel number that is linked to Left Surround Channel. [3]: *Not Used.* [6:4]: Input Channel number that is linked to Right Surround Channel. [7]*: Not Used.* [10:8]: Input Channel number that is linked to LFE Channel. [11]: *Not Used.* [14:12]: Input Channel number that is linked to Center Channel. [15]: *Not Used.* *Default = 0x5432*

Register Name	Address	Word Length	Description
Mixer Configuration Registers			
LR2L_MIX_LEVEL	0x85	2 Bytes	Left and Right into Left Mixing level register. The each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity ("0" : +, "1" : -) and LS 7-bit is the mixing level coefficient. Table A-2 shows the relations between the register value and mixing level. [7..0]: Left channel input into Left channel output mixing level. [15..8]: Right channel input into Left channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
CM2L_MIX_LEVEL	0x86	2 Bytes	Center and MIC into Left Mixing level register. [7..0]: Center channel input into Left channel output mixing level. [15..8]: MIC input into Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
RL2R_MIX_LEVEL	0x87	2 Bytes	Right and Left into Right Mixing level register. [7..0]: Right channel input into Right channel output mixing level. [15..8]: Left channel input into Right channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
CM2R_MIX_LEVEL	0x88	2 Bytes	Center and MIC into Right Mixing level register. [7..0]: Center channel input into Right channel output mixing level. [15..8]: MIC input into Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
LSL2LS_MIX_LEVEL	0x89	2 Bytes	Left Surround and Left into Left Surround Mixing level register. [7..0]: Left Surround channel input into Left Surround channel output mixing level. [15..8]: Left channel input into Left Surround channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
RM2LS_MIX_LEVEL	0x8a	2 Bytes	Right and MIC into Left Surround Mixing level register. [7..0]: Right channel input into Left Surround channel output mixing level. [15..8]: MIC input into Left Surround channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
RSL2RS_MIX_LEVEL	0x8b	2 Bytes	Right Surround and Left into Right Surround Mixing level register. [7..0]: Right Surround channel input into Right Surround channel output mixing level. [15..8]: Left channel input into Right Surround channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
RM2RS_MIX_LEVEL	0x8c	2 Bytes	Right and MIC into Right Surround Mixing level register. [7..0]: Right channel input into Right Surround channel output mixing level. [15..8]: MIC input into Right Surround channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
CL2C_MIX_LEVEL	0x8d	2 Bytes	Center and Left into Center Mixing level register. [7..0]: Center channel input into Center channel output mixing level. [15..8]: Left channel input into Center channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
RM2C_MIX_LEVEL	0x8e	2 Bytes	Right and MIC into Center Mixing level register. [7..0]: Right channel input into Center channel output mixing level. [15..8]: MIC input into Center channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
Equalizer Configuration Registers			
EQ_SEL_ENA	0x8F	2 Bytes	Equalizer configuration Register. [0]: Left channel Equalizer Enable. Active high. *Default = "0" (Disable)* [1]: Right channel Equalizer Enable. Active high. *Default = "0" (Disable)* [2]: Left surround channel Equalizer Enable. Active high. *Default = "0" (Disable)* [3]: Right surround channel Equalizer Enable. Active high. *Default = "0" (Disable)* [4]: Center channel Equalizer Enable. Active high. *Default = "0" (Disable)* [7..5]: *Not Used.* [8]: Left channel Equalizer Select. "0" for Primary filter set and "1" for Secondary filter set. *Default = "0" (Primary filter)* [9]: Right channel Equalizer Select. *Default = "0" (Primary filter)* [10]: Left surround channel Equalizer Select. *Default = "0" (Primary filter)* [11]: Right surround channel Equalizer Select. *Default = "0" (Primary filter)* [12]: Center channel Equalizer Select. *Default = "0" (Primary filter)* [15..13]: *Not Used.* *Default = 0x0000*
EQ_L01_LEVEL	0x90	2 Bytes	Left channel Equalizer 0, 1 level register. -15dB to 15dB in 1dB/step resolution. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Left channel Equalizer 0 level. [7..5]: *Not Used.* [12..8]: Left channel Equalizer 1 level. [15..13]: *Not Used.* *Default = 0x0000 (0dB, 0dB)*
EQ_L23_LEVEL	0x91	2 Bytes	Left channel Equalizer 2, 3 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Left channel Equalizer 2 level. [7..5]: *Not Used.* [12..8]: Left channel Equalizer 3 level. [15..13]: *Not Used.* *Default = 0x0000 (0dB, 0dB)*

Register Name	Address	Word Length	Description
EQ_R01_LEVEL	0x92	2 Bytes	Right channel Equalizer 0, 1 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Right channel Equalizer 0 level. [7..5]: *Not Used*. [12..8]: Right channel Equalizer 1 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_R23_LEVEL	0x93	2 Bytes	Right channel Equalizer 2, 3 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Right channel Equalizer 2 level. [7..5]: *Not Used*. [12..8]: Right channel Equalizer 3 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_LS01_LEVEL	0x94	2 Bytes	Left surround channel Equalizer 0, 1 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Left surround channel Equalizer 0 level. [7..5]: *Not Used*. [12..8]: Left surround channel Equalizer 1 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_LS23_LEVEL	0x95	2 Bytes	Left surround channel Equalizer 2, 3 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Left surround channel Equalizer 2 level. [7..5]: *Not Used*. [12..8]: Left surround channel Equalizer 3 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_RS01_LEVEL	0x96	2 Bytes	Right surround channel Equalizer 0, 1 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Right surround channel Equalizer 0 level. [7..5]: *Not Used*. [12..8]: Right surround channel Equalizer 1 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_RS23_LEVEL	0x97	2 Bytes	Right surround channel Equalizer 2, 3 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Right surround channel Equalizer 2 level. [7..5]: *Not Used*. [12..8]: Right surround channel Equalizer 3 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*

Register Name	Address	Word Length	Description
EQ_C01_LEVEL	0x98	2 Bytes	Center channel Equalizer 0, 1 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Center channel Equalizer 0 level. [7..5]: *Not Used*. [12..8]: Center channel Equalizer 1 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_C23_LEVEL	0x99	2 Bytes	Center channel Equalizer 2, 3 level register. Table A-3 shows the relations between the register value and Equalizer level. [4..0]: Center channel Equalizer 2 level. [7..5]: *Not Used*. [12..8]: Center channel Equalizer 3 level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
EQ_MODE	0x9A	2 Bytes	Equalizer operation mode setting register. “0”=Parallel operation (Graphic EQ mode). In this mode, EQ level is effective. “1”=Cascade operation (Parametric EQ mode). In this mode, EQ level is ineffective. [0]: Primary Equalizer filter set operation mode. [1]: Secondary Equalizer filter set operation mode. [15..2]: *Not Used*. *Default = 0x0000 (Parallel, Parallel)*
EQ_P_SHIFT01	0x9B	2 Bytes	Primary Equalizer filter 0, 1 shifting value for scaling. [4..0]: Primary Equalizer 0 shifting value. [7..5]: *Not Used*. [12..8]: Primary Equalizer 1 shifting value. [15..13]: *Not Used*. *Default = 0x0B07 (11, 7)*
EQ_P_SHIFT23	0x9C	2 Bytes	Primary Equalizer filter 2, 3 shifting value for scaling. [4..0]: Primary Equalizer 2 shifting value. [7..5]: *Not Used*. [12..8]: Primary Equalizer 3 shifting value. [15..13]: *Not Used*. *Default = 0x120F (18, 15)*
EQ_S_SHIFT01	0x9D	2 Bytes	Secondary Equalizer filter 0, 1 shifting value for scaling. [4..0]: Secondary Equalizer 0 shifting value. [7..5]: *Not Used*. [12..8]: Secondary Equalizer 1 shifting value. [15..13]: *Not Used*. *Default = 0x0000 (0, 0)*

Register Name	Address	Word Length	Description
EQ_S_SHIFT23	0x9E	2 Bytes	Secondary Equalizer filter 2, 3 shifting value for scaling. [4..0]: Secondary Equalizer 2 shifting value. [7..5]: *Not Used*. [12..8]: Secondary Equalizer 3 shifting value. [15..13]: *Not Used*. *Default = 0x0000 (0, 0)*
Tone Control Registers			
TB_L_LEVEL	0x9F	2 Bytes	Left channel Bass, Treble level register. -15dB to 15dB in 1dB/step resolution. Table A-3 shows the relations between the register value and tone control level. [4..0]: Left channel Bass level. [7..5]: *Not Used*. [12..8]: Left channel Treble level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
TB_R_LEVEL	0xA0	2 Bytes	Right channel Bass, Treble level register. Table A-3 shows the relations between the register value and tone control level. [4..0]: Right channel Bass level. [7..5]: *Not Used*. [12..8]: Right channel Treble level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
TB_LS_LEVEL	0xA1	2 Bytes	Left Surround channel Bass, Treble level register. Table A-3 shows the relations between the register value and tone control level. [4..0]: Left Surround channel Bass level. [7..5]: *Not Used*. [12..8]: Left Surround channel Treble level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
TB_RS_LEVEL	0xA2	2 Bytes	Right Surround channel Bass, Treble level register. Table A-3 shows the relations between the register value and tone control level. [4..0]: Right Surround channel Bass level. [7..5]: *Not Used*. [12..8]: Right Surround channel Treble level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*
TB_C_LEVEL	0xA3	2 Bytes	Center channel Bass, Treble level register. Table A-3 shows the relations between the register value and tone control level. [4..0]: Center channel Bass level. [7..5]: *Not Used*. [12..8]: Center channel Treble level. [15..13]: *Not Used*. *Default = 0x0000 (0dB, 0dB)*

Register Name	Address	Word Length	Description
TB_FILTER_SHIFT	0xA4	2 Bytes	Treble, Bass filter shifting value for scaling. [4..0]: Bass filter shifting value. [7..5]: *Not Used*. [12..8]: Treble filter shifting value. [15..13]: *Not Used*. *Default = 0x120D (18, 13)*
Bass Management Configuration Registers			
BM_PATH_SELECT	0xA5	2 Bytes	Bass Management path control Register [0]: Subwoofer output path selection control. "0"=Bass Sum is sent to Subwoofer output. "1"=LFE channel is sent to Subwoofer output. *Default = "0" (Bass Sum to Subwoofer).* [1]: Bass Sum low-pass filter bypass control. *Default = "0" (Filter Enable).* "0"=Filter Enable "1"=Bypass (Filter Disable). [2]: Bass Sum low-pass filter order. *Default = "0" (4th order).* "0"=4th order "1"=2nd order. [7..3]: *Not Used*. [8]: Left channel bass management low-cut filter enable control. Active high. "0"=Disable. "1"=Enable. *Default = "0" (Filter Disable).* [9]: Right channel bass management low-cut filter control. Active high. "0"=Disable. "1"=Enable. *Default = "0" (Filter Disable).* [10]: Left surround channel bass management low-cut filter control. Active high. "0"=Disable. "1"=Enable. *Default = "0" (Filter Disable).* [11]: Right surround channel bass management low-cut filter control. Active high. "0"=Disable. "1"=Enable. *Default = "0" (Filter Disable).* [12]: Center channel bass management low-cut filter control. Active high. "0"=Disable. "1"=Enable. *Default = "0" (Filter Disable).* [15..13]: *Not Used*. *Default = 0x0000*
BM_LR2SUM_LEVEL	0xA6	2 Bytes	Left and Right channel into Bass Sum mixing level register. The each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity ("0" : +, "1" : -) and LS 7-bit is the mixing level coefficient. Table A-2 shows the relations between the register value and mixing level. [7..0]: Left channel input into Bass Sum mixing level. [15..8]: Right channel input into Bass Sum mixing level. *Default = 0x4242 ((+) -15dB, (+) –15dB)*
BM_LSRS2SUM_LEVEL	0xA7	2 Bytes	Left surround and Right surround channel into Bass Sum mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Left surround channel input into Bass Sum mixing level. [15..8]: Right surround channel input into Bass Sum mixing level. *Default = 0x4242 ((+) -15dB, (+) –15dB)*

Register Name	Address	Word Length	Description
BM_CLFE2SUM_LEVEL	0xA8	2 Bytes	Center and LFE channel into Bass Sum mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Center channel input into Bass Sum mixing level. [15..8]: LFE channel input into Bass Sum mixing level. *Default = 0x2E42 ((+) -5dB, (+) -15dB)*
BM_LFE_BYPASS_LEVEL	0xA9	2 Bytes	LFE into Subwoofer output bypass level register. This is effective when LFE channel input is bypassed to Subwoofer output. Table A-2 shows the relations between the register value and bypass level. [7..0]: LFE into Subwoofer output bypass level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_L2L_LEVEL	0xAA	2 Bytes	Left channel input into Left channel pass-through mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Left channel input into Left channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFESUM2L_LEVEL	0xAB	2 Bytes	LFE channel and Bass Sum into Left channel output mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Left channel output mixing level. [15..8]: Bass Sum into Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_R2R_LEVEL	0xAC	2 Bytes	Right channel input into Right channel pass-through mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Right channel input into Right channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFESUM2R_LEVEL	0xAD	2 Bytes	LFE channel and Bass Sum into Right channel output mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Right channel output mixing level. [15..8]: Bass Sum into Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_LS2LS_LEVEL	0xAE	2 Bytes	Left surround channel input into Left surround channel pass-through mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Left surround channel input into Left surround channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*

Register Name	Address	Word Length	Description
BM_LFESUM2LS_LEVEL	0xAF	2 Bytes	LFE channel and Bass Sum into Left surround channel output mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Left surround channel output mixing level. [15..8]: Bass Sum into Left surround channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_RS2RS_LEVEL	0xB0	2 Bytes	Right surround channel input into Right surround channel pass-through mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Right surround channel input into Right surround channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFESUM2RS_LEVEL	0xB1	2 Bytes	LFE channel and Bass Sum into Right surround channel output mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Right surround channel output mixing level. [15..8]: Bass Sum into Right surround channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_C2C_LEVEL	0xB2	2 Bytes	Center channel input into Center channel pass-through mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: Center channel input into Center channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFESUM2C_LEVEL	0xB3	2 Bytes	LFE channel and Bass Sum into Center channel output mixing level register. Table A-2 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Center channel output mixing level. [15..8]: Bass Sum into Center channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_FILTER_SHIFT	0xB4	2 Bytes	Bass Management LPF shifting value for scaling. [4..0]: Bass Sum low-pass filter shifting value. [7..5]: *Not Used*. [12..8]: *Reserved*. [15..13]: *Not Used*. *Default = 0x0505*
BM_EQ_TONE_SEQ_SEL	0xB5	2 Bytes	Equalizer, Tone control, Bass Management sequence selection register. [1..0]: Equalizer, Tone control, Bass Management sequence selector. "00" = Equalizer → Tone control → Bass Management. "01" = Tone control → Bass Management → Equalizer. "10" = Bass Management → Equalizer → Tone control. *Default = "00" (Equalizer → Tone control → Bass Management).* [15..2]: *Not Used*. *Default = 0x0000*

Register Name	Address	Word Length	Description
Output Channel Mapping Configuration Registers			
OUT_CH_MAPPING1	0xB6	2 Bytes	Internal processing channel into output channel Mapping Register1. "0" : Left channel "1" : Right channel "2" : Left surround channel "3" : Right surround channel "4" : Subwoofer channel "5" : Center channel "6", "7" : Mute channel [2:0]: Internal processing channel which is linked to Output channel 1. [3]: *Not Used*. [6:4]: Internal processing channel which is linked to Output channel 2. [7]: *Not Used*. [10:8]: Internal processing channel which is linked to Output channel 3. [11]: *Not Used*. [14:12]: Internal processing channel which is linked to Output channel 4. [15]: *Not Used*. *Default = 0x3210*
OUT_CH_MAPPING2	0xB7	2 Bytes	Internal processing channel into output channel Mapping Register2. [2:0]: Internal processing channel which is linked to Output channel 6. [3]: *Not Used*. [6:4]: Internal processing channel which is linked to Output channel 5. [15:7]: *Not Used*. *Default = 0x0054*
REC_SOURCE_SEL	0xB8	2 Bytes	Source for Record output selection register. [0]: Source for Record output. "0"=Left and Right channel of mixer output. "1"=Left and Right channel of mixer input. [15:1]: *Not Used*. *Default = 0x0000 (mixer output)*

Register Name	Address	Word Length	Description
Coefficient for Primary Equalizing Filter Registers			
P_EQ0_A1	0xC0	3 Bytes	-A1 coefficient for Primary Equalizing filter 0. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3F89D8 (120~500Hz Band pass filter)*
P_EQ0_A2	0xC1	3 Bytes	-A2 coefficient for Primary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE07595 (120~500Hz Band pass filter)*
P_EQ0_B0	0xC2	3 Bytes	B0 coefficient for Primary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x003B4F (120~500Hz Band pass filter)*
P_EQ0_B1	0xC3	3 Bytes	B1 coefficient for Primary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (120~500Hz Band pass filter)*
P_EQ0_B2	0xC4	3 Bytes	B2 coefficient for Primary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFFC4B1 (120~500Hz Band pass filter)*
P_EQ1_A1	0xC5	3 Bytes	-A1 coefficient for Primary Equalizing filter 1. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3E66D9 (500~2KHz Band pass filter)*
P_EQ1_A2	0xC6	3 Bytes	-A2 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE19098 (500~2KHz Band pass filter)*
P_EQ1_B0	0xC7	3 Bytes	B0 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x00C894 (500~2KHz Band pass filter)*
P_EQ1_B1	0xC8	3 Bytes	B1 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (500~2KHz Band pass filter)*
P_EQ1_B2	0xC9	3 Bytes	B2 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFF376C (500~2KHz Band pass filter)*

Register Name	Address	Word Length	Description
P_EQ2_A1	0xCA	3 Bytes	-A1 coefficient for Primary Equalizing filter 2. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3995F1 (2K~8KHz Band pass filter)*
P_EQ2_A2	0xCB	3 Bytes	-A2 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE5EA70 (2K~8KHz Band pass filter)*
P_EQ2_B0	0xCC	3 Bytes	B0 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x02F53E (2K~8KHz Band pass filter)*
P_EQ2_B1	0xCD	3 Bytes	B1 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (2K~8KHz Band pass filter)*
P_EQ2_B2	0xCE	3 Bytes	B2 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFD0AC2 (2K~8KHz Band pass filter)*
P_EQ3_A1	0xCF	3 Bytes	-A1 coefficient for Primary Equalizing filter 3. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x2CF124 (8K~24KHz Band pass filter)*
P_EQ3_A2	0xD0	3 Bytes	-A2 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xEDDFAE (8K~24KHz Band pass filter)*
P_EQ3_B0	0xD1	3 Bytes	B0 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x06EFD7 (8K~24KHz Band pass filter)*
P_EQ3_B1	0xD2	3 Bytes	B1 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (8K~24KHz Band pass filter)*
P_EQ3_B2	0xD3	3 Bytes	B2 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). This register is not readable. *Default = 0xF91029 (8K~24KHz Band pass filter)*

Register Name	Address	Word Length	Description
Coefficient for Secondary Equalizing Filter Registers			
S_EQ0_A1	0xD4	3 Bytes	-A1 coefficient for Secondary Equalizing filter 0. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ0_A2	0xD5	3 Bytes	-A2 coefficient for Secondary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ0_B0	0xD6	3 Bytes	B0 coefficient for Secondary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ0_B1	0xD7	3 Bytes	B1 coefficient for Secondary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ0_B2	0xD8	3 Bytes	B2 coefficient for Secondary Equalizing filter 0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ1_A1	0xD9	3 Bytes	-A1 coefficient for Secondary Equalizing filter 1. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ1_A2	0xDA	3 Bytes	-A2 coefficient for Secondary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ1_B0	0xDB	3 Bytes	B0 coefficient for Secondary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ1_B1	0xDC	3 Bytes	B1 coefficient for Secondary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ1_B2	0xDD	3 Bytes	B2 coefficient for Secondary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*

Register Name	Address	Word Length	Description
S_EQ2_A1	0xDE	3 Bytes	-A1 coefficient for Secondary Equalizing filter 2. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ2_A2	0xDF	3 Bytes	-A2 coefficient for Secondary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ2_B0	0xE0	3 Bytes	B0 coefficient for Secondary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ2_B1	0xE1	3 Bytes	B1 coefficient for Secondary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ2_B2	0xE2	3 Bytes	B2 coefficient for Secondary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ3_A1	0xE3	3 Bytes	-A1 coefficient for Secondary Equalizing filter 3. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ3_A2	0xE4	3 Bytes	-A2 coefficient for Secondary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ3_B0	0xE5	3 Bytes	B0 coefficient for Secondary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ3_B1	0xE6	3 Bytes	B1 coefficient for Secondary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
S_EQ3_B2	0xE7	3 Bytes	B2 coefficient for Secondary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*

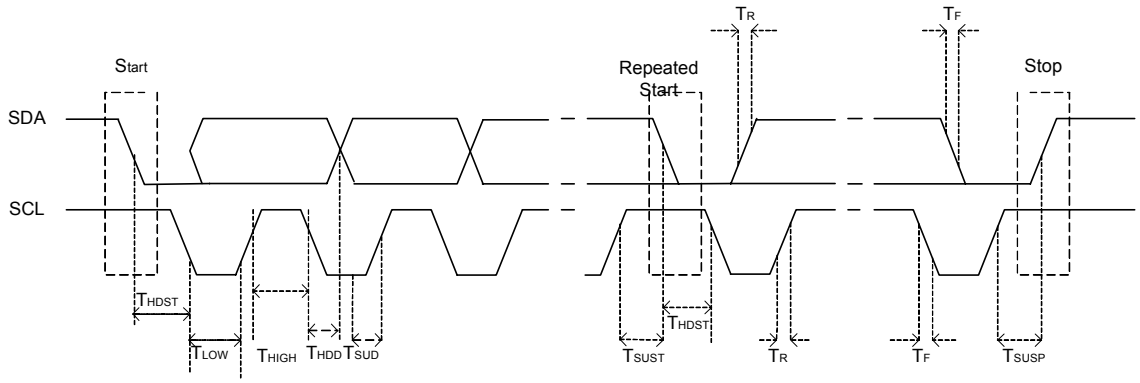
Register Name	Address	Word Length	Description
Coefficient for Tone Control Filter Registers			
BASS_LPF_A1	0xE8	3 Bytes	-A1 coefficient for Bass Low pass filter. The filter is a 1st order filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1}) / (1 + A1 \cdot z^{-1})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FCA6E (200Hz Low pass filter)*
BASS_LPF_B0	0xE9	3 Bytes	B0 coefficient for Bass Low pass filter. B1 coefficient is equal to B0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x001AC8 (200Hz Low pass filter)*
TREBLE_HPF_A1	0xEA	3 Bytes	-A1 coefficient for Treble High pass filter. The filter is a 1st order filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1}) / (1 + A1 \cdot z^{-1})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1A462C (6KHz High pass filter)** * Above default value is not device default value. It is recommended default value. The PS9702B has erroneous default values of treble filter coefficient registers. In real device, 0xEA register has "*0x1D2316*" default value and 0xEB register has "*0x1A462C*" default value. If one wants to use the treble function, 0xEA and 0xEB register must be initialized as the above recommended values.
TREBLE_HPF_B0	0xEB	3 Bytes	B0 coefficient for Treble High pass filter. B1 coefficient is equal to -B0. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1D2316 (6KHz High pass filter)** * Above default value is not device default value. It is recommended default value. The PS9702B has erroneous default values of treble filter coefficient registers. In real device, 0xEA register has "*0x1D2316*" default value and 0xEB register has "*0x1A462C*" default value. If one wants to use the treble function, 0xEA and 0xEB register must be initialized as the above recommended values.

Register Name	Address	Word Length	Description
Coefficient for Bass Management Low Pass Filter Registers			
BM_LPF_A1	0xEC	3 Bytes	-A1 coefficient for Bass Management Low pass filter. The filter is an equally cascaded bi-quad filter (4^{th} order filter). A0 coefficient is fixed at value 1. Sampling Frequency of the filter is 192KHz. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2})^2 / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})^2$ 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FD273 (120Hz Low pass filter)*
BM_LPF_A2	0xED	3 Bytes	-A2 coefficient for Bass Management Low pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE02D6D (120Hz Low pass filter)*
BM_LPF_B0	0xEE	3 Bytes	B0 coefficient for Bass Management Low pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000008 (120Hz Low pass filter)*
BM_LPF_B1	0xEF	3 Bytes	B1 coefficient for Bass Management Low pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000010 (120Hz Low pass filter)*
BM_LPF_B2	0xF0	3 Bytes	B2 coefficient for Bass Management Low pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000008 (120Hz Low pass filter)*
Coefficient for Bass Management High Pass Filter Registers			
BM_HPF_A1	0xF1	3 Bytes	-A1 coefficient for Bass Management High pass filter. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FD273 (120Hz High pass filter)*
BM_HPF_A2	0xF2	3 Bytes	-A2 coefficient for Bass Management High pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE02D6D (120Hz High pass filter)*
BM_HPF_B0	0xF3	3 Bytes	B0 coefficient for Bass Management High pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FE93F (120Hz High pass filter)*
BM_HPF_B1	0xF4	3 Bytes	B1 coefficient for Bass Management High pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xC02D82 (120Hz High pass filter)*
BM_HPF_B2	0xF5	3 Bytes	B2 coefficient for Bass Management High pass filter. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FE93F (120Hz High pass filter)*

AC Characteristics

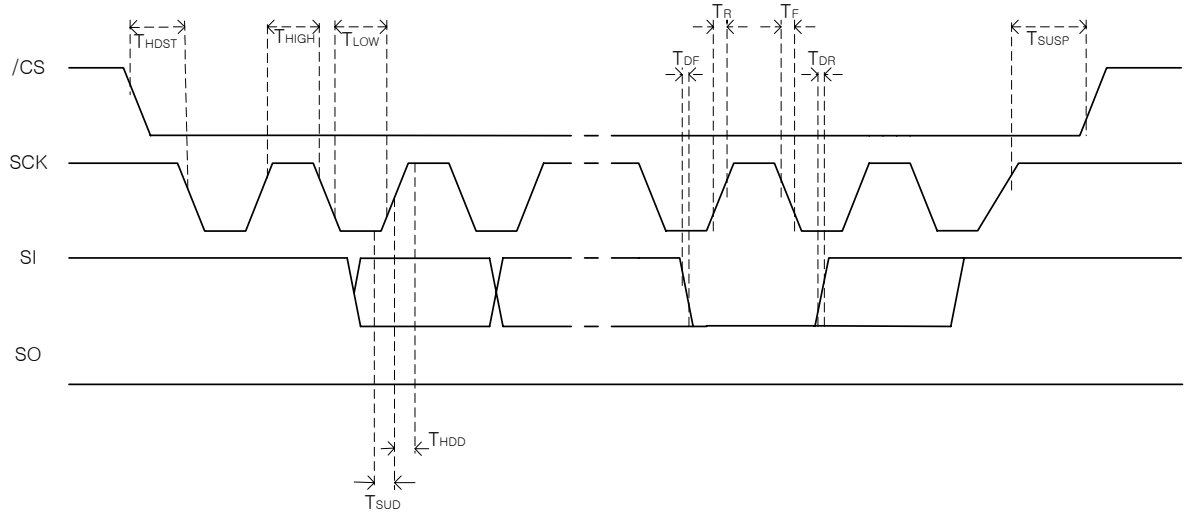
1. I²C Control Interface Timing

Parameter	Symbol	Min	-	Max	Units
SCL Clock Frequency				800	kHz
Start Condition Hold Time (Prior to first clock pulse)	T_{HDST}	200			ns
Clock Low Time	T_{LOW}	400			ns
Clock High Time	T_{HIGH}	400			ns
Setup Time For Repeated Start Condition	T_{SUST}	200			ns
Data Hold Time	T_{HDD}	0			ns
Data Set-Up Time	T_{SUD}	100			ns
Rise Time of both SDA and SCL	T_R			300	ns
Falling Time of both SDA and SCL	T_F			300	ns
Setup Time for Stop Condition	T_{SUSP}	200			ns



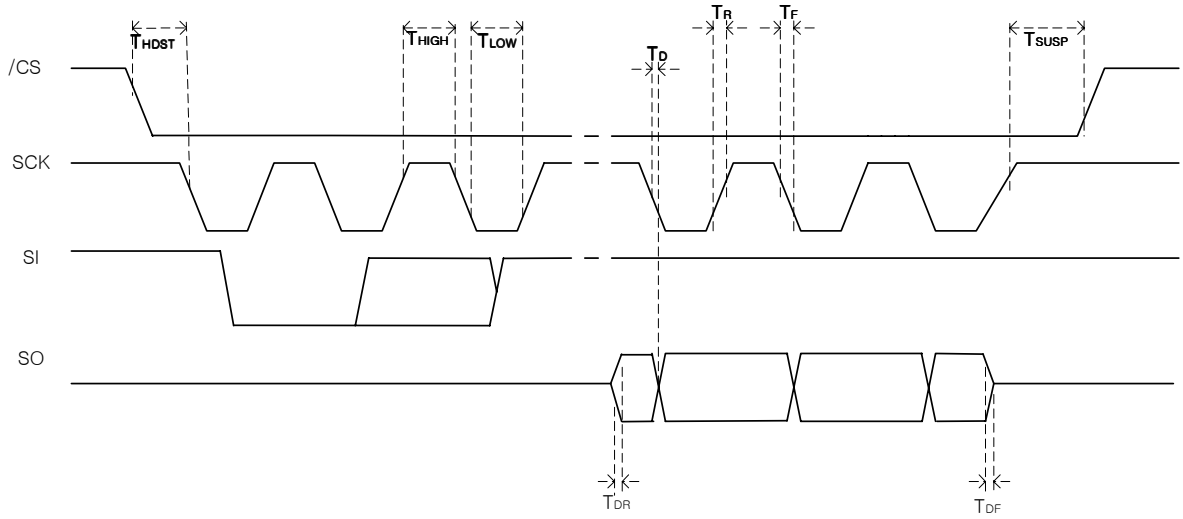
2. SPI Write Timing

Parameter	Symbol	Min	-	Max	Units
Start Condition Hold Time	T_{HDST}	200			ns
Clock High Time	T_{HIGH}	400			ns
Clock Low Time	T_{LOW}	400			ns
SI Setup Time to SCK	T_{SUD}	100			ns
Data Hold Time	T_{HDD}	0			ns
Falling Time of both SI and SCK	T_{DF}			300	ns
Rising Time of both SI and SCK	T_{DR}			300	ns
Setup Time for Stop Condition	T_{SUSP}	200			ns



3. SPI Read Timing

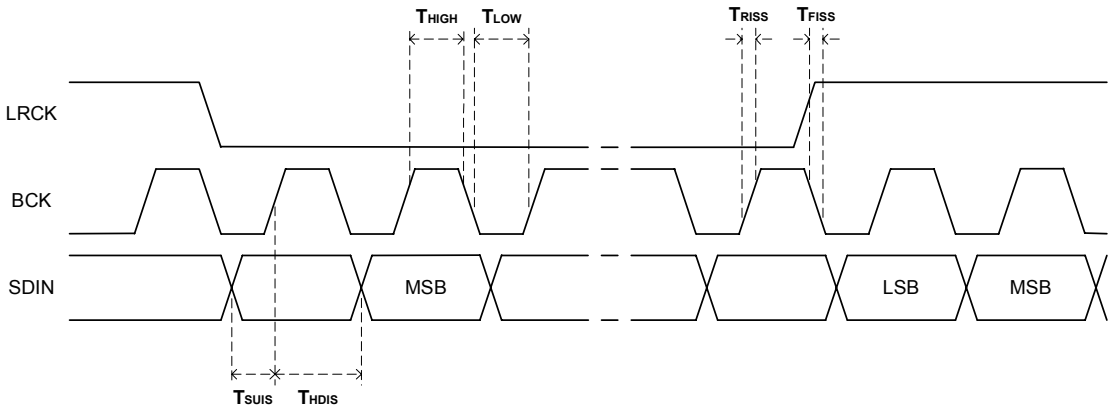
Parameter	Symbol	Min	-	Max	Units
Start Condition Hold Time	T_{HDST}	200			ns
Clock High Time	T_{HIGH}	400			ns
Clock Low Time	T_{LOW}	400			ns
SO Delay time for Valid Data	T_D	100			ns
Falling Time of both SO and SCK	T_{DF}			300	ns
Rising Time of both SO and SCK	T_{DR}			300	ns
Setup Time for Stop Condition	T_{SUSP}	200			ns



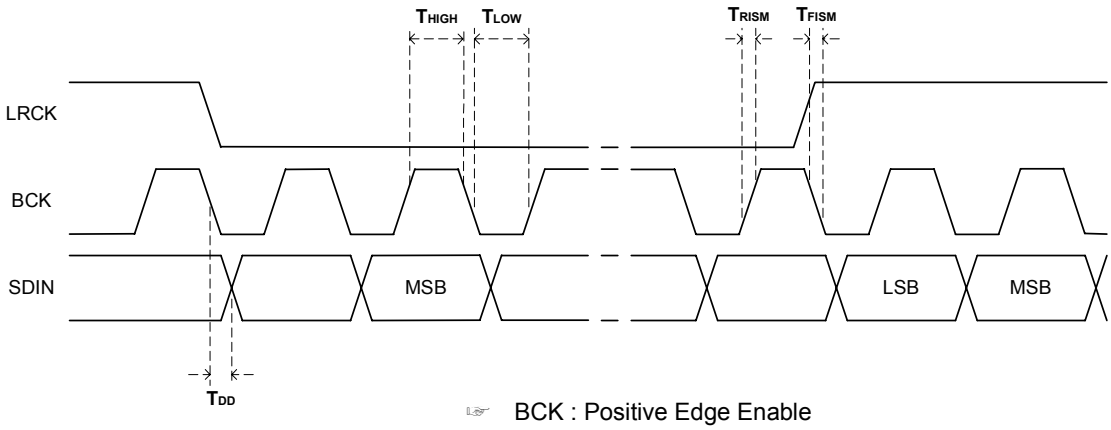
4. I²S Data Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Data Holding Time	T_{HDIS}	25			ns
Data Setup Time	T_{SUIS}	25			ns
Clock High Time	T_{HIGH}	80	180		ns
Clock Low Time	T_{LOW}	80	180		ns
Rising Time of SCK (Slave Mode)	T_{RISS}			20	ns
Falling Time of SCK (Slave Mode)	T_{FISS}			20	ns
Rising Time of SCK (Master Mode)	T_{RISM}		3	5	ns
Falling Time of SCK (Master Mode)	T_{FISM}		3	5	ns
Delay until valid Data	T_{DD}	20		40	ns

Slave Mode



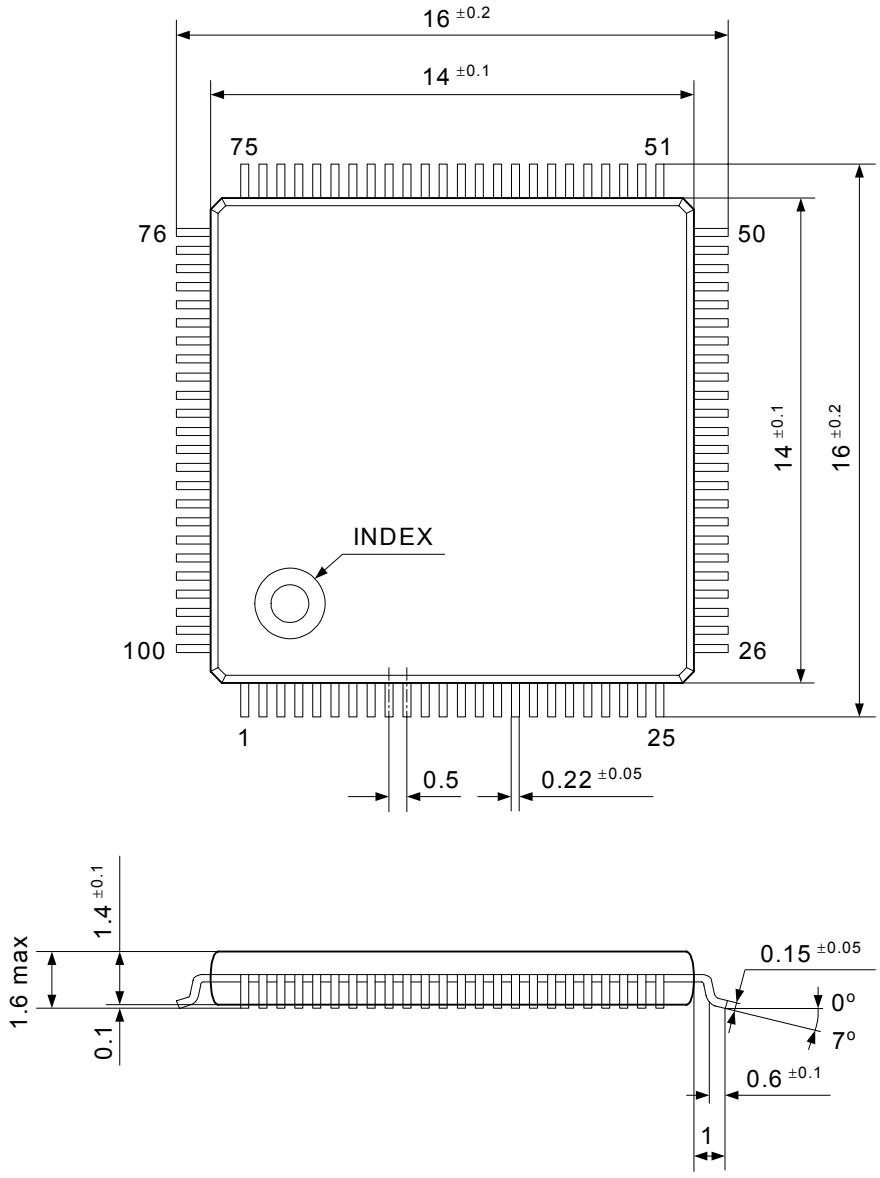
Master Mode



☞ BCK : Positive Edge Enable

Package Dimensions

Unit : mm



Appendix A
Gain-Register Value Table

Table A-1. Volume Gain Values

Gain (dB)	Register Value
24.0	0x00
23.5	0x01
23.0	0x02
22.5	0x03
22.0	0x04
21.5	0x05
21.0	0x06
20.5	0x07
20.0	0x08
19.5	0x09
19.0	0x0A
18.5	0x0B
18.0	0x0C
17.5	0x0D
17.0	0x0E
16.5	0x0F
16.0	0x10
15.5	0x11
15.0	0x12
14.5	0x13
14.0	0x14
13.5	0x15
13.0	0x16
12.5	0x17
12.0	0x18
11.5	0x19
11.0	0x1A
10.5	0x1B
10.0	0x1C
9.5	0x1D
9.0	0x1E
8.5	0x1F
8.0	0x20
7.5	0x21
7.0	0x22
6.5	0x23
6.0	0x24
5.5	0x25
5.0	0x26
4.5	0x27
4.0	0x28
3.5	0x29
3.0	0x2A
2.5	0x2B
2.0	0x2C

Gain (dB)	Register Value
1.5	0x2D
1.0	0x2E
0.5	0x2F
0.0	0x30
-0.5	0x31
-1.0	0x32
-1.5	0x33
-2.0	0x34
-2.5	0x35
-3.0	0x36
-3.5	0x37
-4.0	0x38
-4.5	0x39
-5.0	0x3A
-5.5	0x3B
-6.0	0x3C
-6.5	0x3D
-7.0	0x3E
-7.5	0x3F
-8.0	0x40
-8.5	0x41
-9.0	0x42
-9.5	0x43
-10.0	0x44
-10.5	0x45
-11.0	0x46
-11.5	0x47
-12.0	0x48
-12.5	0x49
-13.0	0x4A
-13.5	0x4B
-14.0	0x4C
-14.5	0x4D
-15.0	0x4E
-15.5	0x4F
-16.0	0x50
-16.5	0x51
-17.0	0x52
-17.5	0x53
-18.0	0x54
-18.5	0x55
-19.0	0x56
-19.5	0x57
-20.0	0x58
-20.5	0x59

Gain (dB)	Register Value
-21.0	0x5A
-21.5	0x5B
-22.0	0x5C
-22.5	0x5D
-23.0	0x5E
-23.5	0x5F
-24.0	0x60
-24.5	0x61
-25.0	0x62
-25.5	0x63
-26.0	0x64
-26.5	0x65
-27.0	0x66
-27.5	0x67
-28.0	0x68
-28.5	0x69
-29.0	0x6A
-29.5	0x6B
-30.0	0x6C
-30.5	0x6D
-31.0	0x6E
-31.5	0x6F
-32.0	0x70
-32.5	0x71
-33.0	0x72
-33.5	0x73
-34.0	0x74
-34.5	0x75
-35.0	0x76
-35.5	0x77
-36.0	0x78
-36.5	0x79
-37.0	0x7A
-37.5	0x7B
-38.0	0x7C
-38.5	0x7D
-39.0	0x7E
-39.5	0x7F
-40.0	0x80
-40.5	0x81
-41.0	0x82
-41.5	0x83
-42.0	0x84
-42.5	0x85
-43.0	0x86

Gain (dB)	Register Value
-43.5	0x87
-44.0	0x88
-44.5	0x89
-45.0	0x8A
-45.5	0x8B
-46.0	0x8C
-46.5	0x8D
-47.0	0x8E
-47.5	0x8F
-48.0	0x90
-48.5	0x91
-49.0	0x92
-49.5	0x93
-50.0	0x94
-50.5	0x95
-51.0	0x96
-51.5	0x97
-52.0	0x98
-52.5	0x99
-53.0	0x9A
-53.5	0x9B
-54.0	0x9C
-54.5	0x9D
-55.0	0x9E
-55.5	0x9F
-56.0	0xA0
-56.5	0xA1
-57.0	0xA2
-57.5	0xA3
-58.0	0xA4
-58.5	0xA5
-59.0	0xA6
-59.5	0xA7
-60.0	0xA8
-60.5	0xA9
-61.0	0xAA
-61.5	0xAB
-62.0	0xAC
-62.5	0xAD
-63.0	0xAE
-63.5	0xAF
-64.0	0xB0
-64.5	0xB1
-65.0	0xB2
-65.5	0xB3

Gain (dB)	Register Value
-66.0	0xB4
-66.5	0xB5
-67.0	0xB6
-67.5	0xB7
-68.0	0xB8
-68.5	0xB9
-69.0	0xBA
-69.5	0xBB
-70.0	0xBC
Mute	0xBD
|	|
Mute	0xFF

Table A-2. Mixer Gain Values

Signal Polarity	Gain (dB)	Register Value	Signal Polarity	Gain (dB)	Register Value	Signal Polarity	Gain (dB)	Register Value
+	18.0	0x00	+	-2.5	0x29	+	-23.0	0x52
+	17.5	0x01	+	-3.0	0x2A	+	-23.5	0x53
+	17.0	0x02	+	-3.5	0x2B	+	-24.0	0x54
+	16.5	0x03	+	-4.0	0x2C	+	-24.5	0x55
+	16.0	0x04	+	-4.5	0x2D	+	-25.0	0x56
+	15.5	0x05	+	-5.0	0x2E	+	-25.5	0x57
+	15.0	0x06	+	-5.5	0x2F	+	-26.0	0x58
+	14.5	0x07	+	-6.0	0x30	+	-26.5	0x59
+	14.0	0x08	+	-6.5	0x31	+	-27.0	0x5A
+	13.5	0x09	+	-7.0	0x32	+	-27.5	0x5B
+	13.0	0x0A	+	-7.5	0x33	+	-28.0	0x5C
+	12.5	0x0B	+	-8.0	0x34	+	-28.5	0x5D
+	12.0	0x0C	+	-8.5	0x35	+	-29.0	0x5E
+	11.5	0x0D	+	-9.0	0x36	+	-29.5	0x5F
+	11.0	0x0E	+	-9.5	0x37	+	-30.0	0x60
+	10.5	0x0F	+	-10.0	0x38	+	-30.5	0x61
+	10.0	0x10	+	-10.5	0x39	+	-31.0	0x62
+	9.5	0x11	+	-11.0	0x3A	+	-31.5	0x63
+	9.0	0x12	+	-11.5	0x3B	+	-32.0	0x64
+	8.5	0x13	+	-12.0	0x3C	+	-32.5	0x65
+	8.0	0x14	+	-12.5	0x3D	+	-33.0	0x66
+	7.5	0x15	+	-13.0	0x3E	+	-33.5	0x67
+	7.0	0x16	+	-13.5	0x3F	+	-34.0	0x68
+	6.5	0x17	+	-14.0	0x40	+	-34.5	0x69
+	6.0	0x18	+	-14.5	0x41	+	-35.0	0x6A
+	5.5	0x19	+	-15.0	0x42	+	-35.5	0x6B
+	5.0	0x1A	+	-15.5	0x43	+	-36.0	0x6C
+	4.5	0x1B	+	-16.0	0x44	+	-36.5	0x6D
+	4.0	0x1C	+	-16.5	0x45	+	-37.0	0x6E
+	3.5	0x1D	+	-17.0	0x46	+	-37.5	0x6F
+	3.0	0x1E	+	-17.5	0x47	+	-38.0	0x70
+	2.5	0x1F	+	-18.0	0x48	+	-38.5	0x71
+	2.0	0x20	+	-18.5	0x49	+	-39.0	0x72
+	1.5	0x21	+	-19.0	0x4A	+	-39.5	0x73
+	1.0	0x22	+	-19.5	0x4B	+	-40.0	0x74
+	0.5	0x23	+	-20.0	0x4C	+	-40.5	0x75
+	0.0	0x24	+	-20.5	0x4D	+	-41.0	0x76
+	-0.5	0x25	+	-21.0	0x4E	+	-41.5	0x77
+	-1.0	0x26	+	-21.5	0x4F	+	-42.0	0x78
+	-1.5	0x27	+	-22.0	0x50		Mute	0x79
+	-2.0	0x28	+	-22.5	0x51		Mute	0x7F

Table A-2. Mixer Gain Values (Continued)

Signal Polarity	Gain (dB)	Register Value
-	18.0	0x80
-	17.5	0x81
-	17.0	0x82
-	16.5	0x83
-	16.0	0x84
-	15.5	0x85
-	15.0	0x86
-	14.5	0x87
-	14.0	0x88
-	13.5	0x89
-	13.0	0x8A
-	12.5	0x8B
-	12.0	0x8C
-	11.5	0x8D
-	11.0	0x8E
-	10.5	0x8F
-	10.0	0x90
-	9.5	0x91
-	9.0	0x92
-	8.5	0x93
-	8.0	0x94
-	7.5	0x95
-	7.0	0x96
-	6.5	0x97
-	6.0	0x98
-	5.5	0x99
-	5.0	0x9A
-	4.5	0x9B
-	4.0	0x9C
-	3.5	0x9D
-	3.0	0x9E
-	2.5	0x9F
-	2.0	0xA0
-	1.5	0XA1
-	1.0	0XA2
-	0.5	0XA3
-	0.0	0XA4
-	-0.5	0xA5
-	-1.0	0xA6
-	-1.5	0xA7
-	-2.0	0xA8

Signal Polarity	Gain (dB)	Register Value
-	-2.5	0xA9
-	-3.0	0xAA
-	-3.5	0xAB
-	-4.0	0xAC
-	-4.5	0xAD
-	-5.0	0xAE
-	-5.5	0xAF
-	-6.0	0xB0
-	-6.5	0xB1
-	-7.0	0xB2
-	-7.5	0xB3
-	-8.0	0xB4
-	-8.5	0xB5
-	-9.0	0xB6
-	-9.5	0xB7
-	-10.0	0xB8
-	-10.5	0xB9
-	-11.0	0xBA
-	-11.5	0xBB
-	-12.0	0xBC
-	-12.5	0xBD
-	-13.0	0xBE
-	-13.5	0xBF
-	-14.0	0xC0
-	-14.5	0xC1
-	-15.0	0xC2
-	-15.5	0xC3
-	-16.0	0xC4
-	-16.5	0xC5
-	-17.0	0xC6
-	-17.5	0xC7
-	-18.0	0xC8
-	-18.5	0xC9
-	-19.0	0xCA
-	-19.5	0xCB
-	-20.0	0xCC
-	-20.5	0xCD
-	-21.0	0xCE
-	-21.5	0xCF
-	-22.0	0xD0
-	-22.5	0xD1

Signal Polarity	Gain (dB)	Register Value
-	-23.0	0xD2
-	-23.5	0xD3
-	-24.0	0xD4
-	-24.5	0xD5
-	-25.0	0xD6
-	-25.5	0xD7
-	-26.0	0xD8
-	-26.5	0xD9
-	-27.0	0xDA
-	-27.5	0xDB
-	-28.0	0xDC
-	-28.5	0xDD
-	-29.0	0xDE
-	-29.5	0xDF
-	-30.0	0xE0
-	-30.5	0xE1
-	-31.0	0xE2
-	-31.5	0xE3
-	-32.0	0xE4
-	-32.5	0xE5
-	-33.0	0xE6
-	-33.5	0xE7
-	-34.0	0xE8
-	-34.5	0xE9
-	-35.0	0xEA
-	-35.5	0xEB
-	-36.0	0xEC
-	-36.5	0xED
-	-37.0	0xEE
-	-37.5	0xEF
-	-38.0	0xF0
-	-38.5	0xF1
-	-39.0	0xF2
-	-39.5	0xF3
-	-40.0	0xF4
-	-40.5	0xF5
-	-41.0	0xF6
-	-41.5	0xF7
-	-42.0	0xF8
	Mute	0xF9
	Mute	0xFF

Table A-3. EQ, Treble, Bass Gain Values

Gain (dB)	Register Value
15.0	0x0F
14.0	0x0E
13.0	0x0D
12.0	0x0C
11.0	0x0B
10.0	0x0A
9.0	0x09
8.0	0x08
7.0	0x07
6.0	0x06
5.0	0x05
4.0	0x04
3.0	0x03
2.0	0x02
1.0	0x01
0.0	0x00

Gain (dB)	Register Value
-1.0	0x1F
-2.0	0x1E
-3.0	0x1D
-4.0	0x1C
-5.0	0x1B
-6.0	0x1A
-7.0	0x19
-8.0	0x18
-9.0	0x17
-10.0	0x16
-11.0	0x15
-12.0	0x14
-13.0	0x13
-14.0	0x12
-15.0	0x11