



# PRMD2

## 50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

14 September 2018

Product data sheet

### 1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) in a leadless ultra small DFN1412-6 (SOT1268) Surface-Mounted Device (SMD) plastic package.

### 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

### 3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

### 4. Quick reference data

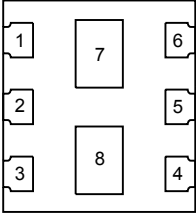
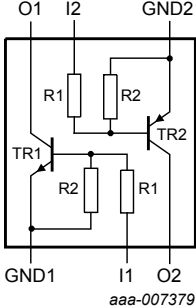
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
$V_{CEO}$	collector-emitter voltage	open base	-	-	50	V
$I_O$	output current		-	-	100	mA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ °C}$	60	-	-	
R1	bias resistor 1	[1]	15.4	22	28.6	k $\Omega$
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>Transparent top view DFN1412-6 (SOT1268)</p>	 <p>aaa-007379</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PRMD2	DFN1412-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm	SOT1268

7. Marking

Table 4. Marking codes

Type number	Marking code
PRMD2	B4

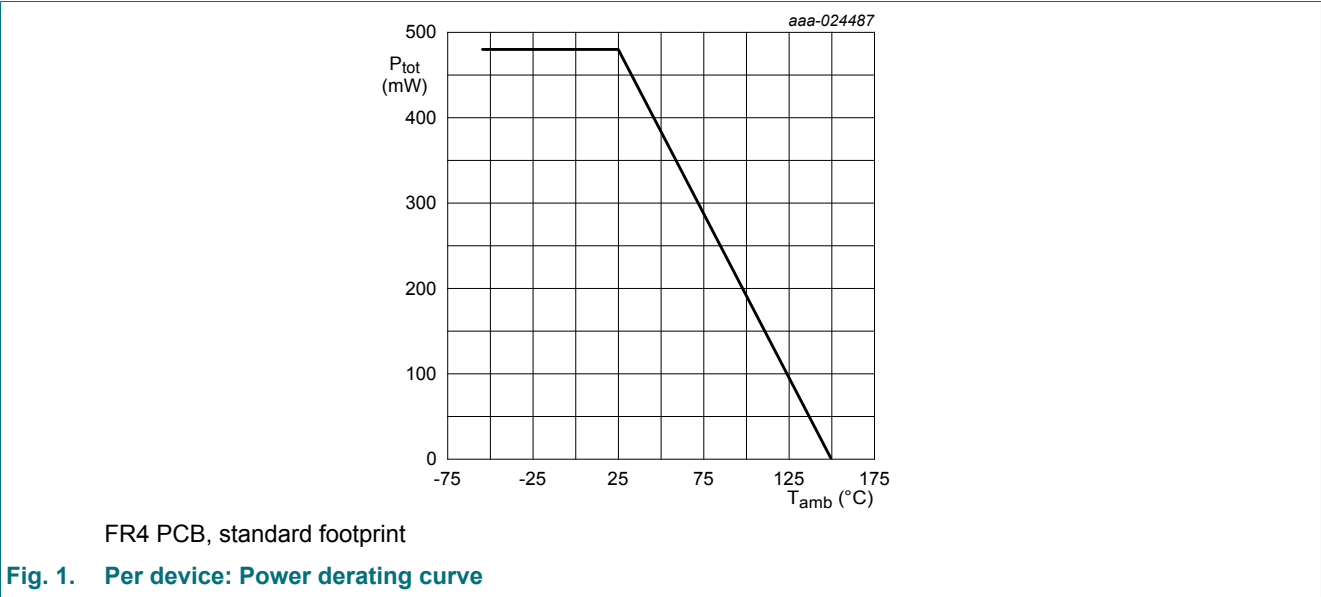
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	10	V
V <sub>I</sub>	input voltage			-10	40	V
I <sub>O</sub>	output current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	325	mW
Per device						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	480	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

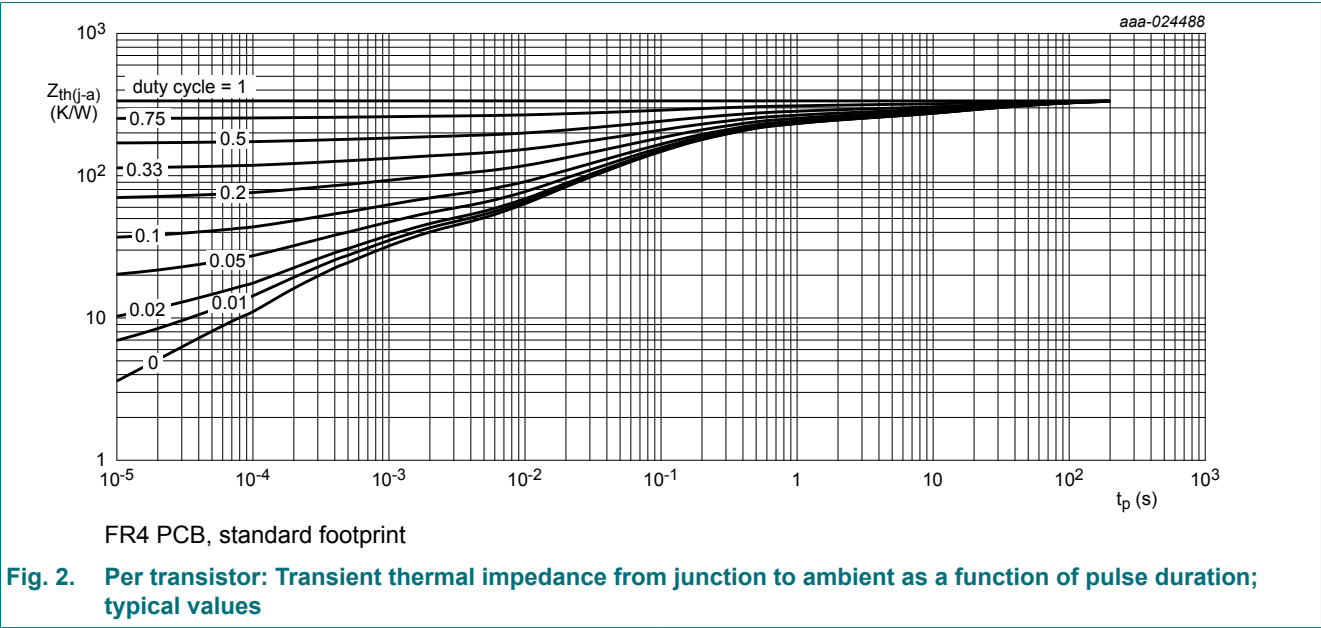


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



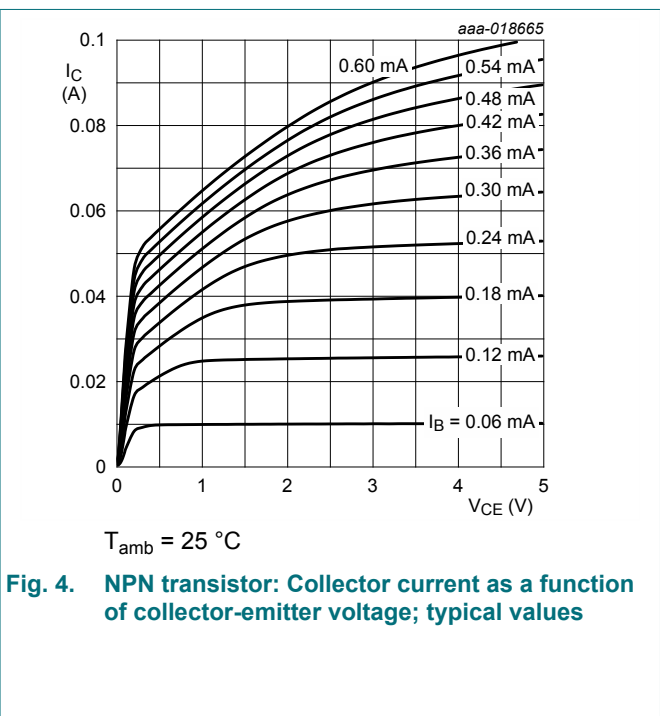
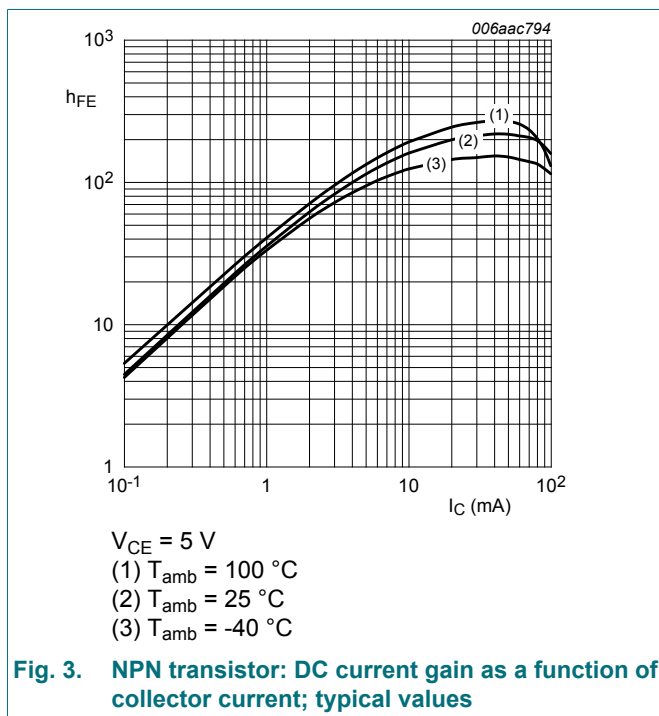
## 10. Characteristics

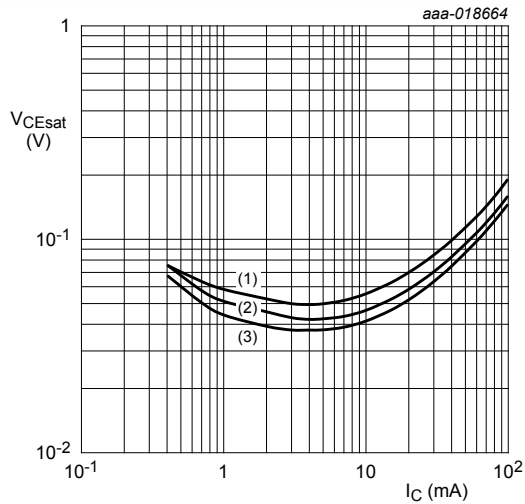
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	1	μA
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C		-	-	5	μA
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	180	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA; T <sub>amb</sub> = 25 °C		60	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA; T <sub>amb</sub> = 25 °C		-	-	150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA; T <sub>amb</sub> = 25 °C		-	1.1	0.8	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 5 mA; T <sub>amb</sub> = 25 °C		2.5	1.7	-	V
R1	bias resistor 1		[1]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C <sub>C</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz; T <sub>amb</sub> = 25 °C		-	-	2.5	pF
		V <sub>CB</sub> = -10 V; I <sub>E</sub> = 0 mA; i <sub>e</sub> = 0 mA; f = 1 MHz; T <sub>amb</sub> = 25 °C		-	-	3	pF
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 10 mA; f = 100 MHz; T <sub>amb</sub> = 25 °C	[2]	-	230	-	MHz
		V <sub>CE</sub> = -5 V; I <sub>C</sub> = -10 mA; f = 100 MHz; T <sub>amb</sub> = 25 °C		-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor





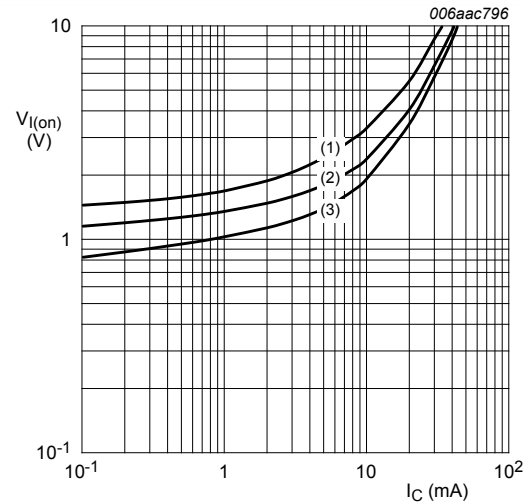
$$I_C/I_B = 20$$

(1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$

(3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig. 5. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values**



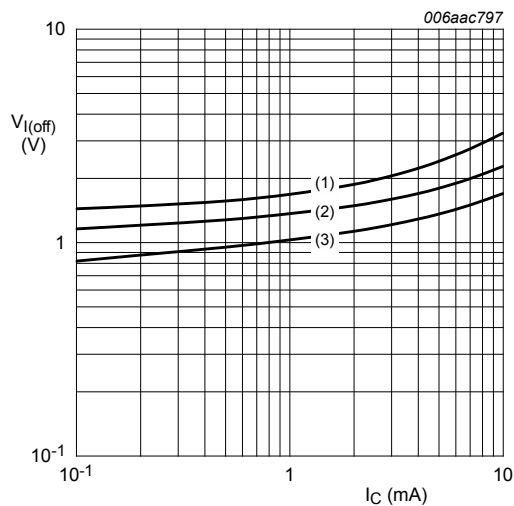
$$V_{CE} = 0.3\text{ V}$$

(1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$

(3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

**Fig. 6. NPN transistor: On-state input voltage as a function of collector current; typical values**



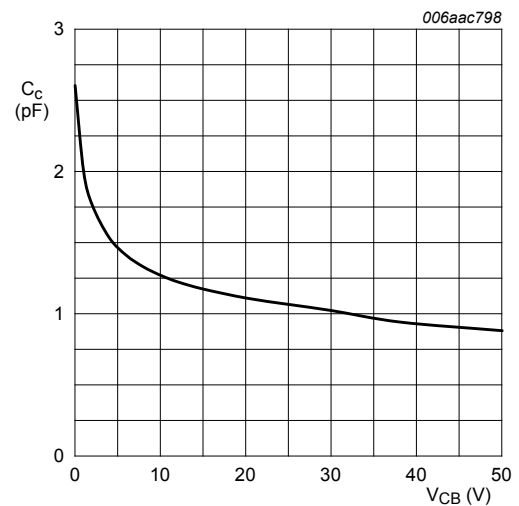
$$V_{CE} = 5\text{ V}$$

(1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$

(3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

**Fig. 7. NPN transistor: Off-state input voltage as a function of collector current; typical values**



$$f = 1\text{ MHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$$

**Fig. 8. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values**

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

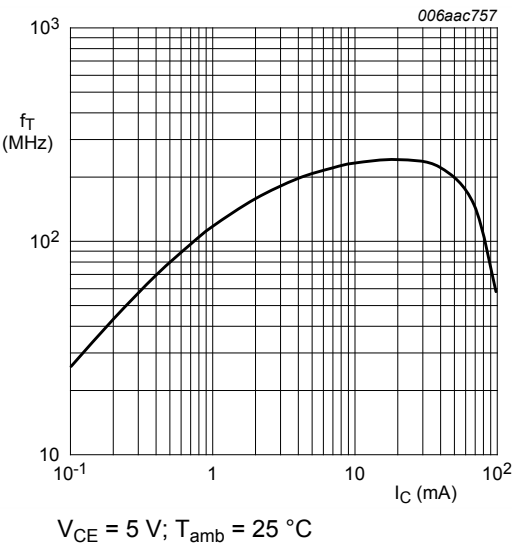


Fig. 9. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor

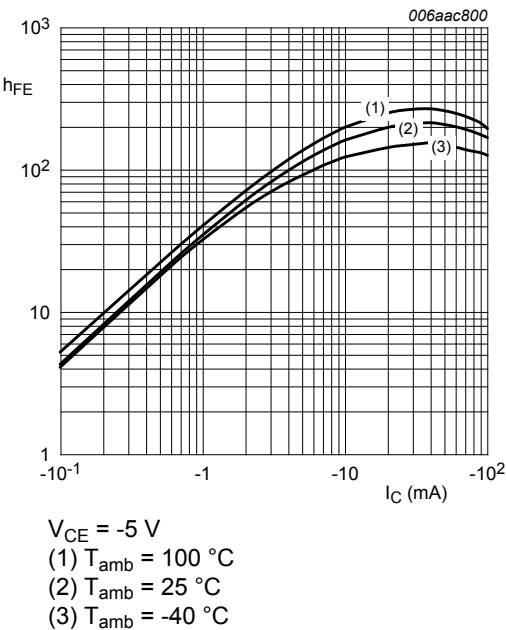


Fig. 10. PNP transistor: DC current gain as a function of collector current; typical values

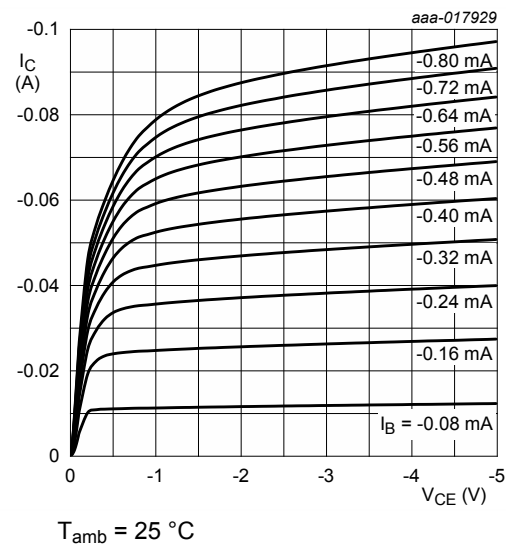


Fig. 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

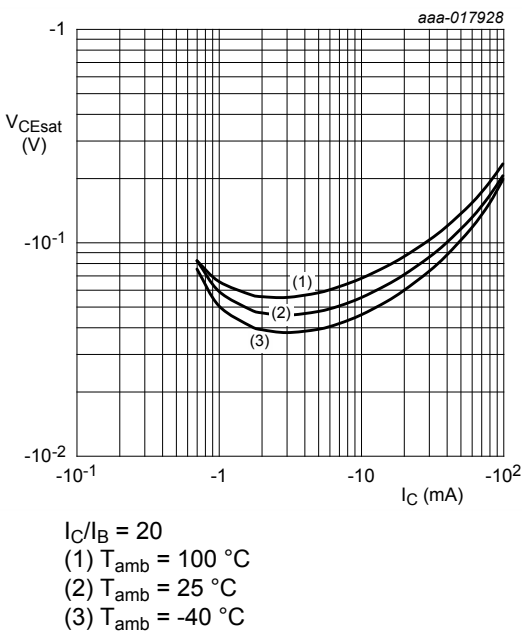


Fig. 12. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

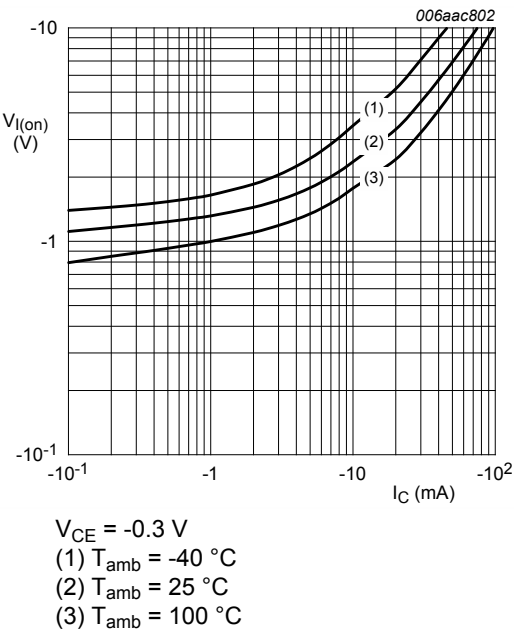


Fig. 13. PNP transistor: On-state input voltage as a function of collector current; typical values

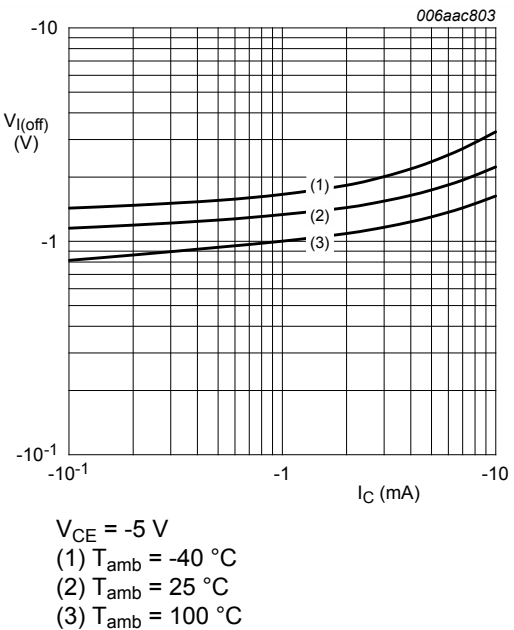


Fig. 14. PNP transistor: Off-state input voltage as a function of collector current; typical values

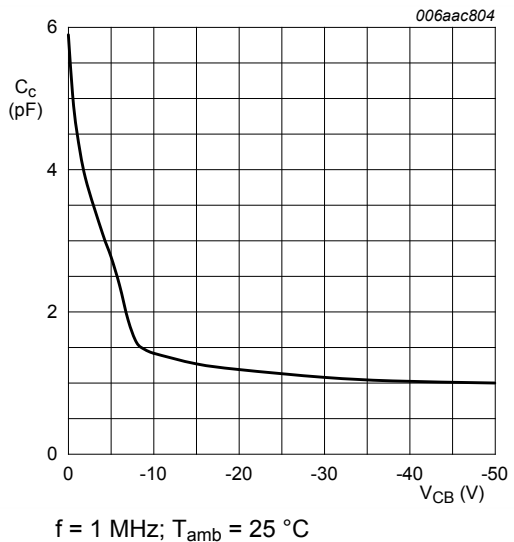


Fig. 15. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values

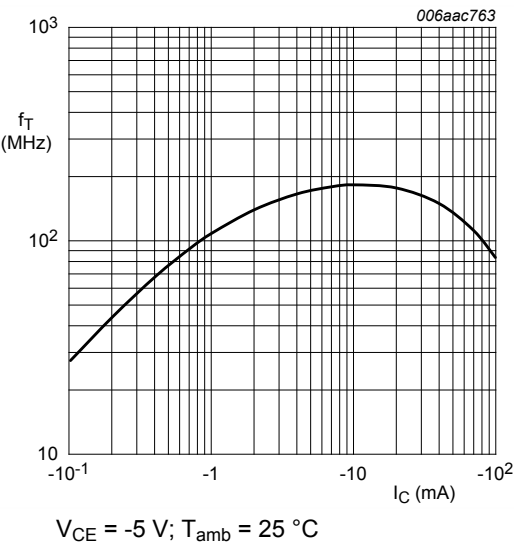


Fig. 16. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

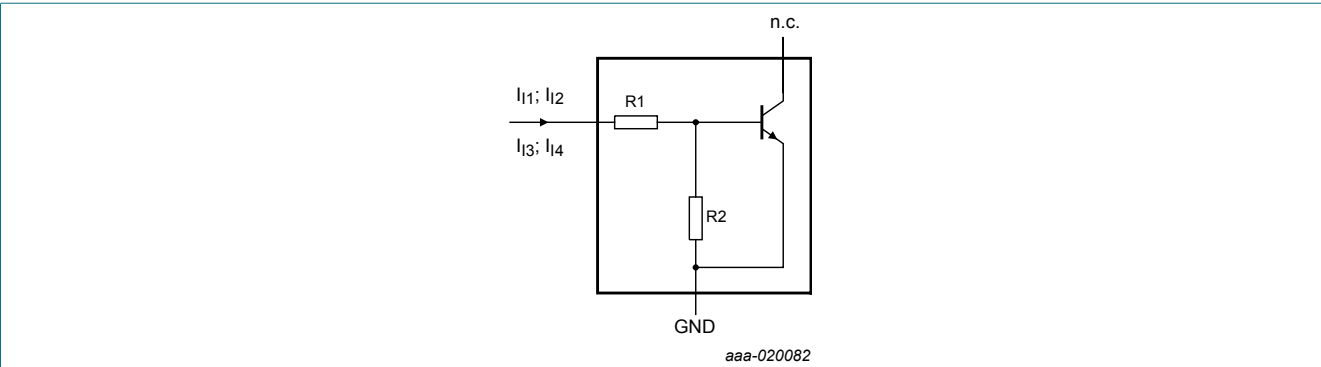


Fig. 17. NPN transistor: Resistor test circuit

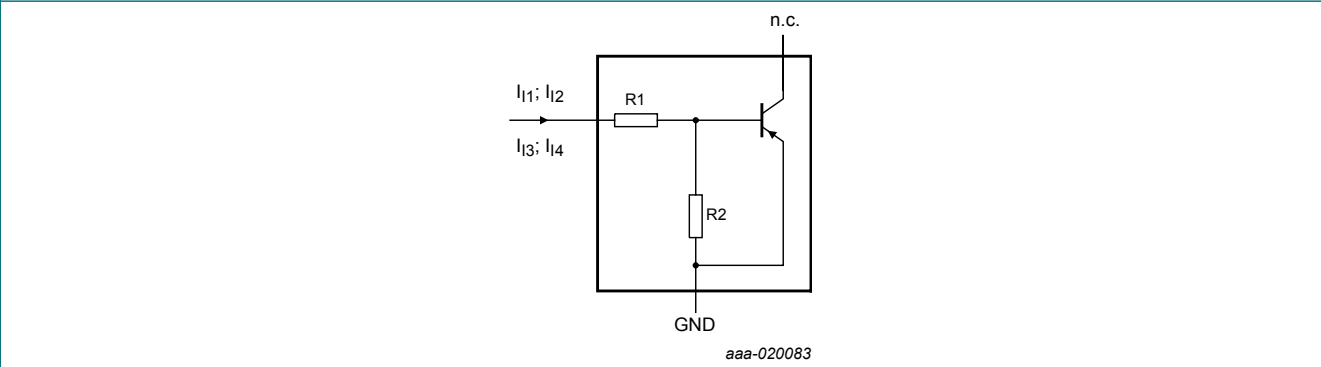


Fig. 18. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Per transistor; for the PNP transistor with negative polarity

R1 (kΩ)	R2 (kΩ)	Test conditions			
		I <sub>I1</sub>	I <sub>I2</sub>	I <sub>I3</sub>	I <sub>I4</sub>
22	22	150 μA	230 μA	-150 μA	-230 μA

12. Package outline

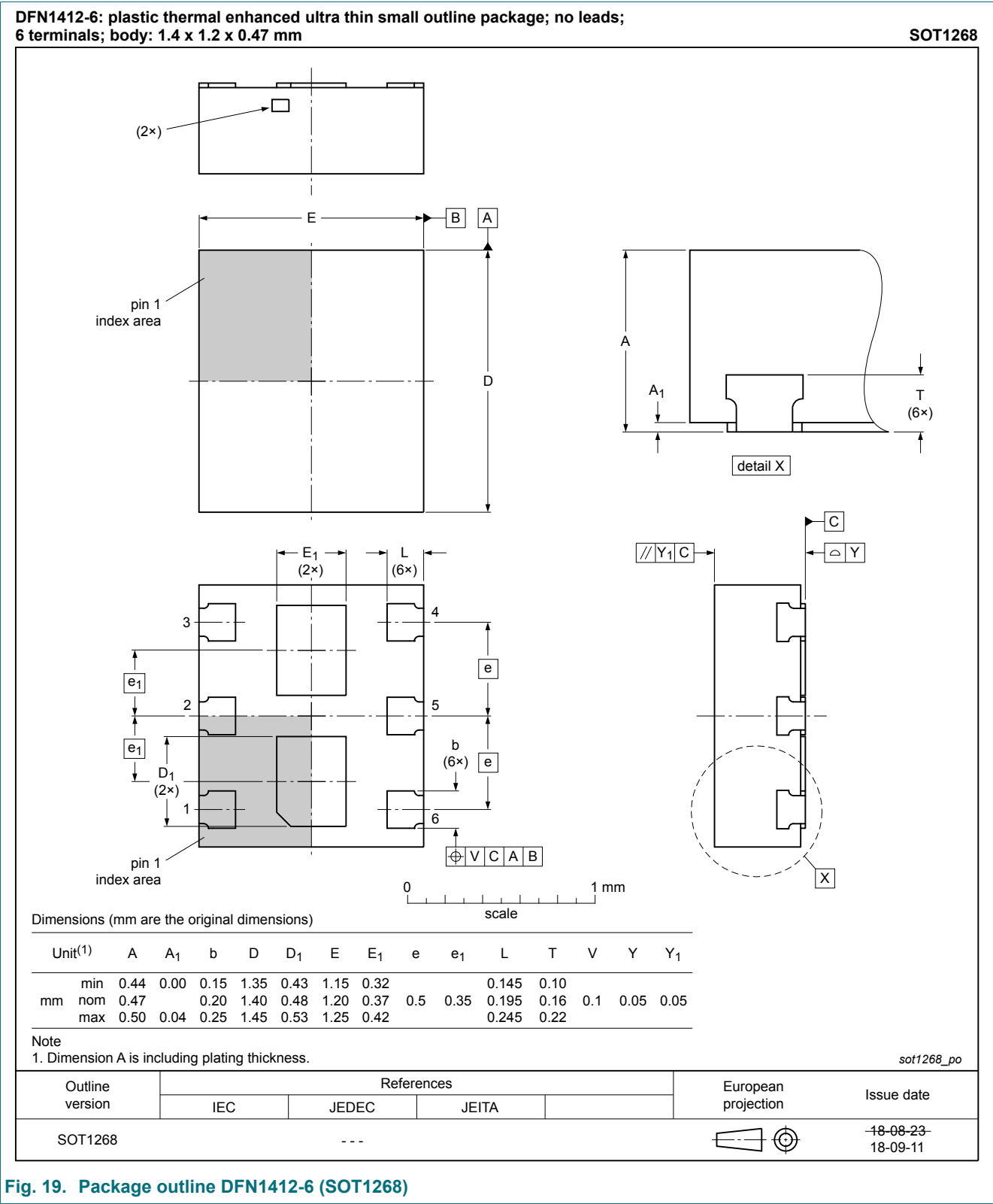


Fig. 19. Package outline DFN1412-6 (SOT1268)

13. Soldering

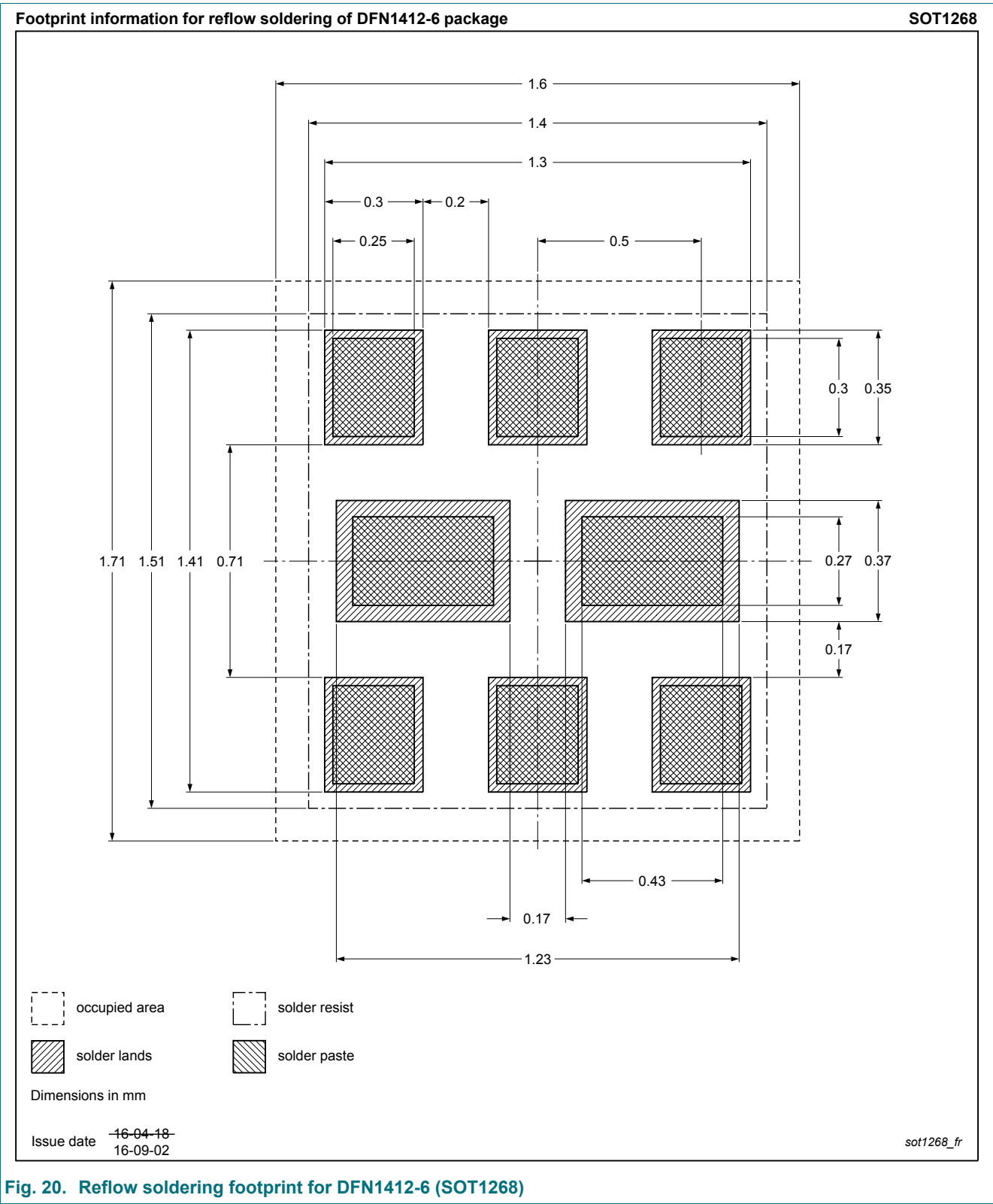


Fig. 20. Reflow soldering footprint for DFN1412-6 (SOT1268)

## 14. Revision history

**Table 9. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PRMD2 v.2	20180914	Product data sheet	-	PRMD2 v.1
Modifications:	<ul style="list-style-type: none"><li>Package outline drawing updated: Unit T added</li></ul>			
PRMD2 v.1	20170614	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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