Crystal Image through Imaging Innovation

PIXELPLUS

2 CH Multi-Standard Analog HD Video Receiver with MIPI Interface

PR2100K

Preliminary Datasheet

Rev 0.7

Last Update : Jun 30, 2020

6th Floor, 105, Gwanggyo-ro, Yeongtong-gu,
Suwong-si, Gyeonggi-do, 16229, Korea
Tel : 82-31-888-5300, FAX : 82-31-888-5398

Contents

Figures

Tables

1. General Description

1.1. Product Overview

The PR2100 is 2 channel HD/SD video receiver which accepts Any Standard and Resolution of Analog HD/SD video and guarantees high quality image for Long-Reach Analog HD applications. It accepts Single-ended/Differential analog HD/SD video signal from camera, then Cable Equalizer compensates cable attenuation, and HD/SD video decoder converts analog video signal to digital component data. The PR2100 supports both 8bit parallel interface with BT1120/BT656 standard and MIPI-CSI2 interface compliant with MIPI-DPHY v1.0 and MIPI-CSI2 v1.0. The PR2100 also provides Bi-Directional Coaxial/UTP PTZ interface so that host can control PTZ camera and receive information from camera with 2-wire serial interface.

1.2. Features

- **Video Decoder**
  - ✓ Multi-standard Analog HD and SD Video with Auto-Detection
    - *All Kind of Analog HD Standard and NTSC/PAL*
  - ✓ Any Resolution of Analog HD and SD Video with Auto-Detection
    - *1080p25/30, 720p25/30/50/60, 960p25/30/50/60 and 480i60, 576i50*
  - ✓ Superior Cable Equalizer for Long-Reach Analog HD Application
  - ✓ Differential Analog Input or Two Single-ended Analog Input with MUX Switch
  - ✓ BT1120/BT656 Parallel Output
    - Multi-Channel Time-Multiplexed Video Output with Dual Edge of Clock
  - ✓ MIPI-CSI2 2/4 Data Lane Configuration
    - 2 Data Lanes for 2 x 720p@25/30, 1 x 1080p@25/30
    - 4 Data Lanes for 4 x 720p@25/30, 2 x 1080p@25/30
    - Multi-Channel Video Output with Virtual CHID and H/V Combined Format
  - ✓ Cascaded Connection for 4ch HD Video Output
- **Bi-Directional PTZ Communication**
  - ✓ Flexible Protocol
- **Host Interface**
  - ✓ I2C Serial Interface
- **Low Power Consumption**
  - ✓ 690/452mW (3.3V/1.8V Parallel Output) / 416mW (MIPI Output) for FHD1080p
- **Package**
  - ✓ 48 eQFN (6mm x 6mm)

1.3. Block Diagram

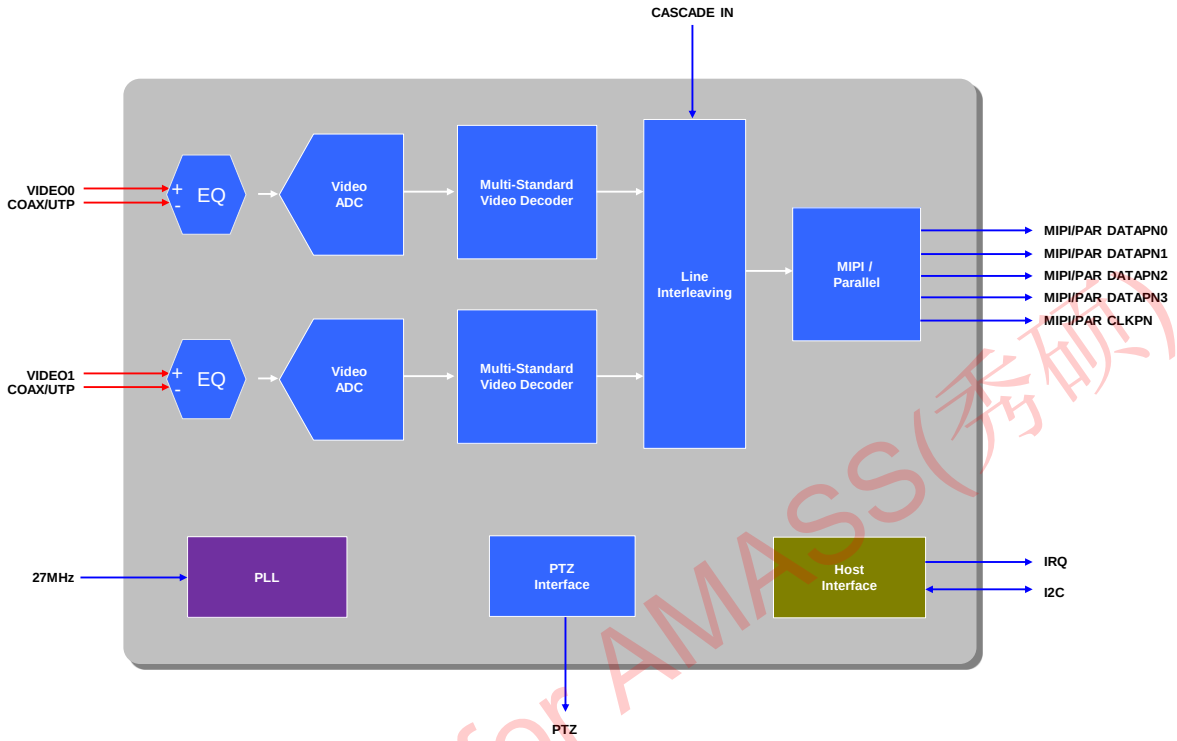


Fig 1. Functional Block Diagram

1.4. Pin Diagram

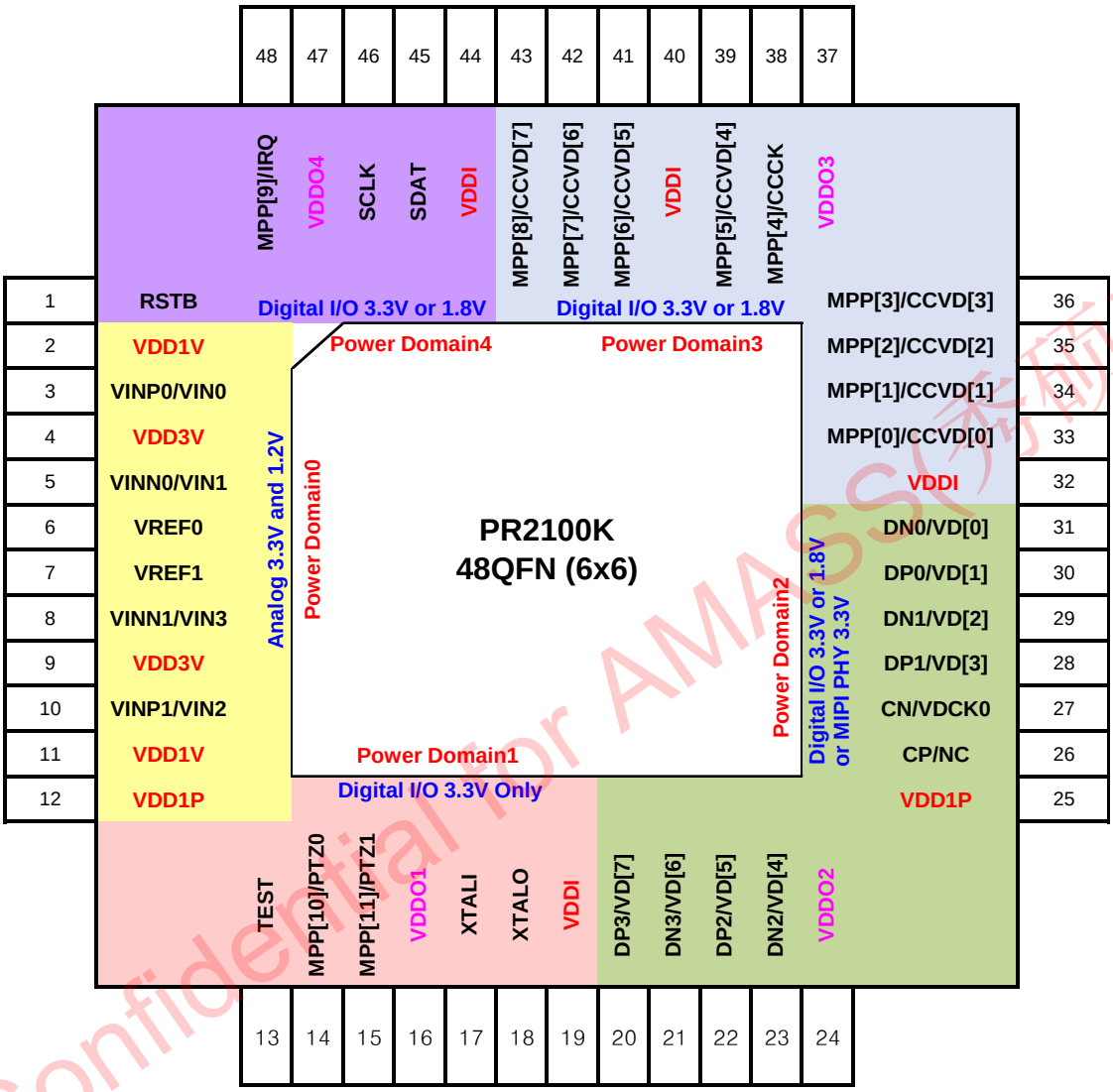


Fig 2. Pin Diagram

1.5. Pin Description

Pin Name	Pin Number	Type	Pin Description
Analog Video Interface (6 Pin)			
VINP0/VIN0	3	A	Analog Video Differential Positive Input or Single-ended VIN0
VINN0/VIN1	5	A	Analog Video Differential Negative Input or Single-ended VIN1
VINP1/VIN2	10	A	Analog Video Differential Positive Input or Single-ended VIN2
VINN1/VIN3	8	A	Analog Video Differential Negative Input or Single-ended VIN3
VREF0	6	A	Analog Voltage Reference Output0
VREF1	7	A	Analog Voltage Reference Output1
Digital Video Interface (10 Pin)			
CN/VDCK0	27	O	Clock 0 for Digital Video Output / MIPI Clock Negative Output
CP/NC	26	O	Not Connected / MIPI Clock Positive Output
DN0/VD[0]	31	O	Digital Video Output[0] / MIPI Data0 Negative Output
DP0/VD[1]	30	O	Digital Video Output[1] / MIPI Data0 Positive Output
DN1/VD[2]	29	O	Digital Video Output[2] / MIPI Data1 Negative Output
DP1/VD[3]	28	O	Digital Video Output[3] / MIPI Data1 Positive Output
DN2/VD[4]	23	O	Digital Video Output[4] / MIPI Data2 Negative Output
DP2/VD[5]	22	O	Digital Video Output[5] / MIPI Data2 Positive Output
DN3/VD[6]	21	O	Digital Video Output[6] / MIPI Data3 Negative Output
DP3/VD[7]	20	O	Digital Video Output[7] / MIPI Data3 Positive Output
Multi-Purpose Pin Interface (12 Pin)			
MPP[0]/CCVD[0]	33	I/O	Multi-purpose Pin inout [0] / Cascaded Connection Data Input[0]
MPP[1]/CCVD[1]	34	I/O	Multi-purpose Pin inout [1] / Cascaded Connection Data Input[1]
MPP[2]/CCVD[2]	35	I/O	Multi-purpose Pin inout [2] / Cascaded Connection Data Input[2]
MPP[3]/CCVD[3]	36	I/O	Multi-purpose Pin inout [3] / Cascaded Connection Data Input[3]
MPP[4]/CCCK	38	I/O	Multi-purpose Pin inout [4] / Cascaded Connection Clock Input
MPP[5]/CCVD[4]	39	I/O	Multi-purpose Pin inout [5] / Cascaded Connection Data Input[4]
MPP[6]/CCVD[5]	41	I/O	Multi-purpose Pin inout [6] / Cascaded Connection Data Input[5]
MPP[7]/CCVD[6]	42	I/O	Multi-purpose Pin inout [7] / Cascaded Connection Data Input[6]
MPP[8]/CCVD[7]	43	I/O	Multi-purpose Pin inout [8] / Cascaded Connection Data Input[7]
MPP[9]/IRQ	48	I/O	Multi-purpose Pin inout [9] / IRQ
MPP[10]/PTZ0	14	I/O	Multi-purpose Pin inout [10] / PTZ0
MPP[11]/PTZ1	15	I/O	Multi-purpose Pin inout [11] / PTZ1
System Control Interface (6 Pin)			
TEST	13	I	Reserved Pin for TEST
RSTB	1	I	System Reset
XTALI	17	I	Crystal (27MHz) Input
XTALO	18	I/O	Crystal (27MHz) Input / Output
SCLK	46	I	I2C Clock Line
SDAT	45	I/O	I2C Data Line
Power and Ground (15 Pin)			
VDD3V	4, 9	P	3.3V Power for Analog Video
VDD1V	2, 11	P	1.25V Power for Analog Video
VDD1P	12, 25	P	1.25V Power for PLL
VDDI	19, 32, 40, 44	P	1.25V Power for Digital Core
VDDO1	16	P	Digital IO Power Domain1 (3.3V Only)
VDDO2	24	P	Digital IO Power Domain2 (3.3V or 1.8V) / MIPI Tx PHY Power Domain2 (3.3V Only)
VDDO3	37	P	Digital IO Power Domain3 (3.3V or 1.8V)
VDDO4	47	P	Digital IO Power Domain4 (3.3V or 1.8V)
VSS	Exposed Pad	G	Ground

1.6. Application Diagram

1.6.1. Parallel Output

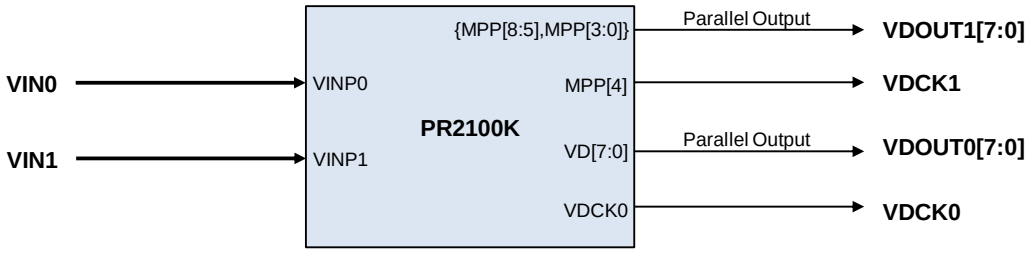


Fig 3. Parallel Output with SDR Mode

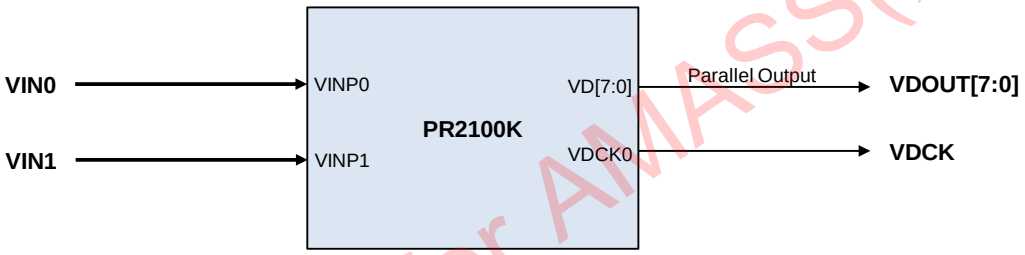


Fig 4. Parallel Output with DDR Mode

1.6.2. MIPI Output

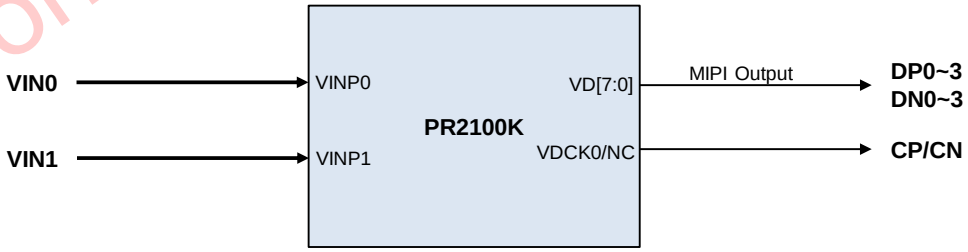


Fig 5. MIPI Output

1.6.3. Both Parallel and MIPI Output

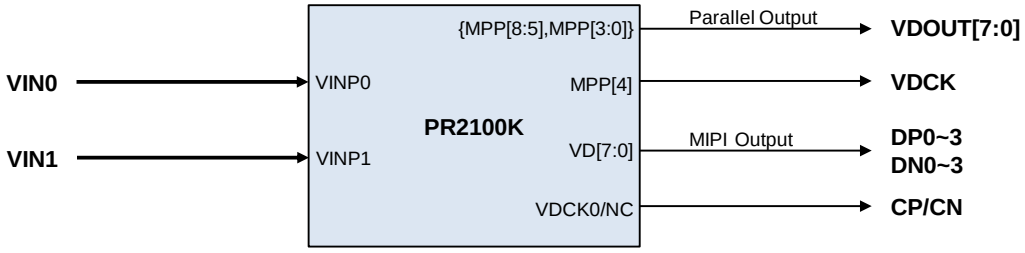


Fig 6. Both Parallel and MIPI Output

1.6.4. Cascaded Operation

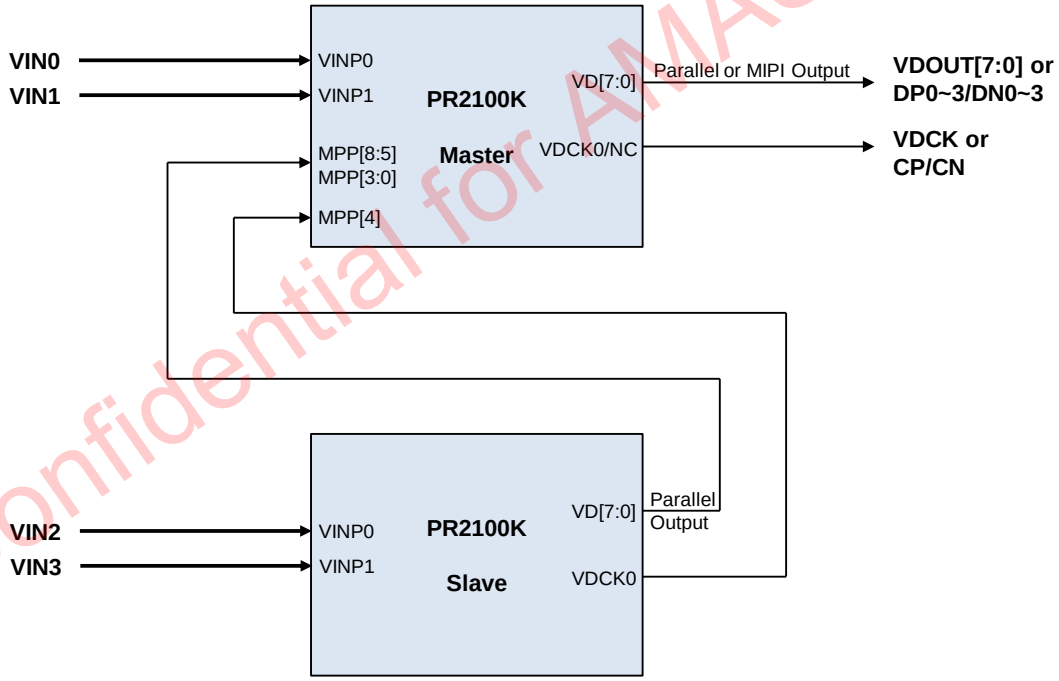


Fig 7. Cascaded Operation Application Diagram

2. Functional Description

2.1. Video Input

2.1.1. Cable Equalizer

The PR2100 includes an adaptive cable equalizer that automatically recovers loss resulted from the long transmission of analog HD/SD video signal over Coaxial (3C-2V/RG-59/RG6) or UTP (Unshielded Twisted-Pair, CAT-5/6) cables as shown in Fig 8. The recommended video input application circuits for Coaxial cable and CAT-5/6 are illustrated in the Fig 9 and Fig 10.

Fig 8. Cable EQ Performance Illustration

Table 1. Transmission Distance for RG6 Coaxial Cable

Cable Type	720p@25/30Hz	720p@50/60Hz	1080p@25/30Hz
RG6 Coaxial	1200m	1000m	1000m

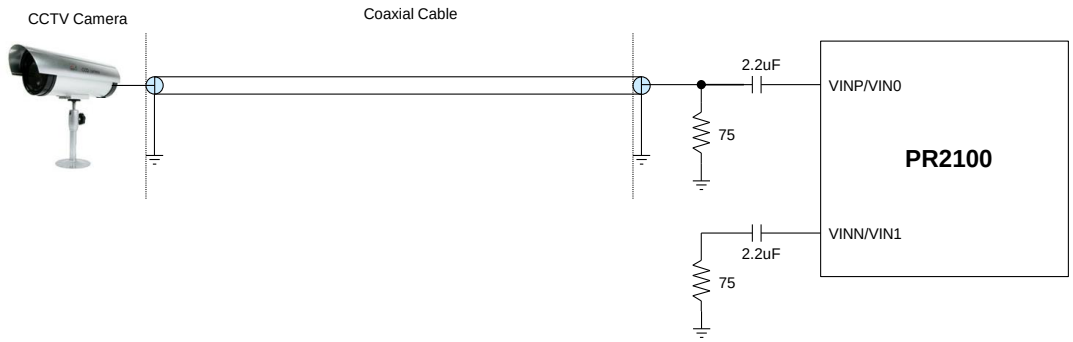


Fig 9. The Recommended Application Circuit for Coaxial Cable

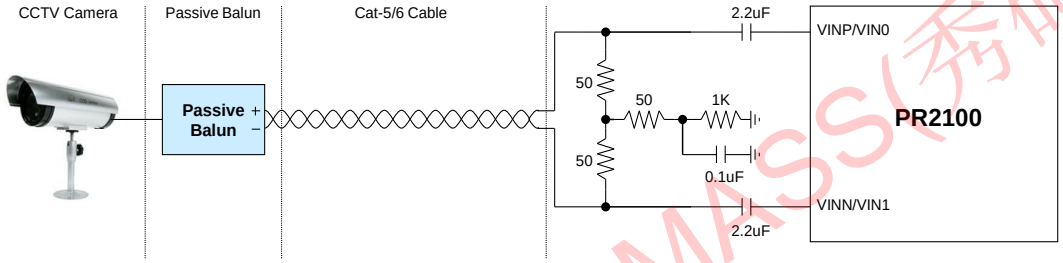


Fig 10. The Recommended Application Circuit for CAT-5/6 Cable

2.1.2. Analog Front End

The analog front end comprises the cable EQ, anti-aliasing filter and ADC to digitize the analog video signal. The analog front end can accept differential video input to improve the noise immunity or two single-ended video inputs with embedded analog MUX switch. The anti-aliasing filters are integrated to provide out-of band noise rejection on the analog video input signal.

2.1.3. Video Decoder

The PR2100 supports all existing HD/SD video standard and all video format (1080p@25/30, 720p@25/30/50/60, 960p@25/30/50/60 and 480i@60/576i@50) with automatic standard and format detection. The adaptive comb filter or band selected filter automatically adjusts its processing mode according to video standard and format with no user intervention required. The PR2100 contains a luminance peaking filter and a chrominance transient improvement (CTI) processor which increase the edge rate on video signal transitions, resulting in a sharper video image. The PR2100 also provides the video control registers such as brightness, contrast, saturation, and hue for the picture adjustment.

2.1.4. Bi-directional Coaxial/UTP PTZ

The PR2100 supports any bidirectional Coaxial/UTP PTZ protocol that transmits the data between a controller and the PTZ (Pan/Tilt/Zoom) camera. The PR2100 can define the H/V location and line width for PTZ protocol with the register PTZ_RX/TX_HST (3x02/22, 4x02/22), PTZ_TX_HPST (3x29/2A, 4x29/2A) and PTZ_RX/TX_LINE_LEN (3x0B/2B, 4x0B/2B). The bit-stream can be comprised of several lines and one line data can be defined via the PTZ_FIFO_WR_DATA (3x11, 4x11) register. Each bit width can be controlled by the PTZ_RX/TX_FREQ (3x03~08, 3x23~28, 4x03~08, 4x23~28) register. The PTZ_RX/TX data transfer can be programmed easily with IRQ interface in PR2100. After one channel PTZ TX data is programmed and the transfer is done, the PR2100 sends the IRQ data to host, then the host will program the other channel. Likewise, if all predefined quantity of PTZ Rx data is filled in the embedded FIFO, the IRQ data is sent to host, then the host will read the PTZ Rx data from it.

2.2. Video Output

The PR2100 supports ITU-R BT.656/1302/1120 format according to the input video format. In case that all video input formats are SD 720H, the video output format can be ITU-R BT.656. But if at least one of SD video input formats is 960H format, the video output format should be ITU-R BT.1302. Likewise, if at least one of video input formats is HD720p or HD1080p, the video output format should be ITU-R BT1120 because four channel output clocks should be synchronous. In other words, all video data of four channels are synchronous with output clock so that two or four channels can be multiplexed and only one clock can be used for it. Each clock can be controlled by 8 phase via the VDCK_DEL (0xE8/E9) register. The PR2100 also supports DDR (Dual Data Rate) format so that the maximum data rate can be raised up to 297MHz.

2.2.1. Output Format

2.2.2.1. One Channel Standard ITU-R BT.656/1302/1120 Format

The video output data is ITU-R BT.656/1302/1120 standard format with 27/36/74.25/148.5MHz. The Fig 11 and Fig 12 show the timing diagram of one channel standard ITU-R BT.656/1302/1120 format.

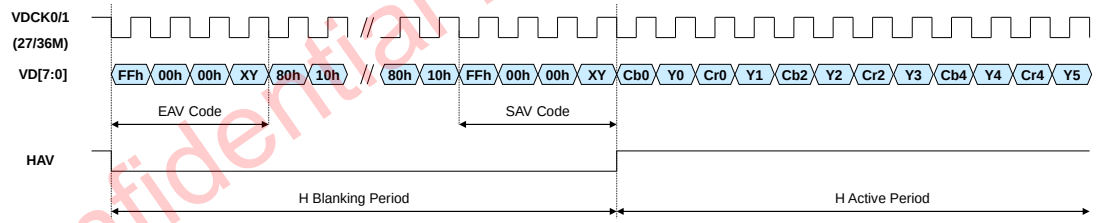


Fig 11. The Timing Diagram of One Channel Standard ITU-R BT.656/1302 Format

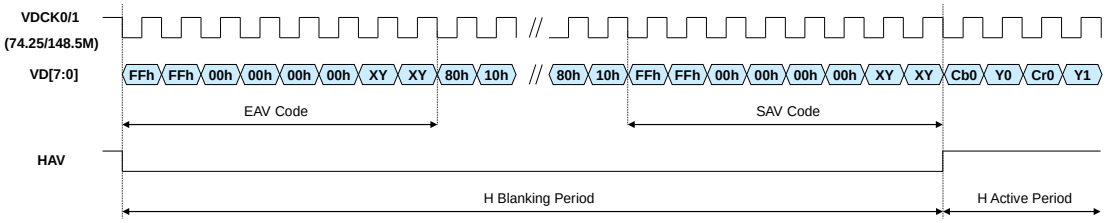


Fig 12. The Timing Diagram of One Channel Standard ITU-R BT.1120 Format

2.2.2.2. Two Channel Multiplexed ITU-R BT.656/1302/1120 Format

In two channel multiplexed format, the video output data from two video channels is multiplexed at 54/72/74.25/148.5/297MHz. The video output data is triggered at clock rising or falling edge for SDR (Single Data Rate) mode, but it is triggered at both clock rising and falling edge for DDR (Dual Data Rate) mode. The video output of each channel is compatible with ITU-R BT.656/1302/1120 format. The Fig 13 and Fig 14 show the timing diagram of two channel multiplexed format for SDR and DDR mode.

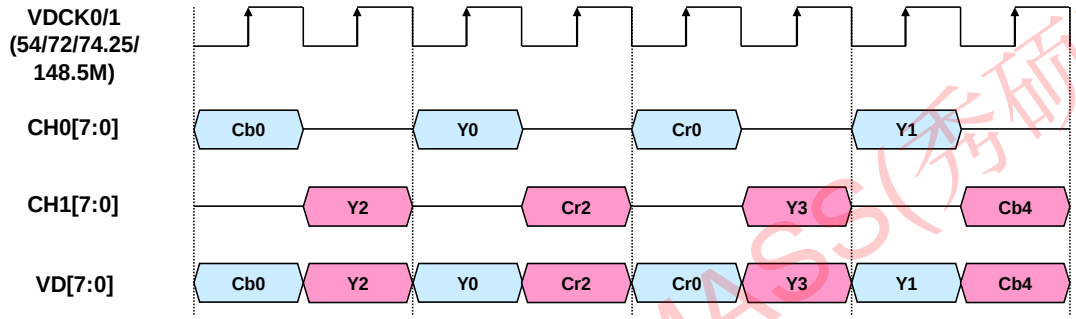


Fig 13. The Timing Diagram of Two Channel Multiplexed Format for SDR Mode

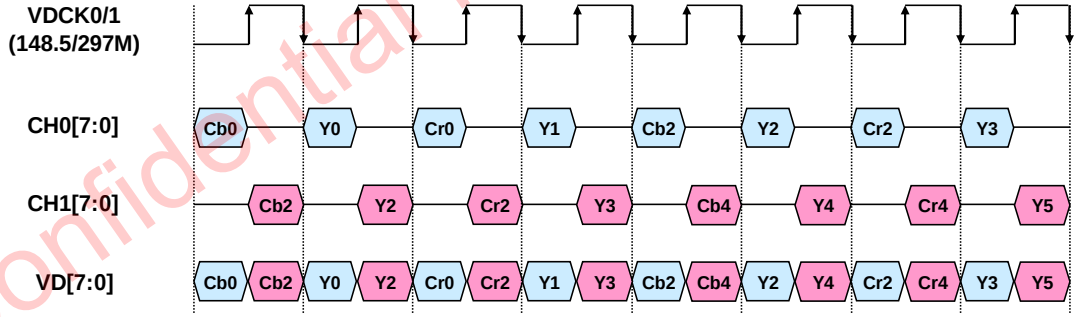


Fig 14. The Timing Diagram of Two Channel Multiplexed Format for DDR Mode

2.2.2.3. Four Channel Multiplexed ITU-R BT.656/1302/1120 Format

In four channel multiplexed format, the video output data from four video channels is multiplexed at 108/144/148.5/297MHz. The video output data is triggered at clock rising or falling edge for SDR (Single Data Rate) mode, but it is triggered at both clock rising and falling edge for DDR (Dual Data Rate) mode. The video output of each channel is compatible with ITU-R BT.656/1302/1120 format. The Fig 15 and Fig 16 show the timing diagram of four channel multiplexed format for SDR and DDR mode.

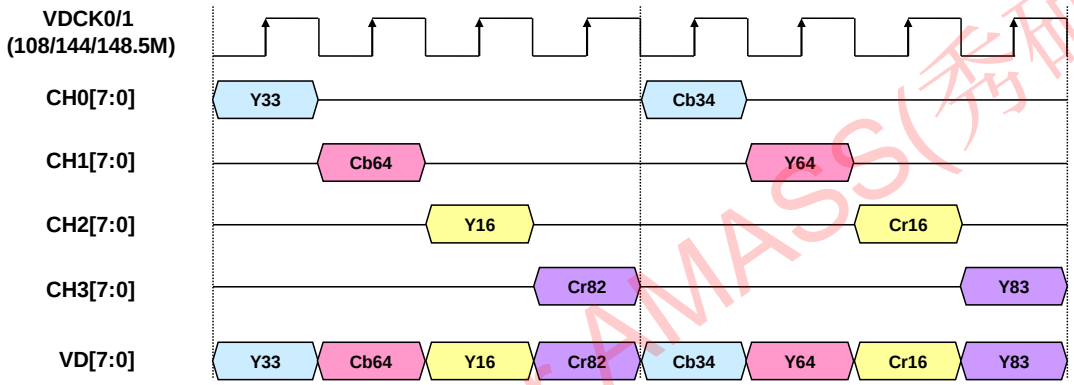


Fig 15. The Timing Diagram of Four Channel Multiplexed Format for SDR Mode

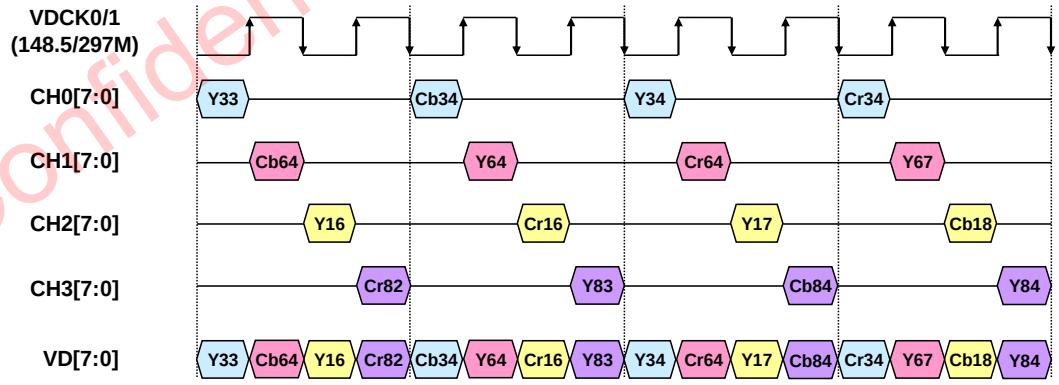


Fig 16. The Timing Diagram of Four Channel Multiplexed Format for DDR Mode

2.2.2. Channel ID Format

2.2.2.1. Channel ID Insertion in SAV/EAV Code

In the multi-channel multiplexed mode for cascaded application, the channel ID can be inserted in 4 LSB of SAV/EAV code in ITU-R BT.656/1120 format as shown in the Table 2 and Table 3.

Table 2. Channel ID Insertion in SAV/EAV Code for Four Channel in ITU-R BT.656 Format

Condition			FVH Value			SAV/EAV Code Sequence for Four CH Format						
Field	V time	H time	F	V	H	1st	2nd	3rd	4th			
									CH1	CH2	CH3	CH4
Even	Blank	EAV	1	1	1	FFh	00h	00h	F0h	F1h	F2h	F3h
		SAV			0				E0h	E1h	E2h	E3h
	Active	EAV		0	1				D0h	D1h	D2h	D3h
		SAV			0				C0h	C1h	C2h	C3h
Odd	Blank	EAV	0	1	1				B0h	B1h	B2h	B3h
		SAV			0				A0h	A1h	A2h	A3h
	Active	EAV		0	1				90h	91h	92h	93h
		SAV			0				80h	81h	82h	83h

Table 3. Channel ID Insertion in SAV/EAV Code for Four Channel in ITU-R BT.1120 Format

Condition		VH Value		SAV/EAV Code Sequence for Four CH Format						
V time	H time	V	H	1st 2nd	3rd 4th	5th 6th	7th/8th			
							CH1	CH2	CH3	CH4
Blank	EAV	1	1	FFh	00h	00h	B0h	B1h	B2h	B3h
	SAV		0				A0h	A1h	A2h	A3h
Active	EAV	0	1				90h	91h	92h	93h
	SAV		0				80h	81h	82h	83h

2.2.3. MIPI Output Format

The PR2100 supports a MIPI interface compliant with MIPI CSI2 V1.00 standard and DPHY V1.00.00 standard with 1 clock lane and 4 data lane. The max data rate of MIPI data lane is up to 594Mbps in HS transmission with YUV 422-8bit format. The four data lane should be used for 4ch 1280x720@25/30Hz or 2ch 1920x1080@25/30Hz format and two data lane can be used for 2ch 1280x720@25/30Hz or 1ch 1920x1080@25/30Hz format.

During MIPI Tx operation, there are two lane states such as Low Power (LP) state and High Speed (HS) state. The HS Tx always drives the lane differentially so that it results in two possible HS lane states such as differential-0 and differential-1. The LP Tx drives two lines of a lane independently with single-ended termination so that it results in four possible LP lane states that are used for Control Mode and Escape Mode. The HS data transmission is used to transfer data in burst mode. It starts from and ends with a stop state (LP-11) of LP Control Mode. The special Escape Mode can only be entered via a request within Control Mode. The data lane shall always exit Escape Mode and return to Control Mode with stop state. If not in HS state or Escape Mode, the data lane shall stay in Control mode.

Table 4. Lane State Description of MIPI Transmission

State Code	Line Voltage Levels		High-Speed	Low-Power	
	DP-Line	DN-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

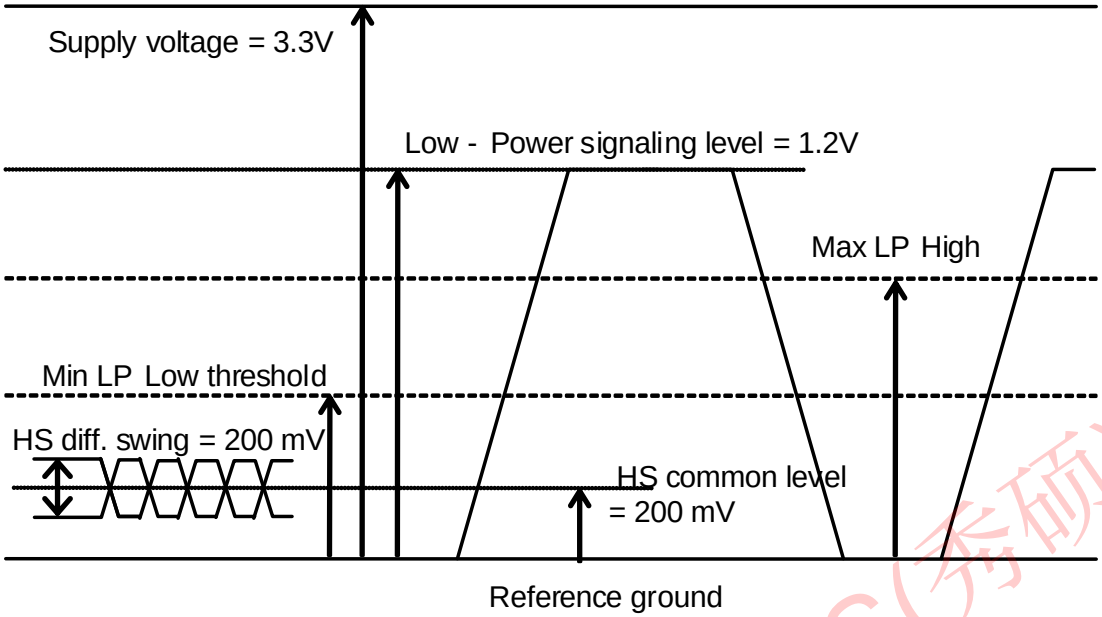


Fig 17. MIPI Signal Levels for HS and LP State

The Low Level Protocol (LLP) is a byte oriented, packet based protocol that supports the transport of image data using Short and Long packet formats. After exiting from the low power state, the Start of Transmission (ST) sequence indicates the start of the packet and the End of Transmission (ET) sequence indicates the end of the packet.

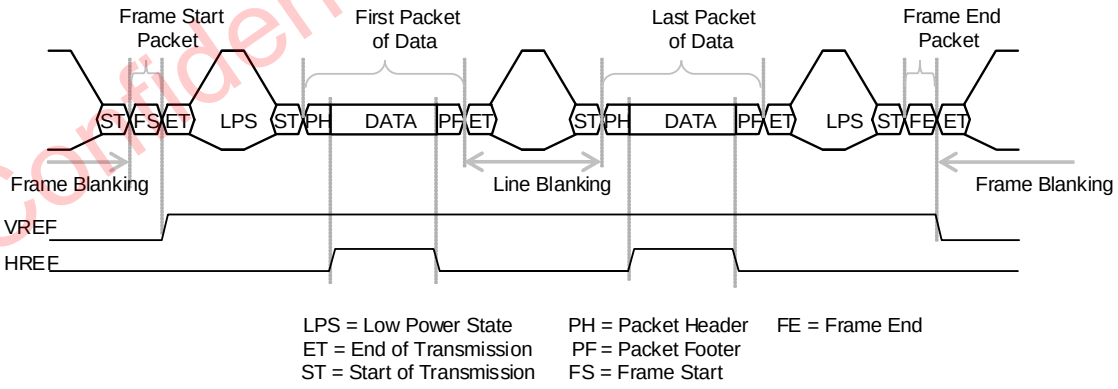


Fig 18. MIPI Low Power Protocol

The PR2100 supports two kinds of Short packet format for frame synchronization such as Frame Start (FS) packet and Frame End (FE) packet. Each image frame shall begin with a FS packet containing the Frame Start Code. The FS Packet shall be followed by one or more long packets containing image data. Each image frame shall end with the FE packet containing the Frame End Code.

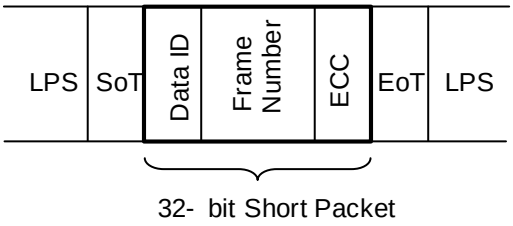


Fig 19. MIPI Short Packet Structure

A Long packet shall consist of 3 elements such as a 32-bit Packet Header (PH), an application Data Payload with a variable number of 8-bit words and a 16-bit Packet Footer (PF).

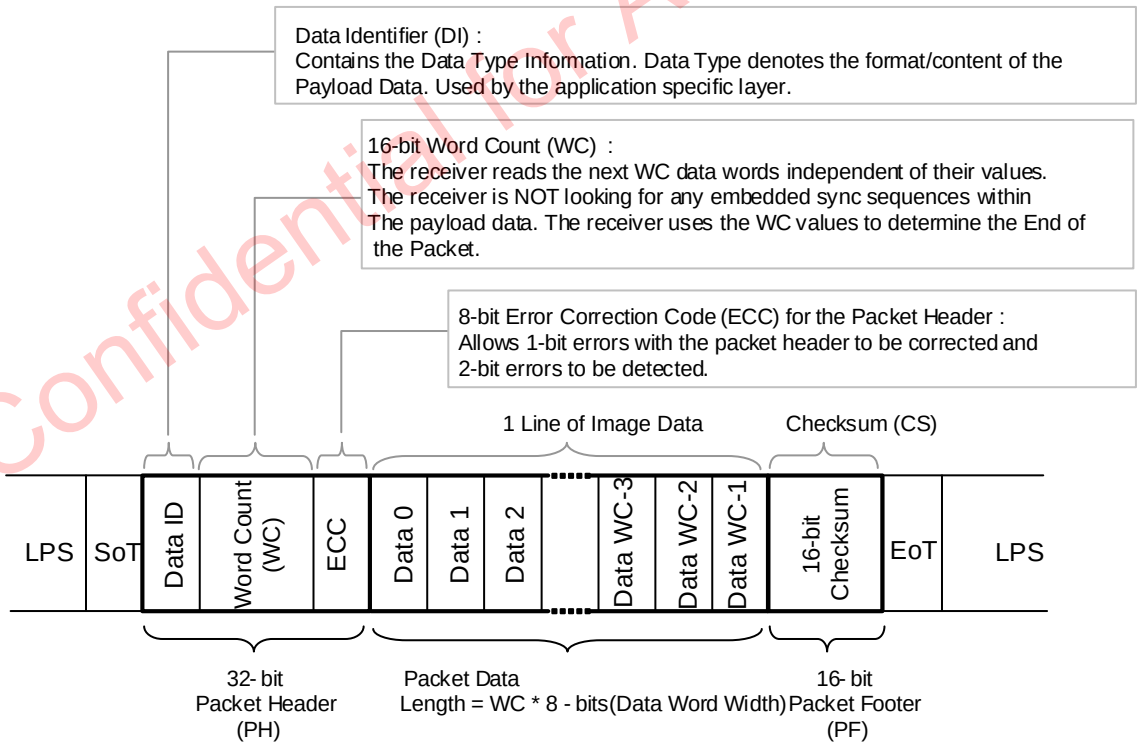


Fig 20. MIPI Long Packet Structure

The Fig 21 shows the detailed Data Payload structure of YUV422 8bit frame format in the Long packet.

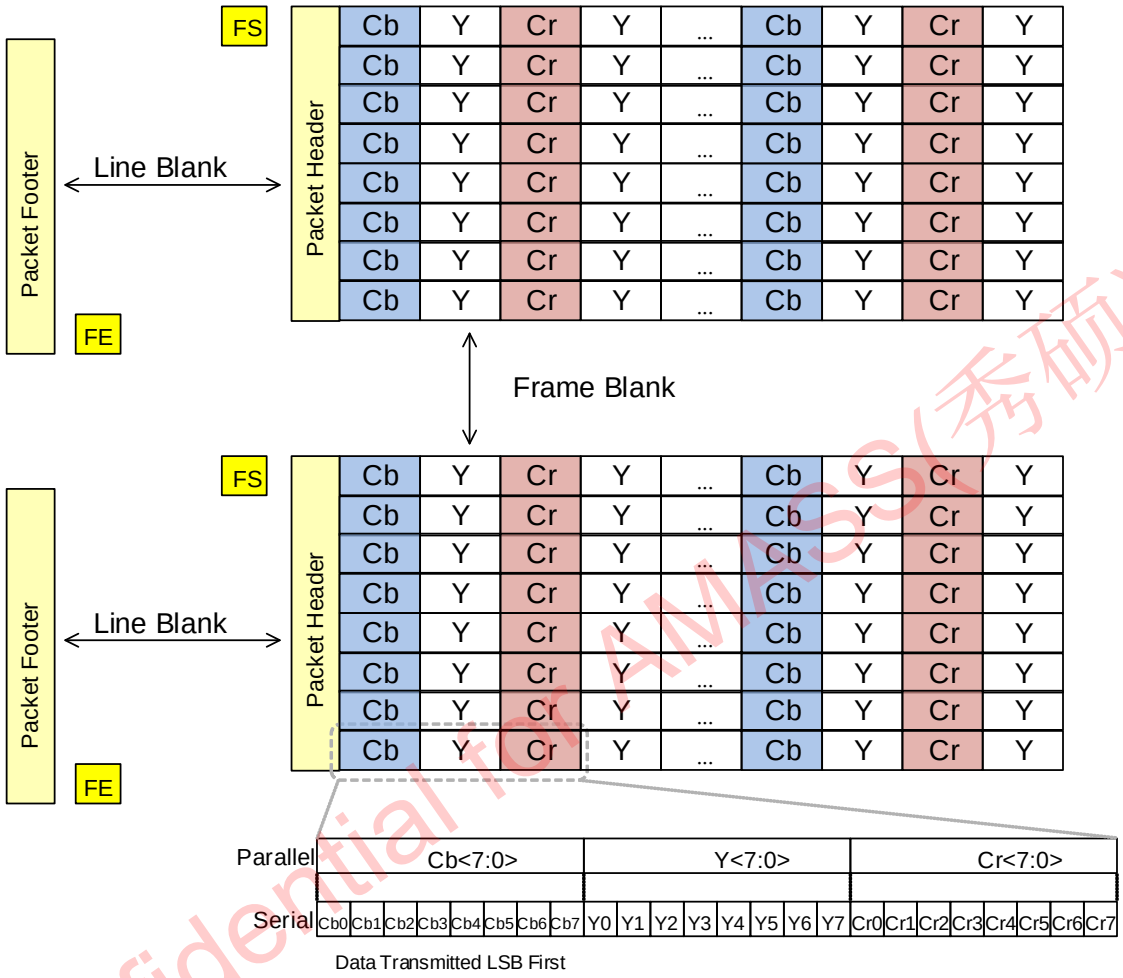


Fig 21. YUV422 8 Bit Frame Format for MIPI Transfer

The Fig 22 and Fig 23 describe the MIPI data lane transmission order for 4 lane and 2 lane mode.

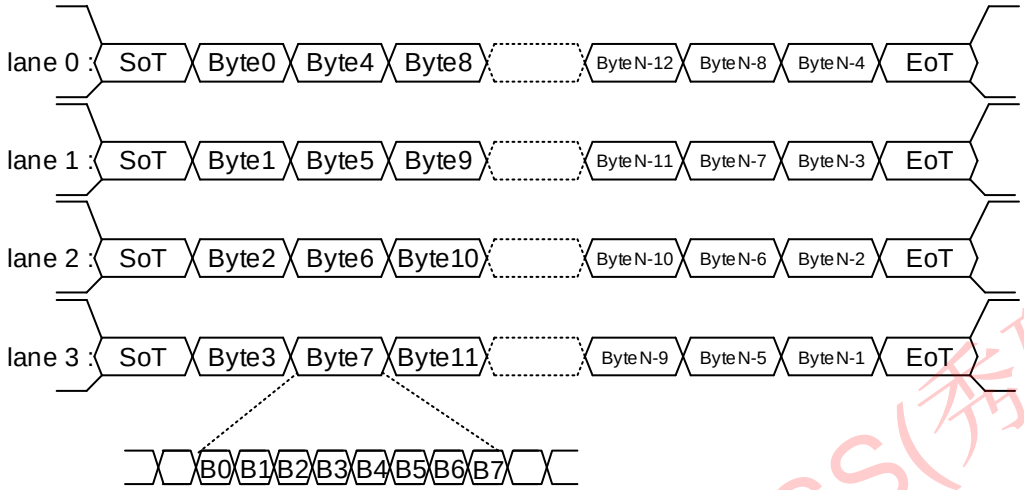


Fig 22. MIPI Data Lane Transmission Order for 4 Lane Mode

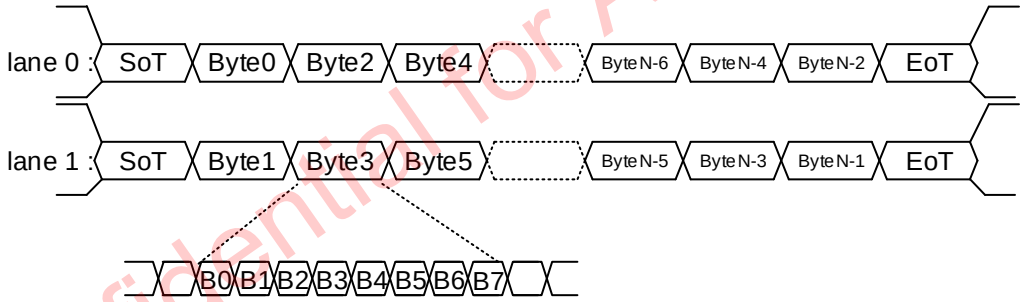


Fig 23. MIPI Data Lane Transmission Order for 2 Lane Mode

PR2100 supports a Virtual Channel Identifier in MIPI CSI-2 V1.00 standard for multi-channel data transfer mode. Four channel data can be line-interleaved with virtual channel ID inserted in each packet header. In this mode, four different frame syncs are inserted in each short packet. The following Fig 24 and Fig 25 describe the multi-channel data transfer mode with virtual channel ID.

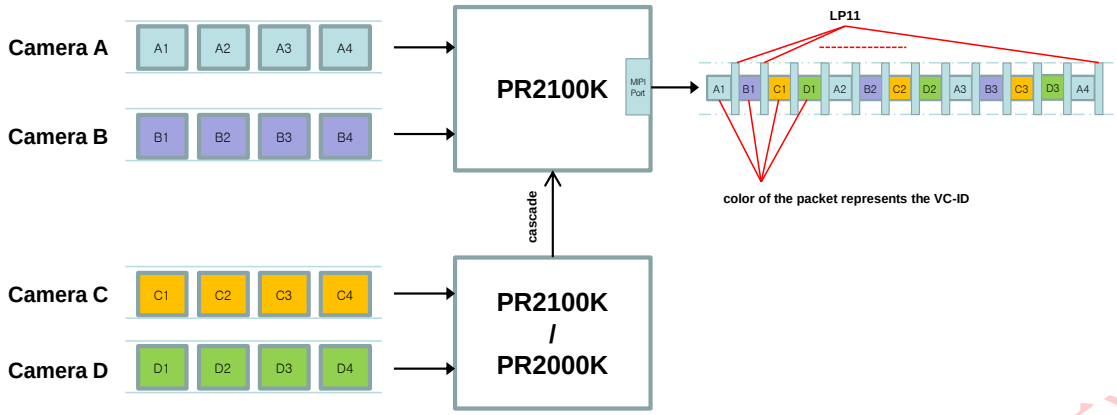


Fig 24. Four Camera Data onto CSI-2 with Virtual Channel ID

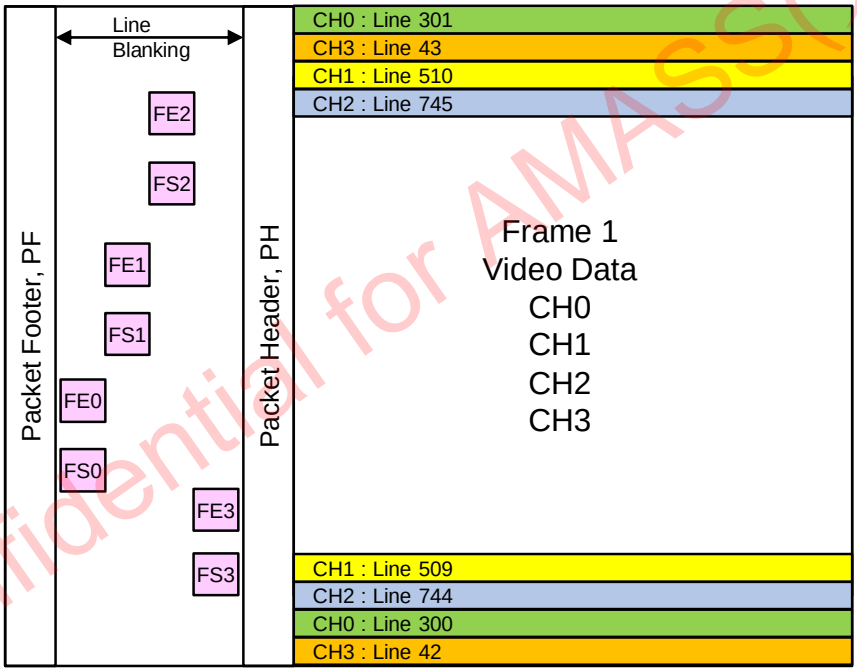


Fig 25. Frame Format of Virtual Channel ID with Each Different Frame Syncs

PR2100 also supports V or H Combined format for multi-channel data transfer mode in MIPI interface. The V or H Combined format is useful when the receiving processor does not support multiple Virtual Channel ID. The V Combined format effectively merges the frames from 4 video sources into a single frame that has 4 times the number of video lines. The receiving processor of V Combined format should separate the image based on order of video line reception. The H Combined format merges the video lines from four camera into a single line. The receiving

processor of H Combined format should separate the single video line into individual channel video components based on position within the combined video line. To differentiate each channel sync from the reference frame sync in V or H Combined format, the channel ID is inserted in the first packet data as described in Table 5. The following Fig 26 and Fig 27 illustrate the multi-channel data transfer mode with V or H Combined format.

Table 5. Channel ID Elements for V or H Combined Format

Name	Bit	Description
CH_NUM	[31:30]	Channel Number
CH_INFO	[29:28]	Channel Information Defined by User
CH_VACT	[27]	Vertical Active (High Active)
FREE_LINE_NUM	[26:16]	Free Running Line Number regardless of Scaling Ratio
CH_VALID	[15]	Channel Valid
FRAME_NUM	[14:12]	Frame Counter
LINE_VALID	[11]	Line Valid
VALID_LINE_NUM	[10:0]	Valid Line Number According to Scaling Ratio

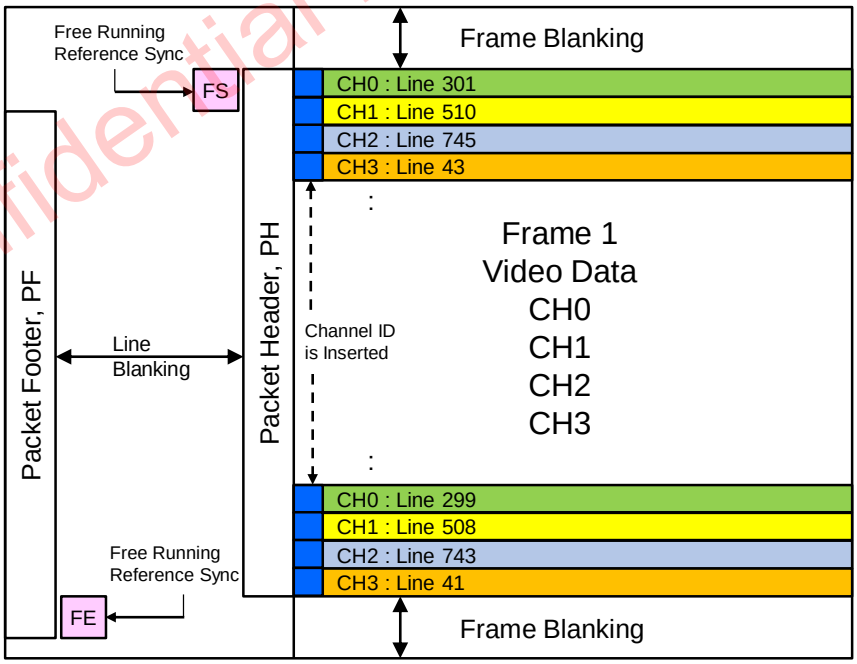


Fig 26. Frame Structure of V Combined Format with One Reference Frame Sync

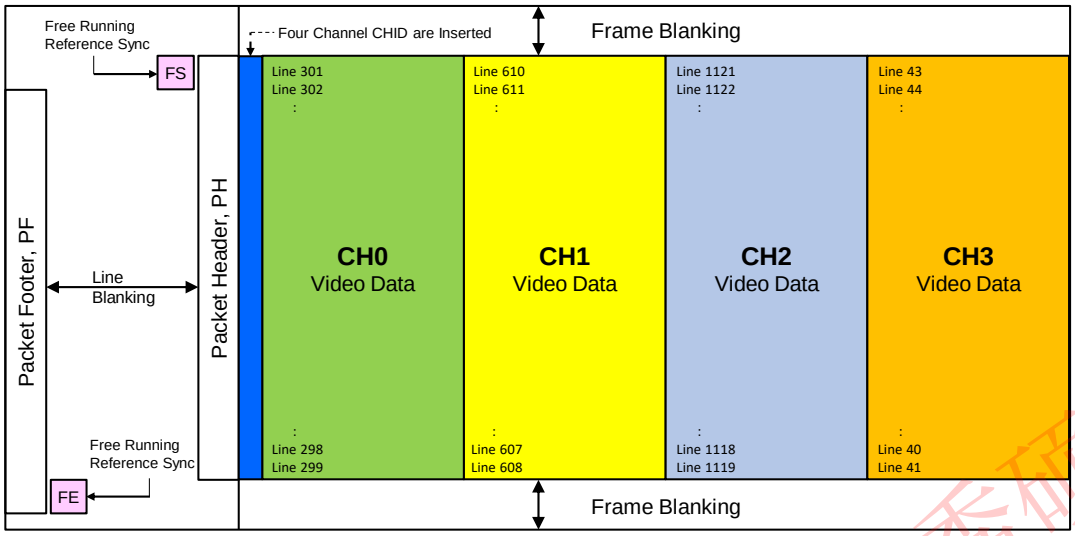


Fig 27. Frame Structure of H Combined Format with One Reference Frame Sync

2.2.4. Chip Cascade

The PR2100 provides a multi-chip cascaded operation supporting channel multiplexed output mode to reduce the interface pin count in both parallel output mode and MIPI output mode. The multi-chip cascaded connection is illustrated in Fig 28.

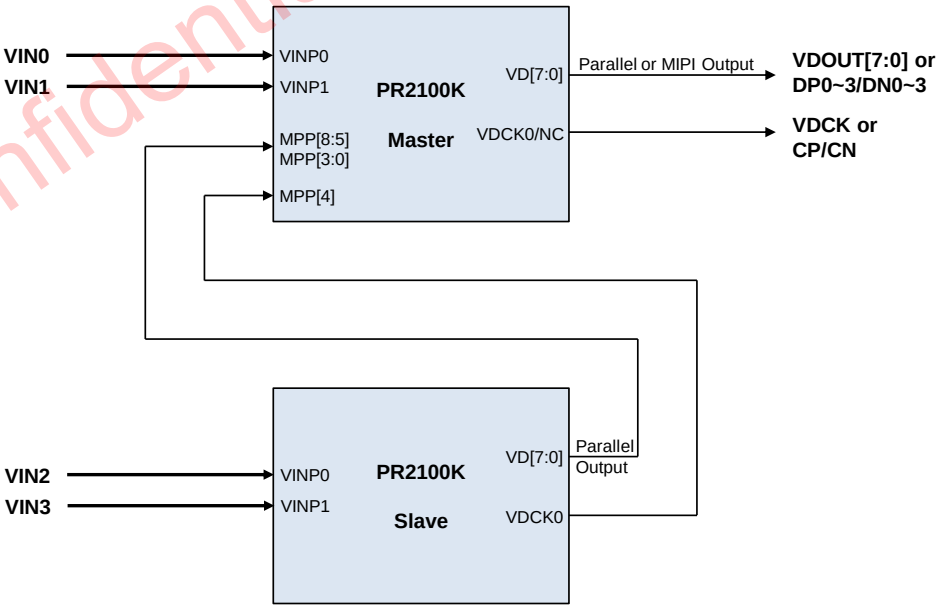


Fig 28. Cascade Connection for Multi-chip Application

2.3. Host Interface

2.3.1. I2C Interface

The PR2100 supports serial interface consisting of two signals, serial data line SDAT (Pin 45) and clock line SCLK (Pin 46) that should be connected to VDDO via pull up resistors. The PR2100 also provides auto-increment mode of sub-address for multi-byte serial read/write operation. The MPP[8:7] (Pin 42,43) are used to select the slave address which are 7'h5C for MPP[8:7] = 0, 7'h5D for MPP[8:7] = 1, 7'h5E for MPP[8:7] = 2, and 7'h5F for MPP[8:7] = 3 when SADDR_LAT_EN (0xFF bit[7]) = "1". The maximum data transfer rate on the bus is up to 400kbit/s. The detailed I2C protocol is shown in the following Fig 29.

I2C Slave Address							R/W
1	0	1	1	1	MPP[8]	MPP[7]	1/0

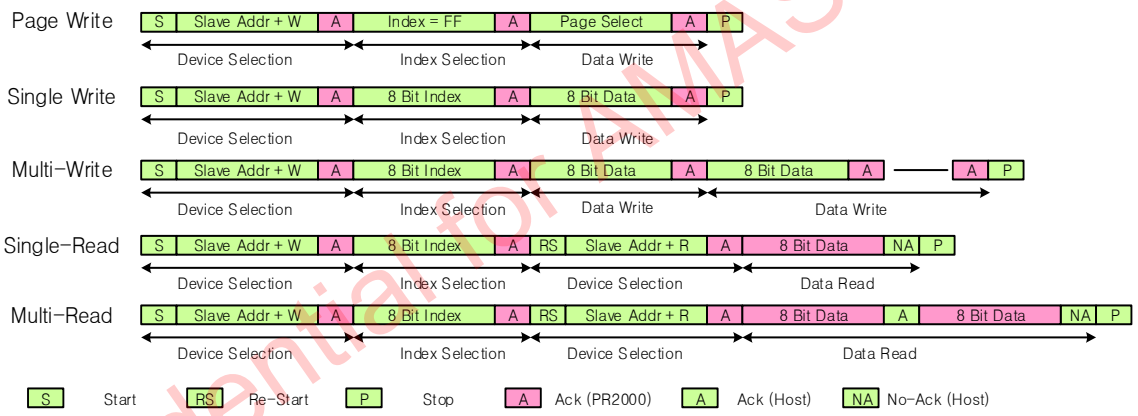


Fig 29. Protocol of I2C Interface

The PR2100 has total 7 page x 256 register map in it so that the page selection register HOST_RW_PAGE (0xFF) should be accessed before any register is programmed. The brief page descriptions are shown in the following Table 6.

Table 6. Page Selection Register Description

Index Page Number	Description
Page 0	Video Format + IRQ + PAD I/O Control
Page 1	CH0 Video Decoder Control
Page 2	CH1 Video Decoder Control
Page 3	CH0 PTZ Control

Page 4	CH1 PTZ Control
Page 5	MIPI Logic Control
Page 6	MIPI PHY Control

2.3.2. GPIO Interface

The MPP[11:0] pins can be used as GPIO pins for general purpose such as monitoring input, programming output and receiving interrupt source. Each GPIO pin can be enabled via the corresponding registers as the following Table 7. The data direction of GPIO can be controlled by the register GPIO_IOB (0xC0 ~ CB) that is set to “1” for input and “0” for output. The output value of GPIO pin can be programmed via the GPIO_OUT (0xC0 ~ CB) register. The input value of GPIO pin can be read via the STATUS_GPIO (0x98 ~ 99) register.

Table 7. Pins and Registers of GPIO

GPIO	Pin Name	Related Register for GPIO
GPIO[0]	MPP[0]	MPP_SEL0[3:0] (0xC0)=“0”, GPIO_IOB0 (0xC0), GPIO_OUT0 (0xC0)
GPIO[1]	MPP[1]	MPP_SEL1[3:0] (0xC1)=“0”, GPIO_IOB1 (0xC1), GPIO_OUT1 (0xC1)
GPIO[2]	MPP[2]	MPP_SEL2[3:0] (0xC2)=“0”, GPIO_IOB2 (0xC2), GPIO_OUT2 (0xC2)
GPIO[3]	MPP[3]	MPP_SEL3[3:0] (0xC3)=“0”, GPIO_IOB3 (0xC3), GPIO_OUT3 (0xC3)
GPIO[4]	MPP[4]	MPP_SEL4[3:0] (0xC4)=“0”, GPIO_IOB4 (0xC4), GPIO_OUT4 (0xC4)
GPIO[5]	MPP[5]	MPP_SEL5[3:0] (0xC5)=“0”, GPIO_IOB5 (0xC5), GPIO_OUT5 (0xC5)
GPIO[6]	MPP[6]	MPP_SEL6[3:0] (0xC6)=“0”, GPIO_IOB6 (0xC6), GPIO_OUT6 (0xC6)
GPIO[7]	MPP[7]	MPP_SEL7[3:0] (0xC7)=“0”, GPIO_IOB7 (0xC7), GPIO_OUT7 (0xC7)
GPIO[8]	MPP[8]	MPP_SEL8[3:0] (0xC8)=“0”, GPIO_IOB8 (0xC8), GPIO_OUT8 (0xC8)
GPIO[9]	MPP[9]	MPP_SEL9[3:0] (0xC9)=“0”, GPIO_IOB9 (0xC9), GPIO_OUT9 (0xC9)
GPIO[10]	MPP[10]	MPP_SELA[3:0] (0xCA)=“0”, GPIO_IOBA (0xCA), GPIO_OUTA (0xCA)
GPIO[11]	MPP[11]	MPP_SELB[3:0] (0xCB)=“0”, GPIO_IOBB (0xCB), GPIO_OUTB (0xCB)

Table 8. MPP[11:0] Pin Configuration

Pin Name	MPP_SEL	IO Type	Pin Description
MPP[0]	0	IO	GPIO[0]
	1	I	Cascaded Video Data Input (CCVD[0])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[0])
MPP[1]	0	IO	GPIO[1]
	1	I	Cascaded Video Data Input (CCVD[1])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[1])
MPP[2]	0	IO	GPIO[2]
	1	I	Cascaded Video Data Input (CCVD[2])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[2])
MPP[3]	0	IO	GPIO[3]
	1	I	Cascaded Video Data Input (CCVD[3])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[3])
MPP[4]	0	IO	GPIO[4]
	1	I	Cascaded Video Clock Input (CCCK)
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Clock Output of CH1 (VDCK1)
MPP[5]	0	IO	GPIO[5]
	1	I	Cascaded Video Data Input (CCVD[4])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[4])
MPP[6]	0	IO	GPIO[6]
	1	I	Cascaded Video Data Input (CCVD[5])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[5])
MPP[7]	0	IO	GPIO[7]
	1	I	Cascaded Video Data Input (CCVD[6])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1

	4	O	Video Data Output of CH1 (VD1[6])
MPP[8]	0	IO	GPIO[8]
	1	I	Cascaded Video Data Input (CCVD[7])
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	O	Video Data Output of CH1 (VD1[7])
MPP[9]	0	IO	GPIO[9]
	1	O	IRQ
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	I	Reserved
MPP[10]	0	IO	GPIO[10]
	1	I	PTZ Control Output for CH0
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	I	Reserved
MPP[11]	0	IO	GPIO[11]
	1	I	PTZ Control Output for CH1
	2	O	Video Sync Output (HSYNC, VSYNC, FLD) for CH0/1
	4	I	Reserved

2.3.3. Interrupt Interface

The PR2100 requests the interrupt to host through the IRQ pin. The polarity of IRQ pin is determined by the IRQOUT_POL (0x80) register. The interrupt is repeated periodically via the IRQOUT_RPT (0x80) register until the host receives interrupt correctly. The PR2100 requests the interrupt to host when the event of video format change, video loss, PTZ and GPIO transition happens. Each event can be activated via the IRQENA (0x90~93, 0xA0~A1, 0xB0~B1) register. When host receives the interrupt from PR2100, the host should read the IRQCLR (0x94~97, 0xA2~A3, 0xB2~B3) register to find out which event requests interrupt service and then write “1” into corresponding bit of the IRQCLR register to clear the interrupt request because the PR2100 maintains the interrupt status until it is cleared. Additionally, the host can read the current state of each event through the STATUS (0x98~9B, 0xA4~A5, 0xB4~B5) register. The event list of interrupt request is described in the following Table 9.

Table 9. Event List of Interrupt Request

Event	Bit Size	Status		Interrupt Mode	
		0	1	Level	Edge
Video Loss	1	Normal	Video Loss	High/Low	Both
Video Format	1	Match	Format Error	High/Low	Both
PTZ Tx Done	1	Normal	Tx Busy	X	Falling
PTZ Tx Error	2	Normal	Tx Error	High	X
PTZ Rx Done	1	Normal	Rx Busy	X	Falling
PTZ Rx Error	4	Normal	Rx Error	High	X
GPIO	12	0	1	High/Low	Rising/Falling/Both
Timer IRQ	2	0	Timer Period	High	X

2.4. Power

The PR2100 has four IO power domains as shown in Fig 2. The VDDO1 (#16) in power domain1 should use only 3.3V IO voltage because the XTALI/O pad requires the 3.3V supply voltage. The VDDO2 (#24) in power domain2 can use 3.3V or 1.8V IO voltage for parallel output mode, but should use only 3.3V IO voltage for MIPI output mode. The VDDO3, VDDO4 (#37, #47) in power domain3/4 can use either 3.3V or 1.8V IO voltage. For 1.8V IO supply voltage mode in power domain2/3/4, the data interface pin has 0 ~ 1.8V voltage range (0V for logic Low and 1.8V for logic High). The VDD1V (#2, #11) and VDD1P (#12, #25) in power domain0 should be applied with 1.2V and VDD3V (#4, #9) in power domain0 should be applied with 3.3V for proper analog IP (Video ADC and PLL) operation. The reference schematics for 1.8V IO supply voltage are illustrated in Chapter 6 (Application Schematic). The multi-chip cascaded connection is not supported with 1.8V IO supply voltage.

2.5. PLL

An analog clock multiplier PLL is used to generate a clock of digital video output from an external 27MHz crystal or external oscillator clock input. A crystal can be connected across terminals Pin 17 (XTALI) and Pin 18 (XTALO), or an external oscillator clock input can be connected to Pin 17 (XTALI). The following Fig 30 and Fig 31 show the reference clock configurations.

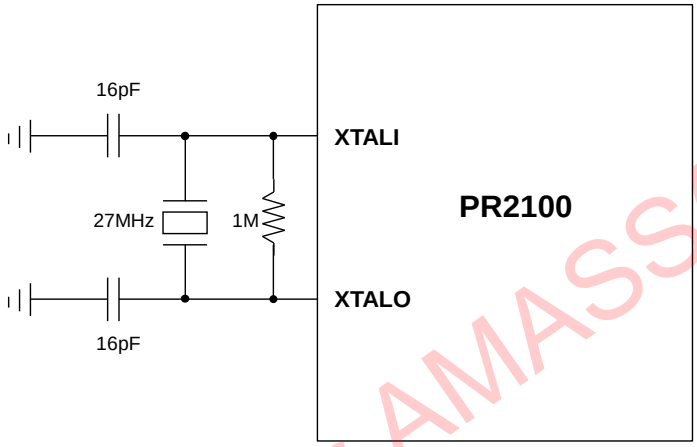


Fig 30. Recommended Crystal Oscillating Circuit

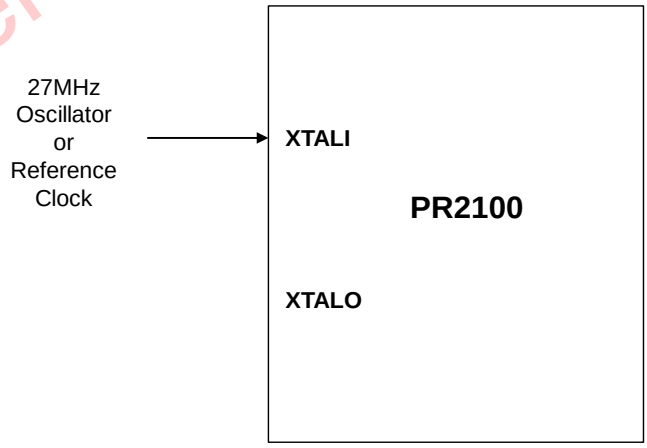


Fig 31. Recommended External Oscillator Clock Input Circuit

3. Register Information

3.1. Register Map

3.1.1. Page 0 (Video Format/EQ and IRQ)

Note : * Read Only Register

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00*	VID_STATUS0_0	DET_IFMT_STD0[1:0]		DET_IFMT_REF0[1:0]		DET_VIDEO0	DET_IFMT_RES0[2:0]		
0x01*	VID_STATUS1_0	LOCK_STD0	LOCK_GAIN0	LOCK_CLAMP0		LOCK_HPLL0	LOCK_C_FINE0	LOCK_CHROMA0	DET_CHROMA0
0x02*	VID_STATUS2_0			DET_STD_HDT2_0	DET_STD_HDT1_0	DET_STD_HDT0_0	DET_STD_HDA0	DET_STD_CVI0	DET_STD_PVI0
~	RESERVED	RESERVED							
0x10	MAN_IFMT0	MAN_IFMT_STD0[1:0]		MAN_IFMT_REF0[1:0]		MAN_IFMT_STD_HDT_N0	MAN_IFMT_RES0[2:0]		
0x11	MAN_IFMT_EN0		VADC_GAIN_SEL0[2:0]			MAN_IFMT_EN0[3:0]			
0x12	MAN_EQ_AC_GN0	DET_SIGNAL0			MAN_EQ_GAIN_MD0[4:0]				
0x13	VADC_EQ_BAND0			MAN_EQ_LOW_BAND0[1:0]			MAN_EQ_HIGH_BAND0[2:0]		
0x14	VADC_CTRL0	RESERVED						VADC_IN_SEL0[1:0]	
0x17 ~ 0x1F	RESERVED	RESERVED							
0x20*	VID_STATUS0_1	DET_IFMT_STD1[1:0]		DET_IFMT_REF1[1:0]		DET_VIDEO1	DET_IFMT_RES1[2:0]		
0x21*	VID_STATUS1_1	LOCK_STD1	LOCK_GAIN1	LOCK_CLAMP1		LOCK_HPLL1	LOCK_C_FINE1	LOCK_CHROMA1	DET_CHROMA1
0x22*	VID_STATUS2_1			DET_STD_HDT2_1	DET_STD_HDT1_1	DET_STD_HDT0_1	DET_STD_HDA1	DET_STD_CVI1	DET_STD_PVI1
~	RESERVED	RESERVED							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x30	MAN_IFMT1	MAN_IFMT_STD1[1:0]		MAN_IFMT_REF1[1:0]		MAN_IFMT_ STD_HDT_N1	MAN_IFMT_RES1[2:0]		
0x31	MAN_IFMT_EN1		VADC_GAIN_SEL1[2:0]			MAN_IFMT_EN1[3:0]			
0x32	MAN_EQ_AC_GN1	DET_SIGNAL1			MAN_EQ_GAIN_MD1[4:0]				
0x33	VADC_EQ_BAND1			MAN_EQ_LOW_BAND1[1:0]			MAN_EQ_HIGH_BAND1[2:0]		
0x34	VADC_CTRL1	RESERVED						VADC_IN_SEL1[1:0]	
0x35 ~ 0x3F	RESERVED	RESERVED							
0x40	mipi_monitor	{4'd0, mipi_monitor[11:8]}							
0x41	mipi_monitor	mipi_monitor[7:0]							
0x42 ~ 0x6F	RESERVED	RESERVED							
0x70	DUMMY_REG0	DUMMY_REG0 (R/W)							
0x71	DUMMY_REG1	DUMMY_REG1 (R/W)							
0x72	DUMMY_REG2	DUMMY_REG2 (R/W)							
0x73	DUMMY_REG3	DUMMY_REG3 (R/W)							
0x74	DUMMY_REG4	DUMMY_REG4 (R/W)							
0x75	DUMMY_REG5	DUMMY_REG5 (R/W)							
0x76	DUMMY_REG6	DUMMY_REG6 (R/W)							
0x77	DUMMY_REG7	DUMMY_REG7 (R/W)							
0x78 ~ 0x7F	RESERVED	RESERVED							
0x80	IRQ_CTRL	IRQOUT_EN		IRQOUT_POL	IRQOUT_RPT		SYNC_GPIO	SYNC_FUNC	SYNC_PTZ
0x81	IRQ_SYNC_PERIOD	IRQ_SYNC_PERIOD							
0x82	TIMER0_PERIOD	IRQ_TIMER0_PERIOD (TIMER_PERIOD = 20msec * IRQ_SYNC_PERIOD * IRQ_TIMER_PERIOD)							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x83*	IRQ_EVENT			EVENT_TIMER	EVENT_GPIO	EVENT_VFD	EVENT_NOVID	EVENT_PTZ1	EVENT_PTZ0
0x84	IRQ_NOVID_MD	IRQ_VFD_PEND	IRQ_NOVID_PEND	IRQ_VFD_MD	IRQ_NOVID_MD	IRQ_GPIO_MD[11:8]			
0x85	IRQ_GPIO_MD	IRQ_GPIO_MD[7:0] (GPIO[11:0] = MPP[11:0]) : 0 : Edge, 1 : Level							
0x86	IRQ_NOVID_LV					IRQ_GPIO_LV[11:8]			
0x87	IRQ_GPIO_LV	IRQ_GPIO_LV[7:0] (GPIO[11:0] = MPP[11:0])							
0x88	IRQ_NOVID_BOTH					IRQ_GPIO_BOTH[11:8]			
0x89	IRQ_GPIO_BOTH	IRQ_GPIO_BOTH[7:0], (0 : Single Edge, 1 : Both Edge Interrupt Enable @ IRQ_LV = 0) for GPIO[7:0]							
0x8A	TIMER1_PERIOD	IRQ_TIMER1_PERIOD (TIMER_PERIOD = 20msec * IRQ_SYNC_PERIOD * IRQ_TIMER1_PERIOD)							
0x8B ~ 0x8F	RESERVED	RESERVED							
0x90	IRQENA_TIMER	IRQENA_TIMER				IRQENA_GPIO[11:8]			
0x91	IRQENA_GPIO	IRQENA_GPIO[7:0] (GPIO[11:0] = MPP[11:0])							
0x92 ~ 0x93	RESERVED	RESERVED							
0x94*	IRQCLR_TIMER	IRQCLR_TIMER				IRQCLR_GPIO[11:8]			
0x95*	IRQCLR_GPIO	IRQCLR_GPIO[7:0] (GPIO[11:0] = MPP[11:0])							
0x96 ~ 0x97	RESERVED	RESERVED							
0x98*	STATUS_TIMER	STATUS_TIMER				STATUS_GPIO[11:8]			
0x99*	STATUS_GPIO	STATUS_GPIO[7:0] (GPIO[11:0] = MPP[11:0])							
0x9A ~ 0x9F	RESERVED	RESERVED							
0xA0	IRQENA_VFD0		IRQ_CC_NOVID_LV2	IRQ_VFD_LV0	IRQ_NOVID_LV0		IRQENA_CC_NOVID2	IRQENA_VFD0	IRQENA_NOVID0
0xA1	IRQENA_PTZ0	IRQENA_PTZ0							
0xA2*	IRQCLR_VFD0						IRQCLR_CC_NOVID2	IRQCLR_VFD0	IRQCLR_NOVID0

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xA3*	IRQCLR_PTZ0	IRQCLR_PTZ0							
0xA4*	STATUS_VFD0						STATUS_CC_NOVID2	STATUS_VFD0	STATUS_NOVID0
0xA5*	STATUS_PTZ0	STATUS_PTZ0							
0xA6 ~ 0xAF	RESERVED	RESERVED							
0xB0	IRQENA_VFD1		IRQ_CC_NOVID_LV3	IRQ_VFD_LV1	IRQ_NOVID_LV1		IRQENA_CC_NOVID3	IRQENA_VFD1	IRQENA_NOVID1
0xB1	IRQENA_PTZ1	IRQENA_PTZ1							
0xB2*	IRQCLR_VFD1						IRQCLR_CC_NOVID3	IRQCLR_VFD1	IRQCLR_NOVID1
0xB3*	IRQCLR_PTZ1	IRQCLR_PTZ1							
0xB4*	STATUS_VFD1						STATUS_CC_NOVID3	STATUS_VFD1	STATUS_NOVID1
0xB5*	STATUS_PTZ1	STATUS_PTZ1							
0xB6 ~ 0xBF	RESERVED	RESERVED							
0xC0	MPP_CTRL0	MPP_POL0	MPP_CH0	MPP_IOB0	GPIO_OUT0	MPP_MD0	MPP_SEL0[2:0]		
0xC1	MPP_CTRL1	MPP_POL1	MPP_CH1	MPP_IOB1	GPIO_OUT1	MPP_MD1	MPP_SEL1[2:0]		
0xC2	MPP_CTRL2	MPP_POL2	MPP_CH2	MPP_IOB2	GPIO_OUT2	MPP_MD2	MPP_SEL2[2:0]		
0xC3	MPP_CTRL3	MPP_POL3	MPP_CH3	MPP_IOB3	GPIO_OUT3	MPP_MD3	MPP_SEL3[2:0]		
0xC4	MPP_CTRL4	MPP_POL4	MPP_CH4	MPP_IOB4	GPIO_OUT4	MPP_MD4	MPP_SEL4[2:0]		
0xC5	MPP_CTRL5	MPP_POL5	MPP_CH5	MPP_IOB5	GPIO_OUT5	MPP_MD5	MPP_SEL5[2:0]		
0xC6	MPP_CTRL6	MPP_POL6	MPP_CH6	MPP_IOB6	GPIO_OUT6	MPP_MD6	MPP_SEL6[2:0]		
0xC7	MPP_CTRL7	MPP_POL7	MPP_CH7	MPP_IOB7	GPIO_OUT7	MPP_MD7	MPP_SEL7[2:0]		
0xC8	MPP_CTRL8	MPP_POL8	MPP_CH8	MPP_IOB8	GPIO_OUT8	MPP_MD8	MPP_SEL8[2:0]		
0xC9	MPP_CTRL9	MPP_POL9	MPP_CH9	MPP_IOB9	GPIO_OUT9	MPP_MD9	MPP_SEL9[2:0]		

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xCA	MPP_CTRLA	MPP_POLA	MPP_CHA	MPP_IOBA	GPIO_OUTA	MPP_MDA	MPP_SELA[2:0]		
0xCB	MPP_CTRLB	MPP_POLB	MPP_CHB	MPP_IOBB	GPIO_OUTB	MPP_MDB	MPP_SELB[2:0]		
0xCC~0xCF	RESERVED	RESERVED							
0xD0	PLL0_CON0	PLL0_PD							
0xD1	PLL0_CON1						PLL0_REF_CNT[2:0]		
0xD2	PLL0_CON2		PLL0_MAIN_CNT[6:0]						
0xD3	RESERVED	RESERVED							
0xD4	PLL1_CON0	PLL1_PD							
0xD5	PLL1_CON1						PLL1_REF_CNT[2:0]		
0xD6	PLL1_CON2		PLL1_MAIN_CNT[6:0]						
0xD7	PLL1_CON3		PLL1_8PH_SEL_2[2:0]				PLL1_8PH_SEL_1[2:0]		
0xD8	PLL2_CON0	PLL2_PD		BGR_PD					
0xD9	PLL2_CON1						PLL2_REF_CNT[2:0]		
0xDA	PLL2_CON2		PLL2_MAIN_CNT[6:0]						
0xDB ~ 0xE1	RESERVED	RESERVED							
0xE2	OUT_FMT				CKOUT_2X_MD	CH_MUX_MD[1:0]		OUTFMT_RATE[1:0]	
0xE3	CHID_NUM	OUTFMT_YC _INV1	OUTFMT_YC _INV0			CHID_NUM1[1:0]		CHID_NUM0[1:0]	
0xE4	CH_SEL0		CH_SEL_B0[2:0]				CH_SEL_A0[2:0]		
0xE5	CH_SEL1		CH_SEL_D0[2:0]				CH_SEL_C0[2:0]		
0xE6	CH_SEL2		CH_SEL_B1[2:0]				CH_SEL_A1[2:0]		
0xE7	CH_SEL3		CH_SEL_D1[2:0]				CH_SEL_C1[2:0]		

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xE8	VDCKP_PHASE			VDCK0_PHASE					
0xE9	VDCKN_PHASE			VDCK1_PHASE					
0xEA	CLK_PWDN				MIPI_DCLK_PWDN	CC_CLK_PWDN	VOUT_CLK_PWDN	VDEC_CLK_PWDN1	VDEC_CLK_PWDN0
0xEB	MIPI_DATA_EN								MIPI_DATA_EN
0xEC ~ 0xEF	RESERVED	RESERVED							
0xF0	PAR_OE_M								VDCK_IOB[0]
0xF1	PAR_OE_L	VD_IOB[7:0]							
0xF2	PAD_DIG_CTL						SYS_SMT_EN	SYS_DRV_SEL	
0xF3	PAD_MPP_CTL		PTZ_SMT_EN	PTZ_DRV_SEL			MPP_SMT_EN	MPP_DRV_SEL	
0xF4	PAD_VD_CTL		VD_SMT_EN	VD_DRV_SEL			VDCK_SMT_EN	VDCK_DRV_SEL	
0xF5 ~ 0xFA	RESERVED	RESERVED							
0xFB*	OPT_ID	0	0	0	0	0	0	0	OPT_ID*
0xFC*	CHIP_ID_MSB	0	0	1	0	0	0	0	1
0xFD*	CHIP_ID_LSB	0	0	0	0	0	0	0	0
0xFE*	REV_ID	REV_ID = 8'h20							
0xFF	PAGE_SEL	SADDR_LATEN					HOST_RW_PAGE[2:0]		

3.1.2. Page 1/2 (Video Decoder 0/1)

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x00	VID_CON0	AGCEN0	AUTO_BGND0	PEAKEN0		PEAKREF0		BGND_MD0	
1x01 ~ 1x10	RESERVED	RESERVED							
1x11	HDELAY_MSB0	VDELAY0[10:8]			HDELAY0[12:8]				
1x12	HACTIVE_MSB0	VACTIVE0[10:8]			HACTIVE0[12:8]				
1x13	HDELAY_LSB0	HDELAY0[7:0]							
1x14	HACTIVE_LSB0	HACTIVE0[7:0]							
1x15	VDELAY0	VDELAY0[7:0]							
1x16	VACTIVE0	VACTIVE0[7:0]							
1x17 ~ 1x1C	RESERVED	RESERVED							
1x1D	CBP_DELAY_MSB0				HSCL_ACTIVE0[12:8]				
1x1E	RESERVED	RESERVED							
1x1F	HSCL_ACTIVE_LSB0	HSCL_ACTIVE0[7:0]							
1x20	CONT0	CONT0							
1x21	BRGT0	BRGT0							
1x22	SAT0	SAT0							
1x23	HUE0	HUE0							
1x24 ~ 1x28	RESERVED	RESERVED							
1x29	DOWN_HSCL_MSB0	DOWN_HSCL0[15:8]							
1x2A	DOWN_HSCL_LSB0	DOWN_HSCL0[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x2B ~ 1x36	RESERVED	RESERVED							
1x37	HD_Y_NOTCH_MD0	COMB_FLT_EN0							
1x38	RESERVED	RESERVED							
1x39	Y_DYN_PEAK_GN0	MAN_NOVID0[1:0]			HPEAK_MD0	HPEAK_GN0			
1x3A	HD_Y_LPF_MD0	NR_EN0			YLPF_MD0				
1x3B ~ 1x3C	RESERVED	RESERVED							
1x3D	CORE_CON0			CTI_CORE0		C_CORE0		HPEAK_CORE0	
1x3E	MAN_CLPF_MD0	MAN_CKIL0				CLPF_MD0			
1x3F	HD_CTI_CON0				CTI_MD0	CTI_GAIN0			
1x40	C_LOOP_CON0_0	PAL_COMP_EN0							
1x41 ~ 1x4C	RESERVED	RESERVED							
1x4D	YC_DELAY0		C_DELAY0			Y_DELAY0			
1x4E	HD_HALF_MD0	MAN_VIN_FMT0						SD_720H_MD0	HD_HALF_MD0
1x4F	OUTFMT_CON0	BT1120_LIM0		VIN_BT656_MD0		CHID_EN0		NOVID_BT11200	
1x50	TST_EQ_POS0_0	HD_CSC_MD0							
1x51 ~ 1x54	RESERVED	RESERVED							
1x55	PTZ_SLICE_LVL0	PTZ_SLICE_LEVEL0							
1x56 ~ 1xBA	RESERVED	RESERVED							
1xBB	EXT_SYNC_CON0		VO_SYNC_CON_EN0						
1xBC	VOSYNC_HDELAY_MSB0				VOUT_SYNC_HDELAY0[12:8]				
1xBD	VOSYNC_HDELAY_LSB0	VOUT_SYNC_HDELAY0[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1xBE	VOSYNC_HACTIVE_MSB0				VOUT_SYNC_HACTIVE0[12:8]				
1xBF	VOSYNC_HACTIVE_LSB0	VOUT_SYNC_HACTIVE0[7:0]							
1xC0	VOSYNC_VDELAY_MSB0						VOUT_SYNC_VDELAY0[10:8]		
1xC1	VOSYNC_VDELAY_LSB0	VOUT_SYNC_VDELAY0[7:0]							
1xC2	VOSYNC_VACTIVE_MSB0	VOUT_HD_PAT_FMT0[3:0]					VOUT_SYNC_VACTIVE0[10:8]		
1xC3	VOSYNC_VACTIVE_LSB0	VOUT_SYNC_VACTIVE0[7:0]							
1xC4	MAN_INFMT_ADD_MSB0	VOUT_HD_PATH_MD0[3:0]				VOUT_HD_PAT_EN0			
1xC5 ~ 1xC8	RESERVED	RESERVED							
1xC9	VISYNC_HDELAY_MSB0				VIN_SYNC_HDELAY0[12:8]				
1xCA	VISYNC_HDELAY_LSB0	VIN_SYNC_HDELAY0[7:0]							
1xCB	VISYNC_HACTIVE_MSB0				VIN_SYNC_HACTIVE0[12:8]				
1xCC	VISYNC_HACTIVE_LSB0	VIN_SYNC_HACTIVE0[7:0]							
1xCD	VISYNC_VDELAY_MSB0	VIN_HD_PAT_FMT0[3:0]				VIN_SYNC_CON_EN0	VIN_SYNC_VDELAY0[10:8]		
1xCE	VISYNC_VDELAY_LSB0	VIN_SYNC_VDELAY0[7:0]							
1xCF	VISYNC_VACTIVE_MSB0	VIN_HD_PATH_MD0[3:0]				VIN_HD_PAT_EN0	VIN_SYNC_VACTIVE0[10:8]		
1xD0	VISYNC_VACTIVE_LSB0	VIN_SYNC_VACTIVE0[7:0]							
1xD1	MIPI_DATA_FLD_CON0				VIN_HD_EN0				
1xD2 ~ 1xD3	RESERVED	RESERVED							
2x00	VID_CON1	AGCEN1	AUTO_BGND1	PEAKEN1		PEAKREF1		BGND_MD1	
~	~	CH1 Register Map							
2xD1	MIPI_DATA_FLD_CON1				VIN_HD_EN1				

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2xD2 ~ 2xD3	RESERVED	RESERVED							

3.1.3. Page 3/4 (PTZ Tx/Rx 0/1)

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
3x00	PTZ_RX_EN0	PTZ_RX_PATH_EN0	PTZ_RX_START0	PTZ_IGNORE_LINE_EN0		PTZ_IGNORE_FRM_EN0	PTZ_RX_FIELD_POL0	PTZ_RX_FIELD_TYPE0	
3x01	PTZ_RX_LINE_CNT0	PTZ_RX_LINE_CNT0					PTZ_RX_HST_OS0		
3x02	PTZ_RX_HST0	PTZ_RX_DATA_POL0	PTZ_RX_HST0						
3x03	PTZ_RX_FREQ_FIRST0_0	PTZ_RX_FREQ_FIRST0[23:16]							
3x04	PTZ_RX_FREQ_FIRST0_1	PTZ_RX_FREQ_FIRST0[15:08]							
3x05	PTZ_RX_FREQ_FIRST0_2	PTZ_RX_FREQ_FIRST0[07:00]							
3x06	PTZ_RX_FREQ0_0	PTZ_RX_FREQ0[23:16]							
3x07	PTZ_RX_FREQ0_1	PTZ_RX_FREQ0[15:08]							
3x08	PTZ_RX_FREQ0_2	PTZ_RX_FREQ0[7:0]							
3x09	PTZ_RX_LPF_LEN0			PTZ_RX_LPF_LEN0					
3x0A	PTZ_Rx_H_PIX_OFFSET0	PTZ_RX_H_PIX_OFFSET0							
3x0B	PTZ_RX_LINE_LEN0			PTZ_RX_LINE_LEN0					
3x0C	PTZ_RX_VALID_CNT0	PTZ_RX_VALID_CNT0							
3x0D	PTZ_RX_TEST_EN0		PTZ_ADDR_HOLD_EN0						
3x0E ~ 3x0F	RESERVED	RESERVED							
3x10	PTZ_FIFO_WR_INIT0	PTZ_WR_ADR_INIT0	PTZ_WR_BIT_SWAP0				PTZ_FIFO_WR_MD0 (Def 0) 0 : Tx Data, 1 : Tx Flag, 2 : Tx Flag_data, 3 : Rx Data(x), 4 : Rx Flag, 5 : Rx Start Flag, 6 : Rx Start Flag Data		
3x11	PTZ_FIFO_WR_DATA0	PTZ_FIFO_WR_DATA0 (ADDRESS HOLD)							
3x12	PTZ_TX_QUEUE_SIZE0*	PTZ_TX_QUEUE_SIZE0							
3x13	PTZ_FIFO_WR_ADDR0*	PTZ_FIFO_WR_ADDR0							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
3x14	PTZ_FIFO_RD_INIT0	PTZ_RD_ADR_INIT0	PTZ_RD_BIT_SWAP0		PTZ_PRE_RD_EN0		PTZ_FIFO_RD_MD0 (Def : 3) 0 : Tx Data(x), 1 : Tx Flag, 2 : Tx Flag Data, 3 : Rx Data, 4 : Rx Flag, 5 : Rx Star Flag, 6 : Rx Start Flag Data		
3x15	PTZ_RX_QUEUE_SIZE0*	PTZ_RX_QUEUE_SIZE0* or FIFO READ ADDR0*							
3x16	PTZ_RX_DATA_DET0*	PTZ_RX_DATA_DET0* (ADDRESS HOLD) or FIFO READ DATA0							
3x17	PTZ_FIFO_RD_ADDR0*	PTZ_FIFO_RD_ADDR0							
3x18	PTZ_RX_HSYN_POL0	PTZ_RX_HSYNC_POL0							
3x19	RESERVED	RESERVED							
3x1A	PTZ_RX_VSYNC_POL0	PTZ_RX_VSYNC_POL0							
3x1B	RESERVED	RESERVED							
3x1C	PTZ_TX_HSYNC_POL0	PTZ_TX_HSYNC_POL0							
3x1D	RESERVED	RESERVED							
3x1E	PTZ_TX_VSYNC_POL0	PTZ_TX_VSYNC_POL0							
3x1F	RESERVED	RESERVED							
3x20	PTZ_TX_EN0	PTZ_TX_PATH_EN0	PTZ_TX_START0				PTZ_TX_FIELD_POL0	PTZ_TX_FIELD_TYPE0	
3x21	PTZ_TX_LINE_CNT0	PTZ_TX_LINE_CNT0					PTZ_TX_HST_OS0		
3x22	PTZ_TX_HST0	PTZ_TX_DATA_POL0	PTZ_TX_HST0						
3x23	PTZ_TX_FREQ_FIRST0_0	PTZ_TX_FREQ_FIRST0[23:16]							
3x24	PTZ_TX_FREQ_FIRST0_1	PTZ_TX_FREQ_FIRST0[15:08]							
3x25	PTZ_TX_FREQ_FIRST0_2	PTZ_TX_FREQ_FIRST0[07:00]							
3x26	PTZ_TX_FREQ0_0	PTZ_TX_FREQ0[23:16]							
3x27	PTZ_TX_FREQ0_1	PTZ_TX_FREQ0[15:08]							
3x28	PTZ_TX_FREQ0_2	PTZ_TX_FREQ0[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
3x29	PTZ_TX_HPST0				PTZ_TX_HPST0[12:8]				
3x2A	PTZ_TX_HPST0	PTZ_TX_HPST0[7:0]							
3x2B	PTZ_TX_LINE_LEN0			PTZ_TX_LINE_LEN0					
~	RESERVED	RESERVED							
4x00	PTZ_RX_EN1	PTZ_RX_PATH_EN1	PTZ_RX_START1	PTZ_IGNORE_LINE_EN1		PTZ_IGNORE_FRM_EN1	PTZ_RX_FIELD_POL1	PTZ_RX_FIELD_TYPE1	
~	~	CH1 Register Map							
4x2B	PTZ_TX_LINE_LEN1			PTZ_TX_LINE_LEN1					
~	RESERVED	RESERVED							

3.1.4. Page 5 (MIPI Controller)

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
5x00	OVERFLOW*				mtx_ch_overflow[4:0]				
5x01	OVERFLOW*					mtx_buf_overflow[3:0]			
5x02~5x08	RESERVED	RESERVED							
5x06*	MTX_CH_SYNC		FSYNC1_OUT	VSYNC1_OUT	HSYNC1_OUT		FSYNC0_OUT	VSYNC0_OUT	HSYNC0_OUT
5x07*	MTX_CH_SYNC		FSYNC3_OUT	VSYNC3_OUT	HSYNC3_OUT		FSYNC2_OUT	VSYNC2_OUT	HSYNC2_OUT
5x08	RESERVED	RESERVED							
5x09	REF_CH_STRT	REF_CH_STRT		TST_CHID_FIX				REF_CH_SEL	
5x0A	REF_CH_VDLY	REF_CH_VDLY							
5x0B	DBG_CH_SEL0		DBG_CH1_SEL				DBG_CH0_SEL		
5x0C	DBG_CH_SEL1		DBG_CH3_SEL				DBG_CH2_SEL		
5x0D	FRAME_MD	CH3_FRAME_MD		CH2_FRAME_MD		CH1_FRAME_MD		CH0_FRAME_MD	
5x0E	VBLK_CODE	VBLK_CODE[07:00] for C							
5x0F	VBLK_CODE	VBLK_CODE[15:08] for Y							
5x10	MTX_CTRL	MTX_PATH_EN	REF_VSTRT_MD	MTX_VBLK_MSK	MTX_CHBLK_MSK	MTX_BLK_LV		MTX_LANE	
5x11	MTX_LONG_DLY_H	REF_VBLK_MD		REF_CH_NUM		MTX_LONG_DLY[11:8]			
5x12	MTX_LONG_DLY_L	MTX_LONG_DLY[7:0]							
5x13	MTX_SHORT_DLY_H	REF_TIME_EN	REF_COMB_MD		REF_HSTRT_MD	MTX_SHORT_DLY[11:8]			
5x14	MTX_SHORT_DLY_L	MTX_SHORT_DLY[7:0]							
5x15	REF_OFFSET	REF_VS_OS_VBLK		REF_VE_OS_VBLK		REF_FE_VOS		REF_FS_VOS	

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
5x16	REF_FE_HDLY			REF_FE_HDLY[13:8]					
5x17	REF_FE_HDLY	REF_FE_HDLY[7:0]							
5x18	REF_FS_HDLY			REF_FS_HDLY[13:8]					
5x19	REF_FS_HDLY	REF_FS_HDLY[7:0]							
5x1A	REF_HTOTAL			REF_HTOTAL[13:8]					
5x1B	REF_HTOTAL	REF_HTOTAL[7:0]							
5x1C	REF_VTOTAL			REF_VTOTAL[13:8]					
5x1D	REF_VTOTAL	REF_VTOTAL[7:0]							
5x1E	CHID_MD	MTX_CHID_EN	REF_LINE_ID_EN	MTX_CHID_MD		MTX_CHID_NUM		MTX_CHID_SIZE	
5x1F	RESERVED	RESERVED							
5x20	MTX_CH0_CTRL	MTX_CH0_EN	CH0_VBLK_MD	MTX_CH0_SEL		MTX_CH0_BUF_SIZE			
5x21	MTX_CH0_HSIZE	CH0_DATA_BLK	CH0_ID_BLK	CH0_INFO		CH0_INT_MD	MTX_CH0_HSIZE[8:6]		
5x22	MTX_CH0_HSIZE	MTX_CH0_HSIZE[5:0] (For 64Bits 4 Pixels unit)						1'b0	1'b0
5x23	MTX_CH0_VSIZE						MTX_CH0_VSIZE[11:8]		
5x24	MTX_CH0_VSIZE	MTX_CH0_VSIZE[7:0]							
5x25	CH0_FS_OS_H			CH0_FS_OS[13:8]					
5x26	CH0_FS_OS_L	CH0_FS_OS[7:0]							
5x27	CH0_FE_OS_H			CH0_FE_OS[13:8]					
5x28	CH0_FE_OS_L	CH0_FE_OS[7:0]							
5x29	REF_CH0_VS_OS	REF_CH0_VS_VOS		REF_CH0_VS_HOS[13:8]					
5x2A	REF_CH0_VS_OS	REF_CH0_VS_HOS[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
5x2B~5x2F	RESERVED	RESERVED							
5x30	MTX_CH1_CTRL	MTX_CH1_EN	CH1_VBLK_MD	MTX_CH1_SEL		MTX_CH1_BUF_SIZE			
5x31	MTX_CH1_HSIZE	CH1_DATA_BLK	CH1_ID_BLK	CH1_INFO		CH1_INT_MD	MTX_CH1_HSIZE[8:6]		
5x32	MTX_CH1_HSIZE	MTX_CH1_HSIZE[5:0] (For 64Bits 4 Pixels unit)						1'b0	1'b0
5x33	MTX_CH1_VSIZE						MTX_CH1_VSIZE[11:8]		
5x34	MTX_CH1_VSIZE	MTX_CH1_VSIZE[7:0]							
5x35	CH1_FS_OS_H			CH1_FS_OS[13:8]					
5x36	CH1_FS_OS_L	CH1_FS_OS[7:0]							
5x37	CH1_FE_OS_H			CH1_FE_OS[13:8]					
5x38	CH1_FE_OS_L	CH1_FE_OS[7:0]							
5x39	REF_CH1_VS_OS	REF_CH1_VS_VOS		REF_CH1_VS_HOS[13:8]					
5x3A	REF_CH1_VS_OS	REF_CH1_VS_HOS[7:0]							
5x3B~5x3F	RESERVED	RESERVED							
5x40	MTX_CH2_CTRL	MTX_CH2_EN	CH2_VBLK_MD	MTX_CH2_SEL		MTX_CH2_BUF_SIZE			
5x41	MTX_CH2_HSIZE	CH2_DATA_BLK	CH2_ID_BLK	CH2_INFO		CH2_INT_MD	MTX_CH2_HSIZE[8:6]		
5x42	MTX_CH2_HSIZE	MTX_CH2_HSIZE[5:0] (For 64Bits 4 Pixels unit)						1'b0	1'b0
5x43	MTX_CH2_VSIZE						MTX_CH2_VSIZE[11:8]		
5x44	MTX_CH2_VSIZE	MTX_CH2_VSIZE[7:0]							
5x45	CH2_FS_OS_H			CH2_FS_OS[13:8]					
5x46	CH2_FS_OS_L	CH2_FS_OS[7:0]							
5x47	CH2_FE_OS_H			CH2_FE_OS[13:8]					

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
5x48	CH2_FE_OS_L	CH2_FE_OS[7:0]							
5x49	REF_CH2_VS_OS	REF_CH2_VS_VOS		REF_CH2_VS_HOS[13:8]					
5x4A	REF_CH2_VS_OS	REF_CH2_VS_HOS[7:0]							
5x4B~5x4F	RESERVED	RESERVED							
5x50	MTX_CH3_CTRL	MTX_CH3_EN	CH3_VBLK_MD	MTX_CH3_SEL		MTX_CH3_BUF_SIZE			
5x51	MTX_CH3_HSIZE	CH3_DATA_BLK	CH3_ID_BLK	CH3_INFO		CH3_INT_MD	MTX_CH3_HSIZE[8:6]		
5x52	MTX_CH3_HSIZE	MTX_CH3_HSIZE[5:0] (For 64Bits 4 Pixels unit)						1'b0	1'b0
5x53	MTX_CH3_VSIZE						MTX_CH3_VSIZE[11:8]		
5x54	MTX_CH3_VSIZE	MTX_CH3_VSIZE[7:0]							
5x55	CH3_FS_OS_H			CH3_FS_OS[13:8]					
5x56	CH3_FS_OS_L	CH3_FS_OS[7:0]							
5x57	CH3_FE_OS_H			CH3_FE_OS[13:8]					
5x58	CH3_FE_OS_L	CH3_FE_OS[7:0]							
5x59	REF_CH3_VS_OS	REF_CH3_VS_VOS		REF_CH3_VS_HOS[13:8]					
5x5A	REF_CH3_VS_OS	REF_CH3_VS_HOS[7:0]							
5x5B~5x5F	RESERVED	RESERVED							
5x60	CH0_HWIDTH			CH0_HWIDTH[13:08]					
5x61	CH0_HWIDTH	CH0_HWIDTH[7:0]							
5x62	CH1_HWIDTH			CH1_HWIDTH[13:08]					
5x63	CH1_HWIDTH	CH1_HWIDTH[7:0]							
5x64	CH2_HWIDTH			CH2_HWIDTH[13:08]					

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
5x65	CH2_HWIDTH	CH2_HWIDTH[7:0]							
5x66	CH3_HWIDTH			CH3_HWIDTH[13:08]					
5x67	CH3_HWIDTH	CH3_HWIDTH[7:0]							
5x68	CH0_VRATE	CH0_VRATE[15:08]							
5x69	CH0_VRATE	CH0_VRATE[7:0]							
5x6A	CH1_VRATE	CH1_VRATE[15:08]							
5x6B	CH1_VRATE	CH1_VRATE[7:0]							
5x6C	CH2_VRATE	CH2_VRATE[15:08]							
5x6D	CH2_VRATE	CH2_VRATE[7:0]							
5x6E	CH3_VRATE	CH3_VRATE[15:08]							
5x6F	CH3_VRATE	CH3_VRATE[7:0]							
5x70~5xFE	RESERVED	RESERVED							

3.1.5. Page 6 (MIPI D-PHY Control)

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
6x00~6x03	RESERVED	RESERVED							
6x04	MIPI_CONTROL_0		MIPI_EN	MIPI_DPHY_PD	CLK_HS_MODE	MIPI_ULP_DATA	MIPI_ULP_CLK		MIPI_STM
6x05	MIPI_CONTROL_1	MIPI_CK_CONTROL[3:0]							
6x06	MIPI_CONTROL_2	MIPI_D0_CONTROL[3:0]				MPI_D1_CONTROL[3:0]			
6x07	MIPI_CONTROL_3	MIPI_D2_CONTROL[3:0]				MPI_D3_CONTROL[3:0]			
6x08	MIPI_CONTROL_4					MIPI_LANE[1:0]			
6x09	MIPI_CONTROL_5	D0_LANE_SWAP[1:0]		D1_LANE_SWAP[1:0]		D2_LANE_SWAP[1:0]		D3_LANE_SWAP[1:0]	
6x0A	RESERVED	RESERVED							
6x0B	MIPI_CONTROL_7	D0_NP_SWAP	D1_NP_SWAP	D2_NP_SWAP	D3_NP_SWAP	MIPI_CK_NP_SWAP			
6x0C~6x0D	RESERVED	RESERVED							
6x0E	DPHY_BIAS_0						DPHY_ISEL[2:0]		
6x0F ~ 6x1B	RESERVED	RESERVED							
6x1C	MIPI_T_LPX	MIPI_T_LPX[7:0]							
6x1D	MIPI_T_CLK_PREPARE	MIPI_T_CLK_PREPARE[7:0]							
6x1E	MIPI_T_HS_PREPARE	MIPI_T_HS_PREPARE[7:0]							
6x1F	MIPI_T_HS_ZERO	MIPI_T_HS_ZERO[7:0]							
6x20	MIPI_T_HS_TRAIL	MIPI_T_HS_TRAIL[7:0]							
6x21	MIPI_T_CLK_ZERO	MIPI_T_CLK_ZERO[7:0]							
6x22	MIPI_T_CLK_TRAIL	MIPI_T_CLK_TRAIL[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
6x23	MIPI_T_CLK_PRE	MIPI_T_CLK_PRE[7:0]							
6x24	MIPI_T_CLK_POST	MIPI_T_CLK_POST[7:0]							
6x25	MIPI_T_WAKEUP	MIPI_T_WAKEUP[7:0]							
6x26	MIPI_T_HSEXIT	MIPI_T_HSEXIT[7:0]							
6x27	MIPI_T_CLK_HSEXIT	MIPI_T_CLK_HSEXIT[7:0]							
6x28	MIPI_ESC_CMD	MIPI_ESC_CMD[7:0]							
6x29 ~ 6x35	RESERVED	RESERVED							
6x36	MIPI_PKT_SIZE0_H	MIPI_PKT_SIZE0_H[7:0]							
6x37	MIPI_PKT_SIZE0_L	MIPI_PKT_SIZE0_L[7:0]							
6x38	MIPI_PKT_SIZE1_H	MIPI_PKT_SIZE1_H[7:0]							
6x39	MIPI_PKT_SIZE1_L	MIPI_PKT_SIZE1_L[7:0]							
6x3A	MIPI_PKT_SIZE2_H	MIPI_PKT_SIZE2_H[7:0]							
6x3B	MIPI_PKT_SIZE2_L	MIPI_PKT_SIZE2_L[7:0]							
6x3C	MIPI_PKT_SIZE3_H	MIPI_PKT_SIZE3_H[7:0]							
6x3D	MIPI_PKT_SIZE3_L	MIPI_PKT_SIZE3_L[7:0]							
6x3E ~ 6x45	RESERVED	RESERVED							
6x46	MIPI_DATA_ID0	MIPI_DATA_ID0[7:0]							
6x47	MIPI_DATA_ID1	MIPI_DATA_ID1[7:0]							
6x48	MIPI_DATA_ID2	MIPI_DATA_ID2[7:0]							
6x49	MIPI_DATA_ID3	MIPI_DATA_ID3[7:0]							

3.2. Register Description

3.2.1. Page 0 Register

Addr	Name	R/W	Bit	Descriptions	Default
0x00 0x20	DET_IFMT_STD	R	[7:6]	Status Information of Detected Video Input Standard 0 : HD-PVI 1 : HD-CVI 2 : HDA 3 : HDT	2'h0
	DET_IFMT_REF	R	[5:4]	Status Information of Detected Video Input Refresh Rate 0 : 25Hz 1 : 30Hz 2 : 50Hz 3 : 60Hz	2'h0
	DET_VIDEO	R	[3]	Status Information of Video Detection 0 : Not Detected 1 : Detected	1'h0
	DET_IFMT_RES	R	[2:0]	Status Information of Detected Video Input Resolution 0 : SD 480i 1 : SD 576i 2 : HD720p 3 : HD1080p 4 : HD960p or HD800p	3'h0
0x01 0x21	LOCK_STD	R	[7]	Lock Status of Video Standard Detection 0 : Not Detected 1 : Detected	1'h0
	LOCK_GAIN	R	[6]	Lock Status of Gain Loop 0 : Not Locked 1 : Locked	1'h0
	LOCK_CLAMP	R	[5]	Lock Status of Clamp Loop 0 : Not Locked 1 : Locked	1'h0
	RESERVED	R	[4]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	LOCK_HPLL	R	[3]	Lock Status of Horizontal PLL Loop 0 : Not Locked 1 : Locked	1'h0
	LOCK_C_FINE	R	[2]	Fine Lock Status of Chroma Phase Tracking Loop 0 : Not Locked 1 : Locked	1'h0
	LOCK_CHROMA	R	[1]	Coarse Lock Status of Chroma Phase Tracking Loop 0 : Not Locked 1 : Locked	1'h0
	DET_CHROMA	R	[0]	Status of Chroma Detection 0 : Not Detected 1 : Detected	1'h0
0x10 0x30	MAN_IFMT_STD	R/W	[7:6]	Set the Video Input Standard 0 : HD-PVI 1 : HD-CVI 2 : HDA 3 : HDT	2'h0
	MAN_IFMT_REF	R/W	[5:4]	Set the Video Input Refresh Rate 0 : 25Hz 1 : 30Hz 2 : 50Hz 3 : 60Hz	2'h0
	MAN_IFMT_STD_HDT_N	R/W	[3]	Set the Video Input Standard of HDT 0 : Old HDT 1 : New HDT	1'h0
	MAN_IFMT_RES	R/W	[2:0]	Set the Video Input Resolution 0 : SD 480i 1 : SD 576i 2 : HD720p 3 : HD1080p	2'h0
0x11	RESERVED	R/W	[7]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
0x31	VADC_GAIN_SEL	R/W	[6:4]	Set the Video ADC Input Gain 0 : x 1 1 : x 1.28 2 : x 1.57 3 : x 1.85 4 : x 2.15 5 : x 2.42 6 : x 2.71 7 : x 3	3'h0
	MAN_IFMT_EN	R/W	[3:0]	Set the Video Input Format Manually with MAN_IFMT_STD, MAN_IFMT_REF and MAN_IFMT_RES [2] : Force the Video Input Standard with MAN_IFMT_STD [1] : Force the Video Input Refresh Rate with MAN_IFMT_REF [0] : Force the Video Input Resolution with MAN_IFMT_RES	4'h0
0x12	MAIN_EQ_ GAIN_MD	R/W	[4:0]	Select the EQ Global Gain 0 : No Gain ~ 16 : Middle Gain ~ 31 : High Gain	5'h0
0x13	VADC_EQ_LOW_ BAND	R/W	[5:4]	Select the EQ Low Bandwidth Gain 0 : No Gain 1 : Low Gain 2 : Middle Gain 3 : High Gain	2'h0
	VADC_EQ_HIGH_ BAND	R/W	[2:0]	Select the EQ High Bandwidth Gain 0 : No Gain 1 : Low Gain 2~6 : Middle Gain 7 : High Gain	3'h0
0x14	RESERVED	R/W	[7:2]	Reserved	6'h0

Addr	Name	R/W	Bit	Descriptions	Default
	VADC_IN_SEL	R/W	[1:0]	Select the Video Input 0 : Differential Input Mode 1 : Single Input Mode with VINP0/1 2 : Single Input Mode with VINP0/1 3 : Single Input Mode with VINN0/1	
0x70	DUMMY_RW_REG0	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x71	DUMMY_RW_REG1	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x72	DUMMY_RW_REG2	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x73	DUMMY_RW_REG3	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x74	DUMMY_RW_REG4	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x75	DUMMY_RW_REG5	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x76	DUMMY_RW_REG6	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x77	DUMMY_RW_REG7	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x80	IRQOUT_EN	R/W	[7:6]	Select the Interrupt Output Mode 0 : Disable 1 : Output Mode 2/3 : Pull-up / Pull Down Mode	1'h0
	IRQOUT_POL	R/W	[5]	Select the Output Polarity for interrupt 0 : Bypass / Pull-Up Mode 1 : Inversion / Pull-Down Mode	1'h0
	IRQOUT_RPT	R/W	[4]	Enable the Repeat Mode of IRQ 0 : Bypass 1 : Enable the Repeat Mode of IRQ	1'h0
	SYNC_GPIO	R/W	[2]	Enable the Synchronized Interrupt with Synchronization Period SYNC_GPIO : For GPIO[11:0] Interrupt SYNC_FUNC : For VFD/NOVID Interrupt SYNC_PTZ : For PTZ Detection Interrupt	1'h0
	SYNC_FUNC	R/W	[1]		1'h0
	SYNC_PTZ	R/W	[0]		1'h0
0x81	IRQ_SYNC_PERIOD	R/W	[7:0]	Select the Interrupt Synchronization Reference Period Synchronization Period = (IRQ_SYNC_PERIOD + 1) * 20msec Period	8'h00
0x82	IRQ_TIMER0_ PERIOD	R/W	[7:0]	Select the Interrupt Wake-up Timer 0 Reference Period Timer Period = (IRQ_WAKE_PERIOD + 1) * Synchronization Period	8'h00
0x83	STATE_TIMER	R	[5]	Pending Status for Interrupt IRQSTATE_TIMER : For Timer0/1 Interrupt IRQSTATE_GPIO : For GPIO[11:0] Interrupt	1'b0
	STATE_GPIO	R	[4]		1'b0
	STATE_VFD	R	[3]		1'b0

Addr	Name	R/W	Bit	Descriptions	Default
	STATE_NOVID	R	[2]	IRQSTATE_VFD : For Video Format detection interrupt	1'b0
	STATE_PTZ1	R	[1]	IRQSTATE_NOVID : For NOVID detection interrupt	1'b0
	STATE_PTZ0	R	[0]	IRQSTATE_PTZ : For PTZ detection interrupt 0 : No Pending 1 : Pending	1'b0
0x84	SYNC_VFD_PEND	R/W	[7]	Select the Interrupt Mode for Video Format Detection 0 : Maintain New Event at Synchronized Mode 1 : Clear New Event by Interrupt Clear at Synchronized Mode	1'b0
	SYNC_NOVID_PEND	R/W	[6]	Select the Interrupt Mode for No Video Detection 0 : Maintain New Event at Synchronized Mode 1 : Clear New Event by Interrupt Clear at Synchronized Mode	1'b0
	IRQ_VFD_MD	R/W	[5]	Select the Interrupt Mode for Video Format Detection 0 : Edge Interrupt (Interrupt when Video format status is changed) 1 : Level Interrupt (Interrupt when Video format status is different from IRQ_VFD_LV	1'h0
	IRQ_NOVID_MD	R/W	[4]	Select the Interrupt Mode for Novideo Detection 0 : Edge Interrupt (Interrupt when Novideo status changed) 1 : Level Interrupt (Interrupt when Novideo status different with IRQ_NOVID_LV	1'h0
	IRQ_GPIO_MD	R/W	[3:0]	Select the Interrupt Mode for GPIO[11:0] 0 : Edge Interrupt 1 : Level Interrupt	12'h00
0x85		R/W	[7:0]		
0x86	IRQ_GPIO_LV	R/W	[3:0]	Select the Interrupt Mode for GPIO [11:0] @ IRQ_GPIO_MD = 0 & GPIO_BOTH = 0 0 : Falling Edge Interrupt 1 : Rising Edge Interrupt @ IRQ_GPIO_MD = 1 0 : Low Level Interrupt 1 : High Level Interrupt	12'h0
0x87		R/W	[7:0]		
0x88	IRQ_GPIO_BOTH	R/W	[3:0]	Select the Interrupt Mode for GPIO[11:0] @IRQ_GPIO_MD = 0 0 : Interrupt by IRQ_GPIO_LV 1 : Interrupt by Rising or Falling Edge	12'h0
0x89		R/W	[7:0]		
0x8A	IRQ_TIMER1_ PERIOD	R/W	[7:0]	Select the Interrupt Wake-up Timer1 Reference Period Timer Period = (IRQ_WAKE_PERIOD + 1) * Synchronization Period	8'h0

Addr	Name	R/W	Bit	Descriptions	Default
0x90	IRQENA_TIMER1	R/W	[7]	Enable the interrupt of Timer 1 0 : Disable 1 : Enable	1'h0
	IRQENA_TIMER0	R/W	[6]	Enable the interrupt of Timer 0 0 : Disable 1 : Enable	1'h0
	IRQENA_GPIO	R/W	[3:0]	Enable the Interrupt of GPIO[11:0] 0 : Disable 1 : Enable	12'h0
0x91		R/W	[7:0]		
0x92	Reserved	R/W	[7:0]	Reserved to 8'h0	8'h0
0x93	Reserved	R/W	[7:0]	Reserved to 8'h0	8'h0
0x94	IRQCLR_TIMER1	R/W	[7]	Clear the interrupt of Timer 1 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0
	IRQCLR_TIMER0	R/W	[6]	Clear the interrupt of Timer 0 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0
	IRQCLR_GPIO	R/W	[3:0]	Clear the Interrupt of GPIO[11:0] 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	12'h0
0x95		R/W	[7:0]		
0x98	STATUS_TIMER1	R/W	[7]	Status of the Interrupt for Timer 1 0 : Low 1 : High	1'b0
	STATUS_TIMER0	R/W	[6]	Status of the Interrupt for Timer 0 0 : Low 1 : High	1'b0
	STATUS_GPIO	R	[3:0]	Status of the Interrupt for GPIO[11:0] 0 : Low 1 : High	12'h0
0x99		R/W	[7:0]		
0xA0	IRQ_CC_ NOVID_LV2	R/W	[6]	Select the Interrupt Mode of No-video Detection for Cascade CH 2 0 : Low Level Interrupt (Normal) 1 : High Level Interrupt (Video Loss)	1'h0
	IRQ_VFD_LV0	R/W	[5]	Select the Interrupt Mode of Video Format Detection for CH 0 0 : Low Level Interrupt 1 : High Level Interrupt	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	IRQ_NOVID_LV0	R/W	[4]	Select the Interrupt Mode of No-video Detection for CH 0 0 : Low Level Interrupt (Normal) 1 : High Level Interrupt (Video Loss)	1'h0
	Reserved	R/W	[3]	Reserved	1'h0
	IRQENA_CC_ NOVID2	R/W	[2]	Enable the Interrupt of No-video Detection for Cascade CH 2 0 : Disable 1 : Enable	1'h0
	IRQENA_VFD0	R/W	[1]	Enable the Interrupt of Video Format Detection for CH 0 0 : Disable 1 : Enable	1'h0
	IRQENA_NOVID0	R/W	[0]	Enable the Interrupt of No-video Detection for CH 0 0 : Disable 1 : Enable	1'h0
0xA1	IRQENA_PTZ0	R/W	[7:0]	Enable the Interrupt of PTZ Detection for CH 0 PTZ[7] for PTZ Rx Data Error Detection PTZ[6] for PTZ Rx Sync Error Detection PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection PTZ[3] for PTZ Rx Done Detection PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection PTZ[0] for Tx Data Done Detection 0 : Disable 1 : Enable	8'h0
0xA2	IRQCLR_CC_ NOVID2	R/W	[2]	Clear the Interrupt of No-video Detection for Cascade CH 2 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0
	IRQCLR_VFD0	R/W	[1]	Clear the Interrupt of Video Format Detection for CH 0 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0
	IRQCLR_NOVID0	R/W	[0]	Clear the Interrupt of No-video Detection for CH 0 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xA3	IRQCLR_PTZ0	R/W	[7:0]	Clear the Interrupt of PTZ Detection for CH 0 PTZ[7] for PTZ Rx Data Error Detection PTZ[6] for PTZ Rx Sync Error Detection PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection PTZ[3] for PTZ Rx Done Detection PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection PTZ[0] for Tx Data Done Detection 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	8’h0
0xA4	STATUS_CC_ NOVID2	R	[2]	Status of the Interrupt for No-video Detection for Cascade CH 2 0 : Video 1 : No-video Detect	1’h0
	STATUS_VFD0	R	[1]	Status of the Interrupt for Video Format Detection for CH 0 0 : No Video Format Change 1 : Detection of the Video Format Change	1’h0
	STATUS_NOVID0	R	[0]	Status of the Interrupt for No-video Detection for CH 0 0 : Video 1 : No-video Detect	1’h0

Addr	Name	R/W	Bit	Descriptions	Default
0xA5	STATUS_PTZ0	R	[7:0]	Status of the Interrupt for PTZ Detection for CH 0 PTZ[7] for PTZ Rx Data Error Detection 0 : No Error 1 : Error PTZ[6] for PTZ Rx Sync Error Detection 0 : No Error 1 : Error PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection 0 : No Error 1 : Error PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection 0 : No Error 1 : Error PTZ[3] for PTZ Rx Done Detection 0 : Idle 1 : Busy PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection 0 : No Error 1 : Error PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection 0 : No Error 1 : Error PTZ[0] for Tx Data Done Detection 0 : Idle 1 : Busy	8'h0
0xB0	IRQ_CC_ NOVID_LV3	R/W	[6]	Select the Interrupt Mode of No-video Detection for Cascade CH 3 0 : Low Level Interrupt (Normal) 1 : High Level Interrupt (Video Loss)	1'h0
	IRQ_VFD_LV1	R/W	[5]	Select the Interrupt Mode of Video Format Detection for CH 1 0 : Low Level Interrupt 1 : High Level Interrupt	1'h0
	IRQ_NOVID_LV1	R/W	[4]	Select the Interrupt Mode of No-video Detection for CH 1 0 : Low Level Interrupt (Normal) 1 : High Level Interrupt (Video Loss)	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	IRQENA_CC_ NOVID3	R/W	[2]	Enable the Interrupt of No-video Detection for Cascade CH 3 0 : Disable 1 : Enable	1'h0
	IRQENA_VFD1	R/W	[1]	Enable the Interrupt of Video Format Detection for CH 1 0 : Disable 1 : Enable	1'h0
	IRQENA_NOVID1	R/W	[0]	Enable the Interrupt of No-video Detection for CH 1 0 : Disable 1 : Enable	1'h0
0xB1	IRQENA_PTZ1	R/W	[7:0]	Enable the Interrupt of PTZ Detection for CH 1 PTZ[7] for PTZ Rx Data Error Detection PTZ[6] for PTZ Rx Sync Error Detection PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection PTZ[3] for PTZ Rx Done Detection PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection PTZ[0] for Tx Data Done Detection 0 : Disable 1 : Enable	8'h0
0xB2	IRQCLR_CC_ NOVID3	R/W	[2]	Clear the Interrupt of No-video Detection for Cascade CH 3 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0
	IRQCLR_VFD1	R/W	[1]	Clear the Interrupt of Video Format Detection for CH 1 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0
	IRQCLR_NOVID1	R/W	[0]	Clear the Interrupt of No-video Detection for CH 1 0 : Done 1 : Clear (After Writing "1", the interrupt will be cleared)	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xB3	IRQCLR_PTZ1	R/W	[7:0]	Clear the Interrupt of PTZ Detection for CH 1 PTZ[7] for PTZ Rx Data Error Detection PTZ[6] for PTZ Rx Sync Error Detection PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection PTZ[3] for PTZ Rx Done Detection PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection PTZ[0] for Tx Data Done Detection 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	8’h0
0xB4	STATUS_CC_ NOVID3	R	[2]	Status of the Interrupt for No-video Detection for Cascade CH 3 0 : Video 1 : No-video Detect	1’h0
	STATUS_VFD1	R	[1]	Status of the Interrupt for Video Format Detection for CH 1 0 : No Video Format Change 1 : Detection of the Video Format Change	1’h0
	STATUS_NOVID1	R	[0]	Status of the Interrupt for No-video Detection for CH 1 0 : Video 1 : No-video Detect	1’h0

Addr	Name	R/W	Bit	Descriptions	Default
0xB5	STATUS_PTZ1	R	[7:0]	Status of the Interrupt for PTZ Detection for CH 1 PTZ[7] for PTZ Rx Data Error Detection 0 : No Error 1 : Error PTZ[6] for PTZ Rx Sync Error Detection 0 : No Error 1 : Error PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection 0 : No Error 1 : Error PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection 0 : No Error 1 : Error PTZ[3] for PTZ Rx Done Detection 0 : Idle 1 : Busy PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection 0 : No Error 1 : Error PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection 0 : No Error 1 : Error PTZ[0] for Tx Data Done Detection 0 : Idle 1 : Busy	8'h0
0xC0 0xC1 0xC2	MPP_POL	R/W	[7]	Select the Polarity of MPP[11:0] Output 0 : Normal Output 1 : Inverted Output	1'h0
0xC3 0xC4 0xC5	MPP_CH	R/W	[6]	Select the Channel of MPP[11:0] Output 0 : CH0 1 : CH1	1'h0
0xC6 0xC7 0xC8	MPP_IOB	R/W	[5]	Select the Input/Output Mode of MPP[11:0] 0 : Output 1 : Input	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xC9 0xCA 0xCB	GPIO_OUT	R/W	[4]	Select the Output Value of GPIO[11:0] when MPP_SEL = 0 0 : Low (“0”) Output 1 : High (“1”) Outupt	1’h0
	MPP_MD	R/W	[3]	Select the Sync Type for MPP[11:0] when MPP_SEL=2 0 : H Sync Output 1 : V Sync Output	1’h0
	MPP_SEL	R/W	[2:0]	Select the Mode for MPP[11:0] Pin 0 : GPIO Mode for MPP[11:0] 1 : Cascaded Video Input Mode for MPP[8:0] (CLK:MPP[4]) IRQ Output for MPP[9] PTZ Output for MPP[11:10] 2 : Video Sync Output Mode for MPP[11:0] 3 : Reserved 4 : Video Data Output Mode for MPP[8:0] (CLK : MPP[4]) 5~7 : Reserved	2’h0
0xD0	PLL0_PD	R/W	[7]	Select the Power Down for PLL0 0 : Normal Operation 1 : Power Down Mode	1’b1
	RESERVED	R/W	[6:0]	Reserved	7’h6
0xD1	RESERVED	R/W	[7:3]	Reserved	5’h4
	PLL0_REF_CNT	R/W	[2:0]	PLL0 Reference Frequency Counter (Default : 3’h3 : 297MHz)	3’h3
0xD2	RESERVED	R/W	[7]	Reserved	1’h0
	PLL0_MAIN_CNT	R/W	[6:0]	PLL0 N-Divider Counter Output Frequency = 27MHz * PLL0_MAIN_CNT/PLL0_REF_CNT (Default : 7’h21 : 297MHz)	7’h21
0xD3	RESERVED	R/W	[7:0]	Reserved	8’h0
0xD4	PLL1_PD	R/W	[7]	Select the Power Down for PLL1 0 : Normal Operation 1 : Power Down Mode	1’b1
	RESERVED	R/W	[6:0]	Reserved	7’h6
0xD5	RESERVED	R/W	[7:3]	Reserved	5’h4
	PLL1_REF_CNT	R/W	[2:0]	PLL1 Reference Frequency Counter (Default : 3’h3 : 297MHz)	3’h3
0xD6	RESERVED	R/W	[7]	Reserved	1’h0

Addr	Name	R/W	Bit	Descriptions	Default
	PLL1_MAIN_CNT	R/W	[6:0]	PLL1 N-Divider Counter Output Frequency = 27MHz * PLL1_MAIN_CNT/PLL1_REF_CNT (Default : 7'h21 : 297MHz)	7'h21
0xD7	RESERVED	R/W	[7]	Reserved	1'h0
	PLL1_8PH_SEL_2	R/W	[6:4]	Control the Phase Delay of VDCK1 Pin 0 : 0/8 Phase 1 : 1/8 Phase 2 : 2/8 Phase 3 : 3/8 Phase 4 : 4/8 Phase 5 : 5/8 Phase 6 : 5/8 Phase 7 : 7/8 Phase	3'h4
	RESERVED	R/W	[3]	Reserved	1'h0
	PLL1_8PH_SEL_1	R/W	[2:0]	Control the Phase Delay of VDCK0 Pin 0 : 0/8 Phase 1 : 1/8 Phase 2 : 2/8 Phase 3 : 3/8 Phase 4 : 4/8 Phase 5 : 5/8 Phase 6 : 5/8 Phase 7 : 7/8 Phase	3'h4
0xD8	PLL2_PD	R/W	[7]	Select the Power Down for PLL2 0 : Normal Operation 1 : Power Down Mode	1'b1
	RESERVED	R/W	[6]	Reserved	3'h0
	BGR_PD	R/W	[5]	Select the Power Down for BGR of PLL0~2 0 : Normal Operation 1 : Power Down Mode	1'b1
	RESERVED	R/W	[4:0]	Reserved	5'h6
0xD9	RESERVED	R/W	[7:3]	Reserved	5'h4
	PLL2_REF_CNT	R/W	[2:0]	PLL2 Reference Frequency Counter (Default : 3'h3 : 297MHz)	3'h3
0xDA	RESERVED	R/W	[7]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	PLL2_MAIN_CNT	R/W	[6:0]	PLL2 N-Divider Counter Output Frequency = 27MHz * PLL2_MAIN_CNT/PLL2_REF_CNT (Default : 7'h21 : 297MHz)	7'h21
0xE2	RESERVED	R/W	[7:5]	Reserved	3'h0
	CKOUT_2X_MD	R/W	[4]	Select the VD Data Output Mode 0 :SDR (Single Data Rate) Output Mode 1 : DDR (Dual Data Rate) Output Mode	1'h0
	CH_MUX_MD	R/W	[3:2]	Select the Channel Multiplexing Mode 0 : 1CH Output Mode 1 : 2CH Multiplexing Output Mode 2,3 : 4CH Multiplexing Output Mode	2'h0
	OUTFMT_RATE	R/W	[1:0]	Select the Video Data Output Rate for One Channel 0 : 148.5MHz Data Rate for 8bit Data Interface 1 : 74.25MHz Data Rate for 8bit Data Interface 2 : 36MHz Data Rate for 8bit Data Interface 3 : 27MHz Data Rate for 8bit Data Interface	2'h0
0xE3	OUTFMT_YC_INV	R/W	[7:6]	Select the VD Data Output Sequence 0 : Cb-Y-Cr-Y 1 : Y-Cb-Y-Cr	1'h0
	RESERVED	R/W	[5:4]	Reserved	2'h0
	CHID_NUM1	R/W	[3:2]	Select the CHID Number for Video CH1 0 : CHID #0 1 : CHID #1 2 : CHID #2 3 : CHID #3	2'h0
	CHID_NUM0	R/W	[1:0]	Select the CHID Number for Video CH0 0 : CHID #0 1 : CHID #1 2 : CHID #2 3 : CHID #3	2'h0
0xE4	RESERVED	R/W	[7]	Reserved	1'h0

<table>
<tr><th>Addr</th><th>Name</th><th>R/W</th><th>Bit</th><th>Descriptions</th><th>Default</th></tr>
<tr><td rowspan="3">0xE6</td><td>CH_SEL_B</td><td>R/W</td><td>[6:4]</td><td>Select the Channel on 2nd Data for VD0/1 Pin
<table><tr><th>Value</th><th>CH#</th></tr><tr><td>0</td><td>Y of CH0</td></tr><tr><td>1</td><td>C of CH0</td></tr><tr><td>2</td><td>Y of CH1</td></tr><tr><td>3</td><td>C of CH1</td></tr><tr><td>4</td><td>Y of CH2</td></tr><tr><td>5</td><td>C of CH2</td></tr><tr><td>6</td><td>Y of CH3</td></tr><tr><td>7</td><td>C of CH3</td></tr></table></td><td>3’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[3]</td><td>Reserved</td><td>1’h0</td></tr>
<tr><td>CH_SEL_A</td><td>R/W</td><td>[2:0]</td><td>Select the Channel on 1st Data for VD0/1 Pin
(Same as the Above CH_SEL_B Control)</td><td>3’h0</td></tr>
<tr><td rowspan="4">0xE5
0xE7</td><td>RESERVED</td><td>R/W</td><td>[7]</td><td>Reserved</td><td>1’h0</td></tr>
<tr><td>CH_SEL_D</td><td>R/W</td><td>[6:4]</td><td>Select the Channel on 4th Data for VD0/1 Pin
<table><tr><th>Value</th><th>CH#</th></tr><tr><td>0</td><td>Y of CH0</td></tr><tr><td>1</td><td>C of CH0</td></tr><tr><td>2</td><td>Y of CH1</td></tr><tr><td>3</td><td>C of CH1</td></tr><tr><td>4</td><td>Y of CH2</td></tr><tr><td>5</td><td>C of CH2</td></tr><tr><td>6</td><td>Y of CH3</td></tr><tr><td>7</td><td>C of CH3</td></tr></table></td><td>3’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[3]</td><td>Reserved</td><td>1’h0</td></tr>
<tr><td>CH_SEL_C</td><td>R/W</td><td>[2:0]</td><td>Select the Channel on 3rd Data for VD0/1 Pin
(Same as the Above CH_SEL_D Control)</td><td>3’h0</td></tr>
</table>

Addr	Name	R/W	Bit	Descriptions	Default
0xE8	VDCK0_PHASE	R/W	[5:0]	Select the Frequency and Phase Mode for VDCK0 [5] : 0 -> Multi-phase Clock Output Mode 1 -> No Multi-Phase Clock Mode [4] : 0 -> 148.5MHz Clock Mode 1 -> 74.25/37.125MHz Clock Mode [3] : When 148.5MHz Mode (0 -> Normal Clock, 1 -> Inverted Clock) When 74.25/37125MHz Mode (0 -> 148.5MHz Clk Latch, 1 -> Inverted 148.5MHz Clk Latch) [2] : 0 -> 74.25MHz Clock Mode 1 -> 37.125MHz Clock Mode [1:0]: When 74.25Mhz Mode (0,2 -> Normal Clock, 1,3 -> Inverted Clock) When 37.125MHz Mode (0 -> 0°, 1 -> 90°, 2 -> 180°, 3 -> 270° Phase)	6'h0
0xE9	VDCK1_PHASE	R/W	[5:0]	Select the Frequency and Phase Mode for VDCK1 (Same as the Above VDCK0_PHASE Control)	6'h0
0xEA	RESERVED	R/W	[7:5]	Reserved	3'h0
	MIPI_DCLK_PWDN	R/W	[4]	Power Down Mode for MIPI Controller Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	CC_CLK_PWDN	R/W	[3]	Power Down Mode for Cascaded Input Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	VOUT_CLK_PWDN	R/W	[2]	Power Down Mode for Video Output Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	VDEC_CLK_PWDN1	R/W	[1]	Power Down Mode for Video Decoder Clock for CH1 0 : Normal Operation 1 : Power Down Mode	1'h0
	VDEC_CLK_PWDN0	R/W	[0]	Power Down Mode for Video Decoder Clock for CH0 0 : Normal Operation 1 : Power Down Mode	1'h0
0xEB	RESERVED	R/W	[7:1]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	MIPI_DATA_EN	R/W	[0]	Enable MIPI Data Path 0 : Disable 1 : Enable	1'h0
0xF0	RESERVED	R/W	[7:2]	Reserved	6'h0
	VDCK_IOB	R/W	[0]	Select the Input/Output Mode of VDCK0 0 : Output 1 : Input	1'h0
0xF1	VD_IOB	R/W	[7:0]	Select the Input/Output Mode of VD[7:0] 0 : Output 1 : Input	8'h0
0xF2	SYS_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for TEST/RSTB/SCLK/SDAT Pin 0 : Normal Input 1 : Schmitt-trigger input	1'h0
	SYS_DRV_SEL	R/W	[1:0]	Select the Drive Strength for TEST/RSTB/SCLK/SDAT Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
0xF3	PTZ_SMT_EN	R/W	[6]	Select the Schmitt-trigger Input for MPP[11:10] Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	PTZ_DRV_SEL	R/W	[5:4]	Select the Drive Strength for MPP[11:10] Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
	MPP_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for MPP[9:0] Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	MPP_DRV_SEL	R/W	[1:0]	Select the Drive Strength for MPP[9:0] Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
0xF4	VD_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for VD[7:0] Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	VD_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_VD[7:0] Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
	VDCK_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for P_VDCK0/1 Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	VDCK_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_VDCK0/1 Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
0xFB	RESERVED	R	[7:1]	Reserved	7'h0
	OPT_ID	R	[0]	Chip Option ID 0 : PR2100 1 : PR2120	1'h0
0xFC	CHIP_ID[15:8]	R	[7:0]	MSB of CHIP ID Data (CHIP_ID[15:0] = 16'h2100)	8'h21
0xFD	CHIP_ID[7:0]	R	[7:0]	LSB of CHIP ID Data	8'h00
0xFE	REV_ID	R	[7:0]	Revision ID	8'h20
0xFF	ADDR_LATCH_EN	R/W	[7]	Enable the Latch of I2C Slave Address 0 : Done 1 : Enable the Latch of I2C Slave Address (Auto-cleared After Latch of I2C Slave Address)	1'h0
	HOST_RW_PAGE	R/W	[2:0]	Select the Page of Host Register Map 0 : Page 0 (Video EQ and MIPI and IRQ) 1 : Page 1 (Video Decoder for CH0) 2 : Page 2 (Video Decoder for CH1) 3 : Page 3 (PTZ Tx/Rx for CH0) 4 : Page 4 (PTZ Tx/Rx for CH1) 5 : Page 5 (MIPI Controller) 6 : Page 6 (MIPI D-PHY)	3'h0

3.2.2. Page 1, 2 Register

Addr	Name	R/W	Bit	Descriptions	Default
1x00 2x00	AGCEN	R/W	[7]	Enable the Automatic Gain Control (AGC) 0 : Disable 1 : Enable	1'h0
	AUTO_BGND	R/W	[6]	Enable the Automatic Background when No video is detected. Background Color is determined with BGND_MD[0] register. 0 : Disable 1 : Enable	1'h0
	PEAKEN	R/W	[5]	Enable the Automatic Peak Control 0 : Disable 1 : Enable	1'h0
	PEAKREF	R/W	[3:2]	Select the Automatic Peak Reference 0 : 100% White 1 : 110% White 2 : 120% White 3 : 130% White	2'h0
	BGND_MD	R/W	[1]	Control the Background Mode 0 : Normal Video Output 1 : Manual Background Mode	1'h0
			[0]	Control the Background Color 0 : Black Background 1 : Blue Background	1'h0
1x11 2x11	VDELAY[10:8]	R/W	[7:5]	MSB of the Vertical Starting Line (VDELAY[10:0])	3'h0
	HDELAY[12:8]	R/W	[4:0]	MSB of the Horizontal Starting Pixels (HDELAY[12:0])	5'h00
1x12 2x12	VACTIVE[10:8]	R/W	[7:5]	MSB of the Vertical Starting Line (VACTIVE[10:0])	3'h0
	HACTIVE[12:8]	R/W	[4:0]	MSB of the Horizontal Active Pixels (HACTIVE[12:0])	5'h00
1x13 2x13	HDELAY[7:0]	R/W	[7:0]	LSB of the Horizontal Starting Pixels (HDELAY[12:0]) : Unit 1 Pixel	8'h00
1x14 2x14	HACTIVE[7:0]	R/W	[7:0]	LSB of the Horizontal Active Pixels (HACTIVE[12:0]) : Unit 1 Pixel	8'h00
1x15 2x15	VDELAY[7:0]	R/W	[7:0]	LSB of the Vertical Starting Line (VDELAY[10:0]) : Unit 1 Line	8'h00

Addr	Name	R/W	Bit	Descriptions	Default
1x16 2x16	VACTIVE[7:0]	R/W	[7:0]	LSB of the Vertical Active Lines (VACTIVE[10:0]) : Unit 1 Line	8'h00
1x1D 2x1D	RESERVED	R/W	[7:5]	Reserved	3'h0
	HSCL_HACTIVE [12:8]	R/W	[4:0]	MSB of the Horizontal Active Pixels for Down Scaled Video Output (HSCL_HACTIVE[12:0])	5'h00
1x1F 2x1F	HSCL_HACTIVE [7:0]	R/W	[7:0]	LSB of the Horizontal Active Pixels for Down Scaled Video Output (HSCL_HACTIVE[12:0])	8'h00
1x20 2x20	CONT	R/W	[7:0]	Control the Contrast for Luminance 0 : Gain 0% ~ 128 : Gain 100% ~ 255 : Gain 200%	8'h00
1x21 2x21	BRGT	R/W	[7:0]	Control the Brightness for Luminance 0 : -100% ~ 128 : 0 ~ 255 : +100%	8'h00
1x22 2x22	SAT	R/W	[7:0]	Control the Saturation for Chrominance 0 : Gain 0% ~ 128 : Gain 100% ~ 255 : Gain 200%	8'h00
1x23 2x23	HUE	R/W	[7:0]	Control the Hue for Chrominance 0 : -180° ~ 128 : 0 ~ 255 : 180°	8'h00
1x29 2x29	DOWN_HSCL [15:8]	R/W	[7:0]	MSB of the Horizontal Down Scaling Ratio (DOWN_HSCL[15:0])	8'h00

<table>
<tr><th>Addr</th><th>Name</th><th>R/W</th><th>Bit</th><th>Descriptions</th><th>Default</th></tr>
<tr><td>1x2A
2x2A</td><td>DOWN_HSCL
[7:0]</td><td>R/W</td><td>[7:0]</td><td>LSB of the Horizontal Down Scaling Ratio (DOWN_HSCL[15:0])</td><td>8’h00</td></tr>
<tr><td rowspan="2">1x37
2x37</td><td>COMB_FLT_EN</td><td>R/W</td><td>[7]</td><td>Enable the Comb Filter
0 : Disable
1 : Enable</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[6:0]</td><td>Reserved</td><td>7’h0</td></tr>
<tr><td rowspan="6">1x39
2x39</td><td rowspan="2">MAN_NOVID</td><td rowspan="2">R/W</td><td>[7]</td><td>Control the No-Video Mode
0 : Auto No-Video Mode
1 : Manual No-Video Mode</td><td>1’h0</td></tr>
<tr><td>[6]</td><td>Select the Manual No-Video Status
0 : No-video Status
1 : Video Status</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[5]</td><td>Reserved</td><td>1’h0</td></tr>
<tr><td>HPEAK_MD</td><td>R/W</td><td>[4]</td><td>Control the Horizontal Peaking Frequency Band
0 : 10 ~ 20MHz
1 : 20 ~ 30MHz</td><td>1’h0</td></tr>
<tr><td>HPEAK_GAIN</td><td>R/W</td><td>[3:0]</td><td>Control the Horizontal Peaking Gain for Luminance
<table>
<tr><th>Value</th><th>Gain</th><th>Value</th><th>Gain</th></tr>
<tr><td>0</td><td>Off</td><td>8</td><td>50%</td></tr>
<tr><td>1</td><td>6.25%</td><td>9</td><td>56.25%</td></tr>
<tr><td>2</td><td>12.5%</td><td>10</td><td>62.5%</td></tr>
<tr><td>3</td><td>18.75%</td><td>11</td><td>68.75%</td></tr>
<tr><td>4</td><td>25%</td><td>12</td><td>75%</td></tr>
<tr><td>5</td><td>31.25%</td><td>13</td><td>81.25%</td></tr>
<tr><td>6</td><td>37.5%</td><td>14</td><td>87.5%</td></tr>
<tr><td>7</td><td>43.75%</td><td>15</td><td>93.75%</td></tr>
</table></td><td>4’h0</td></tr>
<tr><td rowspan="2">1x3A
2x3A</td><td>NR_EN</td><td>R/W</td><td>[7]</td><td>Enable the Noise Reduction
0 : Disable
1 : Enable</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[6:5]</td><td>Reserved</td><td>2’h0</td></tr>
</table>

Addr	Name	R/W	Bit	Descriptions	Default
	YLPF_MD	R/W	[4:0]	Control the Cut-off Frequency of Luminance LPF 0 : Bypass 1 : 37.125MHz 2 : 35MHz 3 : 32MHz 4 : 31MHz 5 : 28MHz 6 : 18MHz 7 : 15MHz 8 : 13MHz 9 : 12MHz 10 : 11MHz 11 : 9MHz 12 : 7MHz	5'h0
1x3D 2x3D	RESERVED	R/W	[7:6]	Reserved	2'h0
	CTI_CORE	R/W	[5:4]	Control the Coring Range for CTI 0 : No Coring 1 : +/- 2 2 : +/- 4 3 : +/- 8	2'h0
	C_CORE	R/W	[3:2]	Control the Coring Range for Chroma Output 0 : No Coring 1 : +/- 2 2 : +/- 4 3 : +/- 8	2'h0
	HPEAK_CORE	R/W	[1:0]	Control the Coring Range for Luminance Horizontal Peaking 0 : No Coring 1 : +/- 2 2 : +/- 4 3 : +/- 8	2'h0
1x3E 2x3E	MAN_CKIL	R/W	[7:6]	Control the Color Killing Mode Manually 0 ~ 1 : Auto Color Killing Mode 2 : Always Color Alive 3 : Always Color Killed	2'h0
	RESERVED	R/W	[5:4]	Reserved	2'h0

<table>
<tr><th>Addr</th><th>Name</th><th>R/W</th><th>Bit</th><th>Descriptions</th><th>Default</th></tr>
<tr><td></td><td>CLPF_MD</td><td>R/W</td><td>[3:0]</td><td>Control the Cut-off Frequency of Chrominance LPF
0 : Bypass
1 : 9MHz
2 : 8MHz
3 : 6MHz
4 : 5MHz
5 : 4MHz
6 : 3MHz
7 : 2.5MHz
8 : 2MHz</td><td>4’h0</td></tr>
<tr><td rowspan="4">1x3F
2x3F</td><td>CTI_MD</td><td>R/W</td><td>[4]</td><td>Control the CTI (Chroma Transient Improvement) Frequency Band
0 : 3 ~ 4MHz
1 : 1 ~ 2MHz</td><td>1’h0</td></tr>
<tr><td>CTI_GAIN</td><td>R/W</td><td>[3:0]</td><td>Control the CTI (Chroma Transient Improvement) Gain
<table>
<tr><th>Value</th><th>Gain</th><th>Value</th><th>Gain</th></tr>
<tr><td>0</td><td>Off</td><td>8</td><td>50%</td></tr>
<tr><td>1</td><td>6.25%</td><td>9</td><td>56.25%</td></tr>
<tr><td>2</td><td>12.5%</td><td>10</td><td>62.5%</td></tr>
<tr><td>3</td><td>18.75%</td><td>11</td><td>68.75%</td></tr>
<tr><td>4</td><td>25%</td><td>12</td><td>75%</td></tr>
<tr><td>5</td><td>31.25%</td><td>13</td><td>81.25%</td></tr>
<tr><td>6</td><td>37.5%</td><td>14</td><td>87.5%</td></tr>
<tr><td>7</td><td>43.75%</td><td>15</td><td>93.75%</td></tr>
</table></td><td>4’h0</td></tr>
<tr><td rowspan="2">1x40
2x40</td><td>PAL_COMP_EN</td><td>R/W</td><td>[7]</td><td>Enable the PAL Chroma Phase Alternating Compensation Mode
0 : Bypass
1 : PAL Phase Alternating Compensation Mode</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[6:0]</td><td>Reserved</td><td>7’h0</td></tr>
</table>

Addr	Name	R/W	Bit	Descriptions	Default
1x4D 2x4D	C_DELAY	R/W	[6:4]	Control the Chrominance Delay Compared to Luminance (2 Pixel Unit) 0 : No Delay ~ 3 : 6 CK Delay ~ 7 : 14CK Delay	3'h0
	Y_DELAY	R/W	[3:0]	Control the Luminance Delay Compared to Chrominance (1 Pixel Unit) 0 : No Delay ~ 8 : 8 CK Delay ~ 15 : 15CK Delay	4'h0
1x4E 2x4E	MAN_VIN_FMT	R/W	[7:4]	Select the Cascaded Input Pixel Number 0 ~ 7 : Auto Detection Mode 8 : 720 Pixel during H Active Period 9 : 960 Pixel during H Active Period 10 : 1280 Pixel during H Active Period 11 : 1920 Pixel during H Active Period	4'h0
	RESERVED	R/W	[3:2]	Reserved	2'h0
	SD_720H_MD	R/W	[1]	Select the Down Scaler Mode to Convert SD960H to SD 720H 0 : SD960H Mode for SD Video Input 1 : Convert SD960H to SD720H Mode	1'h0
	HD_HALF_MD	R/W	[0]	Select the Down Scaler Mode to Convert HD to HD CIF 0 : HD Full 1 : HD CIF	1'h0
1x4F 2x4F	BT1120_LIM	R/W	[7]	Select the Data Range of BT1120 Output 0 : 1 ~ 254 Data Range 1 : 16 ~ 240 Data Range	1'h0
	RESERVED	R/W	[6]	Reserved	1'h0
	VIN_BT656_MD	R/W	[5]	Select the Digital Interface Standard for Cascade Input 0 : BT1120 Mode 1 : BT656 Mode	1'h0
	RESERVED	R/W	[4]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	CHID_EN	R/W	[3:2]	Enable the CHID Insertion for Time Multiplexed Video Output [3] : Enable the CHID Insertion in H Blanking Region [2] : Enable the CHID Insertion in BT656/BT1120 Sync Code	2'h0
	NOVID_BT1120	R/W	[1:0]	Control the No-video Flag Mode in BT656/BT1120 Sync Code 0 ~ 1 : No No-video Flag in BT656/BT1120 Sync Code 2 : No-video Flag = 1 in MSB of BT656/BT1120 Sync Code 3 : No-video Flag = 0 in MSB of BT656/BT1120 Sync Code	2'h0
1x50 2x50	HD_CSC_MD	R/W	[7:6]	Control the Color Space Converter Mode for HD Video Input 0, 1 : Bypass 2 : BT601 to BT709 3 : BT709 to BT601	2'h0
	OUTFMT_BT656_MD	R/W	[5]	Select the Digital Interface Standard for Video Output 0 : BT1120 Mode 1 : BT656 Mode	1'h0
	OUTFMT_EMB_SYNC_BYP	R/W	[3]	Select the Embedded Sync Insertion of Video Data Output 0 : Embedded Sync is Inserted 1 : Embedded Sync is Not Inserted	1'h0
1x55 2x55	PTZ_SLICE_LEVEL	R/W	[7:0]	Control the Threshold Value for PTZ Slicing	8'h0
1xBB 2xBB	RESERVED	R/W	[7]	Reserved	1'h0
	VO_SYNC_CON_EN	R/W	[6]	Enable the VOUT Sync (H/V DELAY, H/V ACTIVE) Control 0 : Bypass 1 : Enable the VOUT Sync Control	1'h0
	RESERVED	R/W	[5:0]	Reserved	6'h0
1xBC 2xBC	RESERVED	R/W	[7:5]	Reserved	3'h0
1xBC 2xBC	VOUT_SYNC_HDELAY	R/W	[4:0]	Select the Starting Pixel Delay of H Sync for MIPI/Parallel Output 13'h000 : No Delay 13'h004 : 4 Pixel Delay	13'h0
1xBD 2xBD		R/W	[7:0]		
1xBE 2xBE	VOUT_SYNC_HACTIVE	R/W	[4:0]	Select the Active Pixel Number of H Sync for MIPI/Parallel Output 13'h2D0 : 720 Pixel 13'h500 : 1280 Pixel 13'h780 : 1920 Pixel	13'h0
1xBF 2xBF		R/W	[7:0]		

Addr	Name	R/W	Bit	Descriptions	Default
1xC0 2xC0	VOUT_SYNC_ VDELAY	R/W	[2:0]	Select the Starting Line Delay of V Sync for MIPI/Parallel Output 13'h000 : No Delay 13'h002 : 2 Line Delay	13'h0
1xC1 2xC1		R/W	[7:0]		
1xC2 2xC2	VOUT_HD_ PAT_FMT	R/W	[7:4]	Select the Format of Video Output Pattern Generator 0 : 1280x720p@25 1 : 1280x720p@30 2 : 1280x720p@50 3 : 1280x720p@60 4 : 1920x1080p@25 5 : 1920x1080p@30 6 : 1920x1080i@50 7 : 1920x1080i@60 8 : 960x576i@50 9 : 960x480i@60 10 : 720x576i@50 11 : 720x480i@60	4'h0
1xC3 2xC3	VOUT_SYNC_ VACTIVE	R/W	[2:0]	Select the Active Line Number of V Sync for MIPI/Parallel Output 13'h2D0 : 720 Line 13'h320 : 800 Line 13'h3C0 : 960 Line 13'h438 : 1080 Line	13'h0
		R/W	[7:0]		
1xC4 2xC4	VOUT_HD_ PAT_MD	R/W	[7:4]	Select the Pattern of Video Output Pattern Generator 0 : White 1 : Yellow 2 : Cyan 3 : Green 4 : Magenta 5 : Red 6 : Blue 7 : Black 8 : Color Bar 9 : Ramp 10 : Inverse Color Bar 11 : Combination Pattern	4'h0

Addr	Name	R/W	Bit	Descriptions	Default
	VOUT_HD_ PAT_EN	R/W	[3]	Enable the Video Output Pattern Generator 0 : Disable 1 : Enable	1'h0
	RESERVED	R/W	[2:0]	Reserved	3'h0
1xC9 2xC9	RESERVED	R/W	[7:5]	Reserved	3'h0
1xC9 2xC9	VIN_SYNC_ HDELAY	R/W	[4:0]	Select the Starting Pixel Delay of H Sync for Cascaded Input 13'h000 : No Delay 13'h004 : 4 Pixel Delay	13'h0
1xCA 2xCA		R/W	[7:0]		
1xCB 2xCB	VIN_SYNC_ HACTIVE	R/W	[4:0]	Select the Active Pixel Number of H Sync for Cascaded Input 13'h2D0 : 720 Pixel 13'h500 : 1280 Pixel 13'h780 : 1920 Pixel	13'h0
1xCC 2xCC		R/W	[7:0]		
1xCD 2xCD	VIN_HD_ PAT_FMT	R/W	[7:4]	Select the Format of Cascaded Video Input Pattern Generator 0 : 1280x720p@25 1 : 1280x720p@30 2 : 1280x720p@50 3 : 1280x720p@60 4 : 1920x1080p@25 5 : 1920x1080p@30 6 : 1920x1080i@50 7 : 1920x1080i@60 8 : 960x576i@50 9 : 960x480i@60 10 : 720x576i@50 11 : 720x480i@60	4'h0
	VIN_SYNC_CON_EN	R/W	[3]	Enable the Cascaded VIN Sync (H/V DELAY, H/V ACTIVE) Control 0 : Bypass 1 : Enable the VOUT Sync Control	1'h0
	VIN_SYNC_ VDELAY	R/W	[2:0]	Select the Starting Line Delay of V Sync for Cascaded Input 13'h000 : No Delay 13'h002 : 2 Line Delay	13'h0
1xCE 2xCE		R/W	[7:0]		

Addr	Name	R/W	Bit	Descriptions	Default
1xCF 2xCF	VIN_HD_ PAT_MD	R/W	[7:4]	Select the Pattern of Cascaded Video Input Pattern Generator 0 : White 1 : Yellow 2 : Cyan 3 : Green 4 : Magenta 5 : Red 6 : Blue 7 : Black 8 : Color Bar 9 : Ramp 10 : Inverse Color Bar 11 : Combination Pattern	4'h0
	VIN_HD_ PAT_EN	R/W	[3]	Enable the Cascaded Video Input Pattern Generator 0 : Disable 1 : Enable	1'h0
	VIN_SYNC_ VACTIVE	R/W	[2:0]	Select the Active Line Number of V Sync for Cascaded Input 13'h2D0 : 720 Line 13'h320 : 800 Line 13'h3C0 : 960 Line 13'h438 : 1080 Line	13'h0
1xD0 2xD0		R/W	[7:0]		
1xD1 2xD1	RESERVED	R/W	[7:5]	Reserved	3'h0
	VIN_HD_EN	R/W	[4]	Enable the Cascade Video Input 0 : Disable 1 : Enable	1'h0
	RESERVED	R/W	[3:0]	Reserved	4'h0

3.2.3. Page 3, 4 Register

Addr	Name	R/W	Bit	Descriptions	Default
3x00 4x00	PTZ_RX_PATH_EN	R/W	[7]	Enable the PTZ Receiver Path 0 : Disable or Initialize for PTZ Rx 1 : Enable the PTZ Path	1'h0
	PTZ_RX_START	R/W	[6]	Start the PTZ Rx 0 : Null Operation 1 : Start the PTZ Rx	1'h0
	PTZ_IGNORE_LINE_EN	R/W	[5:4]	Enable the PTZ Receiver Ignore Mode 0 : Disable 1 : Enable	2'h0
	PTZ_IGNORE_FRM_EN	R/W	[3]	Ignore PTZ Receiver Frame 0 : Normal 1 : continuous PTZ Frame Ignore	1'h0
	PTZ_RX_FIELD_POL	R/W	[2]	Select the Field Polarity for PTZ Rx 0 : Even Field High 1 : Odd Field High	1'h0
	PTZ_RX_FIELD_TYPE	R/W	[1:0]	Select the PTZ Rx Field Mode 0 : All 1 : Even Field 2 : Odd Field 3 : Reserved	2'h0
3x01 4x01	PTZ_RX_LINE_CNT	R/W	[7:3]	Select the PTZ Receive Line Size / Frame	5'h00
	PTZ_RX_HST_OS	R/W	[2:0]	Select the PTZ Receive Line Starting Offset for Even FLD 0 : + 0 Line Offset 1 : + 1 Line Offset 2 : + 2 Line Offset 3 : + 3 Line Offset 4 : - 0 Line Offset 5 : - 1 Line Offset 6 : - 2 Line Offset 7 : - 3 Line Offset	3'h0
3x02 4x02	PTZ_RX_DATA_POL	R/W	[7]	PTZ Receive Data Inversion 0 :Normal 1 : Inversion	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	PTZ_RX_HST	R/W	[6:0]	LSB of PTZ_RX_HST0 PTZ Rx Valid Line Starting Position	7'h00
3x03 4x03	PTZ_RX_FREQ_FIRST [23:16]	R/W	[7:0]	MSB of PTZ_RX_FREQ_FIRST[23:0]	8'h00
3x04 4x04	PTZ_RX_FREQ_FIRST [15:8]	R/W	[7:0]	Middle Bits of PTZ_RX_FREQ_FIRST[23:0]	8'h00
3x05 4x05	PTZ_RX_FREQ_FIRST [7:0]	R/W	[7:0]	LSB of PTZ_RX_FREQ_FIRST[23:0] PTZ Bit-width for 1st Bit Bit-width = 2^24 / (PTZ_RX_FREQ_FIRST * 148.5M)	8'h00
3x06 4x06	PTZ_RX_FREQ	R/W	[7:0]	PTZ_RX_FREQ [23:16]	8'h00
3x07 4x07	PTZ_RX_FREQ	R/W	[7:0]	PTZ_RX_FREQ [15:08]	8'h00
3x08 4x08	PTZ_RX_FREQ	R/W	[7:0]	PTZ_RX_FREQ [07:00] PTZ Bit-width for All bit's except 1st Bit Bit-width = 2^24 / (PTZ_RX_FREQ * 148.5M)	8'h00
3x09 4x09	RESERVED	R/W	[7:6]	Reserved	2'h0
	PTZ_RX_LPF_LEN	R/W	[5:0]	Select the PTZ_RX LPF Taps 0 : No Filtering ~ 63 : 63 Taps	6'h00
3x0A 4x0A	PTZ_RX_H_PIX_OFFSET	R/W	[7:0]	RX H Starting Offset for PTZ Start Bit	8'h00
3x0B 4x0B	RESERVED	R/W	[7:6]	Reserved	2'h0
	PTZ_RX_LINE_LEN	R/W	[5:0]	Bit Length / Line for PTZ Data	6'h00
3x0C 4x0C	PTZ_RX_VALID_CNT	R/W	[7:0]	All Byte Length per Command of PTZ Data	8'h00
3x0D 4x0D	RESERVED	R/W	[7]	Reserved	1'h0
	PTZ_ADDR_HOLD_EN	R/W	[6]	Stop the Auto Increment of Host Register Address and Hold the Address	1'h0
	RESERVED	R/W	[5:0]	Reserved	6'h00
3x0E 4x0E	RESERVED	R/W	[7:0]	Reserved	8'h00
3x0F 4x0F	RESERVED	R/W	[7:0]	Reserved	8'h00

Addr	Name	R/W	Bit	Descriptions	Default
3x10 4x10	PTZ_WR_ADR_INIT	R/W	[7]	Initialize the FIFO Write Address 0 : Normal Write 1 : Initialize the Write FIFO Address (Auto Cleared)	1'h0
	PTZ_WR_BIT_SWAP	R/W	[6]	Swap the FIFO Write Data Bit 0 : FIFO write with host_wr_data[7:0] 1 : FIFO write with host_wr_data[0:7]	1'h0
	RESERVED	R/W	[5:3]	Reserved	3'h0
	PTZ_FIFO_WR_MD	R/W	[2:0]	Select the Write FIFO Path 0 : Tx Data 1 : Tx Flag Pattern 2 : Tx Flag Data 3 : Reserved (Rx Data) 4 : Rx Flag Pattern 5 : Rx Start Flag Pattern 6 : Rx Start Flag Data	3'h0
3x11 4x11	PTZ_FIFO_WR_DATA	R/W	[7:0]	FIFO Write Data	8'h00
3x12 4x12	PTZ_TX_QUEUE_SIZE	R	[7:0]	The Status of Remained FIFO Size for PTZ Tx Data	8'h00
3x13 4x13	PTZ_FIFO_WR_ADDR	R	[7:0]	Current FIFO Write Address	8'hff
3x14 4x14	PTZ_RD_ADR_INIT	R/W	[7]	Initialize the FIFO Read Address 0 : Normal Read 1 : Initialize Read FIFO Address (Auto Cleared)	1'h0
	PTZ_RD_BIT_ SWAP	R/W	[6]	Swap the FIFO Read Data Bit 0 : FIFO read with host_rd_data[7:0] 1 : FIFO read with host_rd_data[0:7]	1'h0
	RESERVED	R/W	[5]	Reserved	1'h0
	PTZ_PRE_RD_EN	R/W	[4]	Enable the FIFO Pre-Read 0 : No Pre-read 1 : Enable the Pre-read (Auto Cleared)	1'h0
	RESERVED	R/W	[3]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	PTZ_FIFO_RD_MD	R/W	[2:0]	Select the Read FIFO Path 0 : Tx Data 1 : Tx Flag Pattern 2 : Tx Flag Data 3 : Rx Data 4 : Rx Flag Pattern 5 : Rx Start Flag Pattern 6 : Rx Start Flag Data	3'h0
3x15 4x15	PTZ_RX_QUEUE_SIZE	R/W	[7:0]	The Status of Remained FIFO size for PTZ Rx Data	8'h00
3x16 4z16	PTZ_RX_DATA	R	[7:0]	The Read FIFO Data	8'h00
3x17 4x17	PTZ_FIFO_RD_ADDR	R/W	[7:0]	Current FIFO Read Address	8'hff
3x18 4x18	PTZ_RX_HSYNC_POL	R/W	[7]	Select the Rx HSYNC Polarity	1'h0
3x1A 4x1A	PTZ_RX_VSYNC_POL	R/W	[7]	Select the Rx VSYNC Polarity	1'h0
3x1C 4x1C	PTZ_TX_HSYNC_POL	R/W	[7]	Select the PTZ Tx HSYNC Polarity	1'h0
3x1E 4x1E	PTZ_TX_VSYNC_POL	R/W	[7]	Select the PTZ Tx VSYNC Polarity	1'h0
3x20 4x20	PTZ_TX_PATH_EN	R/W	[7]	Enable the PTZ Tx Path 0 : Disable the PTZ Tx Path 1 : Enable the PTZ Tx Path	1'h0
	PTZ_TX_START	R/W	[6]	Start the PTZ Tx 0 : No Start 1 : Start PTZ Tx (Auto cleared when PTZ Tx Started)	1'h0
	RESERVED	R/W	[5:3]	Reserved	3'h0
	PTZ_TX_FIELD_POL	R/W	[2]	Select the Field Polarity for PTZ Tx 0 : Even Field is High 1 : Odd Field is High	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	PTZ_TX_FIELD_TYPE	R/W	[1:0]	Select the PTZ Tx Field Mode 0 : All 1 : Odd Field 2 : Even Field 3 : Reserved	2'h0
3x21	PTZ_TX_LINE_CNT	R/W	[7:3]	PTZ TX Line size per frame	5'h00
4x21	PTZ_TX_HST_OS	R/W	[2:0]	Select the PTZ Transmitter Line Starting Offset for Even FLD 0 : + 0 Line Offset 1 : + 1 Line Offset 2 : + 2 Line Offset 3 : + 3 Line Offset 4 : - 0 Line Offset 5 : - 1 Line Offset 6 : - 2 Line Offset 7 : - 3 Line Offset	3'h0
3x22 4x22	PTZ_TX_DATA_POL	R/W	[7]	Select the Data Polarity 0 : Normal 1 : Data Polarity Inversion	1'h0
	PTZ_TX_HST	R/W	[6:0]	Select the PTZ Starting Line Number	8'h00
3x23 4x23	PTZ_TX_FREQ_FIRST [23:16]	R/W	[7:0]	MSB of PTZ_TX_FREQ_FIRST[23:0]	8'h00
3x24 4x24	PTZ_TX_FREQ_FIRST [15:8]	R/W	[7:0]	Middle Bits of PTZ_TX_FREQ_FIRST[23:0]	8'h00
3x25 4x25	PTZ_TX_FREQ_FIRST [7:0]	R/W	[7:0]	LSB of PTZ_TX_FREQ_FIRST[23:0] Tx Bit width for 1st PTZ Tx Bit = 1/148.5M x 2^24 / PTZ_TX_FREQ_FIRST	8'h00
3x26 4x26	PTZ_TX_FREQ[23:16]	R/W	[7:0]	MSB of PTZ_TX_FREQ[23:0]	8'h00
3x27 4x27	PTZ_TX_FREQ[15:08]	R/W	[7:0]	Middle Bits of PTZ_TX_FREQ[23:0]	8'h00
3x28 4x28	PTZ_TX_FREQ[7:0]	R/W	[7:0]	LSB of PTZ_TX_FREQ[23:0] Tx Bit width except 1st PTZ Tx Bit = 1/148.5M x 2^24 / PTZ_TX_FREQ	8'h00
3x29	RESERVED	R/W	[7:5]	Reserved	3'h0
4x29	PTZ_TX_HPST[12:8]	R/W	[4:0]	MSB of PTZ_TX_HPST[12:0]	5'h00

Addr	Name	R/W	Bit	Descriptions	Default
3x2A 4x2A	PTZ_TX_HPST[7:0]	R/W	[7:0]	LSB of PTZ_TX_HPST[12:0] PTZ Tx Starting Location	8'h00
3x2B	RESERVED	R/W	[7:6]	Reserved	2'h0
4x2B	PTZ_TX_LINE_LEN	R/W	[5:0]	PTZ Tx Line Length per frame	6'h00
3x2C 4x2C	PTZ_TX_ALL_DATA_LEN	R/W	[7:0]	All Byte Length per Command of PTZ Tx Data	8'h00

3.2.4. Page 5 Register

Addr	Name	R/W	Bit	Descriptions	Default
5x00	MTX_CH_OVERFLOW	R	[4:0]	Timing Overflow Detection in MIPI Tx (Read Only) [4] : For Read Channel [3] : For Write Ch 3 [2] : For Write Ch 2 [1] : For Write Ch 1 [0] : For Write Ch 0 0 : Normal 1 : Overflow	5'h0
5x01	MTX_BUF_OVERFLOW	R	[3:0]	Buffer Overflow Detection in MIPI Tx (Read Only) [3] : For R/W Ch 3 [2] : For R/W Ch 2 [1] : For R/W Ch 1 [0] : For R/W Ch 0 0 : Normal 1 : Overflow	4'h0
5x06	FSYNC1_OUT	R	[6]	F Sync for CH 1 (Read Only)	1'h0
	VSYNC1_OUT	R	[5]	V Sync for CH 1 (Read Only)	1'h0
	HSYNC1_OUT	R	[4]	H Sync for CH 1 (Read Only)	1'h0
	FSYNC0_OUT	R	[2]	F Sync for CH 0 (Read Only)	1'h0
	VSYNC0_OUT	R	[1]	V Sync for CH 0 (Read Only)	1'h0
	HSYNC0_OUT	R	[0]	H Sync for CH 0 (Read Only)	1'h0
5x07	FSYNC3_OUT	R	[6]	F Sync for CH 3 (Read Only)	1'h0
	VSYNC3_OUT	R	[5]	V Sync for CH 3 (Read Only)	1'h0
	HSYNC3_OUT	R	[4]	H Sync for CH 3 (Read Only)	1'h0
	FSYNC2_OUT	R	[2]	F Sync for CH 2 (Read Only)	1'h0
	VSYNC2_OUT	R	[1]	V Sync for CH 2 (Read Only)	1'h0
	HSYNC2_OUT	R	[0]	H Sync for CH 2 (Read Only)	1'h0
5x09	REF_CH_STRT	R/W	[7]	Control Reference Timing Mode for Video Input Channel 0 : Free-running by Setting 1 : Use Video input Channel Timing	1'b0
	TST_CHID_FIX	R/W	[5:4]	Control MIPI Tx CHID Mode 0/1 : Normal (Reserved) 2~3 : Enable Test Mode	2'b0

Addr	Name	R/W	Bit	Descriptions	Default
	REF_CH_SEL	R/W	[1:0]	Select Video Input Channel @ REF_CH_STRT_EN = 1 0 : CH 0 Timing ~ 3 : CH 3 Timing	2'b0
5x0A	REF_CH_VDLY	R/W	[7:0]	Reference V Start Offset from Channel V Active End 0 : No Delay ~ 8'hFF : Max Delay	8'h0
5x0B	DBG_CH1_SEL	R/W	[6:4]	Select MTX_DEBUG[5:3] DEBUG[5] : Hsync 0 ~ 3, rd_ovf DEBUG[4] : Vsync 0 ~ 3, wr_ovf DEBUG[3] : Fsync 0 ~ 3, buf_ovf	3'h0
	DBG_CH0_SEL	R/W	[2:0]	Select MTX_DEBUG[2:0] DEBUG[2] : Hsync 0 ~ 3, rd_ovf DEBUG[1] : Vsync 0 ~ 3, wr_ovf DEBUG[0] : Fsync 0 ~ 3, buf_ovf	3'h0
5x0C	DBG_CH3_SEL	R/W	[6:4]	Select MTX_DEBUG[11:9] DEBUG[11] : Hsync 0 ~ 3, rd_ovf DEBUG[10] : Vsync 0 ~ 3, wr_ovf DEBUG[9] : Fsync 0 ~ 3, buf_ovf	3'h0
	DBG_CH2_SEL	R/W	[2:0]	Select MTX_DEBUG[8:6] DEBUG[8] : Hsync 0 ~ 3, rd_ovf DEBUG[7] : Vsync 0 ~ 3, wr_ovf DEBUG[6] : Fsync 0 ~ 3, buf_ovf	3'h0
5x0D	CH3_FRAME_MD	R/W	[7:6]	MIPI Frame Mode for CH3	2'b0
	CH2_FRAME_MD	R/W	[5:4]	MIPI Frame Mode for CH2	2'b0
	CH1_FRAME_MD	R/W	[3:2]	MIPI Frame Mode for CH1	2'b0
	CH0_FRAME_MD	R/W	[1:0]	MIPI Frame Mode for CH0 0 : Fixed to 0 1 : Fixed to 1 for Odd, 2 for Even 2 : Free-running for Progressive 3 : Free-running for Interlace	2'b0
5x0E	VBLK_CODE_Y	R/W	[7:0]	Select Vertical Blank Code for Y	8'h80
5x0F	VBLK_CODE_C	R/W	[7:0]	Select Vertical Blank Code for C	8'h10
5x10	MTX_PATH_EN	R/W	[7]	Enable MTX Controller Path 0 : Disable 1 : Enable	1'd0

Addr	Name	R/W	Bit	Descriptions	Default
	REF_VSTRT_MD	R/W	[6]	Select MTX Controller Mode * Refer to Table for MTX Controller Mode (Next to Page 5 Register Description)	1'b0
	MTX_VBLK_MSK	R/W	[5]	Enable Data Masking for Vblank 0 : Bypass 1 : Enable Masking with VBLK_CODE	1'b0
	MTX_CHBLK_MSK	R/W	[4]	Enable Data Masking for Novideo Ch 0 : Bypass 1 : Enable Masking with VBLK_CODE	1'b0
	MTX_BLK_LV	R/W	[3:2]	Select Channel Blank Color 0 : Black 1 : Gray 2 : White 3 : Blue	1'd0
	MTX_LANE	R/W	[1:0]	Select MIPI Tx Lane Number 0 : 1 Lane 1 : 2 Lane 2/3 : 4 Lane	1'b0
5x11	REF_VBLK_MD	R/W	[7]	Enable H Sync during Vertical Blank 0 : Disable 1 : Enable	1'b0
	REF_CH_NUM	R/W	[5:4]	Control MIPI Transfer CH Size 0 : 1 CH 1 : 2 CH 2 : 3 CH 3 : 4 CH	2'h0
	MTX_LONG_DLY[11:8]	R/W	[3:0]	Next Packet Delay after MIPI Long Packet	4'b0
5x12	MTX_LONG_DLY[7:0]	R/W	[7:0]	0 : No Delay ~ 120 : Recommend	8'd0
5x13	REF_TIME_EN	R/W	[7]	Synchronize with Frame Start/Stop for Reference Timing (Com-V/H Mode) 0 : No Synchronize 1 : Synchronize with Frame Start/Stop	1'b0

Addr	Name	R/W	Bit	Descriptions	Default
	REF_COMB_MD	R/W	[6:5]	Select MTX Controller Mode * Refer to Table for MTX Controller Mode (Next to Page 5 Register Description)	2'b0
	REF_HSTRT_MD	R/W	[4]	Select MTX Controller Mode * Refer to Table for MTX Controller Mode (Next to Page 5 Register Description)	1'b0
	MTX_SHORT_DLY[11:8]	R/W	[3:0]	Next Packet Delay after MIPI Short Packet	4'b0
5x14	MTX_SHORT_DLY[7:0]	R/W	[7:0]	0 : No Delay ~ 120 : Recommend	8'd0
5x15	REF_VS_OS_VBLK	R/W	[7:6]	Control V Start Offset of V Blank in Reference Timing 0 : No Offset ~ 3 : -3 Line	2'b0
	REF_VE_OS_VBLK	R/W	[5:4]	Control V End Offset of V Blank in Reference Timing 0 : No Offset ~ 3 : +3 Line	2'b0
	REF_FE_VOS	R/W	[3:2]	Control V End of Frame Sync in Reference Timing 0 : No Offset ~ 3 : -3 Line	2'b0
	REF_FS_VOS	R/W	[1:0]	Control V Start of Frame Sync in Reference Timing 0 : No Offset ~ 3 : +3 Line	2'b0
5x16	REF_FE_HDLY[13:8]	R/W	[5:0]	Control H End of Frame Sync in Reference Timing 0 : No Offset ~	6'd0
5x17	REF_FE_HDLY[7:0]	R/W	[7:0]		8'd0
5x18	REF_FS_HDLY[13:8]	R/W	[5:0]	Control H Start of Frame Sync in Reference Timing 0 : No Offset ~	6'd0
5x19	REF_FS_HDLY[7:0]	R/W	[7:0]		8'd0
5x1A	REF_HTOTAL[13:8]	R/W	[5:0]	Control Frame H Total Width for Reference Timing	6'd0
5x1B	REF_HTOTAL[7:0]	R/W	[7:0]		8'd0
5x1C	REF_VTOTAL[13:8]	R/W	[5:0]	Control Frame V Total Height for Reference Timing	6'd0
5x1D	REF_VTOTAL[7:0]	R/W	[7:0]		8'd0

Addr	Name	R/W	Bit	Descriptions	Default
5x1E	MTX_CHID_EN	R/W	[7]	Enable MTX CHID Packet 0 : Disable 1 : Enable	1'd0
	REF_LINE_ID_EN	R/W	[6]	Select MTX CHID format for Line valid 0 : No Line Valid 1 : Line Valid	1'b0
	MTX_CHID_MD	R/W	[5:4]	Select MTX CHID format 0 : 16 Bits CHID with Y/C MUX 1 : 16 Bits CHID with Y/C Sep 2 : 32 Bits CHID with Y/C MUX 3 : 32 Bits CHID with Y/C Sep	2'b0
	MTX_CHID_NUM	R/W	[3:2]	Control MTX CHID Transfer Number 0 : 1 CH ~ 3 : 4 CH	2'b0
	MTX_CHID_SIZE	R/W	[1:0]	Control MTX CHID Bit-width / CH 0 : 16 Bits ~ 3 : 64 Bits	2'b0
5x20 5x30 5x40 5x50	MTX_CH_EN	R/W	[7]	Enable MTX Channel 0 : Disable 1 : Enable	1'd0
	CH_VBLK_MD	R/W	[6]	Enable Data Transfer during V Blank 0 : Disable 1 : Enable	1'b0
	MTX_CH_SEL	R/W	[5:4]	Select MTX Input Channel 0 : CH 0 ~ 3 : CH 3	2'b0
	MTX_CH_BUF_SIZE	R/W	[3:0]	Control Buffer Size for MTX CH 5 : Minimum Required Size ~ 9 : Max value for FHD ~ 14 : Max value for HD	4'b0

Addr	Name	R/W	Bit	Descriptions	Default
5x21 5x31 5x41 5x51	CH_DATA_BLK	R/W	[7]	Enable Channel Blank 0 : Normal 1 : Channel Blank as MTX_BLK_LV	1'd0
	CH_ID_BLK	R/W	[6]	Enable CHID Blank 0 : Normal 1 : Channel ID Blank	1'b0
	CH_INFO	R/W	[5:4]	Select Channel Info @ CHID 0 ~ 3 : User Defined Channel Info Extend ID [29:28]	2'b0
	CH_INT_MD	R/W	[3]	Select Input Format 0 : Progressive 1 : Interface	1'b0
	MTX_CH_HSIZE[10:8]	R/W	[2:0]	Control MTX CH Horizontal Width (Unit : Pixel) Bit[1:0] = 0 (Reserved) 720 : For 720H 960 : For 960H 1280 : For HD 1920 : For FHD	3'b0
5x22 5x32 5x42 5x52	MTX_CH_HSIZE[7:0]	R/W	[7:0]		8'd0
5x23 5x33 5x43 5x53	MTX_CH0_VSIZE[10:8]	R/W	[2:0]	Control MTX CH Vertical Height (Unit : Line) 240 : For SD 720 : For 720HD 960 : For 960HD 1080 : For FHD	3'd0
5x24 5x34 5x44 5x54	MTX_CH_VSIZE[7:0]	R/W	[7:0]		8'd0
5x25 5x35 5x45 5x55	MTX_CH_FS_OS[10:8]	R/W	[2:0]	CH Frame End Packet Start Delay 0 : No Offset ~	3'd0
5x26 5x36 5x46 5x56	MTX_CH_FS_OS[7:0]	R/W	[7:0]		8'd0

Addr	Name	R/W	Bit	Descriptions	Default
5x27 5x37 5x47 5x57	MTX_CH_FE_OS[10:8]	R/W	[2:0]	CH Frame Start Packet Delay 0 : No Offset ~	3'd0
5x28 5x38 5x48 5x58	MTX_CH_FE_OS[7:0]	R/W	[7:0]		8'd0
5x29 5x39 5x49 5x59	REF_CH_VS_VOS	R/W	[7:6]	Frame Start Packet Vertical Delay @ COM-H/V or Fixed-VC Mode (VSTRT_MD = 1) 0 : No Offset ~ 3 : + 3 Line Offset	2'd0
	REF_CH_VS_HOS[13:8]	R/W	[5:0]		6'd0
5x2A 5x3A 5x4A 5x5A	REF_CH_VS_HOS[7:0]	R/W	[7:0]	Frame Start Packet Pixel Delay @ COM-H/V or Fixed-VC Mode (VSTRT_MD = 1) use Recommend value	8'd0
5x60	CH0_HWIDTH[13:8]	R/W	[5:0]	CH0 Horizontal Width in VC-Fixed Mode	6'd0
5x61	CH0_HWIDTH [7:0]	R/W	[7:0]	(VSTRT_MD = 1 & HSTRT_MD = 1)	8'd0
5x62	CH1_HWIDTH[13:8]	R/W	[5:0]	CH1 Horizontal Width in VC-Fixed Mode	6'd0
5x63	CH1_HWIDTH [7:0]	R/W	[7:0]	(VSTRT_MD = 1 & HSTRT_MD = 1)	8'd0
5x64	CH2_HWIDTH[13:8]	R/W	[5:0]	CH2 Horizontal Width in VC-Fixed Mode	6'd0
5x65	CH2_HWIDTH [7:0]	R/W	[7:0]	(VSTRT_MD = 1 & HSTRT_MD = 1)	8'd0
5x66	CH3_HWIDTH[13:8]	R/W	[5:0]	CH3 Horizontal Width in VC-Fixed Mode	6'd0
5x67	CH3_HWIDTH [7:0]	R/W	[7:0]	(VSTRT_MD = 1 & HSTRT_MD = 1)	8'd0
5x68	CH0_VRATE[15:8]	R/W	[7:0]	CH0 Vertical Output Rate in REF_ VSTRT_MD	8'd0
5x69	CH0_VRATE[7:0]	R/W	[7:0]	16'hAAAA : 720/1080 Rate 16'hFFFF : Bypass	8'd0
5x6A	CH1_VRATE[15:8]	R/W	[7:0]	CH1 Vertical Output Rate in REF_ VSTRT_MD	8'd0
5x6B	CH1_VRATE[7:0]	R/W	[7:0]	16'hAAAA : 720/1080 Rate 16'hFFFF : Bypass	8'd0
5x6C	CH2_VRATE[15:8]	R/W	[7:0]	CH2 Vertical Output Rate in REF_ VSTRT_MD	8'd0
5x6D	CH2_VRATE[7:0]	R/W	[7:0]	16'hAAAA : 720/1080 Rate 16'hFFFF : Bypass	8'd0

Addr	Name	R/W	Bit	Descriptions	Default
5x6E	CH3_VRATE[15:8]	R/W	[7:0]	CH3 Vertical Output Rate in REF_ VSTRT_MD 16'hAAAA : 720/1080 Rate 16'hFFFF : Bypass	8'd0
5x6F	CH3_VRATE[7:0]	R/W	[7:0]		8'd0

Table for MTX Controller Mode (5x10, 5x13 Address)

	REF_VSTRT_MD	REF_HSTRT_MD	REF_COMB_MD		MIPI Output Mode
Individual VC	0	X	X		MIPI Virtual Channel Mode with FIFO Output Selection
VC-Fixed	1	1	x	x	MIPI Virtual Channel Mode with N x {[CHID, DATA] / H} with Reference Output Timing
Combine H Sep I	1	0	0	0	[N x CHID + N x DATA] / H with Reference Output Timing
Combine H Sep II	1	0	0	1	{N x [CHID, DATA] } / H with Reference Output Timing
Combine V Sep	1	0	1	x	N x {[CHID, DATA] / H} with Reference Output Timing

3.2.5. Page 6 Register

Addr	Name	R/W	Bit	Descriptions	Default
6x04	RESERVED	R/W	[7]	Reserved	1'h0
	MIPI_EN	R/W	[6]	Enable MIPI Controller 0 : Disable 1 : Enable	1'h0
	MIPI_DPHY_PD	R/W	[5]	MIPI D-PHY Global Power Down 0 : Disable 1 : Enable	1'h0
	CLK_HS_MODE	R/W	[4]	MIPI Clock Lane HS Mode 0 : LP & HS Mode 1 : Only HS Mode	1'h0
	MIPI_ULP_DATA	R/W	[3]	Enable MIPI ULP Data 0 : Disable 1 : Enable	1'h0
	MIPI_ULP_CLK	R/W	[2]	Enable MIPI ULP Clock 0 : Disable 1 : Enable	1'h0
	RESERVED	R/W	[1]	Reserved	1'h0
	MIPI_STM	R/W	[0]	Enable the MIPI Serializer Test Pattern Mode 0 : Disable 1 : Enable	1'h0
6x05	MIPI_CK_CONTROL	R/W	[7:4]	Control MIPI CKP/CKN State 4'b0000 : Normal Operation Mode 4'b0001 : CP/CN = LP-00 state 4'b0010 : CP/CN = LP-01 state 4'b0011 : CP/CN = LP-10 state 4'b0100 : CP/CN = LP-11 state 4'b0101 : CP/CN = HS-0 state 4'b0110 : CP/CN = HS-1 state 4'b0111 : CP/CN = Hi-z state 4'b1000 : CP/CN = ULP state 4'b1010 : CP/CN = Power Down Mode	4'hA
	RESERVED	R/W	[3:0]	Reserved	4'h0

Addr	Name	R/W	Bit	Descriptions	Default
6x06	MIPI_D0_CONTROL	R/W	[7:4]	Control MIPI DP0/DN0 State 4'b0000 : Normal Operation Mode 4'b0001 : DP0/DN0 = LP-00 state 4'b0010 : DP0/DN0 = LP-01 state 4'b0011 : DP0/DN0 = LP-10 state 4'b0100 : DP0/DN0 = LP-11 state 4'b0101 : DP0/DN0 = HS-0 state 4'b0110 : DP0/DN0 = HS-1 state 4'b0111 : DP0/DN0 = Hi-z state 4'b1000 : DP0/DN0 = ULP state 4'b1010 : DP0/DN0 = Power Down Mode	4'hA
	MIPI_D1_CONTROL	R/W	[3:0]	Control MIPI DP1/DN1 State 4'b0000 : Normal Operation Mode 4'b0001 : DP1/DN1 = LP-00 state 4'b0010 : DP1/DN1 = LP-01 state 4'b0011 : DP1/DN1 = LP-10 state 4'b0100 : DP1/DN1 = LP-11 state 4'b0101 : DP1/DN1 = HS-0 state 4'b0110 : DP1/DN1 = HS-1 state 4'b0111 : DP1/DN1 = Hi-z state 4'b1000 : DP1/DN1 = ULP state 4'b1010 : DP1/DN1 = Power Down Mode	4'hA
6x07	MIPI_D2_CONTROL	R/W	[7:4]	Control MIPI DP0/DN0 State 4'b0000 : Normal Operation Mode 4'b0001 : DP2/DN2 = LP-00 state 4'b0010 : DP2/DN2 = LP-01 state 4'b0011 : DP2/DN2 = LP-10 state 4'b0100 : DP2/DN2 = LP-11 state 4'b0101 : DP2/DN2 = HS-0 state 4'b0110 : DP2/DN2 = HS-1 state 4'b0111 : DP2/DN2 = Hi-z state 4'b1000 : DP2/DN2 = ULP state 4'b1010 : DP2/DN2 = Power Down Mode	4'hA

Addr	Name	R/W	Bit	Descriptions	Default
	MIPI_D3_CONTROL	R/W	[3:0]	Control MIPI DP0/DN0 State 4'b0000 : Normal Operation Mode 4'b0001 : DP3/DN3 = LP-00 state 4'b0010 : DP3/DN3 = LP-01 state 4'b0011 : DP3/DN3 = LP-10 state 4'b0100 : DP3/DN3 = LP-11 state 4'b0101 : DP3/DN3 = HS-0 state 4'b0110 : DP3/DN3 = HS-1 state 4'b0111 : DP3/DN3 = Hi-z state 4'b1000 : DP3/DN3 = ULP state 4'b1010 : DP3/DN3 = Power Down Mode	4'hA
6x08	RESERVED	R/W	[7:4]	Reserved	4'h0
	MIPI_LANE	R/W	[3:2]	Select MIPI Lane Mode 0 : 1 Lane 1 : 2 Lane 2 : 4 Lane	2'h0
	RESERVED	R/W	[1:0]	Reserved	2'h0
6x09	D0_LANE_SWAP	R/W	[7:6]	Swap Data for Data0 Lane 0 : D0 Lane Data 1 : D1 Lane Data 2 : D2 Lane Data 3 : D3 Lane Data	2'h0
	D1_LANE_SWAP	R/W	[5:4]	Swap Data for Data1 Lane 0 : D0 Lane Data 1 : D1 Lane Data 2 : D2 Lane Data 3 : D3 Lane Data	2'h1
	D2_LANE_SWAP	R/W	[3:2]	Swap Data for Data2 Lane 0 : D0 Lane Data 1 : D1 Lane Data 2 : D2 Lane Data 3 : D3 Lane Data	2'h2
	D3_LANE_SWAP	R/W	[1:0]	Swap Data for Data3 Lane 0 : D0 Lane Data 1 : D1 Lane Data 2 : D2 Lane Data 3 : D3 Lane Data	2'h3
6x0B	D0_NP_SWAP	R/W	[7]	Swap N/P Line for Data0 Lane 0 : Normal N/P 1 : Swap N/P	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	D1_NP_SWAP	R/W	[6]	Swap N/P Line for Data1 Lane 0 : Normal N/P 1 : Swap N/P	1'h0
	D2_NP_SWAP	R/W	[5]	Swap N/P Line for Data2 Lane 0 : Normal N/P 1 : Swap N/P	1'h0
	D3_NP_SWAP	R/W	[4]	Swap N/P Line for Data3 Lane 0 : Normal N/P 1 : Swap N/P	1'h0
	MIPI_CK_NP_SWAP	R/W	[3]	Swap N/P Line for Clock Lane 0 : Normal N/P 1 : Swap N/P	1'h0
	RESERVED	R/W	[2:0]	Reserved	3'h0
6x0E	RESERVED	R/W	[7:3]	Reserved	5'h0
	DPHY_ISEL	R/W	[2:0]	Control MIPI HS Mode Reference Current 0 : HS Output Swing 150mV : 4 : HS Output Swing 200mV (Default) : 7 : HS Output Swing 237.5mV (Step 12.5mV)	3'h4
6x1C	MIPI_T_LPX	R/W	[7:0]	Select the Transition Time for LP Data transfer	8'h09
6x1D	MIPI_T_CLK_PREPARE	R/W	[7:0]	Select the Time of LP00 State for Clock Lane	8'h08
6x1E	MIPI_T_HS_PREPARE	R/W	[7:0]	Select the Time of LP00 State for Data Lane	8'h09
6x1F	MIPI_T_HS_ZERO	R/W	[7:0]	Select the Time of HS Zero State at Start for Data Lane	8'h11
6x20	MIPI_T_HS_TRAIL	R/W	[7:0]	Select the Time of HS Zero State at End for Data Lane	8'h0C
6x21	MIPI_T_CLK_ZERO	R/W	[7:0]	Select the Time of HS Zero State at Start for Clock Lane	8'h28
6x22	MIPI_T_CLK_TRAIL	R/W	[7:0]	Select the Time of HS Zero State at End for Clock Lane	8'h0B
6x23	MIPI_T_CLK_PRE	R/W	[7:0]	Select the Time of Data Transfer Start from Clock Lane	8'h01
6x24	MIPI_T_CLK_POST	R/W	[7:0]	Select the Time of Clock Transfer End from Data Transfer End	8'h12
6x25	MIPI_T_WAKEUP	R/W	[7:0]	Select the Time of Exit Time from ULP State	8'h82
6x26	MIPI_T_HSEXIT	R/W	[7:0]	Select the Time of LP11 to HS Burst State for Data Lane	8'h11
6x27	MIPI_T_CLK_HSEXIT	R/W	[7:0]	Select the Time of LP11 to HS Burst State for Clock Lane	8'h11
6x28	MIPI_ESC_CMD	R/W	[7:0]	Select the Data of LP Data Transfer	8'h00
6x36	MIPI_PKT_SIZE0_H	R/W	[7:0]	Select the MSB of Package Size in MIPI Active Line for CH0 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h0A

Addr	Name	R/W	Bit	Descriptions	Default
6x37	MIPI_PKT_SIZE0_L	R/W	[7:0]	Select the LSB of Package Size in MIPI Active Line for CH0 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h00
6x38	MIPI_PKT_SIZE1_H	R/W	[7:0]	Select the MSB of Package Size in MIPI Active Line for CH1 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h0A
6x39	MIPI_PKT_SIZE1_L	R/W	[7:0]	Select the LSB of Package Size in MIPI Active Line for CH1 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h00
6x3A	MIPI_PKT_SIZE2_H	R/W	[7:0]	Select the MSB of Package Size in MIPI Active Line for CH2 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h0A
6x3B	MIPI_PKT_SIZE2_L	R/W	[7:0]	Select the LSB of Package Size in MIPI Active Line for CH2 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h00
6x3C	MIPI_PKT_SIZE3_H	R/W	[7:0]	Select the MSB of Package Size in MIPI Active Line for CH3 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h0A
6x3D	MIPI_PKT_SIZE3_L	R/W	[7:0]	Select the LSB of Package Size in MIPI Active Line for CH3 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	8'h00
6x46	MIPI_DATA_ID0	R/W	[7:0]	Select the Data ID for CH0	8'h1E
6x47	MIPI_DATA_ID1	R/W	[7:0]	Select the Data ID for CH1	8'h5E
6x48	MIPI_DATA_ID2	R/W	[7:0]	Select the Data ID for CH2	8'h9E
6x49	MIPI_DATA_ID3	R/w	[7:0]	Select the Data ID for CH3	8'hDE

4. Electrical Characteristics

4.1. DC Electrical Characteristics

Table 10. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V, VDDO Pin	-0.5		4.6	V	
Voltage for VDD1V, VDD1P, VDDI Pin	-0.5		1.8	V	
Voltage for Digital Input Pin	-0.5		3.8	V	
Storage Temperature	-40		125	°C	
Junction Temperature	-40		125	°C	
Peak Temperature on Reflow Soldering			260	°C	15 Sec

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition

Table 11. Recommended Operating Conditions for Power and Temperature

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V	3.0	3.3	3.6	V	
Voltage for VDDO	3.0/1.62	3.3/1.8	3.6/1.98	V	
Voltage for VDD1V, VDD1P, VDDI	1.19	1.25	1.32	V	
Ambient Operation Temperature	-40		85	°C	

Note : Power On/Off sequence should keep the following rule

- Apply power to VDD3V, VDDO and VDD1V, VDD1P, VDDI at the same time
- If it is difficult to apply the power to these pins at the same time, apply the power to VDD3V, VDDO first and to VDD1V, VDD1P, VDDI later
- Cut the power of VDD3V, VDDO and VDD1V, VDD1P, VDDI at the same time
- If it is difficult to cut the power of these pins at the same time, cut the power of VDD1V, VDD1P, VDDI first and of VDD3V, VDDO later

Table 12. Recommended Operating Conditions for Digital I/O

Parameter	For 1.8V I/O			For 3.3V I/O			Unit	Condition
	Min	Typ	Max	Min	Typ	Max		
Digital Inputs								
Input High Voltage	1.2			2.0			V	
Input Low Voltage	-0.3		0.6	-0.3		0.8	V	
Input Capacitance		2.23			2.23		pF	
Input Leakage Current			±10			±10	uA	
Digital Output								
Output High Voltage	1.4			2.9			V	
Output Low Voltage			0.4			0.4	V	
Output Driving Current	2.4		9.6	5.0		20.0	mA	
Tri-state Output Current			±10			±10	uA	
Output Capacitance		2.39			2.23		pF	

Table 13. Supply Current and Power Dissipation for HD720p@25/30

Parameter	Parallel			MIPI (4 Lane)			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Current at VDD1V (1.25V)	58	67	69	58	67	69	mA
Supply Current at VDD1P (1.25V)	1	1	1	1	1	1	mA
Supply Current at VDDI (1.25V)	148	170	180	148	170	180	mA
Supply Current at VDD3V (3.3V)	14	15	16	14	15	16	mA
Supply Current at VDDO (3.3V / 1.8V)	36 / 18	46 / 21	60 / 24	8	10	11	mA
Power Dissipation for 3.3V VDDO	424	499	563	331	380	402	mW
Power Dissipation for 1.8V VDDO	337	385	409	-	-	-	mW

Note : VDDO (Pin 16) should be supplied only with 3.3V.

VDDO (Pin 24) should be supplied only with 3.3V for MIPI Tx Interface.

VDDO (Pin 37) can be supplied with 3.3V or 1.8V for Parallel Video Interface.

VDDO (Pin 47) can be supplied with 3.3V or 1.8V for Parallel Video Interface.

Table 14. Supply Current and Power Dissipation for FHD1080p@25/30

Parameter	Parallel			MIPI (4 Lane)			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Current at VDD1V (1.25V)	58	67	69	58	67	69	mA
Supply Current at VDD1P (1.25V)	1	1	1	1	1	1	mA
Supply Current at VDDI (1.25V)	164	188	200	164	188	200	mA
Supply Current at VDD3V (3.3V)	14	15	16	14	15	16	mA
Supply Current at VDDO (3.3V / 1.8V)	83 / 38	97 / 46	110 / 53	13	14	15	mA
Power Dissipation for 3.3V VDDO	599	690	753	368	416	440	mW
Power Dissipation for 1.8V VDDO	393	452	486	-	-	-	mW

Note : VDDO (Pin 16) should be supplied only with 3.3V.

VDDO (Pin 24) should be supplied only with 3.3V for MIPI Tx Interface.

VDDO (Pin 37) can be supplied with 3.3V or 1.8V for Parallel Video Interface.

VDDO (Pin 47) can be supplied with 3.3V or 1.8V for Parallel Video Interface.

4.2. AC Electrical Characteristics

Table 15. Analog Input and Output Parameter

Parameter	Symbol	Min	Typ	Max	Unit
Video ADCs					
Differential Non-Linearity	DLE		± 0.5	± 1	
Integral Non-Linearity	ILE		± 1	± 3	
Signal-to-Noise Ratio	SNR	50	55		dB
Analog Clock PLL					
RMS Jitter	rms_{pll}		8		ps
Duty Cycle	dt_{pll}	45		55	%
Lock Time	t_{lock}		50		us
Crystal Input					
Nominal Frequency	$f_{x\text{-}tal}$		27		MHz
Frequency Deviation	$\Delta f_{x\text{-}tal}$	-50		50	ppm
Duty Cycle	$dt_{x\text{-}tal}$			55	%

Table 16. Serial Host Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Bus free time between STOP and START	t1	1.3			us
Data Hold time	t2	0		0.9	us
Data Setup time	t3	0.1			us
Setup time for a(repeated) START condition	t4	0.6			us
Setup time for a STOP condition	t5	0.6			us
Hold time (repeated) START	t6	0.6			us
Rise time SDA and SCL signal	t7			250	ns
Fall time SDA and SCL signal	t8			250	ns
Capacitive load for each bus line	C_b			400	pF
I^2C Clock frequency	f_{I2C}			400	KHz

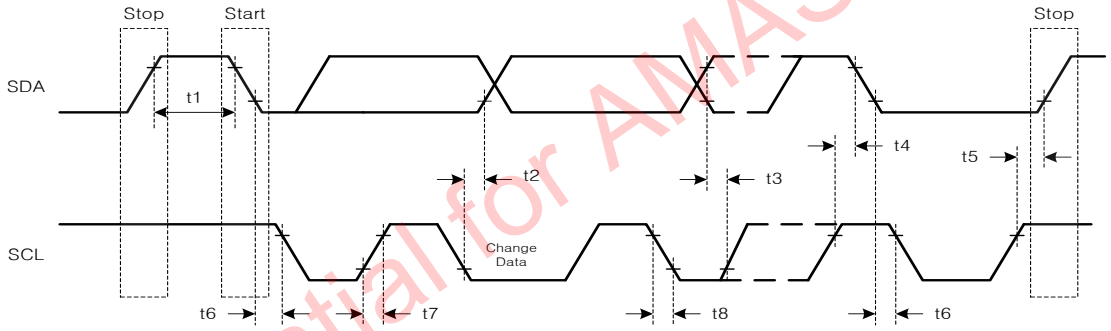


Fig 32. Serial Host Interface Timing Diagram

Table 17. MIPI LP Transmitter Timing

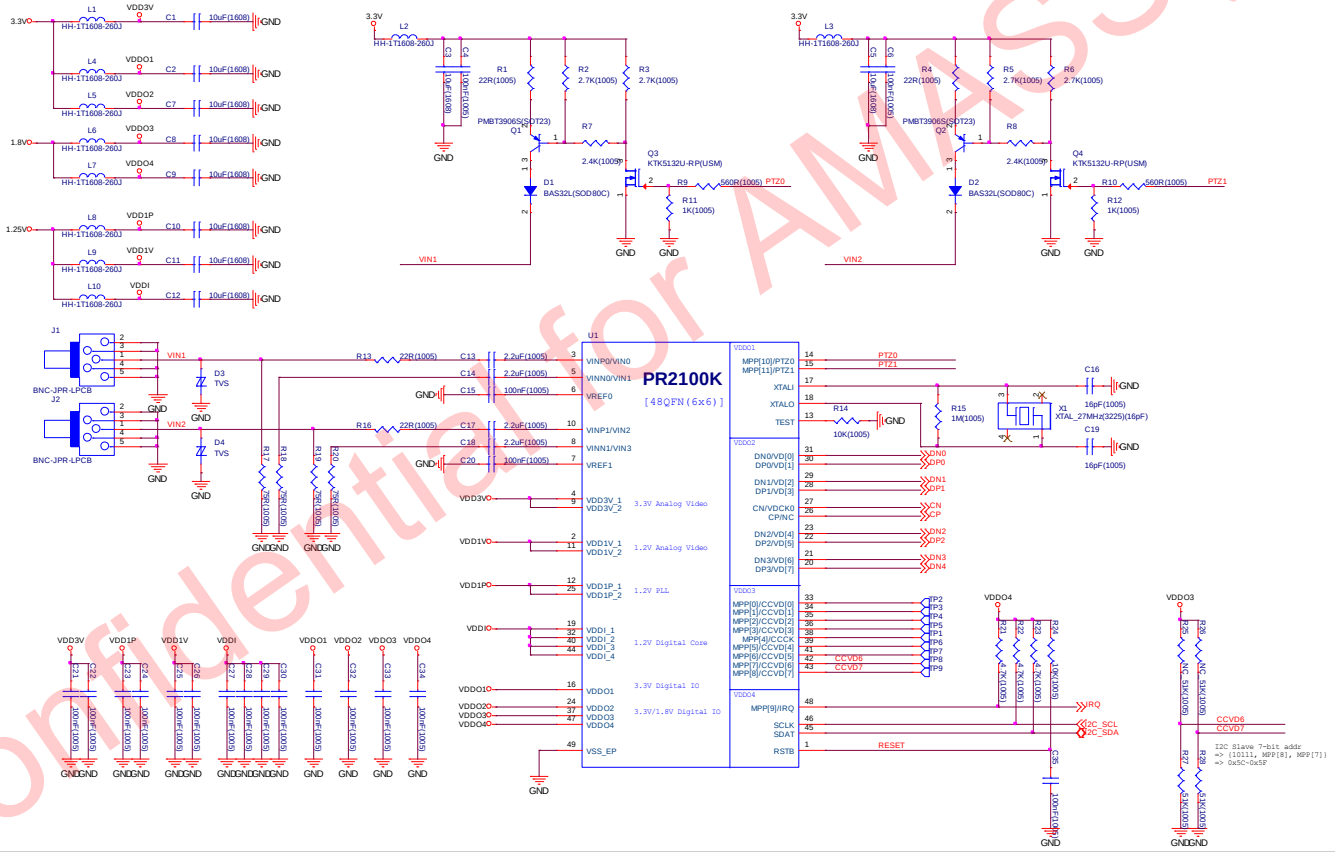
Parameter	Symbol	Min	Typ	Max	Unit
15% ~ 85% rise/fall time	t_{RLP}/t_{FLP}			25	ns
30% ~ 85% rise time in EOT state	t_{REOT}			35	ns
Slew rate	dV/dt_{SR}			120	mV/ns
Load capacitance	C_{LOAD}	0		70	pF
Thevenin output low level	V_{OL}	-50		50	mV
Thevenin output High level	V_{OH}	1.1	1.2	1.3	V
Output Impedance	Z_{OLP}	110			Ohm

Table 18. MIPI HS Transmitter Timing

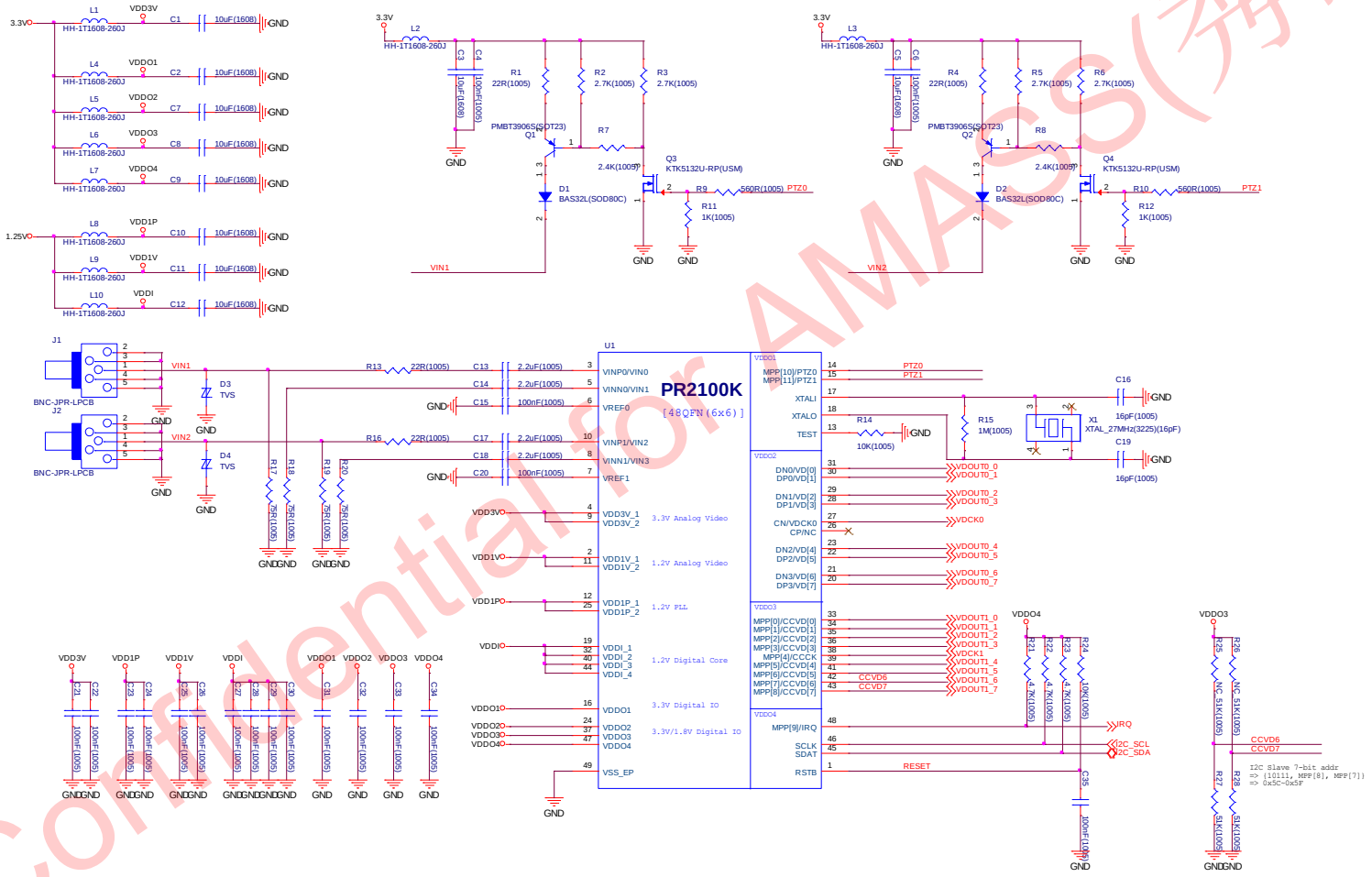
Parameter	Symbol	Min	Typ	Max	Unit
20% ~ 80% rise/fall time	t_R/t_F	150		0.3UI	ps
HS transmit differential voltage	V_{OD}	140	200	270	mV
HS transmit static common mode voltage	V_{CMTX}	150	200	250	mV
V_{OD} mismatch when output is Differntial-1 or Differntial-0	ΔV_{OD}			10	mV
V_{CMTX} mismatch when output is Differntial-1 or Differntial-0	ΔV_{CMTX}			5	mV
HS output high voltage	V_{OHHS}			360	mV
Single ended output impedance	Z_{OS}	40	50	62.5	Ohm
Single ended output impedance mismatch	ΔZ_{OS}			10	%
Common-level variation for 50~450MHz	ΔV_{CMTX}			25	mV

5. Application Schematic

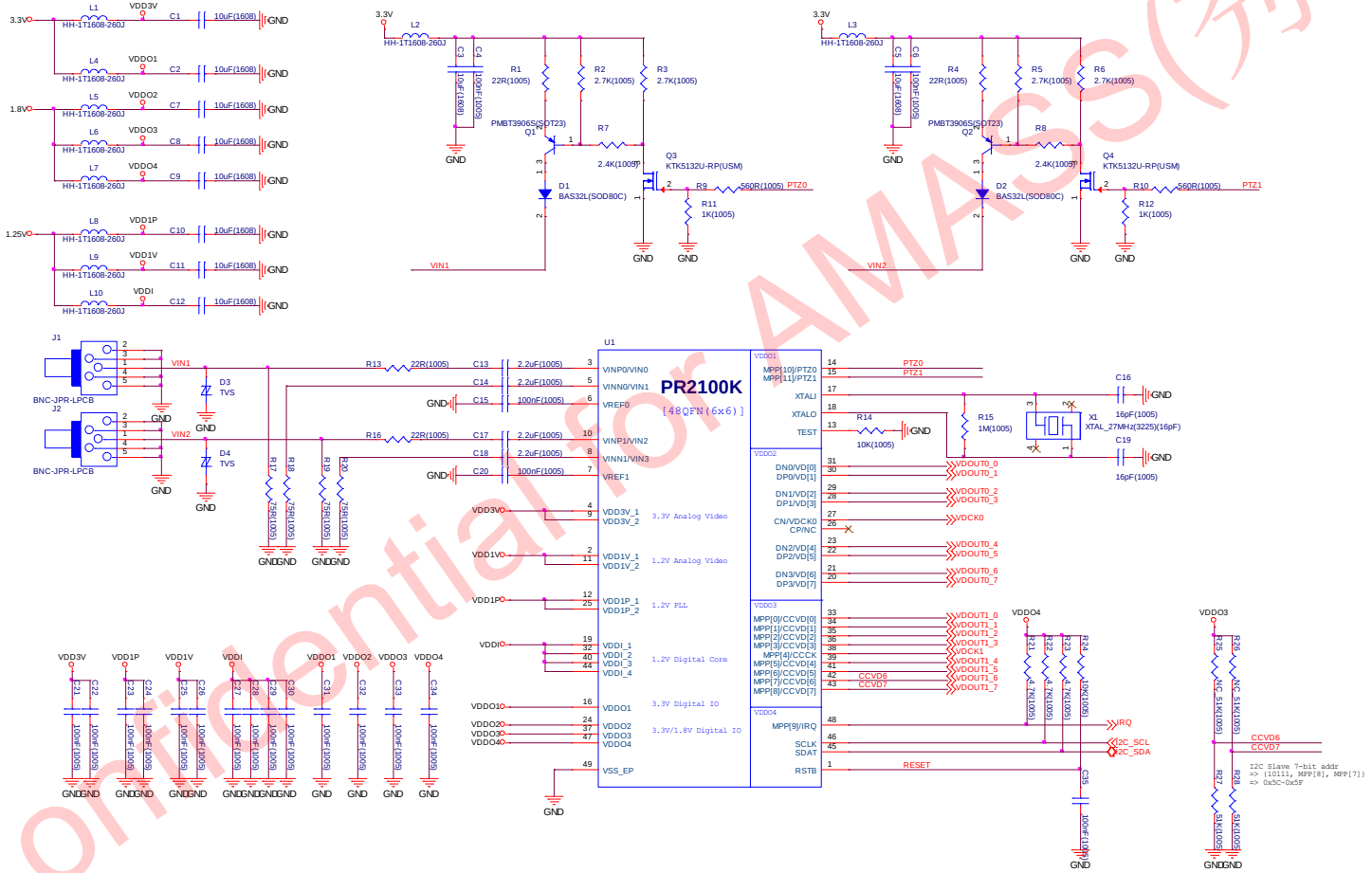
5.1. MIPI Output



5.2. Parallel Output with 3.3V Interface

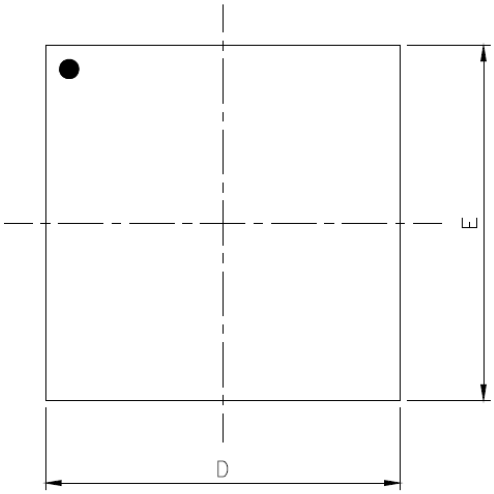


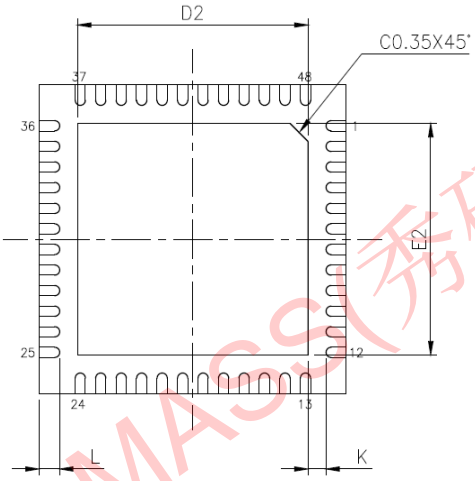
5.3. Parallel Output with 1.8V Interface

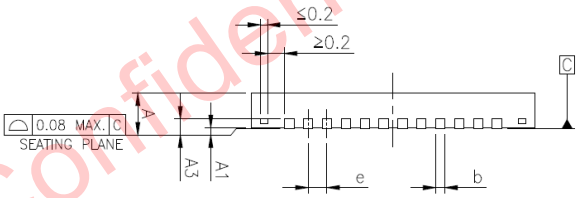


6. Package Specification

6.1. 48Pin eQFN Package Mechanical Drawing







SYMBO	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		6.00 BSC	
D2	4.45	4.50	4.55
E		6.00 BSC	
E2	4.45	4.50	4.55
e		0.40 BSC	
K	0.20	-	-
L	0.35	0.40	0.45

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

7. Revision History

Version	Date	Description
V0.1	2019.10.31	Preliminary datasheet is released
V0.2	2019.11.14	Register descriptions are added
V0.3	2019.01.20	Change VDCK1 (26 Pin) to NC for Parallel Video Output (P.8 ~ 9) Channel ID Information is Added (P.25) Add the Register Description for 1x50/2x50 Register (P.79) Recommended Operating Condition is Updated (105°C -> 85°C, P102) Power Dissipation Table is Updated (P.104) Change VDCK1 connection for Video Output (P.108 ~ P.110)
V0.4	2020.04.16	Update IO Power Description for Digital IO/MIPI (P.9, 104)
V0.5	2020.04.27	Update Operating Conditions for Digital I/O (P.103)
V0.6	2020.04.29	Change MIPI Max Data Rate per Lane from 1.2Gbps to 600Mbps (P.6, 19)
V0.7	2020.06.30	Change Max CH Number of HD720@30/25 for MIPI 4 Lane Mode