WESTERN DIGITAL
CORPORATION

PR1472-01 (PSAR)
Programmable Synchronous & Asynchronous Receiver

FEATURES

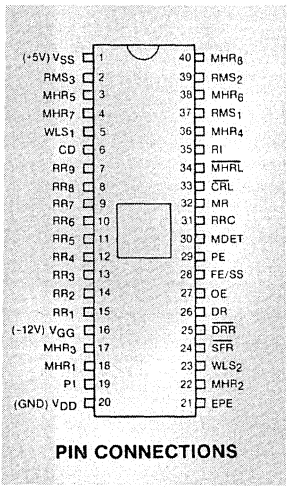
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC (1X CLOCK) PR1472-01; DC TO 100K BITS/SEC PR1472
- PROGRAMMABLE MATCH (FILL) CHARACTER WITH MATCH DETECT FLAG.
- INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION
- NINE BIT WIDE RECEIVER HOLDING REGISTER
- SELECTABLE 5, 6, 7 OR 8 BITS PER CHARACTER
- EVEN/ODD OR NO PARITY SELECT
- PROGRAMMABLE CLOCK RATE; 1X, 16X, 32X OR 64X
- AUTOMATIC START AND STOP BIT STRIPPING
- AUTOMATIC CHARACTER STATUS AND FLAG GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE CAPABILITY
- DOUBLE BUFFERED
- TTL & DTL COMPATIBLE — INTERNAL ACTIVE PULLUP
- COMPATIBLE TRANSMITTER, PT1482

GENERAL DESCRIPTION

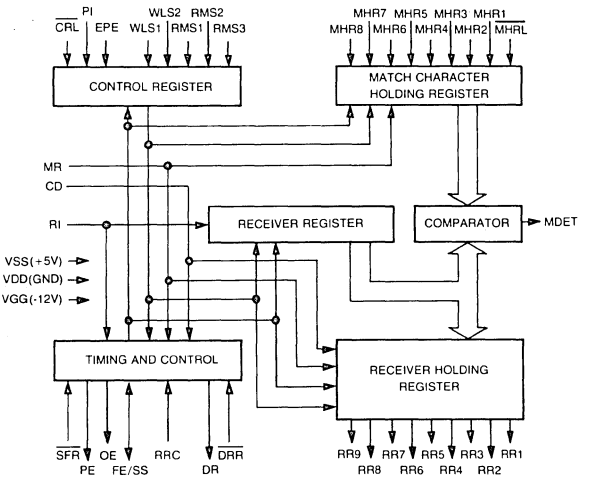
The Western Digital PR1472 (PSAR) is a programmable receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

Contiguous synchronous serial characters are compared to a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit(s) which are stripped from the data. Four internal registers, in conjunction with Three-State Outputs provide full system versatility.

The PSAR is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a Compatible Transmitter, PT1482.



PIN CONNECTIONS



PR1472 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 Volt Supply
37, 39, 2	RECEIVER MODE SELECT	RMS_1, RMS_2, RMS_3	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS_1, RMS_2, and RMS_3 inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load and Chip Disable, select the Receiver operating mode. RMS_1, RMS_2, and RMS_3 may be strobed or hard-wired to the appropriate input voltage. **RMS_3 RMS_2 RMS_1 Selected Operating Mode** 0 0 0 ASYNCH OR ISOCH, 1X CLOCK 0 0 1 ASYNCH OR ISOCH, 16X CLOCK 0 1 0 ASYNCH OR ISOCH, 32X CLOCK 0 1 1 ASYNCH OR ISOCH, 64X CLOCK 1 X 0 SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION 1 X 1 SYNCH-INTERNAL CHARACTER SYNCHRONIZATION NOTE: When operating in asynchronous or isochronous mode with 1X clock there is no protection against false start bits. A high-level input voltage, V_{IH}, applied to CD disables RMS_1, RMS_2 and RMS_3.
18,22 17, 36, 3, 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR_1, MHR_2, MHR_3, MHR_4, MHR_5, MHR_6, MHR_7, MHR_8	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the Match-Character Holding Register Load, $\overline{MHRL}$. Parallel 8-bit characters are input into the Match-Character Holding Register with the $\overline{MHRL}$ Strobe (pin 34). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. These inputs may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IL}, applied to CD disables MHR_1 and MHR_8.
5,23	WORD LENGTH SELECT	WLS_1, WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the Control Register Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: **WLS_2 WLS_1 Selected Word Length** V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS WLS_1 and WLS_2 may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
6	CHIP DISABLE	CD	This line controls the disable associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line disables inputs and removes drive from push-pull output buffers causing them to float. Drivers of disables outputs are not required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **Input Lines** — **Three-State Output Lines** $\overline{CRL}$ — $\overline{DRR}$ — PE — RR_1-RR_8 EPE — $\overline{SFR}$ — FE PI — $\overline{MHRL}$ — OE WLS_1WLS_2 — MHR_1-MHR_8 RMS_1-RMS_3
7-15	RECEIVER HOLDING-REGISTER DATA OUTPUT	RR_9-RR_1	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the Receiver Holding Register outputs, RR_1-RR_9. The parallel data character, including parity (RR_9), appears on these lines. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 15) is the least significant bit of the character. A high-level input voltage, V_{IH}, applied to CD disables RR_1-RR_9.
16	V_{GG} POWER SUPPLY	V_{GG}	– 12 Volts Supply.
19	PARITY INHIBIT	PI	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the EPE and PI inputs.
21	EVEN PARITY ENABLE	EPE	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be verified by the receiver. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, select odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable. PI and EPE may be strobed or hard-wired to the appropriate input voltage. **PI** — **EPE** — **Selected Parity** — **Comments** V_{IL} — V_{IL} — Odd — CD = V_{IL} V_{IL} — V_{IH} — Even — CD = V_{IL} V_{IH} — X — None — CD = V_{IL} NOTE: If CD = V_{IH}, no programming is performed since inputs are disabled. X — either V_{IL} or V_{IH}. When programmed, the appropriate parity is verified following the last data bit of a character, immediately preceding the stop element of asynchronous and isochronous characters. A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
29	PARITY ENABLE	PE	A high-level input V_{IH} enables parity. A low level input V_{IH} disables parity.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
24	STATUS FLAG RESET	$\overline{SFR}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{SFR}$ input. A low-level input voltage, V_{IL}, applied to this line resets the PE, FE and OE Status Flags.
25	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{DRR}$ input. A low-level input voltage, V_{IL}, applied to this line resets the DR Flag. A high-level input voltage, V_{IH}, applied to CD disables $\overline{DRR}$.
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first SYN character, when located and transferred to the Receiver Holding Register, will not cause DR to go to a high-level output voltage, V_{OH}, but will cause MDET to go to a high-level output voltage. Character transfer to the Receiver Holding Register occurs in the center of the last bit of a synchronous character or the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated.
27	OVERRUN ERROR FLAG	OE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the OE input. A high-level output voltage, V_{OH}, indicates that the prevously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character or in the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated. A high-level input voltage, V_{OH}, applied to CD disables OE.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. If programmed for the ASYNCHRONOUS or ISOCHRONOUS MODE, a low-level input voltage, V_{IL}, applied to CD (pin 6) enables the FRAMING ERROR FLAG output which indicates the status of the STOP BIT detection circuit. A high-level output voltage, V_{OH}, indicates that the character transferred to the Receiver Holding Register has no valid STOP BIT; i.e., the bit following the PARITY BIT is not a high-level input voltage, V_{IH}. This transfer occurs in the center of the first stop element at which time this flag is updated. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tri-state or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION, a transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, initiates the automatic internal "SYN" CHARACTER search operation.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
28	FRAMING ERROR/ SYN SEARCH	FE/SS	Prior to initiation of this operation, the Receiver Holding Register is "transparent" so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the Match-Character Holding Register during initialization), the Receiver Holding Register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage. V_{OH}, but, the Data Received (DR) FLAG does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the Receiver Holding Register to become "transparent." If programmed for EXTERNAL CHARACTER SYNCHRONIZATION, the system external to the P/SAR examines the data stream for "SYN" characters when SYN SEARCH is a low-level input voltage, V_{IL}. The Receiver Holding Register is "transparent" which allows the contents of the RECEIVER REGISTER to be monitored as it ripples through the shift register. When the external logic locates a "SYN" CHARACTER, indicated by a high-level input voltage, V_{OH}, on MDET, the SYN SEARCH line is externally raised to a high-level input voltage, V_{IH}. This high-level input voltage causes character synchronization to be initiated, returns the Receiver Holding Register to a "non-transparent" condition, causing subsequent characters to be transferred to the RECEIVER HOLDING REGISTER (when the center of the last bit of a character is recognized) and raises the DR FLAG.
30	MATCH DETECT FLAG	MDET	A high-level output voltage, V_{OH}, indicates that the contents of the Transmitter Register are identical to the contents of the Match-Character Holding Register. This flag is set to a high-level output voltage, V_{OH}, at the center of the first STOP ELEMENT of an asynchronous or isochronous character.
31	RECEIVER REGISTER CLOCK	RRC	This fifty (50) percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a rate determined by RMS_1, RMS_2 and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
32	MASTER RESET	MR	A high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets the contents of the Receiver Holding Register to a high-level output voltage, V_{OH}, resets the contents of the Match-Character Holding Register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL}, but does not effect the contents of the control register.
33	$\overline{\text{CONTROL REGISTER LOAD}}$	$\overline{\text{CRL}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{CRL}}$ input. A low-level input voltage, V_{IL}, applied to this line enables inputs to DC "D Type" Latches of the Control Register and loads it with Control Bits (EPE, PI, RMS_1, RMS_2, RMS_3, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables CRL.
34	$\overline{\text{MATCH CHARACTER HOLDING REGISTER LOAD}}$	$\overline{\text{MHRL}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{MHRL}}$ input. A low-level input voltage, V_{IL}, applied to this line enables input to DC "D Type" Latches of the Match-Character Holding Register and loads it with the Match-Character Holding Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{MHRL}}$.
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the Receiver Register determined by the character length, parity and the number of stop bits programmed. A high-level input voltage, V_{IH}, must be present when no ASYNCHRONOUS data is being received.

ORGANIZATION

PR1472 block diagram is illustrated on page 1.

Control Register — Programming of the PSAR is accomplished by loading the 7 Bit Control register. Mode selection, clock division, word length, and parity are selected when the Control Register Load (CRL) signal is activated.

Receiver Register — The Receiver Register is used to store the incoming data stream. The contents of this register can be gated to the Holding register during the transparent mode, or compared with the Match Holding Register. When a character is assembled it is transferred to the Receiver Holding Register.

Receiver Holding Register — The Receiver Holding Register, a buffer register, is used to store the assembled character.

Match Holding Register — The Match Holding Register is used to store the match character. The contents of this register are compared with the receiver register to establish character synchronization.

Timing & Control — The Timing and Control Logic generates the required control signals to assemble characters, match comparison, bit stripping, and generation of status/flag signals.

SYNCHRONOUS MODE OPERATION

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no Start or Stop bits. Character synchronization (the "framing" of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control.

Referring to the Block Diagram of the Receiver, the Chip Disable (CD) enables or disconnects various in-

puts and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, DRR, SFR, PE, and OE and the outputs of the Receiver Holding Register, are also controlled by CD. It is necessary that CD enable these lines to allow strobing information in these registers and to allow examination of these output flags and data.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

Enabled by CD, the Control Register is loaded by strobing $\overline{CRL}$ to a low-level input voltage which defines mode of operation and clock rate selection, character length and selected parity if required. Table 1 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires Receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly. The P/SAR programmably accommodates internal or external character synchronization.

Programmed for internal character synchronization, a high-level input voltage on the Sync Search line, the Receiver Holding Register is "transparent" and its contents are identical to the Receiver Holding Register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver Register Clock (RRC), shifts through the Receiver Register and is compared with the preprogrammed character in the Match-Character Holding Register. A match, indicated by a high-level output voltage on Match Detect (MDET), returns the Receiver Holding register to its non-transparent state and initializes timing and control logic but does not set the Data Received Flag to a high-level output voltage. The character following the match will be transferred to the Receiver Holding Register at the receipt of the center of its last bit and the Data Received Flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, Match Detect will continue to be a high-level output voltage when the Data Received Flag is set. Therefore, sequence verification can be performed by the system (additional hardware or software as desired).

Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the Receiver Holding Register sets the associated Data Received Register Flag (DR) to a high-level output voltage. The transfer of a character to the Receiver Holding Register, if the Data Received Register Flag had already been set to a high-level output voltage, causes the previous character to be lost (written over) and is alerted by an Overrun Error Flag which is a high-level output voltage. In normal operation, the Data Received Flag is reset by $\overline{DRR}$ when the Receiver Holding Register is serviced (unloaded). The Status Flags, $\overline{PE}$ and OE, are also provided with an external reset $\overline{SFR}$ so that block status and character status may be (accumulated) verified. A low-level input voltage on Sync Search causes character synchronization to be lost and initiates transparency of the Receiver Holding Register.

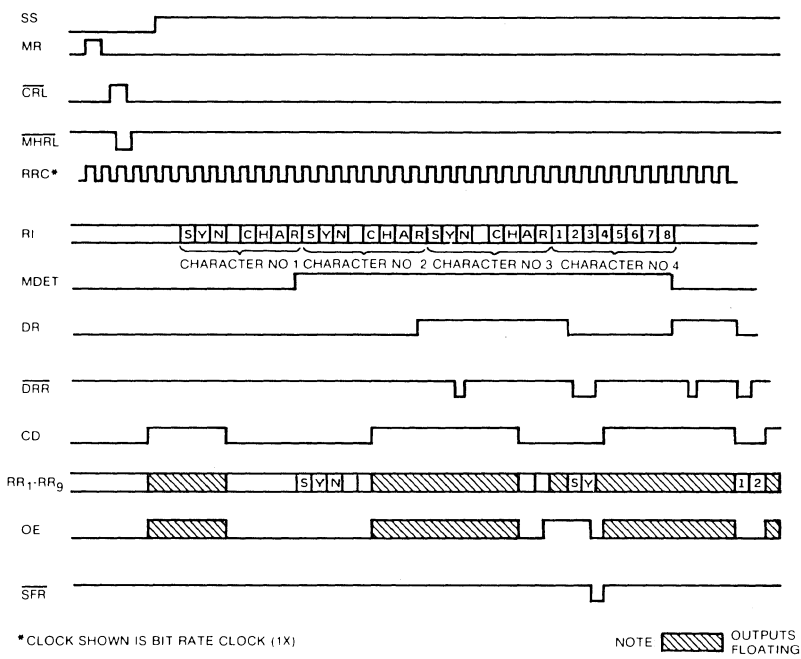
External character synchronization, programmed by the Control Register, is similar to the description above with the exception that the Sync Search line controls the nontransparency of the Receiver Holding Register directly and comparison is done externally. Upon recognition of the appropriate synchronizing pattern, the Sync Search line is set to a high-level input voltage prior to the end of the last bit. Raising the Sync Search line to a high-level input voltage causes the buffer to go "nontransparent", initializing timing and control circuitry to "frame" characters. The first bit received after a high-level input voltage is applied to Sync Search, defines the start of the "frame". Character length defined by the Control Register defines the end of the "frame".

Table 1. SYNC MODE CONTROL DEFINITION

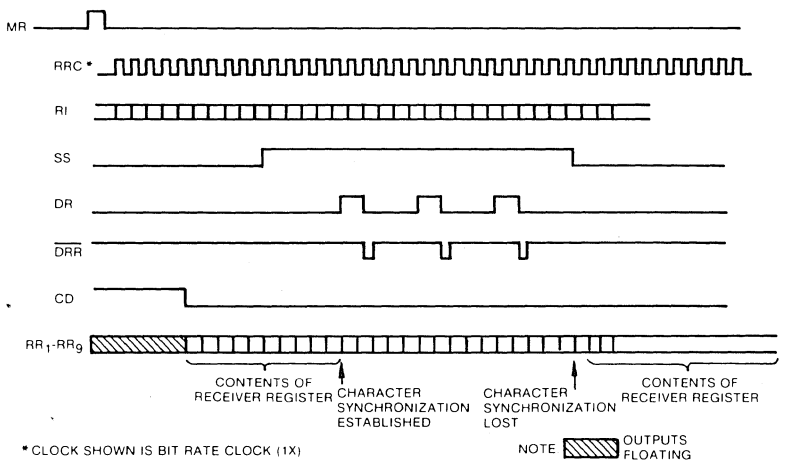
CONTROL WORD					CHARACTER FORMAT	
R W W						
M L L				E		
S S S			P	P	DATA	PARITY BIT
3 2 1			I	E	BITS	CHECKED
1 0 0			0	0	5	ODD
1 0 0			0	1	5	EVEN
1 0 0			1	X	5	NONE
1 0 1			0	0	6	ODD
1 0 1			0	1	6	EVEN
1 0 1			1	X	6	NONE
1 1 0			0	0	7	ODD
1 1 0			0	1	7	EVEN
1 1 0			1	X	7	NONE
1 1 1			0	0	8	ODD
1 1 1			0	1	8	EVEN
1 1 1			1	X	8	NONE
↑ Sets to SYNC Mode						

If RMS_1 = 1, the receiver operates in the internal character SYNC mode.

If RMS_1 = 0, character SYNC must be externally provided.



(INTERNAL SYNCHRONIZATION)



(EXTERNAL SYNCHRONIZATION)

SYNCHRONOUS TIMING DETAIL

ASYCHRONOUS & ISOCHRONOUS MODE

The completed assembly of a parallel character, by the P/SAR, from a serial data stream and buffered by its Receiver Holding Register is indicated by the status of the Data Received (DR) Flag. The assembly of character from a serial data stream consisting of a start bit, data, parity (if programmed), and a stop interval is initiated by the Start bit transition.

Verification of parity and receipt of a valid stop bit is accomplished prior to the character transfer to the Receiver Holding Register. Simultaneously, this data is compared with a preprogrammed character in the Match-Character Holding Register.

Status Flags, Data Received, Parity Error, Framing Error, Overrun Error and Match Detect are loaded into status registers during character transfer to the Receiver Holding Register.

Referring to the Block Diagram of the Receiver, the Chip Disable enables or disconnects various inputs and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, $\overline{DRR}$, $\overline{SFR}$, PE, FE, OE and the outputs of the Receiver Holding Register are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output data and flags.

Device operation is programmed subequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage, and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Characer Holding Register to be reset to a low-level output voltage.

When the Receiver is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage defines the mode of operation and clock rate selection, character length and selected parity if required. Table 2 illustrates all the programmable asynchronous formats.

A mark to space transition on the receiver input initializes the clock counter causing it to count to the theoretical center of the start bit. At this time, the input is sampled. A high-level input voltage at the Receiver Input causes the first mark to space transition to be interpreted as a noise spike and resets all timing and control logic. This provides one-half data bit noise immunity on all clock selection rates except 1X. A low-level input voltage at the Receiver Input at the theoretical center of the start bit causes timing and control circuitry to sample the theoretical center of succeeding data bits. This data is shifted through the Receiver Register. When an entire character (as defined by the Control Register) is assembled in the Receiver Register, the line is "tested" for a valid stop bit at its theoretical center. This character is also compared with the contents of the Match-Character Holding Register at the center of the stop bit and its parity is verified. A parallel transfer occurs, loading the contents of the Receiver Register (less start and stop bits) into the Receiver Holding Register. The status of the parity verification, framing error, and overrun error circuitry are also loaded into their approriate registers to provide output error flags when the Data Received Flag is set. If the Data Received Flag had not been reset prior to the assembly of the current character, the previous character is lost and this is indicated by a high-level output voltage on the Overrun Error Flag.

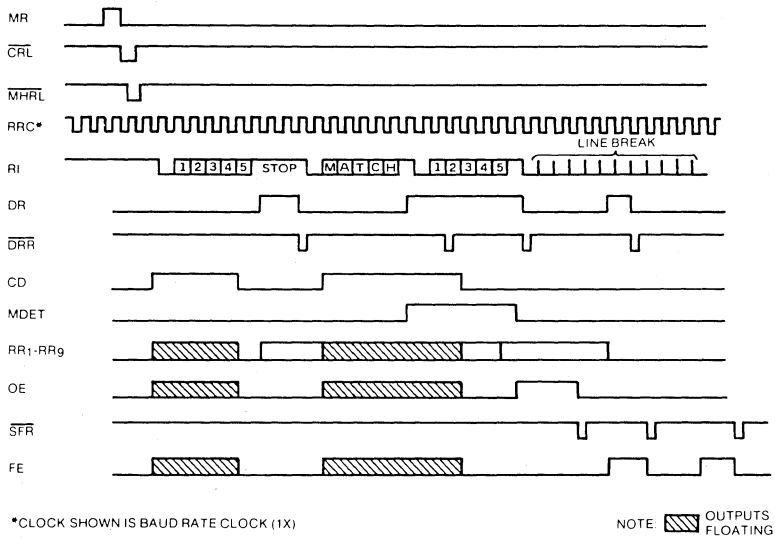
Table 2. ASYNCHRONOUS OR ISOCHRONOUS MODE CONTROL DEFINITION

RMS3	WLS2	WLS1	PI	EPE	Start Bit	Data Bits	Added Parity Bit	Stop Elements
0	0	0	0	0	1	5	Odd	1 or more
0	0	0	0	1	1	5	Even	1 or more
0	0	0	1	X	1	5	None	1 or more
0	0	1	0	0	1	6	Odd	1 or more
0	0	1	0	1	1	6	Even	1 or more
0	0	1	1	X	1	6	None	1 or more
0	1	0	0	0	1	7	Odd	1 or more
0	1	0	0	1	1	7	Even	1 or more
0	1	0	1	X	1	7	None	1 or more
0	1	1	0	0	1	8	Odd	1 or more
0	1	1	0	1	1	8	Even	1 or more
0	1	1	1	X	1	8	None	1 or more

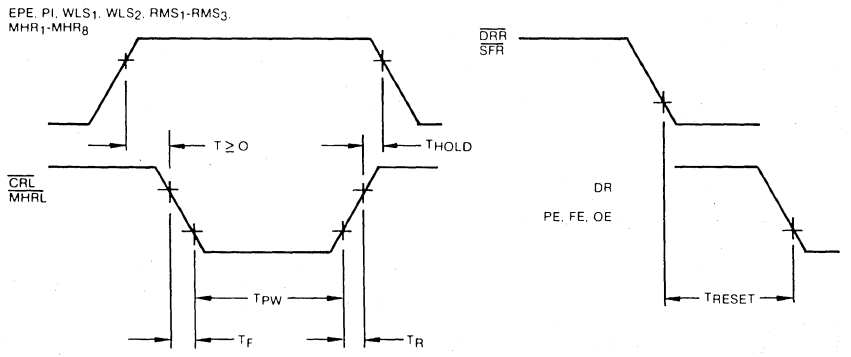
↑ Set to ASYNC or ISOC Mode

When RMS_3 is 0 (ASYNC or ISOC Mode), RMS_2 and RMS_3 determine the clock frequency according to the following table:

RMS_2	RMS_1	Clock Frequency
0	0	1X Baud Rate
0	1	16X Baud Rate
1	0	32X Baud Rate
1	1	64X Baud Rate

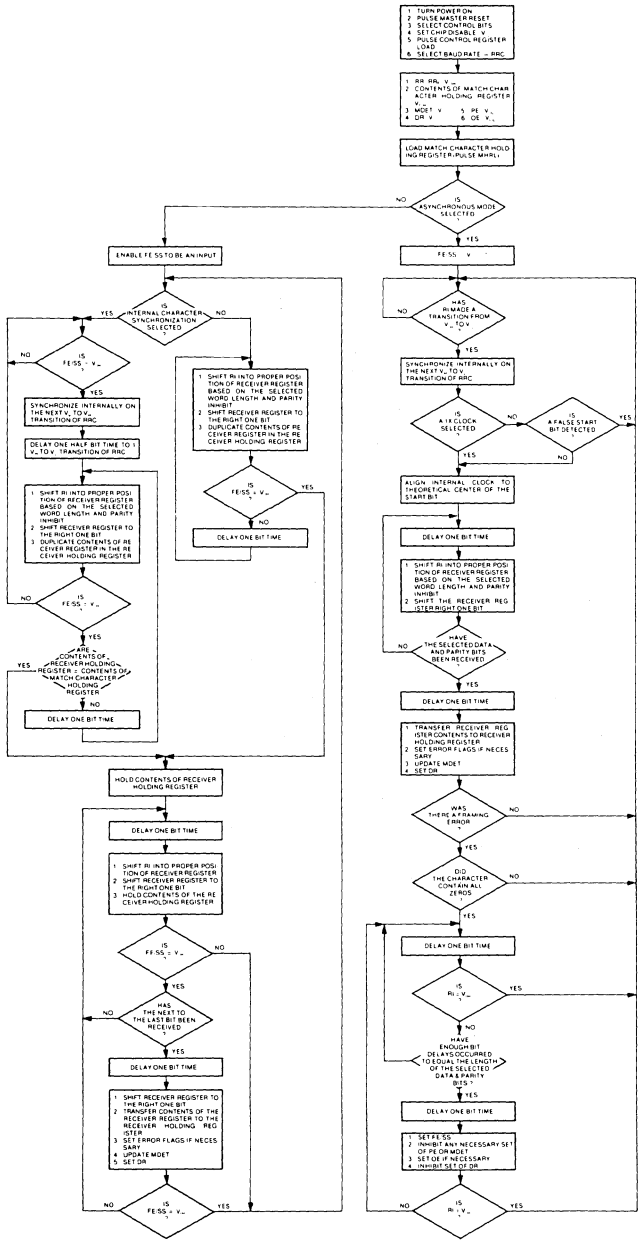


ASYNCHRONOUS & ISOCHRONOUS TIMING EXAMPLE

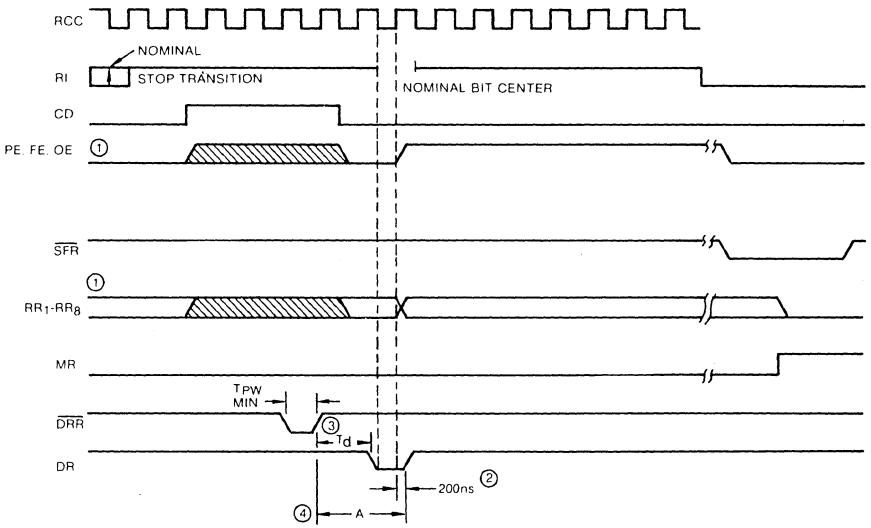


DATA INPUT LOAD CYCLE **RESET DELAY**

SWITCHING WAVEFORMS



PR1472 SYNCHRONOUS ASYNCHRONOUS RECEIVER FLOW CHART



1 DATA AND ERROR FLAGS ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT.
2 DR IS DELAYED 200ns FROM DATA AND ERROR FLAGS.
3 THE DELAY BETWEEN DRR AND DR = T_d = 500ns.
4 $\overline{DRR}$ SHOULD BE HIGH A MINIMUM OF "A" ns (T_d + 1.2 CLOCK + 200ns) PRIOR TO THE NEXT RISING EDGE OF DR

TIMING DETAIL

MAXIMUM RATINGS

V_{GG} Supply Voltage	+0.3V to −20V
V_{DD} Supply Voltage	+0.3V to −20V
Clock Input Voltage*	+0.3V to −20V
Logic Input Voltage*	+0.3V to −20V
Logic Output Voltage*	+0.3V to −20V
Storage Temperature Ceramic	−65°C to +150°C
Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

*$V_{GG} = V_{DD} = OV$

NOTE: These voltages are measured with respect to V_{SS} (Substrate).

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = OV$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+70°C$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
	INPUT LOGIC LEVELS[1]			
V_{IL}	Low-level Input Voltage		0.8V	$V_{SS} = 4.75V$
V_{IH}	High-level Input Voltage	V_{SS}-1.5V		
	OUTPUT LOGIC LEVELS[2]			
V_{OL}	Low-level Output Voltage		0.4V	$V_{SS} = 5.25V$ $I_{OL} = 1.6mA$
V_{OH}	High-level Output Voltage	V_{SS}-1.0V		$V_{SS} = 4.75V$ $I_{OH} = -100uA$
	INPUT CURRENT[1]			
I_{IL}	Low-level Input Current (each input)		-1.6mA	$V_{SS} = 5.25V$ $V_{IN} = 0.4V$

**Not more than one output should be shorted at a time.

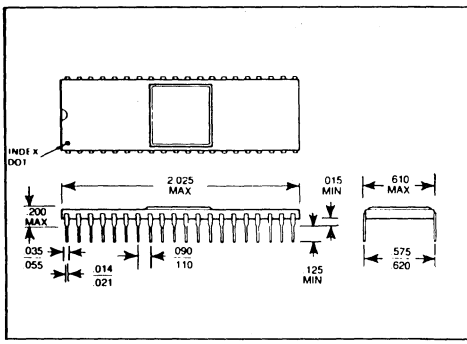
NOTE: 1) Inputs under Chip Disable control when disabled, (V_{IH} applied to CD), are logically disabled and appear as a single TTL Load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically and electrically disconnected and caused to float. The Three-State Output has three stages; (1) Low impedance to V_{CC} (2) Low impedance to GND (3) High impedance OFF ≃ 10 Megohm.

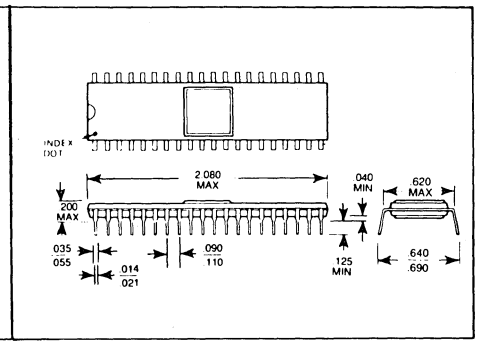
SWITCHING CHARACTERISTICS

($V_{SS} - V_{CC} = 5V$, $V_{DD} = OV$, $V_{GG} = -12V$, $T_A = 25°C$, $C_L = 20$ pf)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	PR1472-00
		DC	640 KHz	PR1472-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
$T_{\overline{CRL}}$	Control Register Load	250 nsec		
$T_{\overline{MHRL}}$	Match-Character Holding Register Load	250 nsec		
$T_{\overline{DRR}}$	Data Received Reset	200 nsec		
$T_{\overline{SFR}}$	Status Flag Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay	500 nsec		
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	



PR1472A CERAMIC PACKAGE



PR1472B PLASTIC PACKAGE

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