PORA

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

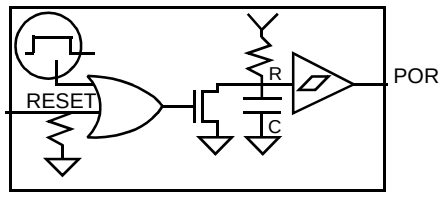
PORA is a power-on-reset.

When power is applied, the POR output is asserted low for at least 2 microseconds after the logic circuits become operational. The active high RESET input also drives the POR signal to its active low state. Since the PORA is a corner function cell the RESET pin must be driven through the core.

For proper operation, user-designed external circuitry must provide a V_{DD} power slew rate of at least one volt per microsecond. This ensures that the reset pulse will be properly output when V_{DD} falls to zero and immediately returns to its valid range.

Logic Symbol

PORA



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Load
RESET	4.4 eql

HDL Syntax

Verilog ..... PORA *inst_name* (RESET, POR);

VHDL..... *inst_name*: PORA port map (RESET, POR);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	1917.7	Eq-load

See page 2-15 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	8	16	23	31 (max)
RESET	POR	t_{PLH}	18289.49				
RESET	POR	t_{PHL}	16.28				

Delay will vary with input conditions. See page 2-17 for interconnect estimates.