PIXELPLUS CO., LTD.

Preliminary
Data sheet

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

PO8030D

Customer

Rev 0.6

Last update : 28. Oct. 2013

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1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Revision History*

Version	Date [D/M/Y]	Notes	Writer
0.0	03/03/2010	*(Preliminary)*	Bo Hyun Moon
0.1	17/08/2010	Customer datasheet	JS SON
0.2	08/11/2010	Added DC	JS SON
0.3	30/11/2011	Added AC characteristics	Heung Seok Park
0.4	14/09/2012	Modified of P.4, 81	Seung Jun Baek
0.5	23/05/2013	Modified HVDD voltage margin. (1.8 ~ 3.3V -> 2.8V or 3.3V)	JunHyuck Lee
0.6	28/10/2013	Modified the Typical Parameter	SangHyun Han

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please send a mail to support@pixelplus.co.kr.

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

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1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Features

▷ 648 x 488 total pixel array with RGB bayer color filters and micro-lens.

▷ Power supply :
AVDD : 2.8V,
DVDD : 1.5V or 1.8V, HVDD : 2.8V or 3.3V

▷ Output formats : CCIR656, 8bit YCbCr422, 8bit RGB Bayer, RGB565, 8bit Mono.

▷ Image processing on chip : lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto black level compensation, auto white balance, auto exposure control and back light compensation.

▷ Max. 30 frames/sec progressive scan @ 24 MHz master clock for VGA.

▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.

▷ VGA / QVGA / QQVGA / CIF / QCIF / QQCIF Scaling.

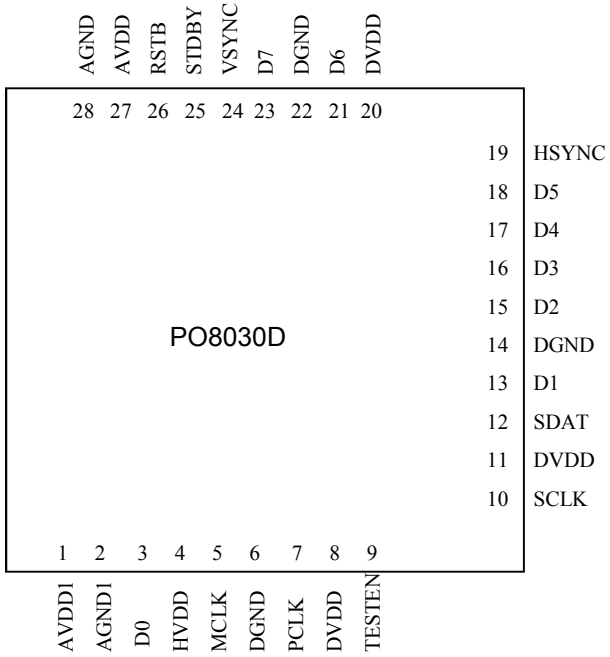
▷ Horizontal / Vertical mirroring.

▷ 50Hz, 60Hz flicker automatic cancellation.

▷ Soft reset.

▷ High Image Quality and High low light performance.

▷ Large angle response.



[Fig. 1] PIN Description (CLCC)

[Table 1] Typical Parameters

Parameter	Typical value
Pixel Size	2.8 um x 2.8 um
Effective Pixel Array	648 x 488
Effective Image Area	1.814 mm x 1.366 mm
Optical Format	1/8 inch
Input Clock frequency	24 MHz
Max. Frame Rate	Variable up to 30fps
Dark Signal	20.5 [mV/sec] @60℃
Sensitivity	1.06 [V/Lux.sec]
Power Consumption	58.7 mW @Dynamic
	4.5 uW @Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 70 [℃]
Dynamic Range	60.3 [dB]
SNR	40.8 [dB]

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	AVDD1	P	Analog VDD1 : 2.8V DC. 0.1uF to AGND1
2	AGND1	P	Analog ground1.
3	D0	O	Bit 0 of data output.
4	HVDD	P	Digital vdd for I/O. Voltage range for all output signals is 0V ~ HVDD. 0.1uF to DGND
5	MCLK	I	Master clock input pad.
6	DGND	P	Digital ground for core circuits.
7	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
8	DVDD	P	Digital vdd for core logic : 1.5/1.8V DC. 0.1uF capacitor to DGND.
9	TESTEN	I	Chip Test Mode enable. User have to connect this terminal to DGND
10	SCLK	I	2-wire serial interface clock input.
11	DVDD	P	Digital vdd for core logic : 1.5/1.8V DC. 0.1uF capacitor to DGND.
12	SDAT	I/O	2-wire serial interface data bus.
13	D1	O	Bit 1 of data output.
14	DGND	P	Digital ground for core.
15	D2	O	Bit 2 of data output.
16	D3	O	Bit 3 of data output.
17	D4	O	Bit4 of data output.
18	D5	O	Bit5 of data output.
19	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
20	DVDD	P	Digital vdd for core logic : 1.5/1.8V DC. 0.1uF capacitor to DGND.
21	D6	O	Bit6 of data output.
22	DGND	P	Digital ground for core.
23	D7	O	Bit 7 of data output.
24	VSYNC	O	Vertical sync : Indicates the start of a new frame.
25	STDBY	I	Power standby mode. When Standby='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<7:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. But it is possible to control internal registers through 2-wire serial interface bus in Standby mode. All registers retain their current values.
26	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
27	AVDD	P	Analog VDD : 2.8V DC. 0.1uF to AGND
28	AGND	P	Analog ground.

[Table 2] Pin Descriptions

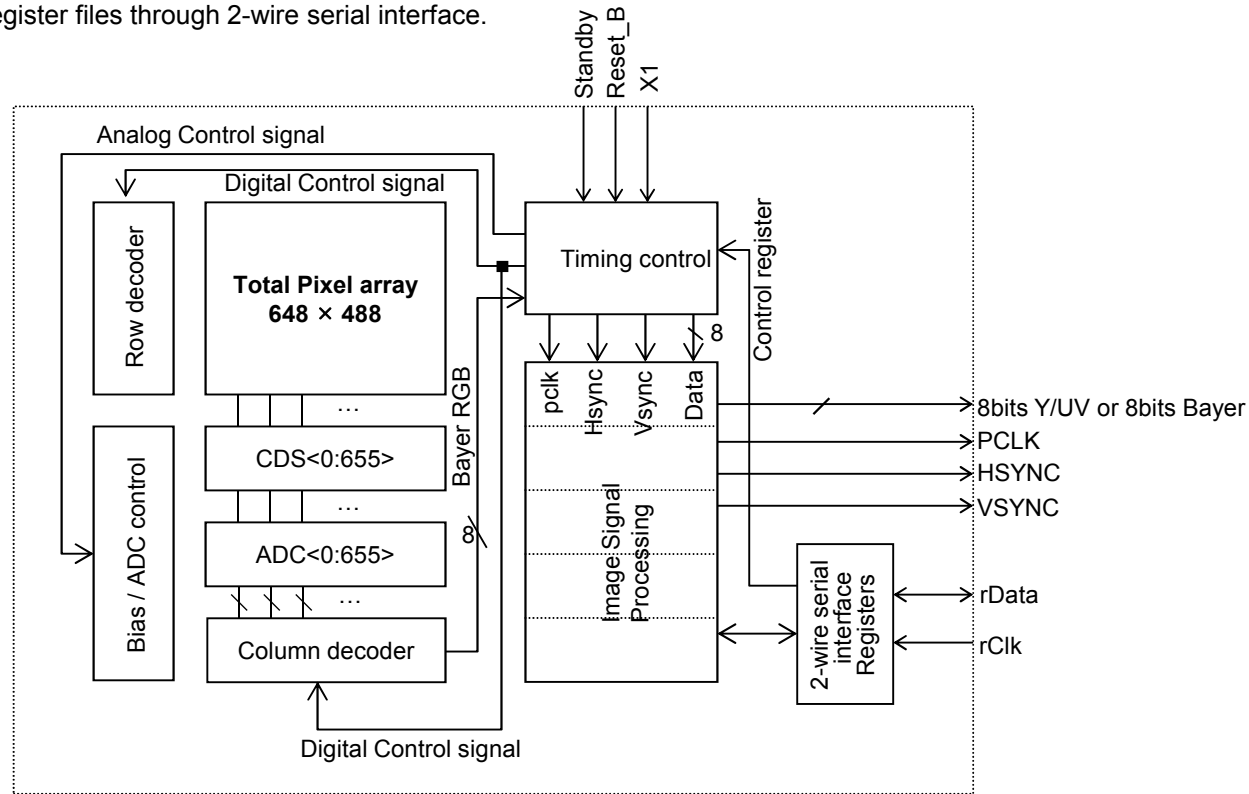
1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Signal Environment

PO8030D has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PO8030D input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ Chip Architecture

PO8030D has 648 x 488 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.

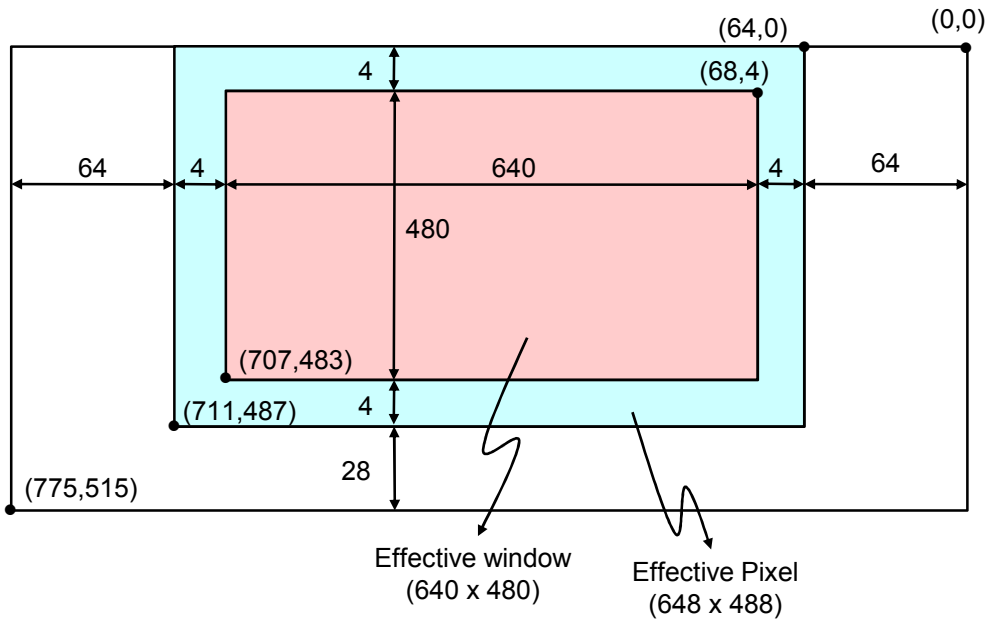


[Fig. 2] Block Diagram

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

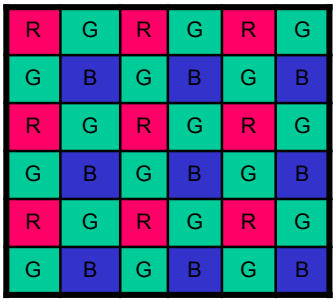
▶ Frame Structure and Windowing

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.A-04h, A-05h)* and *frameheight(Reg.A-06h, A-07h).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Default window array of 640 x 480 pixels is positioned at *(68, 4).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size(frame rate). [Table 3] shows *windowx, y start/stop(Reg.A-08h ~ A-0Fh)* registers value for default window and maximum window.



[Fig. 3] Default data structure of frame and window. (Top view)

▶ Data Formats



[Fig. 4] Bayer Color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PO8030D provides this Bayer pattern RGB data through an 8bit channel. It takes one PCLK to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PO8030D adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 8 bits output pins in such a way RGB565. It takes two PCLK's to pass one pixel RGB data to output bus.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B – Y), \quad V = 0.877 (R – Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

[Fig. 5] 4:2:2 YUV data sequence.

PO8030D supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PO8030D also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

$$C_B = 0.564 (B – Y) + 128$$
$$C_R = 0.713 (R – Y) + 128$$

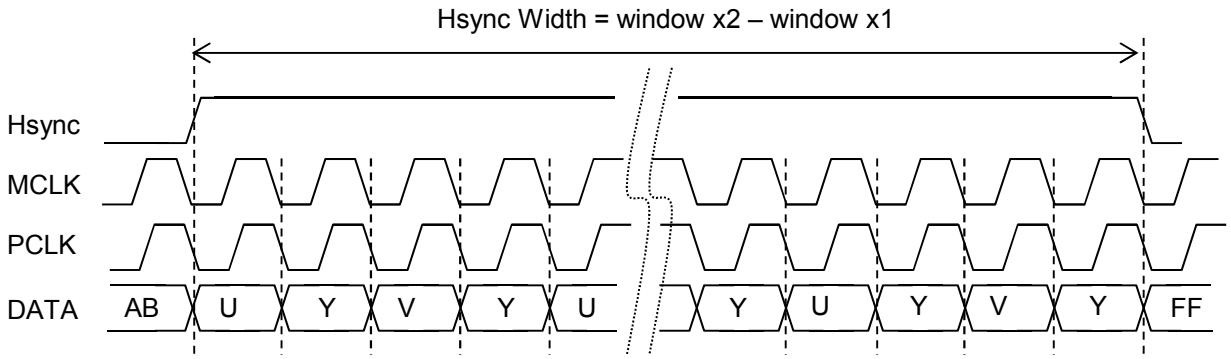
▶ Data and Synchronization Timing

[Fig. 6] shows the default data sequence of PO8030D. In [Fig. 6] Hsync / PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. Hsync can be set to be active high or active low. The sequence default YUV data is [U,Y, V, Y, …] for common even / odd rows.

The width of Hsync can be programmed by *windowx1 / x2(Reg.A-08h, 09h, 0Ch, 0Dh)* and given by

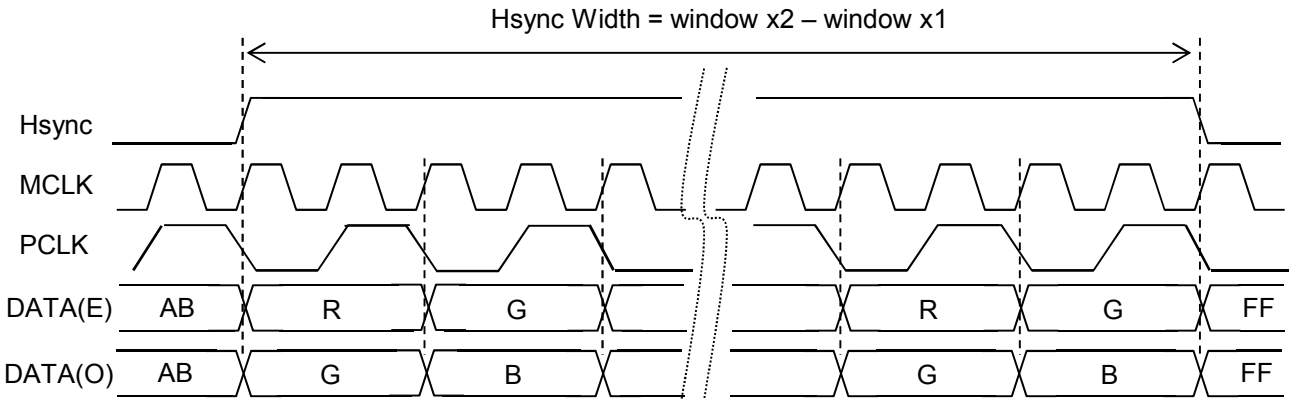
Hsync Width = *windowx2* - *windowx1*

Data value can be selected in Invalid or blanking region .



[Fig. 6] Timing diagram for Hsync, MCLK, PCLK and Data (default)

The default sequence Bayer data is [RGRG…] for even rows and [GBGB…] for odd rows. The data order can be changed by register (*bit7 and bit6 of Reg.B-07h).*



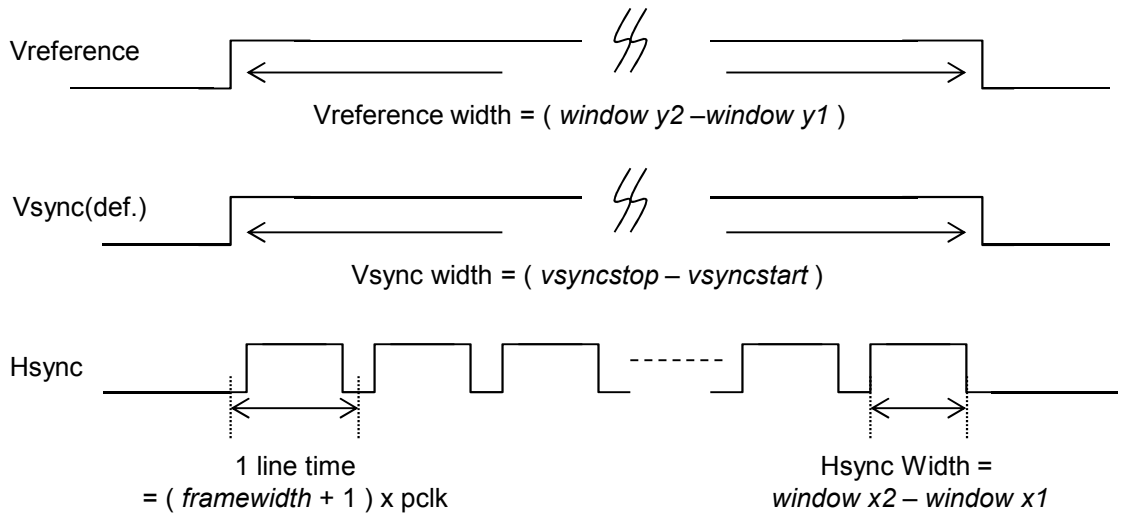
[Fig. 7] Timing diagram for Hsync, MCLK, PCLK and Data (Bayer)

In [Fig. 8], Vsync polarity also can have any combinations possible and can be set to be active high or active low. The width of Vsync can be programmed by *vsyncstart / vsyncstop(Reg.A-10h ~ 13h)* and given by

Vsync Width = (*vsyncstop* – *vsyncstart*).

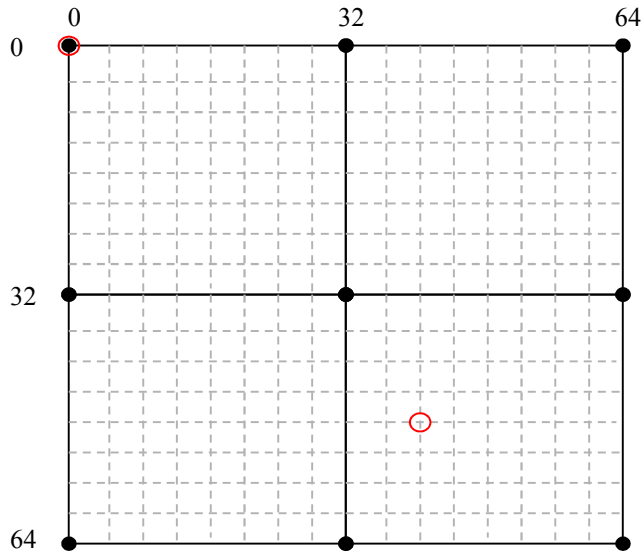
The width of Vreference can be programmed by register *windowy1 / y2(Reg.A-0Ah, 0Bh, 0Eh, 0Fh)* and given by

Vreference width = (*windowy2* - *windowy1*).



[Fig. 8] Timing diagram for Vsync and Hsync

▶ Scaling



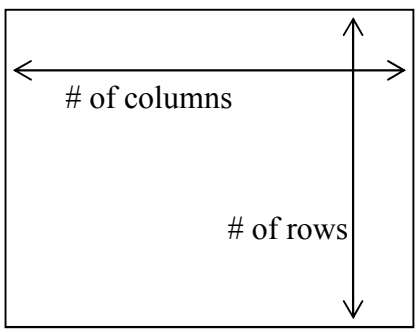
[Fig. 9] Free Scaling

- ● Full image pixel locations
  X points = 32 * M
  Y points = 32 * N
- ○ Scaled image sampling points
  X Sampling points = reg_scale_X * P
  Y Sampling points = reg_scale_Y * Q

← Example
Reg_scale_x = 40
Reg_scale_y = 48

(reg_window_x1, reg_window_y1)

minimum = (1, 1)

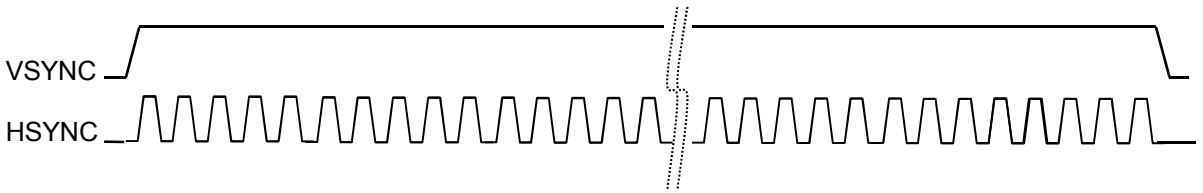


(reg_window_x2, reg_window_y2)

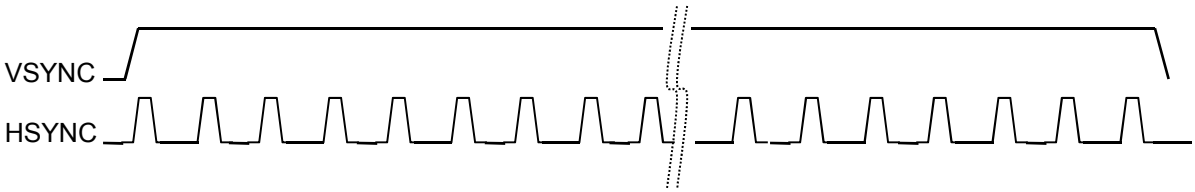
[Fig. 10] Effective Image Size

Effective Image. # of columns = reg_window_x2 - reg_window_x1

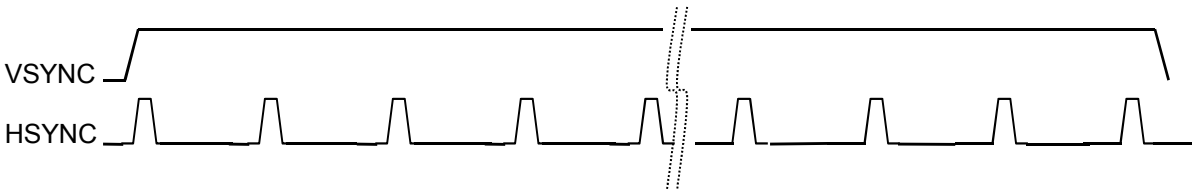
Effective Image. # of rows = reg_window_y2 - reg_window_y2



[No scaling case : default]

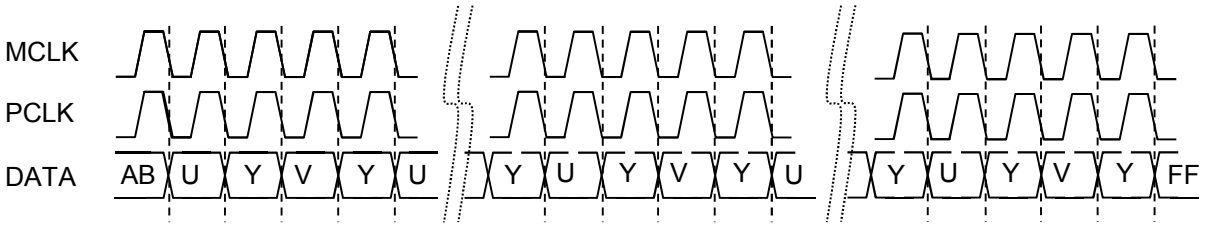


[QVGA scaling case]

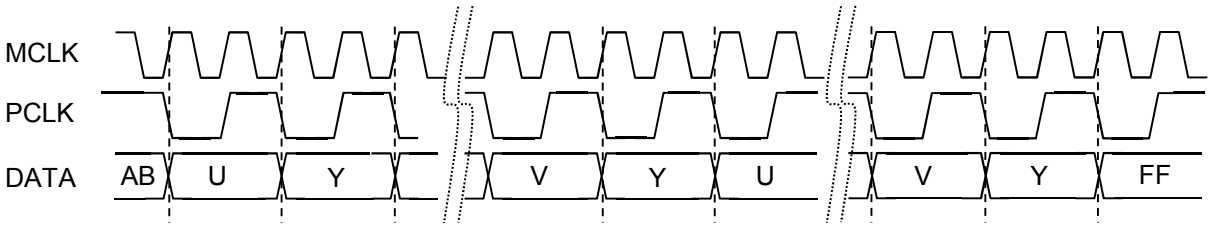


[QQVGA scaling case]

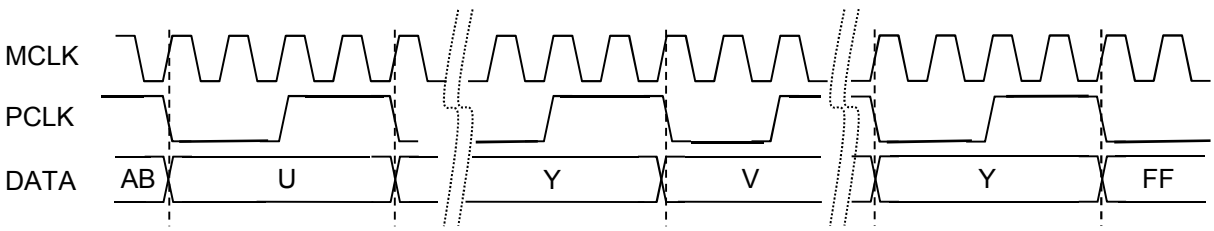
[Fig. 11] Timing diagram for VSYNC and HSYNC (scaling modes)



[No scaling case : default]



[QVGA scaling case]



[QQVGA scaling case]

[Fig. 12] Timing diagram for PCLK and Data (scaling modes)

▶ 2-wire Serial Interface Description

The registers of PO8030D are written and read through the 2-wire Serial Interface. The PO8030D has 2-wire Serial Interface slave. The PO8030D is controlled by the Register Access Clock (SCLK), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PO8030D through the Register Access Data (SDAT) line. The SCLK and SDAT lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCLK pulse is provided by the master. The data must be sGroup During the HIGH period of the SCLK : it can only change when the SCLK is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

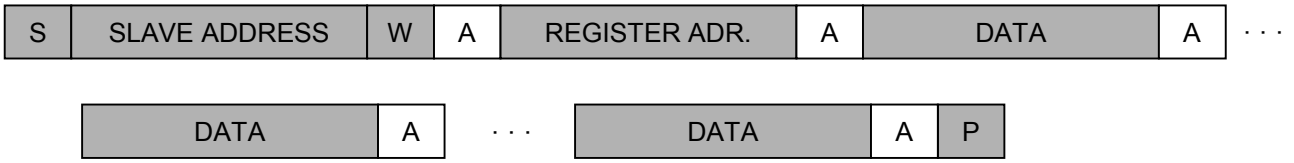
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PO8030D uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

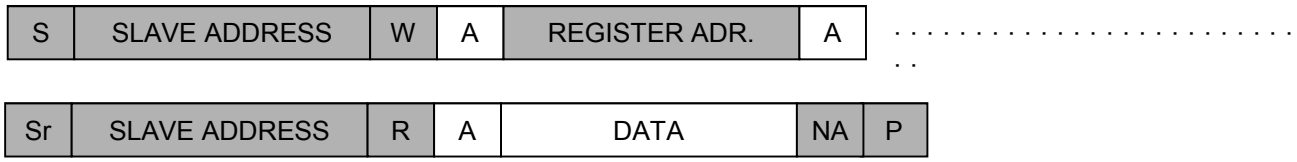
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

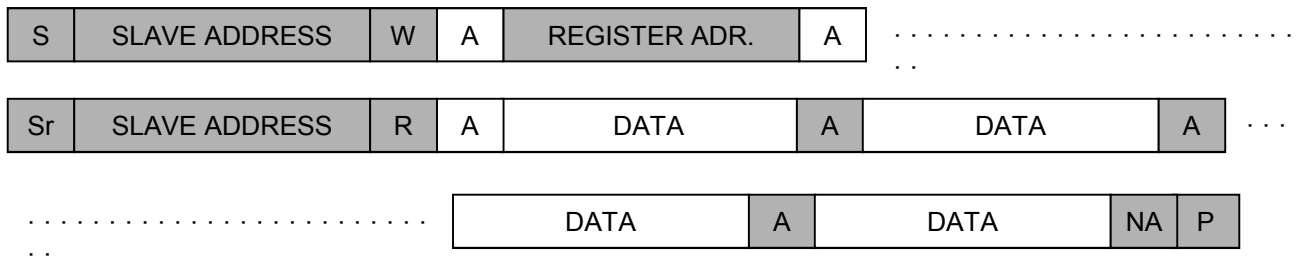
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



S: Start condition. Sr : Repeated Start (Start without preceding stop.)
SLAVE ADDRESS: write address = DCh = 11011100b
read address = DDh = 11011101b
R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	128	80	10000000	RO	0	0	Device ID
1	01	DeviceID_L	48	30	00110000	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	Revision number
3	03	bank	0	00	00000000	RW	5	0	Register group selector
4	04	framewidth_h	3	03	00000011	RW	6	aev	Framewidth
5	05	framewidth_l	7	07	00000111	RW	6	aev	
6	06	frameheight_h	2	02	00000010	RW	6	aev	Frameheight
7	07	frameheight_l	3	03	00000011	RW	6	aev	
8	08	windowx1_h	0	00	00000000	RW	6	aev	Window
9	09	windowx1_l	1	01	00000001	RW	6	aev	
10	0A	windowy1_h	0	00	00000000	RW	6	aev	
11	0B	windowy1_l	1	01	00000001	RW	6	aev	
12	0C	windowx2_h	2	02	00000010	RW	6	aev	
13	0D	windowx2_l	128	80	10000000	RW	6	aev	
14	0E	windowy2_h	1	01	00000001	RW	6	aev	
15	0F	windowy2_l	224	E0	11100000	RW	6	aev	
16	10	vsyncstartrow_h	0	00	00000000	RW	5	0	Vsync generation
17	11	vsyncstartrow_l	10	0A	00001010	RW	5	0	
18	12	vsyncstoprow_h	1	01	00000001	RW	5	0	
19	13	vsyncstoprow_l	234	EA	11101010	RW	5	0	
20	14	vsynccolumn_h	0	00	00000000	RW	5	0	
21	15	vsynccolumn_l	16	10	00010000	RW	5	0	
23	17	inttime_h	0	00	00000000	RW	6	aev	Integration time (line & column)
24	18	inttime_m	128	80	10000000	RW	6	aev	
25	19	inttime_l	0	00	00000000	RW	6	aev	
26	1A	globalgain	0	00	00000000	RW	6	aev	Analog gain
27	1B	digitalgain	64	40	01000000	RW	6	aev	Digital gain
35	23	wb_rgain	94	5E	01011110	RW	6	aev	White balance gain
36	24	wb_ggain	64	40	01000000	RW	6	aev	
37	25	wb_bgain	93	5D	01011101	RW	6	aev	
39	27	redgain_l	0	00	00000000	RW	5	0	Monitoring register

(Group A – continued)

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
53	35	auto_fwx1_h	0	00	00000000	RW	5	0	AE full window selection
54	36	auto_fwx1_l	1	01	00000001	RW	5	0	
55	37	auto_fwx2_h	2	02	00000010	RW	5	0	
56	38	auto_fwx2_l	128	80	10000000	RW	5	0	
57	39	auto_fwy1_h	0	00	00000000	RW	5	0	
58	3A	auto_fwy1_l	1	01	00000001	RW	5	0	
59	3B	auto_fwy2_h	1	01	00000001	RW	5	0	
60	3C	auto_fwy2_l	224	E0	11100000	RW	5	0	
61	3D	auto_cwx1_h	0	00	00000000	RW	5	0	AE center window selection
62	3E	auto_cwx1_l	214	D6	11010110	RW	5	0	
63	3F	auto_cwx2_h	1	01	00000001	RW	5	0	
64	40	auto_cwx2_l	171	AB	10101011	RW	5	0	
65	41	auto_cwy1_h	0	00	00000000	RW	5	0	
66	42	auto_cwy1_l	161	A1	10100001	RW	5	0	
67	43	auto_cwy2_h	1	01	00000001	RW	5	0	
68	44	auto_cwy2_l	64	40	01000000	RW	5	0	
91	5B	pad_control	64	40	01000000	RW	5	0	Pad control
92	5C	trap	0	00	00000000	RW	5	0	Trap
105	69	softreset	0	00	00000000	RW	5	0	Soft reset
106	6A	clkdiv	0	00	00000000	RW	6	aev	Clock divider

(Group A – continued)

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
108	6C	bayer_control_01	0	00	00000000	RW	6	aev	Bayer control

(Group A – continued)

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
223	DF	adcoffset	36	24	00100100	RW	6	aev	ADC offset value
225	E1	front_black_ref0	0	00	00000000	RW	5	0	Manual black level fitting reference
226	E2	front_black_ref1	0	00	00000000	RW	5	0	
227	E3	front_black_ref2	0	00	00000000	RW	5	0	
228	E4	front_black_ref3	0	00	00000000	RW	5	0	
229	E5	front_black_ref4	0	00	00000000	RW	5	0	
230	E6	front_black_ref5	0	00	00000000	RW	5	0	
231	E7	front_black_min	255	FF	11111111	RW	5	0	
232	E8	front_black_max	127	7F	01111111	RW	5	0	
233	E9	front_black	0	00	00000000	RW	6	aev	Manual black level
235	EB	lens_coffset	0	00	00000000	RO	0	0	Lens address offset
236	EC	lens_roffset	0	00	00000000	RO	0	0	

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
256	00	DeviceID_H	128	80	10000000	RO	0	0	Device ID
257	01	DeviceID_L	48	30	00110000	RO	0	0	
258	02	RevNumber	0	00	00000000	RO	0	0	Revision number
259	03	bank	0	00	00000000	RW	5	0	Register group selector
260	04	isp_func_0	247	F7	11110111	RW	6	aev	Isp function control
261	05	isp_func_1	251	FB	11111011	RW	6	aev	
262	06	isp_func_2	0	00	00000000	RW	6	aev	
320	40	lens_gainr	0	00	00000000	RW	6	aev	Lens gain
321	41	lens_gaing	0	00	00000000	RW	6	aev	
323	43	lens_gainb	0	00	00000000	RW	6	aev	Lens gain
334	4E	format	0	00	00000000	RW	6	aev	Format control
337	51	dpc_offset	20	14	00010100	RW	5	0	DPC offset
350	5E	edge_gain	32	20	00100000	RW	5	0	Edge gain
354	62	ccr_m11	69	45	01000101	RW	5	0	Color correction matrix value
355	63	ccr_m12	160	A0	10100000	RW	5	0	
356	64	ccr_m13	133	85	10000101	RW	5	0	
357	65	ccr_m21	143	8F	10001111	RW	5	0	
358	66	ccr_m22	69	45	01000101	RW	5	0	
359	67	ccr_m23	150	96	10010110	RW	5	0	
360	68	ccr_m31	132	84	10000100	RW	5	0	
361	69	ccr_m32	148	94	10010100	RW	5	0	
362	6A	ccr_m33	56	38	00111000	RW	5	0	
365	6D	gm_y0	0	00	00000000	RW	5	0	Gamma reference
366	6E	gm_y1	11	0B	00001011	RW	5	0	
367	6F	gm_y2	23	17	00010111	RW	5	0	
368	70	gm_y3	34	22	00100010	RW	5	0	
369	71	gm_y4	46	2E	00101011	RW	5	0	

(Group B – continued)

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
370	72	gm_y5	64	40	01000000	RW	5	0	Gamma reference
371	73	gm_y6	80	50	01010000	RW	5	0	
372	74	gm_y7	110	6E	01101110	RW	5	0	
373	75	gm_y8	136	88	10001000	RW	5	0	
374	76	gm_y9	174	AE	10101110	RW	5	0	
375	77	gm_y10	202	CA	11001010	RW	5	0	
376	78	gm_y11	220	DC	11011100	RW	5	0	
377	79	gm_y12	236	EC	11101100	RW	5	0	
378	7A	gm_y13	246	F6	11110110	RW	5	0	
379	7B	gm_y14	255	FF	11111111	RW	5	0	
399	8F	sketch_offset	140	8C	10001100	RW	6	aev	Sketch offset
403	93	scale_x	32	20	00100000	RW	6	aev	Scale control
404	94	scale_y	32	20	00100000	RW	6	aev	
405	95	scale_th_h	0	00	00000000	RW	6	aev	
406	96	scale_th_l	10	0A	00001010	RW	6	aev	
410	9A	auto_off	0	00	0	RW	5	0	Auto off (MCU off)
413	9D	ycontrast	64	40	01000000	RW	6	aev	Y contrast
414	9E	ybrightness	0	00	00000000	RW	6	aev	Y brightness
415	9F	y_max	0	00	00000000	RO	0	0	Y max clamping
431	AF	sync_ccirFF	255	FF	11111111	RW	5	0	CCIR656 Control
432	B0	sync_ccir00	0	00	00000000	RW	5	0	
433	B1	sync_ccir80	128	80	10000000	RW	5	0	
434	B2	sync_ccir10	16	10	00010000	RW	5	0	
435	B3	sync_blankSAV	182	B6	10110110	RW	5	0	
436	B4	sync_blankEAV	157	9D	10011101	RW	5	0	
437	B5	sync_activSAV	171	AB	10101011	RW	5	0	
438	B6	sync_activEAV	128	80	10000000	RW	5	0	
439	B7	sync_control_0	0	00	00000000	RW	6	aev	Sync control
440	B8	sync_control_1	0	00	00000000	RW	6	aev	
441	B9	sync_control_2	0	00	00000000	RW	6	aev	

(Group B – continued)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
496	F0	fd_period_a_h	0	00	00000000	RW	5	0	Flicker period for A state
497	F1	fd_period_a_m	128	80	10000000	RW	5	0	
498	F2	fd_period_a_l	221	DD	11011101	RW	5	0	
499	F3	fd_period_b_h	0	00	00000000	RW	5	0	Flicker period for B state
500	F4	fd_period_b_m	154	9A	10011010	RW	5	0	
501	F5	fd_period_b_l	163	A3	10100011	RW	5	0	

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
512	00	DeviceID_H	128	80	10000000	RO	0	0	Device ID
513	01	DeviceID_L	48	30	00110000	RO	0	0	
514	02	RevNumber	0	00	00000000	RO	0	0	Revision number
515	03	bank	0	00	00000000	RW	5	0	Register group selector
516	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control
518	06	auto_control_3	0	00	00000000	RW	6	autov	
523	0B		238	EE	11101110	RW	5	0	Event control
530	12	exposure_t	0	00	00000000	RW	6	autov	Exposure
531	13	exposure_h	0	00	00000000	RW	6	autov	
532	14	exposure_m	128	80	10000000	RW	6	autov	
533	15	exposure_l	0	00	00000000	RW	6	autov	
555	2B	ae_ysat1	208	D0	11010000	RW	6	autov	Y saturation threshold
556	2C	ae_ysat2	208	D0	11010000	RW	6	autov	Rgb saturation threshold
557	2D	sratio_weight	8	08	00001000	RW	5	0	Saturation ratio center weight
558	2E	sratio	0	00	00000000	RW	5	0	Saturation ratio for monitoring
560	30	ae_weight_c	12	0C	00001100	RW	5	0	Ae center weight
561	31	ae_weight_p	52	34	00110100	RW	5	0	Ae peripheral weight

(Group C – continued)

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group C

GROUP C										
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
563	33	ymean_ref0	16	10	00010000	RW	5	0	Ymean extention reference
564	34	ymean_ref1	16	10	00010000	RW	5	0	
565	35	ymean_ref2	16	10	00010000	RW	5	0	
566	36	ymean_ref3	16	10	00010000	RW	5	0	
567	37	ymean_h	0	00	00000000	RW	5	0	Ymean
568	38	ymean_l	128	80	10000000	RW	5	0	
570	3A	max_yt1	112	70	01110000	RW	6	autov	Min / max ytarget control reference
571	3B	max_yt2	112	70	01110000	RW	6	autov	
572	3C	min_yt1	112	70	01110000	RW	6	autov	
573	3D	min_yt2	112	70	01110000	RW	6	autov	
574	3E	gg_ref0	16	10	00010000	RW	6	autov	
575	3F	gg_ref1	64	40	01000000	RW	6	autov	
576	40	sratio_ref0	0	00	00000000	RW	6	autov	Ytarget control reference
577	41	sratio_ref1	0	00	00000000	RW	6	autov	
578	42	sratio_ref2	0	00	00000000	RW	6	autov	
579	43	sratio_ref3	0	00	00000000	RW	6	autov	
580	44	yt_step	8	08	00001000	RW	5	0	
581	45	ytarget	112	70	01110000	RW	5	0	Ytaget
582	46	user_wyt	128	80	10000000	RW	6	autov	User wyt
584	48	ae_up_speed	8	08	00001000	RW	6	autov	Ae speed control
585	49	ae_down_speed	12	0C	00001100	RW	6	autov	
586	4A	ae_lock	2	02	00000010	RW	6	autov	AE lock range
588	4C	auto_flag	0	00	00000000	RW	5	0	Auto flag
598	56	awb_p1Ax	0	00	00000000	RW	5	0	Awb sampling range selection
599	57	awb_p1Ay	255	FF	11111111	RW	5	0	
600	58	awb_p2Ax	255	FF	11111111	RW	5	0	
601	59	awb_p2Ay	0	00	00000000	RW	5	0	
602	5A	awb_osAx	255	FF	11111111	RW	5	0	
603	5B	awb_osAy	255	FF	11111111	RW	5	0	
604	5C	awb_slopeA	0	00	00000000	RW	5	0	
605	5D	awb_p1Bx	0	00	00000000	RW	5	0	
606	5E	awb_p1By	255	FF	11111111	RW	5	0	
607	5F	awb_p2Bx	255	FF	11111111	RW	5	0	
608	60	awb_p2By	0	00	00000000	RW	5	0	
609	61	awb_osBx	255	FF	11111111	RW	5	0	
610	62	awb_osBy	255	FF	11111111	RW	5	0	
611	63	awb_slopeB	0	00	00000000	RW	5	0	
612	64	awb_maxc	248	F8	11111000	RW	5	0	
613	65	awb_minc	0	00	00000000	RW	5	0	
614	66	awb_sfcount	255	FF	11111111	RW	5	0	
616	68	awb_weight_c	21	15	00010101	RW	5	0	awb weight control

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
617	69	awb_weight_p	43	2B	00101011	RW	5	0	awb weight control
618	6A	awb_wspeed	4	04	00000100	RW	5	0	Awb weight control
620	6C	rg_ratio_a	128	80	10000000	RW	5	0	Target awb ratio fitting reference
621	6D	bg_ratio_a	128	80	10000000	RW	5	0	
622	6E	rg_ratio_b	128	80	10000000	RW	5	0	
623	6F	bg_ratio_b	128	80	10000000	RW	5	0	
624	70	rg_ratio_c	128	80	10000000	RW	5	0	
625	71	bg_ratio_c	128	80	10000000	RW	5	0	
626	72	ratio_axis_a	64	40	01000000	RW	5	0	
627	73	ratio_axis_b	80	50	01010000	RW	5	0	
628	74	ratio_axis_c	96	60	01100000	RW	5	0	
632	78	awb_lock	2	02	00000010	RW	5	0	Awb lock range
633	79	awb_speed	8	08	00001000	RW	5	0	Awb speed
635	7B	awb_rgain_min1	0	00	00000000	RW	5	0	Awb gain min / max clamping control reference
636	7C	awb_rgain_min2	0	00	00000000	RW	5	0	
637	7D	awb_rgain_max1	255	FF	11111111	RW	5	0	
638	7E	awb_rgain_max2	255	FF	11111111	RW	5	0	
639	7F	awb_bgain_min1	0	00	00000000	RW	5	0	
640	80	awb_bgain_min2	0	00	00000000	RW	5	0	
641	81	awb_bgain_max1	255	FF	11111111	RW	5	0	
642	82	awb_bgain_max2	255	FF	11111111	RW	5	0	
643	83	awb_cmp_th1_h	2	02	00000010	RW	5	0	
644	84	awb_cmp_th1_m	3	03	00000011	RW	5	0	
645	85	awb_cmp_th2_h	4	04	00000100	RW	5	0	
646	86	awb_cmp_th2_m	6	06	00000110	RW	5	0	
648	88	cs11_a	37	25	00100101	RW	5	0	Cs matrix fitting reference
649	89	cs12_a	0	00	00000000	RW	5	0	
650	8A	cs21_a	0	00	00000000	RW	5	0	
651	8B	cs22_a	37	25	00100101	RW	5	0	
652	8C	cs11_b	37	25	00100101	RW	5	0	
653	8D	cs12_b	0	00	00000000	RW	5	0	
654	8E	cs21_b	0	00	00000000	RW	5	0	
655	8F	cs22_b	37	25	00100101	RW	5	0	
656	90	cs11_c	37	25	00100101	RW	5	0	
657	91	cs12_c	0	00	00000000	RW	5	0	
658	92	cs21_c	0	00	00000000	RW	5	0	
659	93	cs22_c	37	25	00100101	RW	5	0	
660	94	lens_gainr_a	0	00	00000000	RW	5	0	Lens gain fitting reference
661	95	lens_gainb_a	0	00	00000000	RW	5	0	
662	96	lens_gainr_b	0	00	00000000	RW	5	0	
663	97	lens_gainb_b	0	00	00000000	RW	5	0	
664	98	lens_gainr_c	0	00	00000000	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
665	99	lens_gainb_c	0	00	00000000	RW	5	0	Lens gain fitting reference
666	9A	axis_a	0	00	00000000	RW	5	0	Cs matrix / lens gain fitting reference
667	9B	axis_b	2	02	00000010	RW	5	0	
668	9C	axis_c	0	00	00000000	RW	5	0	
669	9D	user_cs	48	30	00110000	RW	5	0	User cs gain
670	9E	cs11	0	00	00000000	RW	6	aev	Cs matrix
671	9F	cs12	66	42	01000010	RW	6	aev	
672	A0	cs21	0	00	00000000	RW	6	aev	
673	A1	cs22	106	6A	01101010	RW	6	aev	
675	A3	dark_lens0	0	00	00000000	RW	5	0	Lens dark filter reference
678	A6	dark_lens1	0	00	00000000	RW	5	0	Lens dark filter reference
679	A7	dark_lens2	0	00	00000000	RW	5	0	
680	A8	dark_lens_max	0	00	00000000	RW	5	0	
681	A9	dark_lens	0	00	00000000	RW	6	aev	Lens dark filter result
682	AA	dark_dpc_p0	0	00	00000000	RW	5	0	Dpc_p drak filter reference
685	AD	dark_dpc_p1	0	00	00000000	RW	5	0	Dpc_p drak filter reference
686	AE	dark_dpc_p2	0	00	00000000	RW	5	0	
687	AF	dark_dpc_p_max	0	00	00000000	RW	5	0	
688	B0	dark_dpc_p	0	00	00000000	RW	6	aev	Dpc_p dark filter result
689	B1	dark_dpc_n0	0	00	00000000	RW	5	0	Dpc_n dark filter reference
692	B4	dark_dpc_n1	0	00	00000000	RW	5	0	Dpc_n dark filter reference
693	B5	dark_dpc_n2	0	00	00000000	RW	5	0	
694	B6	dark_dpc_n_max	0	00	00000000	RW	5	0	
695	B7	dark_dpc_n	0	00	00000000	RW	6	aev	Dpc_n dark filter result
716	CC	dir_offset	16	10	00010000	RW	6	aev	Dir offset dark filter result
717	CD	dark_edgemax_p0	127	7F	01111111	RW	5	0	Edgemax_p dark filter reference
720	D0	dark_edgemax_p1	127	7F	01111111	RW	5	0	Edgemax_p dark filter reference
721	D1	dark_edgemax_p2	127	7F	01111111	RW	5	0	
722	D2	darkedgemax_p_min	127	7F	01111111	RW	5	0	
723	D3	dark_edgemax_p	127	7F	01111111	RW	6	aev	Edgemax_p dark filter result
724	D4	dark_edgemax_m0	127	7F	01111111	RW	5	0	Edgemax_m dark filter reference
727	D7	dark_edgemax_m1	127	7F	01111111	RW	5	0	Edgemax_m dark filter reference
728	D8	dark_edgemax_m2	127	7F	01111111	RW	5	0	
729	D9	darkedgemax_m_min	127	7F	01111111	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
730	DA	dark_edgemax_m	127	7F	01111111	RW	6	aev	Edgemax_m dark filter result
737	E1	intp	0	00	00000000	RW	6	aev	Intp dark filter result
738	E2	dark_ccr0	0	00	00000000	RW	5	0	Ccr dark filter reference
741	E5	dark_ccr1	32	20	00100000	RW	5	0	Ccr dark filter reference
742	E6	dark_ccr2	48	30	00110000	RW	5	0	
743	E7	dark_ccr_max	32	20	00100000	RW	5	0	
744	E8	dark_ccr	0	00	00000000	RW	6	aev	Ccr dark filter result
745	E9	dark_gm0	16	10	00010000	RW	5	0	Gm dark filter reference
748	EC	dark_gm1	16	10	00010000	RW	5	0	Gm dark filter reference
749	ED	dark_gm2	16	10	00010000	RW	5	0	
750	EE	dark_gm_max	16	10	00010000	RW	5	0	
751	EF	dark_gm	16	10	00010000	RW	6	aev	Gm dark filter result
759	F7	dark_edge_th0	2	02	00000010	RW	5	0	Edgeth dark filter reference
762	FA	dark_edge_th1	4	04	00000100	RW	5	0	Edgeth dark filter reference
763	FB	dark_edge_th2	8	08	00001000	RW	5	0	
764	FC	dark_edge_th_max	8	08	00001000	RW	5	0	
765	FD	dark_edge_th	2	02	00000010	RW	6	aev	Edgeth dark filter result

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
768	00	DeviceID_H	128	80	10000000	RO	0	0	Device ID
769	01	DeviceID_L	48	30	00110000	RO	0	0	
770	02	RevNumber	0	00	00000000	RO	0	0	Revision number
771	03	bank	0	00	00000000	RW	5	0	Register group selector
772	04	m_tg_frameheight_H	0	00	00000000	RO	0	0	Tg framehieht monitoring
773	05	m_tg_frameheight_L	0	00	00000000	RO	0	0	
774	06	tgglbgain	0	00	00000000	RO	0	0	Tg globalgain monitoring
775	07	m_inttime_tgout_H	0	00	00000000	RO	0	0	Tg integration time monitoring
776	08	m_inttime_tgout_M	0	00	00000000	RO	0	0	
777	09	m_inttime_tgout_L	0	00	00000000	RO	0	0	
778	0A	tg_errors	0	00	00000000	RO	0	0	Tg error monitoring
792	18	num_center_byte2	0	00	00000000	RO	0	0	Number of pixel in ae center window
793	19	num_center_byte1	0	00	00000000	RO	0	0	
794	1A	num_center_byte0	0	00	00000000	RO	0	0	
795	1B	num_peri_byte2	0	00	00000000	RO	0	0	Number of pixel in ae peripheral window
796	1C	num_peri_byte1	0	00	00000000	RO	0	0	
797	1D	num_peri_byte0	0	00	00000000	RO	0	0	
798	1E	num_sat_c_byte2	0	00	00000000	RO	0	0	Number of saturation pixel in ae center window
799	1F	num_sat_c_byte1	0	00	00000000	RO	0	0	
800	20	num_sat_c_byte0	0	00	00000000	RO	0	0	
801	21	num_sat_peri_byte2	0	00	00000000	RO	0	0	Number of saturation pixel in ae peripheral window
802	22	num_sat_peri_byte1	0	00	00000000	RO	0	0	
803	23	num_sat_peri_byte0	0	00	00000000	RO	0	0	
804	24	sum_center_byte3	0	00	00000000	RO	0	0	Sumation of pixel in ae center window
805	25	sum_center_byte2	0	00	00000000	RO	0	0	
806	26	sum_center_byte1	0	00	00000000	RO	0	0	
807	27	sum_center_byte0	0	00	00000000	RO	0	0	
808	28	sum_peri_byte3	0	00	00000000	RO	0	0	Sumation of pixle in ae peripheral window
809	29	sum_peri_byte2	0	00	00000000	RO	0	0	
810	2A	sum_peri_byte1	0	00	00000000	RO	0	0	
811	2B	sum_peri_byte0	0	00	00000000	RO	0	0	
812	2C	auto_fcnt	0	00	00000000	RO	0	0	Auto frame counter monitoring
813	2D	monitor_sfcount	0	00	00000000	RO	0	0	Awb sfcounter monitoring
815	2F	awb_flag	0	00	00000000	RO	0	0	Awb flack monitoring
816	30	avg_r_c	0	00	00000000	RO	0	0	Average of rgb in awb center window
817	31	avg_g_c	0	00	00000000	RO	0	0	
818	32	avg_b_c	0	00	00000000	RO	0	0	
819	33	avg_r_p	0	00	00000000	RO	0	0	Average of rgb in awb peripheral window
820	34	avg_g_p	0	00	00000000	RO	0	0	
821	35	avg_b_p	0	00	00000000	RO	0	0	
822	36	m_awb_weight_c	0	00	00000000	RO	0	0	Current awb weight monitoring
823	37	m_awb_weight_p	0	00	00000000	RO	0	0	
825	39	monitor_proximity	0	00	00000000	RO	0	0	Proximity monitoring

(Group D – continued)

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
841	49	lens_x	0	00	00000000	RW	5	0	Lens center position
842	4A	lens_y	0	00	00000000	RW	5	0	
843	4B	lens_scale	81	51	01010001	RW	5	0	Lens scale
847	4F	cnt_init	0	00	00000000	RW	5	0	Counter reset
848	50	rcount_init_h	0	00	00000000	RW	5	0	Rcount reset value
849	51	rcount_init_l	0	00	00000000	RW	5	0	
850	52	ccount_init_h	0	00	00000000	RW	5	0	Ccount reset value
851	53	ccount_init_l	0	00	00000000	RW	5	0	
855	57	dark_ycontrast0	64	40	01000000	RW	5	0	Dark Y contrast fitting control
856	58	dark_ycontrast1	64	40	01000000	RW	5	0	
857	59	dark_ycontrast2	64	40	01000000	RW	5	0	
859	5B	dark_ybrightness0	0	00	00000000	RW	5	0	Dark Y brightness fitting control
860	5C	dark_ybrightness1	0	00	00000000	RW	5	0	
861	5D	dark_ybrightness2	0	00	00000000	RW	5	0	

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. This will initialize all of the registers to their default values.

(0~3) DeviceID, RevNumber, Register Selector

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	128	80	10000000	RO	0	0	Device ID
1	01	DeviceID_L	48	30	00110000	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	Revision number
3	03	bank	0	00	00000000	RW	5	0	Register group selector

▷ DeviceID, RevNumber, Register Selector

Indicate PO8030D device ID, reversion number, Register Select.
Common registers of Group A(00h) / B(01h) / C(02h) / D(03h).

(4~7) FrameWidth, FrameHeight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
4	04	framewidth_h	3	03	00000011	RW	6	aev	Framewidth
5	05	framewidth_l	7	07	00000111	RW	6	aev	
6	06	frameheight_h	2	02	00000010	RW	6	aev	Frameheight
7	07	frameheight_l	3	03	00000011	RW	6	aev	

▷ FrameWidth, FrameHeight

FrameWidth is the number of columns to be counted during one line time. FrameHeight is the number of rows. Column(Row) counter value is incremented 1 by 1 until it reaches FrameWidth(FrameHeight), then it is reset to 0. FrameHeight and FrameWidth determines the frame rate. Frame rate is given as follows.

Frame Rate = freq (pclk) / ((FrameHeight +1) X (FrameWidth+1))

For example, If Pixel clock (pclk) = 12 MHz, FrameHeight = 776d and FrameWidth = 516d. then, the frame rate is 30 fps for VGA Mode. If you double the Frame Height , you cut the frame rate by half.

< Group A >

(8~15) Window

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
8	08	windowx1_h	0	00	00000000	RW	6	aev	Window
9	09	windowx1_l	1	01	00000001	RW	6	aev	
10	0A	windowy1_h	0	00	00000000	RW	6	aev	
11	0B	windowy1_l	1	01	00000001	RW	6	aev	
12	0C	windowx2_h	2	02	00000010	RW	6	aev	
13	0D	windowx2_l	128	80	10000000	RW	6	aev	
14	0E	windowy2_h	1	01	00000001	RW	6	aev	
15	0F	windowy2_l	224	E0	11100000	RW	6	aev	

▷ Window

Window can be defined by 4 parameters : WindowX1, WindowY1, WindowX2, and WindowY2. Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. Hsync signal indicates if the image data output is from a pixel that lies within the window area or not. Output data stream does not stop for pixels lying outside the window : just the Hsync signal is de-asserted.

The actual window position in the frame is given as

upper right corner = (Window X1 + 1, Window Y1)

lower left corner = (Window X2, Window Y2 - 1)

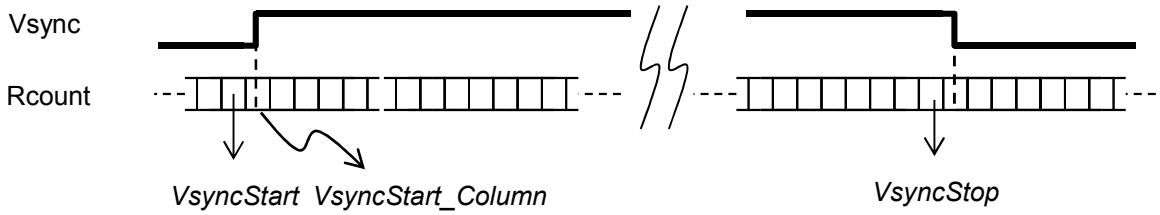
All the coordinates are with respect to the maximum window origin (0, 0) of <Fig. 3>. Window position and size are with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

(16~21) Vsync Row Start/Stop, Vsync Column Start

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
16	10	vsyncstartrow_h	0	00	00000000	RW	5	0	Vsync generation
17	11	vsyncstartrow_l	10	0A	00001010	RW	5	0	
18	12	vsyncstoprow_h	1	01	00000001	RW	5	0	
19	13	vsyncstoprow_l	234	EA	11101010	RW	5	0	
20	14	vsynccolumn_h	0	00	00000000	RW	5	0	
21	15	vsynccolumn_l	16	10	00010000	RW	5	0	

▷ Output Vsync Generation

Output Vsync Row Start/Stop points and Column Start point



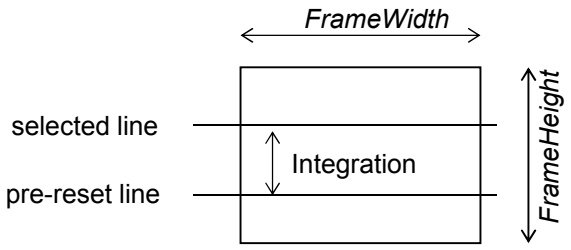
< Group A >

(23~25) Integration time

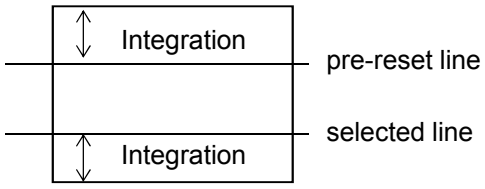
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
23	17	inttime_h	0	00	00000000	RW	6	aev	Integration time (line & column)
24	18	inttime_m	128	80	10000000	RW	6	aev	
25	19	inttime_l	0	00	00000000	RW	6	aev	

▷ Integration time

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. 17h and 18h registers indicate how many line times the integration will continue until they are all reset. 19h register further sub-divides one line time into 256 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time. As the row counter value is incremented from 0 to FrameHeight, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PO8030D is 1/ 256 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line



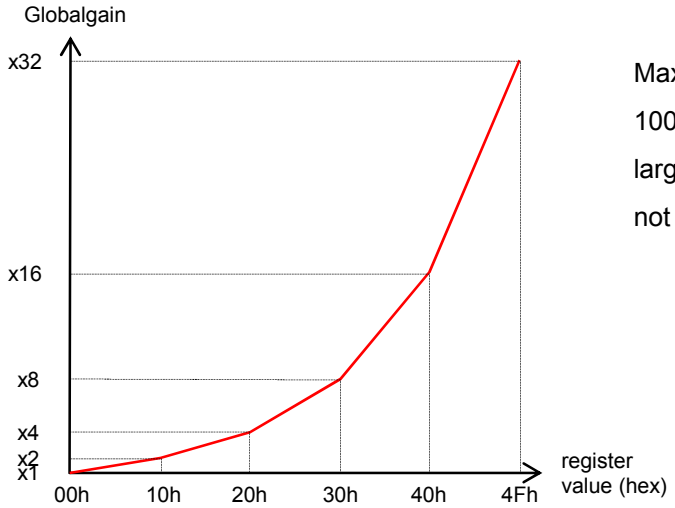
Case 2. Select line preceding reset line

(26) Global gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
26	1A	globalgain	0	00	00000000	RW	6	aev	Analog gain

▷ **Global gain**

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of GlobalGain. The relation between GlobalGain and amplification factor is shown in the picture below.



Maximum value of *GlobalGain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.

(27) Digital gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
27	1B	digitalgain	64	40	01000000	RW	6	aev	Digital gain

▷ **Daigital gain**

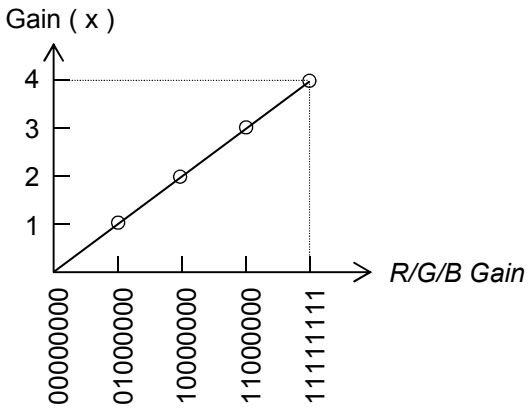
digitalgain[7:6] : Integer

digitalgain[5:0] : Fraction

(35~37) White balance gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
35	23	wb_rgain	94	5E	01011110	RW	6	aev	White balance gain
36	24	wb_ggain	64	40	01000000	RW	6	aev	
37	25	wb_bgain	93	5D	01011101	RW	6	aev	

▷ **white balance red/green/blue gain**



R / G / B gain can be used for white balance control. Bit7 of *R/G/B Gain* is weighted by 2, bit6 by 1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, … respectively. That is, *R/G/B gain* is a binary number with decimal point between bit6 and bit5.

(39,41) White balance red/blue

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
39	27	redgain_l	0	00	00000000	RW	5	0	Monitoring register
41	29	blugain_l	0	00	00000000	RW	5	0	Monitoring register

▷ **white balance red/blue gain (fraction bit)**

Read only registers.

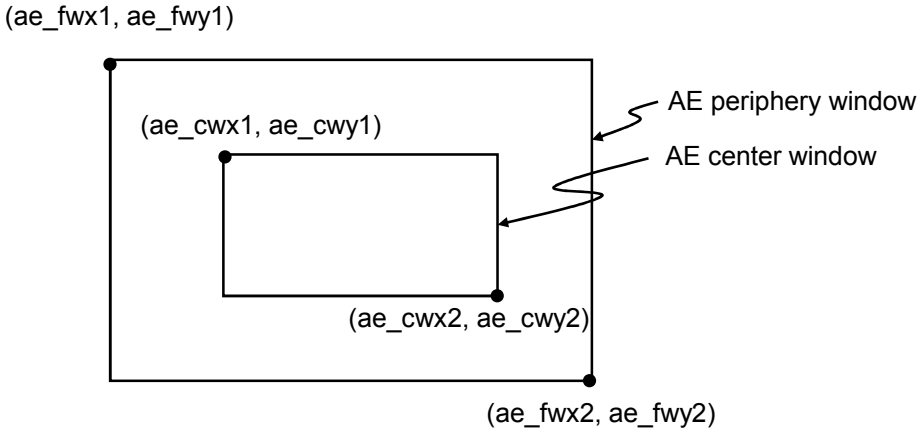
< Group A >

(53~68) AE windows

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
53	35	auto_fwx1_h	0	00	00000000	RW	5	0	AE full window selection
54	36	auto_fwx1_l	1	01	00000001	RW	5	0	
55	37	auto_fwx2_h	2	02	00000010	RW	5	0	
56	38	auto_fwx2_l	128	80	10000000	RW	5	0	
57	39	auto_fwy1_h	0	00	00000000	RW	5	0	
58	3A	auto_fwy1_l	1	01	00000001	RW	5	0	
59	3B	auto_fwy2_h	1	01	00000001	RW	5	0	
60	3C	auto_fwy2_l	224	E0	11100000	RW	5	0	
61	3D	auto_cwx1_h	0	00	00000000	RW	5	0	AE center window selection
62	3E	auto_cwx1_l	214	D6	11010110	RW	5	0	
63	3F	auto_cwx2_h	1	01	00000001	RW	5	0	
64	40	auto_cwx2_l	171	AB	10101011	RW	5	0	
65	41	auto_cwy1_h	0	00	00000000	RW	5	0	
66	42	auto_cwy1_l	161	A1	10100001	RW	5	0	
67	43	auto_cwy2_h	1	01	00000001	RW	5	0	
68	44	auto_cwy2_l	64	40	01000000	RW	5	0	

▷ AE windows

AE window control registers.



< Group A >

(91) PAD control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
91	5B	pad_control	64	40	01000000	RW	5	0	Pad control

register name : pad_control								
register #	bit#	name	default	**64**	default(h)	**40**	default(b)	**01000000**
91d (5Bh)	7	stdby	0	register stdby on/off ('1' : stdby mode, '0' : normal mode)				
	6	hiz	1	data output pad hiz on/off ('1' : hiz, '0' not hiz)				
	5	stdby_level	0	stdby data output pad level selector ("1x" : hiz, "01" : high, "00" : low)				
	4		0					
	3	clkoff	0	clock kill control register ('1' : clock Kill, '0' : not kill)				
	2	trapf	0	trap stdby frame selector				
	1		0					
	0		0					

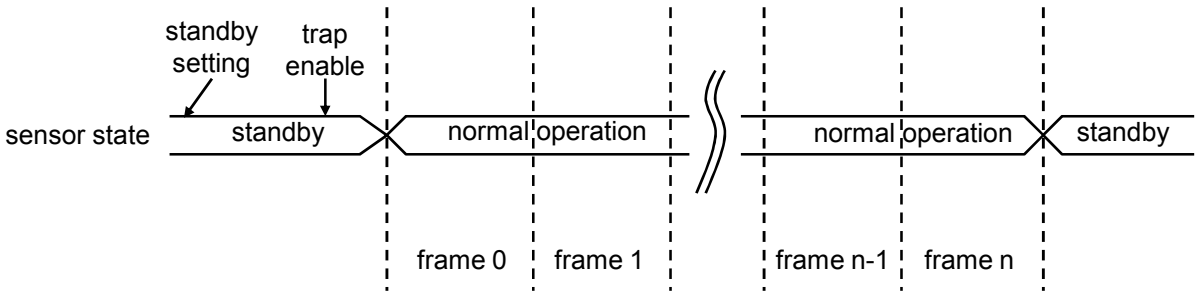
< Group A >

(92) Trap

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
92	5C	trap	0	00	00000000	RW	5	0	Trap

▷ **Trap**

If user want to operate PO8030D to Ambient Light sensor or Proximity sensor only, then user can control operation time with this register. Example operation timing is as belows.



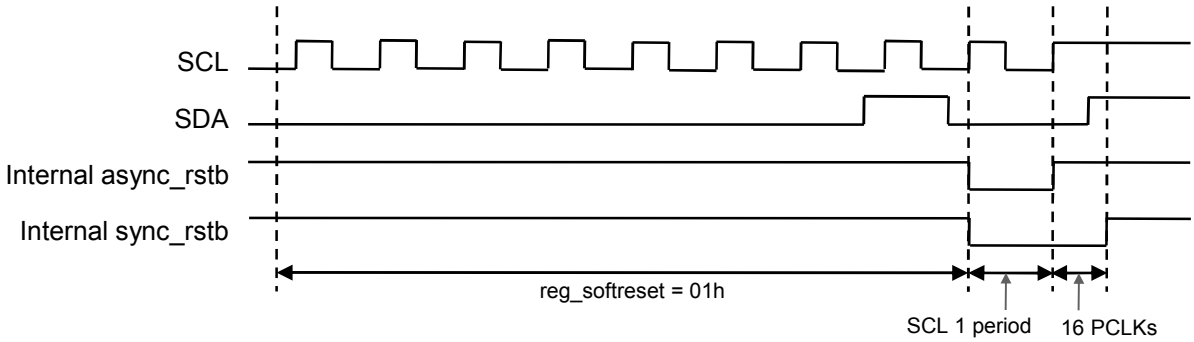
- n = reg_trapf

(105) Soft reset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
105	69	softreset	0	00	00000000	RW	5	0	Soft reset

▷ **Soft reset**

Soft reset bit is reg_softreset[0].



(106) Clock divider

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
106	6A	clkdiv	0	00	00000000	RW	6	aev	Clock divider

▷ **Clock divider**

reg_clkdiv	PPCLK	PCLK
00h	MCLK	PPCLK x 1/2
01h	MCLK x 2/3	PPCLK x 1/2
02h	MCLK x 1/2	PPCLK x 1/2
03h	MCLK x 1/3	PPCLK x 1/2
04h	MCLK x 1/4	PPCLK x 1/2
05h	MCLK x 1/8	PPCLK x 1/2
else	MCLK	PPCLK x 1/2

< Group A >

(108) Bayer control 01

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
108	6C	bayer_control_01	0	00	00000000	RW	6	aev	Bayer control

register name : bayer_control_01								
register #	bit#	name	default	**00**	default(h)	**00**	default(b)	**00000000**
108d (6Ch)	7	vm	0	vertical mirror ON/OFF 0b : Vertical Mirror disable. 1b : Vertical Mirror enable.				
	6	hm	0	horizontal mirror ON/OFF 0b : Horizontal Mirror disable. 1b : Horizontal Mirror enable.				
	5							
	4							
	3							
	2							
	1							
	0							

< Group A >

(223) ADC offset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
223	DF	adcoffset	36	24	00100100	RW	6	aev	ADC offset value

▷ **ADCoffset**

ADCoffset control registers.

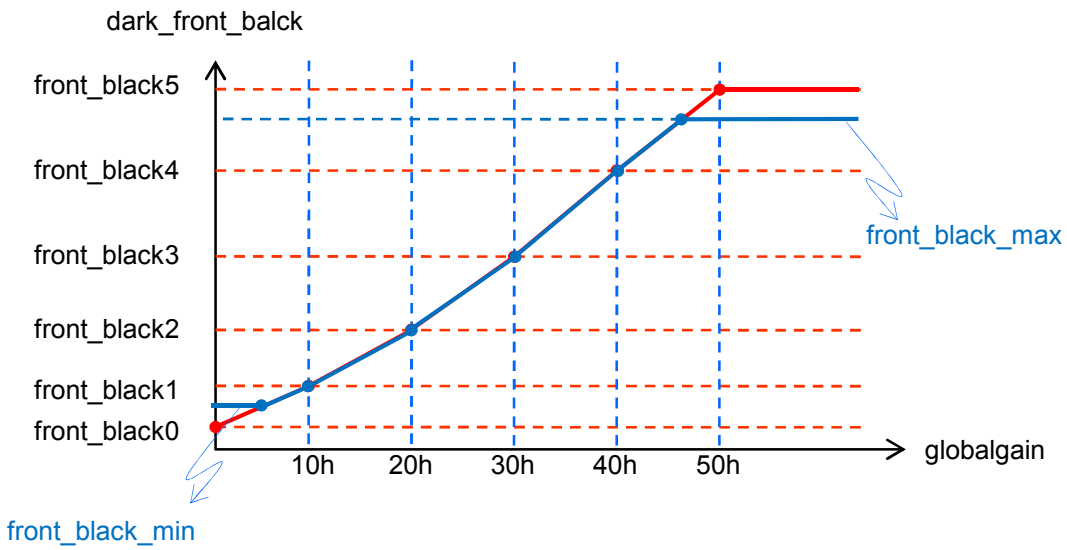
(225~233) Manual black level fitting reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
225	E1	front_black_ref0	0	00	00000000	RW	5	0	Manual black level fitting reference
226	E2	front_black_ref1	0	00	00000000	RW	5	0	
227	E3	front_black_ref2	0	00	00000000	RW	5	0	
228	E4	front_black_ref3	0	00	00000000	RW	5	0	
229	E5	front_black_ref4	0	00	00000000	RW	5	0	
230	E6	front_black_ref5	0	00	00000000	RW	5	0	
231	E7	front_black_min	255	FF	11111111	RW	5	0	
232	E8	front_black_max	127	7F	01111111	RW	5	0	
233	E9	front_black	0	00	00000000	RW	6	aev	Manual black level

▷ **Black level fitting reference**

front_black control registers.

When auto_control_3[2] is 1b, dark_front_black is calculated by automatically.



★ When auto_control_3[2] is 0b, User can program front_black manually.

★ front_black : [7] : sign bit, [6:0] : magnitude

< Group A >

(235~236) lens offset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
235	EB	lens_coffset	0	00	00000000	RO	0	0	Lens address offset
236	EC	lens_roffset	0	00	00000000	RO	0	0	

▷ **lens_coffset**

Lens address column offset

lens_coffset[7] : sign bit

lens_coffset[6:0] : magnitude

▷ **lens_roffset**

Lens address row offset

lens_roffset[7] : sign bit

lens_roffset[6:0] : magnitude

▶ Register Tables (Detailed) : Group B

(260) ISP function control 0

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
260	04	isp_func_0	247	F7	11110111	RW	6	aev	Isp function control

register name : isp_func_0								
register #	bit#	name	default	**247**	default(h)	**F7**	default(b)	**11110111**
260d (04h)	7	lens_en	1	'0' : disable, '1' : enable lens shading compensation				
	6							
	5							
	4							
	3							
	2							
	1	ccr_en	1	'0' : disable, '1' : enable color correction				
	0							

(261) ISP function control 1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
261	05	isp_func_1	251	FB	11111011	RW	6	aev	Isp function control

register name : isp_func_1								
register #	bit#	name	default	**251**	default(h)	**FB**	default(b)	**11111011**
261d (05h)	7							
	6							
	5							
	4							
	3	edge_en	1	'0' : disable, '1' : enable edge enhancement				
	2							
	1							
	0							

< Group B >

(262) ISP function control 2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
262	06	isp_func_2	0	00	00000000	RW	6	aev	Isp function control

register name : isp_func_2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
262d (06h)	7							
	6							
	5							
	4							
	3	emboss_en	0	embossing effect enable/disable				
	2	emboss_mode	0	embossing effect mode selection				
	1	sketch_en	0	sketch effect enable/disable				
	0	prox	0	proximity sensor mode selection				

< Group B >

(320~323) Lens gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
320	40	lens_gainr	0	00	00000000	RW	6	aev	Lens gain
321	41	lens_gaing	0	00	00000000	RW	6	aev	
323	43	lens_gainb	0	00	00000000	RW	6	aev	Lens gain

▷ **Lens gain**

Lens Shading Gain : 0x20 = x 1 gain.

(334) Format

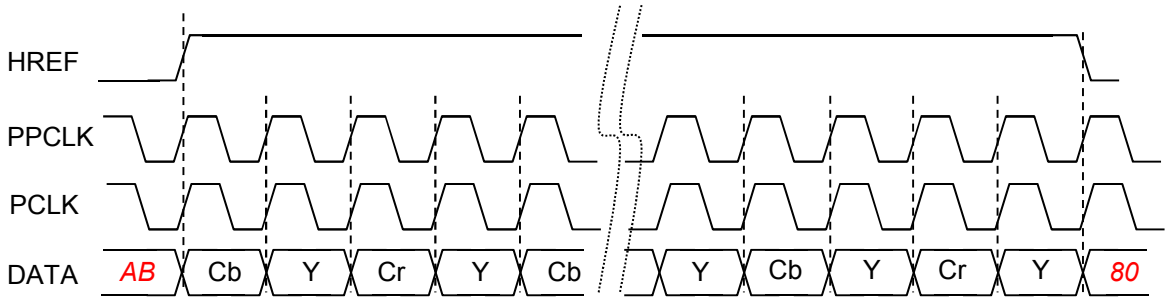
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
334	4E	format	0	00	00000000	RW	6	aev	Format control

register name : format								
register #	bit#	name	default	**13**	default(h)	**0D**	default(b)	**00001101**
334d (4Eh)	7	format_control	0	00h : cbycry 01h : crycby 02h : ycbycr 03h : ycrycb 10h : rggb 11h : gbrg 12h : grbg 13h : bggr 30h : rgb565 31h : rgb565 (byte swap) 32h : bgr565 33h : bgr565 (byte swap) 36h : rgb444 37h : rgb444 (byte swap) 41h : dpc bayer 44h : yyyy				
	6		0					
	5		0					
	4		0					
	3		1					
	2		1					
	1		0					
	0		1					

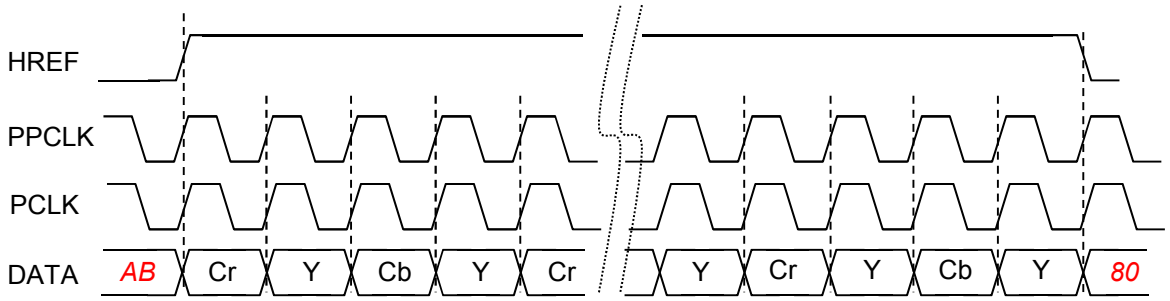
< Group B >

▷ Output timing diagrams for format register (1/4)

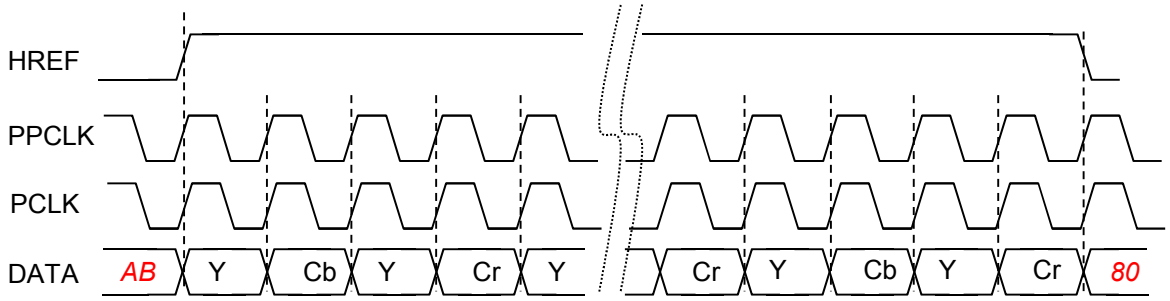
When format is 00h (Cb, Y, Cr, Y …),



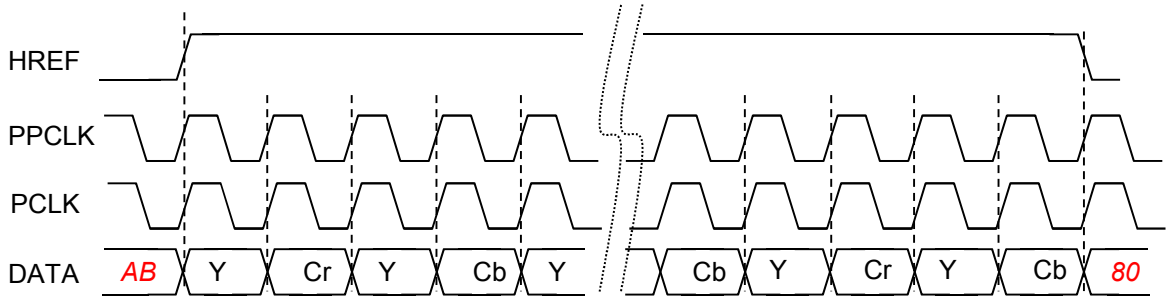
When format is 01h (Cr, Y, Cb, Y, …),



When format is 02h (Y, Cb, Y, Cr, …),



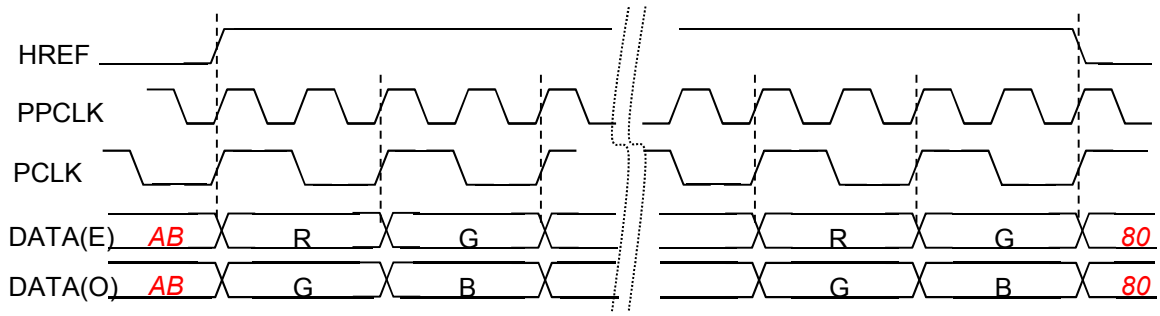
When format is 03h (Y, Cr, Y, Cb, …),



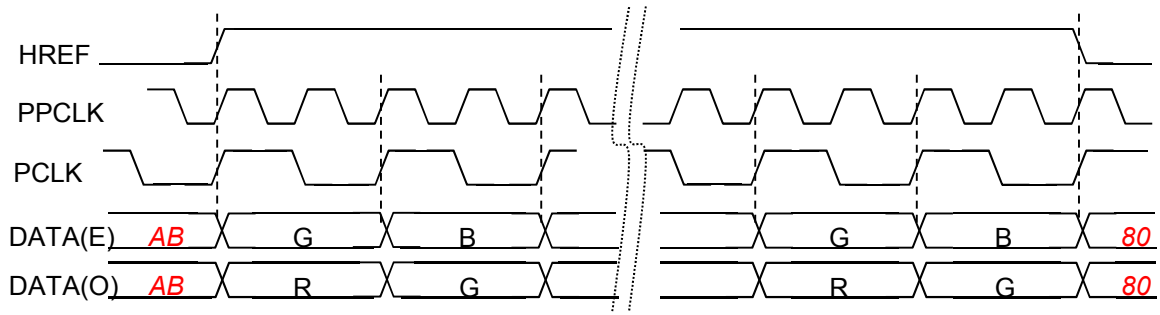
< Group B >

▷ Output timing diagrams for format register (2/4)

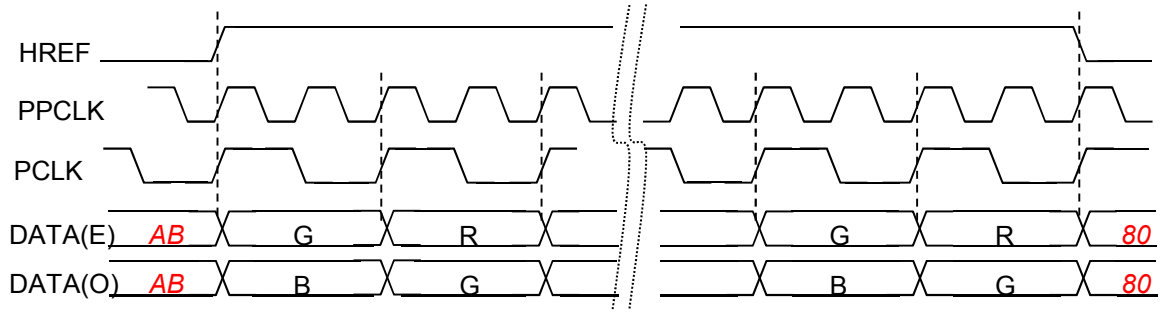
When format is 10h (ISP bayer, RGRG, GBGB, …),



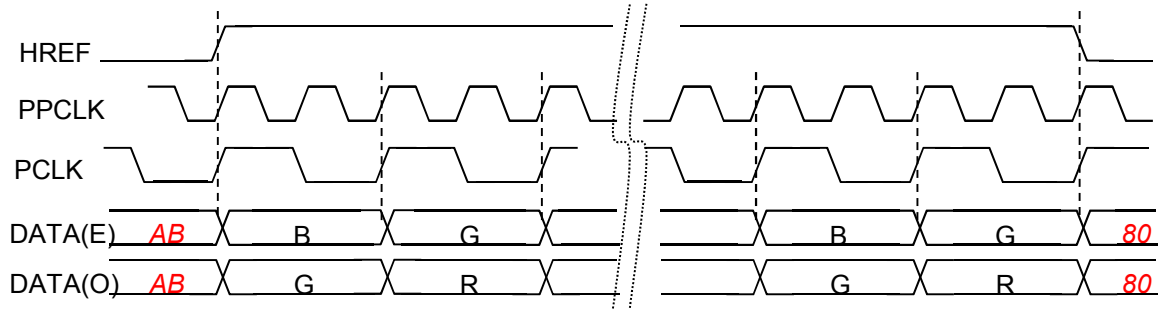
When format is 11h (ISP bayer, GBGB, RGRG, …),



When format is 12h (ISP bayer, GRGR, BGBG, …),



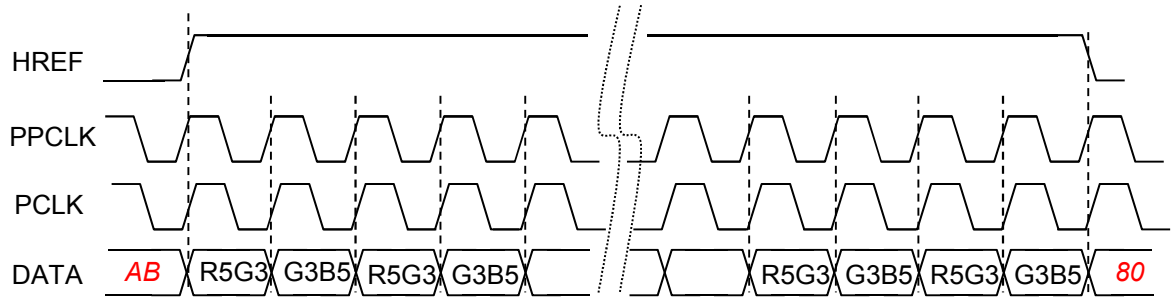
When format is 13h (ISP bayer, BGBG, GRGR, …),



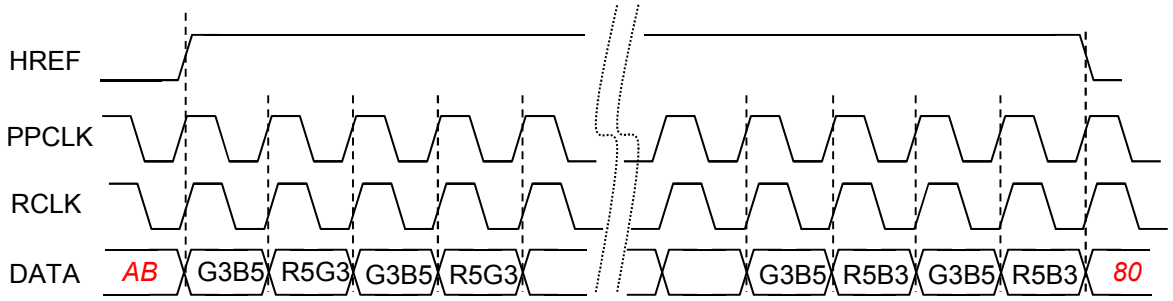
< Group B >

▷ Output timing diagrams for format register (3/4)

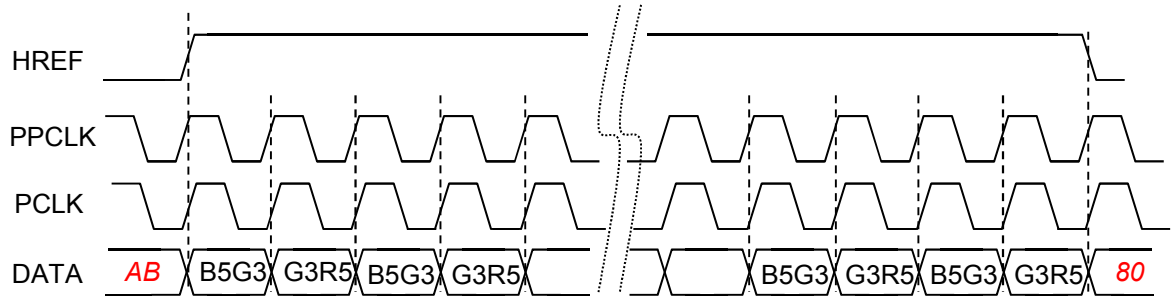
When format is 30h(R5G3, G3B5, …),



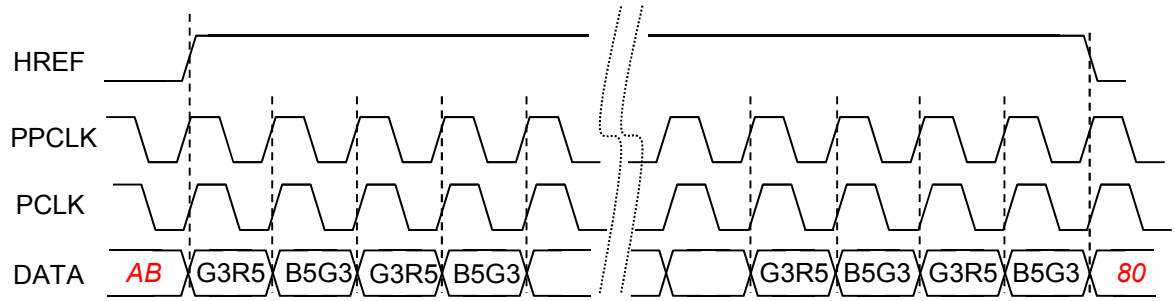
When format is 31h(G3B5, R5B3, …),



When format is 32h(B5G3, G3R5, …),



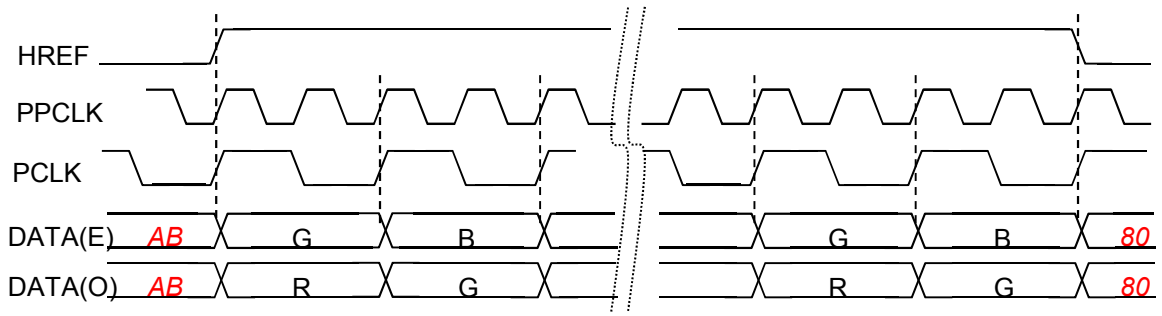
When format is 33h(G3R5, B5G3, …),



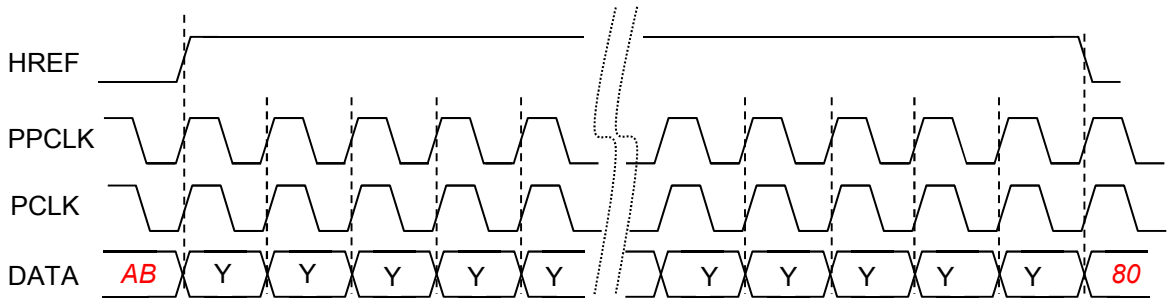
< Group B >

▷ Output timing diagrams for format register (4/4)

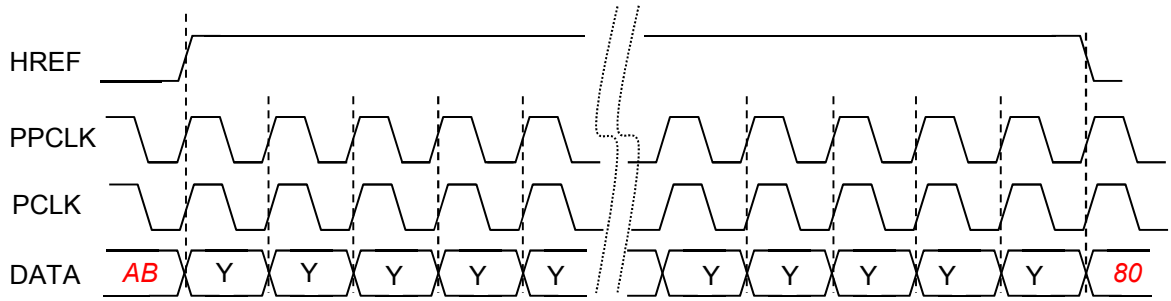
When format is 41h (DPC Bayer),



When format is 43h(for mono sensor),



When format is 44h(only Y),



< Group B >

(350) Edge gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
350	5E	edge_gain	32	20	00100000	RW	5	0	Edge gain

▷ **Edge gain**

Edge gain factor

< Group B >

(354~362) Color correction matrix

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
354	62	ccr_m11	69	45	01000101	RW	5	0	Color correction matrix value
355	63	ccr_m12	160	A0	10100000	RW	5	0	
356	64	ccr_m13	133	85	10000101	RW	5	0	
357	65	ccr_m21	143	8F	10001111	RW	5	0	
358	66	ccr_m22	69	45	01000101	RW	5	0	
359	67	ccr_m23	150	96	10010110	RW	5	0	
360	68	ccr_m31	132	84	10000100	RW	5	0	
361	69	ccr_m32	148	94	10010100	RW	5	0	
362	6A	ccr_m33	56	38	00111000	RW	5	0	

▷ Color correction matrix

The color specifications of the image sensor differ from the fabrication process like color filter. Due to the spectral characteristics of the optics, the native RGB data may not provide a faithful color rendition.

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

< Group B >

(365~379) Gamma coefficient

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
365	6D	gm_y0	0	00	00000000	RW	5	0	Gamma reference
366	6E	gm_y1	11	0B	00001011	RW	5	0	
367	6F	gm_y2	23	17	00010111	RW	5	0	
368	70	gm_y3	34	22	00100010	RW	5	0	
369	71	gm_y4	46	2E	00101011	RW	5	0	
370	72	gm_y5	64	40	01000000	RW	5	0	Gamma reference
371	73	gm_y6	80	50	01010000	RW	5	0	
372	74	gm_y7	110	6E	01101110	RW	5	0	
373	75	gm_y8	136	88	10001000	RW	5	0	
374	76	gm_y9	174	AE	10101110	RW	5	0	
375	77	gm_y10	202	CA	11001010	RW	5	0	
376	78	gm_y11	220	DC	11011100	RW	5	0	
377	79	gm_y12	236	EC	11101100	RW	5	0	
378	7A	gm_y13	246	F6	11110110	RW	5	0	
379	7B	gm_y14	255	FF	11111111	RW	5	0	

▷ Gamma coefficient

Y Gamma Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.

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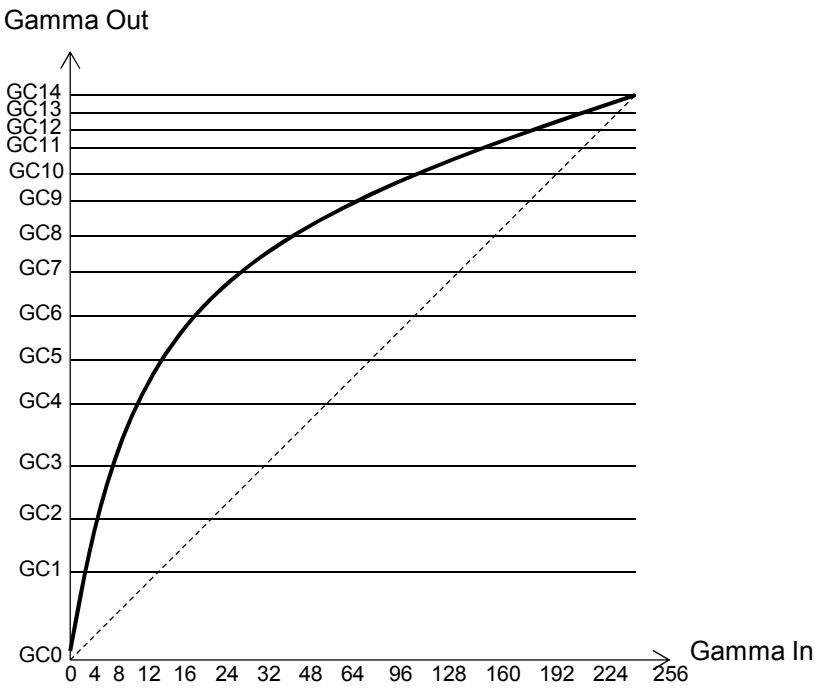

GC : Gamma coefficient

< Group B >

(399) Sketch offset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
399	8F	sketch_offset	140	8C	10001100	RW	6	aev	Sketch offset

▷ **Sketch offset**

Sketch offset is applied to chrominance signal which ranges from 0 to 255.

(403~406) Scale control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
403	93	scale_x	32	20	00100000	RW	6	aev	Scale control
404	94	scale_y	32	20	00100000	RW	6	aev	
405	95	scale_th_h	0	00	00000000	RW	6	aev	
406	96	scale_th_l	10	0A	00001010	RW	6	aev	

▷ **Scale control**

scale_x : Horizontal scale factor, 20h = x1

scale_y : Vertical scale factor , 20h = x1

scale_th_h/l : Scale buffer size control register.

< Group B >

(410) AUTO off

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
410	9A	auto_off	0	00	0	RW	5	0	Auto off (MCU off)

▷ **Auto off**

Auto on/off control register

(413~414) Y contrast & brightness

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
413	9D	ycontrast	64	40	01000000	RW	6	aev	Y contrast
414	9E	ybrightness	0	00	00000000	RW	6	aev	Y brightness

▷ **Y contast & brightness**

Luminance (Y) = Conversion Y x reg_y_contrast + reg_y_brightness
Brightness = [7] : [6:0] = Sign : Magnitude

(415) Y max

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
415	9F	y_max	0	00	00000000	RO	0	0	Y max clamping

▷ **Y max**

Output Y max. control register

(426~428) Cb/Cr_offset and C_max

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
426	AA	cb_offset	128	80	10000000	RW	6	aev	Cb offset
427	AB	cr_offset	128	80	10000000	RW	6	aev	Cr offset
428	AC	c_max	0	00	00000000	RO	0	0	Cb/Cr max

▷ **CbCr offset**

Cb/Cr color offset control register.

- ▶ Cb` = Cb ± reg_cb_offset
- ▶ Cr` = Cr ± reg_cr_offset

▷ **C max**

Max. color clamping control register.

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(431~438) CCIR656 control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
431	AF	sync_ccirFF	255	FF	11111111	RW	5	0	CCIR656 Control
432	B0	sync_ccir00	0	00	00000000	RW	5	0	
433	B1	sync_ccir80	128	80	10000000	RW	5	0	
434	B2	sync_ccir10	16	10	00010000	RW	5	0	
435	B3	sync_blankSAV	182	B6	10110110	RW	5	0	
436	B4	sync_blankEAV	157	9D	10011101	RW	5	0	
437	B5	sync_activSAV	171	AB	10101011	RW	5	0	
438	B6	sync_activEAV	128	80	10000000	RW	5	0	

▷ ***sync_ccirFF***

CCIR data format FFh

▷ ***sync_ccir00***

CCIR data format 00h

▷ ***sync_ccir80***

CCIR data format 80h

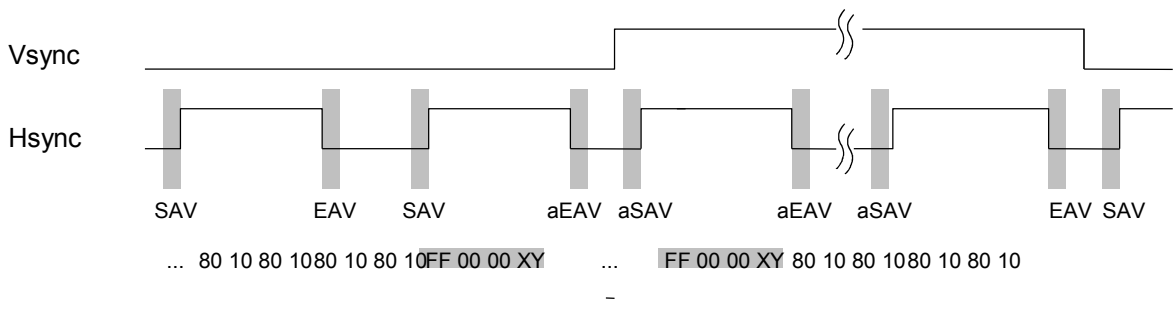
▷ ***sync_ccir10***

CCIR data format 10h

▷ ***ccir656 sync index value***

EAV and SAV data value for synchronization.

Address	Name	Description
20h	*BlankSAV*	Blank Range Start of Video
21h	*BlankEAV*	Blank Range End of Video
22h	*ActiveSAV*	Active Range Start of Video
23h	*ActiveEAV*	Active Range End of Video



EAV : blank EAV,
aEAV : Active EAV,

SAV : blank SAV
aSAV : Active SAV

< Group B >

(440) Sync control 1

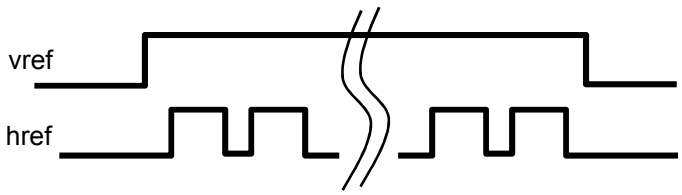
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
440	B8	sync_control_1	0	00	00000000	RW	6	aev	Sync control

register name : sync_control_1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
440d (B8h)	7	x	0	reserved				
	6	sync_vsyncPolarity	0	vsync polarity change				
	5	sync_hsyncAllLines	0	hsync output all lines enable(black and active)				
	4	sync_hsyncPolarity	0	hsync polarity change				
	3	sync_pclkwindow	0	pclk window				
	2	sync_pclkPolarity	0	pclk polarity change				
	1	x	0	reserved				
	0	x	0	reserved				

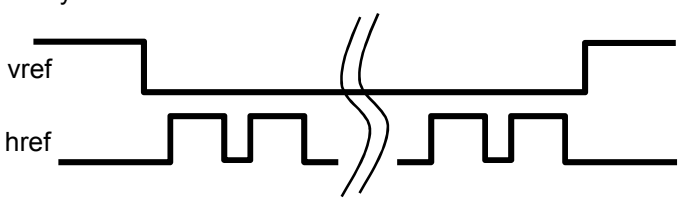
▷ ***Sync_vsyncpolarity***

Output vsync polarity control register.

▶ vsyncPolarity = '0'



▶ vsyncPolarity = '1'

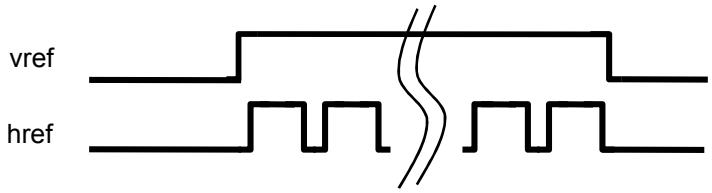


< Group B >

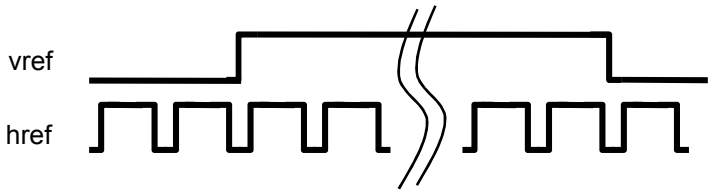
▷ Sync_hsyncAllLines

Output hsync control register.

▶ hsyncAllLines = '0'



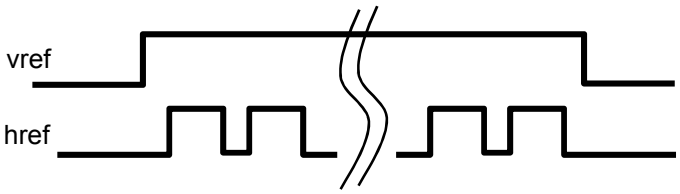
▶ hsyncAllLines = '1'



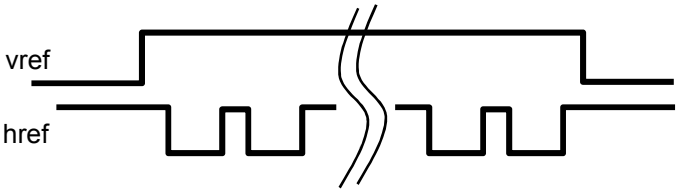
▷ Sync_hsyncpolarity

Output hsync polarity control register.

▶ hsyncPolarity = '0'



▶ hsyncPolarity = '1'

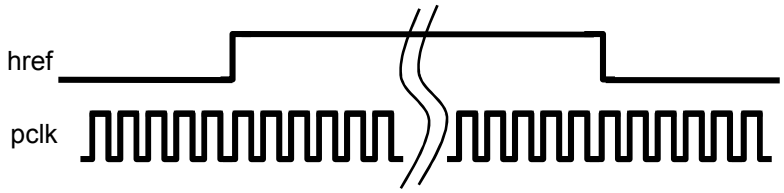


< Group B >

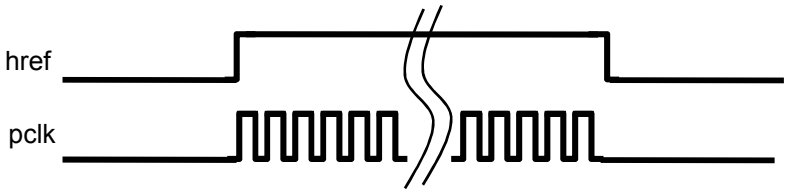
▷ Sync_pclkwindow

Output pclk control register.

▶ pclkwindow = '0'



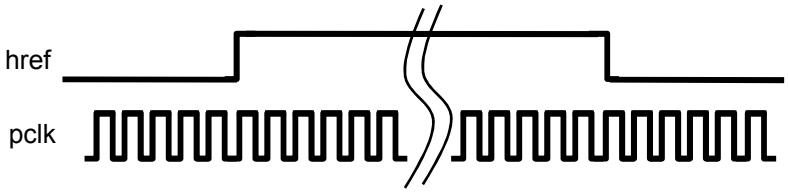
▶ pclkwindow = '1'



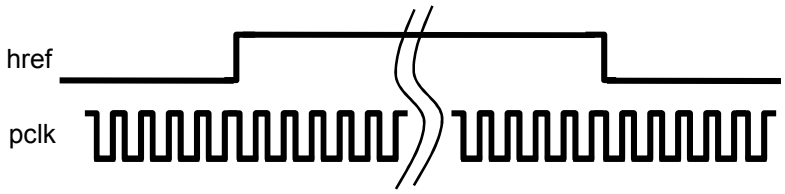
▷ Sync_pclkpolarity

Output pclk polarity control register.

▶ pclkpolarity = '0'



▶ pclkpolarity = '1'



< Group B >

(441) Sync control 2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
441	B9	sync_control_2	0	00	00000000	RW	6	aev	Sync control

register name : sync_control_2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
441d (B9h)	7	x	0	reserved				
	6	x	0	reserved				
	5	mclkphase_en	0	output pclk phase using mclke nable				
	4	mclkphase	0	output pclk phase option @ opclk_sel='1'				
	3		0					
	2		0					
	1		0					
	0		0					

< Group B >

(496~501) Flicker control registers

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
496	F0	fd_period_a_h	0	00	00000000	RW	5	0	Flicker period for A state
497	F1	fd_period_a_m	128	80	10000000	RW	5	0	
498	F2	fd_period_a_l	221	DD	11011101	RW	5	0	
499	F3	fd_period_b_h	0	00	00000000	RW	5	0	Flicker period for B state
500	F4	fd_period_b_m	154	9A	10011010	RW	5	0	
501	F5	fd_period_b_l	163	A3	10100011	RW	5	0	

▷ Flicker period A & B

fd_period_A can be programmed by flicker period for 1/120 sec.

fd_period_B can be programmed by flicker period for 1/100 sec.

Flicker period for 1/120 sec and 1/100 sec are calculated by as below.

$$\text{fd\_period\_A} = \frac{256\ d^{*}\ \text{PCLK FREQ.}}{120d\ *\ \text{framewidth}}$$

$$\text{fd\_period\_B} = \frac{256\ d^{*}\ \text{PCLK FREQ.}}{100d\ *\ \text{framewidth}}$$

Where, framewidth is register value. PCLK FREQ. is frequency of pixel clock.

< Group B >

▶ Register Tables (Detailed) : Group C

(516) Auto_control_1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
516	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control

register name : auto_control_1								
register #	bit#	name	default	**152**	default(h)	**98**	default(b)	**10011000**
516d (04h)	7							
	6							
	5							
	4							
	3							
	2	AWB mode	0	1b : manual mode 0b : auto mode				
	1	AE mode	0	00b : auto exposure mode 01b : manual exposure mode 1 (exposure writing mode) 10b : Reserved 11b : manual exposure mode 3 (direct writing mode)				
	0		0					

▷ AWB mode

When auto_control_1[2] is '1', auto white balance does not operation and you can write white balance gain (Reg. A-23h~25h). Please set disable, before writing white balance gain.

▷ AE mode

This product provides auto exposure mode and 3 types of manual exposure mode. User can select auto exposure mode by writing auto_control_1[1:0].

★ auto_control_1[1:0] = 00b (auto exposure mode)

When auto_control_1[1:0] is 00b, integration time, globalgain and **digitalgain** are calculated by auto exposure block. Refer to auto exposure reference registers (Reg. C-16h~24h).

★ auto_control_1[1:0] = 01b (manual exposure mode1)

When auto_control_1[1:0] is 01b, you can control integration time, globalgain and **digitalgain** by exposure registers (Reg. C-12h~15h). Refer to exposure registers (Reg. C-12h~15h) and auto exposure reference registers (Reg. C-16h~24h).

★ auto_control_1[1:0] = 11b (manual exposure mode3)

When auto_control_1[1:0] is 11b, you can write integration time, globalgain and **digitalgain** registers. Refer to Reg. A-17h~1Bh.

(518) Auto_control_3

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
518	06	auto_control_3	0	00	00000000	RW	6	autov	Auto control

register name : auto_control_3								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
518d (06h)	7	rg/bg ratio fitting	0	1b : rg/bg ratio (AWB target) fitting enable 0b : disable				
	6	rg/bg ratio x-axis	0	1b : rg/bg ratio fitting by bmean/gmean 0b : rg/bg ratio fitting by rmean/gmean				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	front_black fitting	0	1b : front_black fitting enable 0b : disable				
	1	x	0	Reserved				
	0	ycontrast/brightness fitting	0	1b : ycontrast/brightness fitting enable 0b : disable				

▷ Rg/bg ratio fitting & rg/bg ratio x-axis (bit7 & bit6)

rg/bg ratio fitting (bit7) is enable bit for AWB target fitting function. In addition, rg/bg ratio x-axis is x-axis selection bit for AWB target fitting function. For more information, please refer to AWB target fitting reference registers (Reg. C-6Ch~76h).

▷ Front_black fitting (bit2)

front_balck fitting is enable bit for front_black fitting function. For more information, please refer to front_black fitting reference registers (Reg. A-F6h~FDh).

▷ Ycontrast/brightness fitting (bit0)

ycontrast/brightness fitting is enable bit for ycontrast/brightness fitting function. For more information, please refer to ycontrast/brightness fitting reference registers (Reg. D-57h~5Dh).

< Group C >

(530~533) Exposure

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
530	12	exposure_t	0	00	00000000	RW	6	autov	Exposure
531	13	exposure_h	0	00	00000000	RW	6	autov	
532	14	exposure_m	128	80	10000000	RW	6	autov	
533	15	exposure_l	0	00	00000000	RW	6	autov	

▷ Exposure

When auto_control_1[1:0] is 00b, exposure registers are calculated by auto exposure block.

Exposure registers are used in calculating integration time, globalgain and **digital gain**.

When auto_control_1[1:0] is 01b, user can write exposure registers.

Set auto_control_1[1:0] to 01b, before writing exposure registers.

< Group C >

(555~558) Saturation ratio

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
555	2B	ae_ysat1	208	D0	11010000	RW	6	autov	Y saturation threshold
556	2C	ae_ysat2	208	D0	11010000	RW	6	autov	Rgb saturation threshold
557	2D	sratio_weight	8	08	00001000	RW	5	0	Saturation ratio center weight
558	2E	sratio	0	00	00000000	RW	5	0	Saturation ratio for monitoring

▷ Ae_ysat1 & ae_ysat2

ae_ysat1 is the threshold value in R,G,B saturation. ae_ysat2 is the threshold value in Y saturation.

▷ Sratio_weight

sratio_weight : Saturation ratio weight factor.

▷ Sratio

sratio : Saturation ratio value for monitoring

$$SR\_c/p = \frac{(\text{\# of saturation pixel in AE window})\_c/p}{(\text{\# of pixel in AE window})\_c/p}$$

$$sratio = \frac{(SR\_c \times sratio\_weight) + (SR\_p \times (16 - sratio\_weight))}{16}$$

< Group C >

(560~561) AE weight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
560	30	ae_weight_c	12	0C	00001100	RW	5	0	Ae center weight
561	31	ae_weight_p	52	34	00110100	RW	5	0	Ae peripheral weight

▷ **ae_weight_c & ae_weight_p**

ae_weight_c : AE center weight for back light compensation.

ae_weight_p : AE peripheral weight for back light compensation.

caution) ae_weight_c & ae_weight_p should be, ae_weight_c + ae_weight_p = 64d

(563~568) Y mean reference & Y mean

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
563	33	ymean_ref0	16	10	00010000	RW	5	0	Ymean extention reference
564	34	ymean_ref1	16	10	00010000	RW	5	0	
565	35	ymean_ref2	16	10	00010000	RW	5	0	
566	36	ymean_ref3	16	10	00010000	RW	5	0	
567	37	ymean_h	0	00	00000000	RW	5	0	Ymean
568	38	ymean_l	128	80	10000000	RW	5	0	

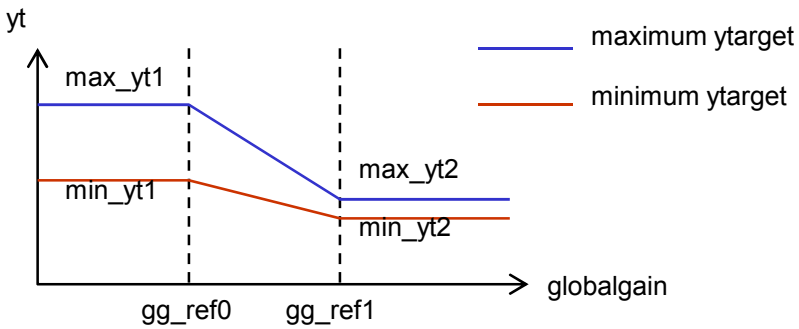
< Group C >

(570~575) Min/Max Y target reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
570	3A	max_yt1	112	70	01110000	RW	6	autov	Min / max ytarget control reference
571	3B	max_yt2	112	70	01110000	RW	6	autov	
572	3C	min_yt1	112	70	01110000	RW	6	autov	
573	3D	min_yt2	112	70	01110000	RW	6	autov	
574	3E	gg_ref0	16	10	00010000	RW	6	autov	
575	3F	gg_ref1	64	40	01000000	RW	6	autov	

▷ **Min/max_yt1/2**

User can program dynamic y_target with these registers. Dynamic y_target means that y_target can be changed to match current brightness automatically.



When auto_control_2[5] is 1b, min./max. y_target is given like graph.

When auto_control_2[5] is 0b, min./max. y_target is given like min_yt1 / max_yt1.

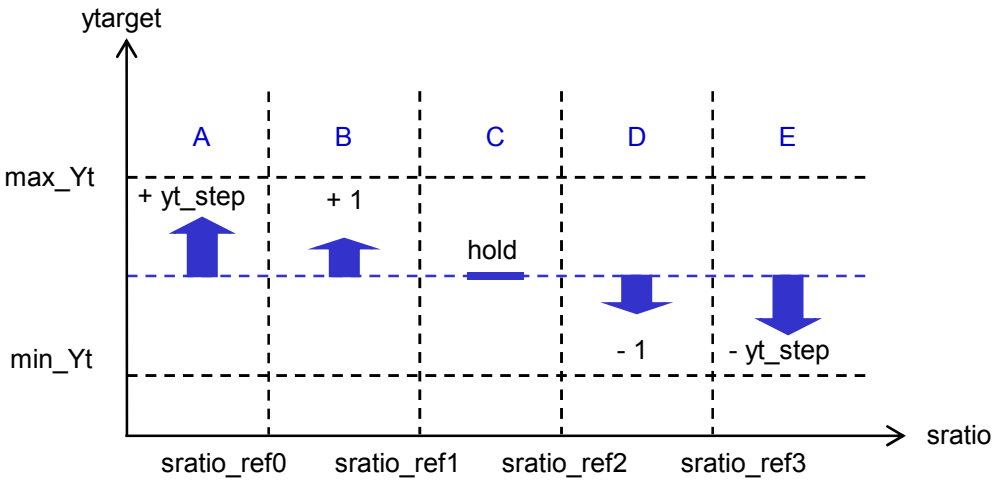
< Group C >

(576~582) Y target reference & Y target

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
576	40	sratio_ref0	0	00	00000000	RW	6	autov	Ytarget control reference
577	41	sratio_ref1	0	00	00000000	RW	6	autov	
578	42	sratio_ref2	0	00	00000000	RW	6	autov	
579	43	sratio_ref3	0	00	00000000	RW	6	autov	
580	44	yt_step	8	08	00001000	RW	5	0	
581	45	ytarget	112	70	01110000	RW	5	0	Ytaget
582	46	user_wyt	128	80	10000000	RW	6	autov	User wyt

▷ Sratio_ref0/1/2/3

Saturation ratio reference fitting registers for y_target control.



▷ Yt_step

Y target step control register.

▷ Ytarget

Y target register.

▷ User_wyt

Weighted Y target control register.

Final Ytarget is given as

Ytarget = (ytarget x user_wyt) / 128d

< Group C >

(584~585) AE speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
584	48	ae_up_speed	8	08	00001000	RW	6	autov	Ae speed control
585	49	ae_down_speed	12	0C	00001100	RW	6	autov	

▷ Ae_up_speed & ae_down_speed

ae_up_speed : AE up speed control .

ae_down_speed : AE down speed control .

Setting range of both register is 01h to 10h. If ae_up_speed and ae_down_speed have high value, auto exposure speed will be faster. However, high ae_up_speed and ae_down_speed value may cause AE oscillation.

(586,588) AE lock range & auto flag

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
586	4A	ae_lock	2	02	00000010	RW	6	autov	AE lock range
588	4C	auto_flag	0	00	00000000	RW	5	0	Auto flag

▷ Ae_lock

ae_lock : AE lock range control register. *(lock range = | Ymean ~ Ytarget | / Ytarget)*

Setting range of ae_lock is 00h to FFh. If ae_lock has low value, auto exposure lock range will be smaller. However, small value of ae_lock may cause AE oscillation.

▷ Auto_flag

Current AE state indicator.

If auto_flag[7] = ‘0b’ , then AE state is “hold”

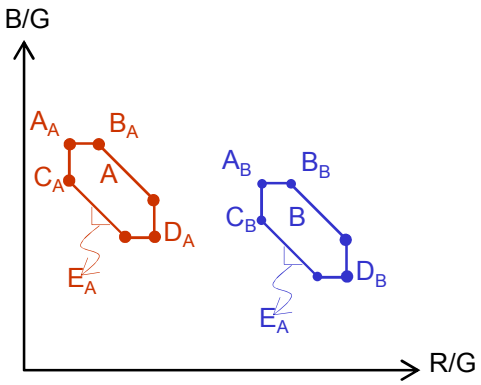
If auto_flag[7] = ‘1b’ , then AE state is “not hold”

(598~614) AWB data sampling control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
598	56	awb_p1Ax	0	00	00000000	RW	5	0	Awb sampling range selection
599	57	awb_p1Ay	255	FF	11111111	RW	5	0	
600	58	awb_p2Ax	255	FF	11111111	RW	5	0	
601	59	awb_p2Ay	0	00	00000000	RW	5	0	
602	5A	awb_osAx	255	FF	11111111	RW	5	0	
603	5B	awb_osAy	255	FF	11111111	RW	5	0	
604	5C	awb_slopeA	0	00	00000000	RW	5	0	
605	5D	awb_p1Bx	0	00	00000000	RW	5	0	
606	5E	awb_p1By	255	FF	11111111	RW	5	0	
607	5F	awb_p2Bx	255	FF	11111111	RW	5	0	
608	60	awb_p2By	0	00	00000000	RW	5	0	
609	61	awb_osBx	255	FF	11111111	RW	5	0	
610	62	awb_osBy	255	FF	11111111	RW	5	0	
611	63	awb_slopeB	0	00	00000000	RW	5	0	
612	64	awb_maxc	248	F8	11111000	RW	5	0	
613	65	awb_minc	0	00	00000000	RW	5	0	
614	66	awb_sfcount	255	FF	11111111	RW	5	0	

▷ AWB data sample area control registers

These registers are used for more correct AWB operation.



A_A : (awb_p1Ax, awb_p1Ay)
B_A : (awb_p1Ax+awb_osAx, awb_p1Ay)
C_A : (awb_p1Ax, awb_p1Ay-awb_osAy)
D_A : (awb_p2Ax, awb_p2Ay)
E_A : awb_slopeA

A_B : (awb_p1Bx, awb_p1By)
B_B : (awb_p1Bx+awb_osBx, awb_p1By)
C_B : (awb_p1Bx, awb_p1By-awb_osBy)
D_B : (awb_p2Bx, awb_p2By)
E_B : awb_slopeB

If data are not included in region A or region B, then all of data are bad samples and not used AWB operations. In addition, if one of R, G, B is bigger than awb_maxc or lower than awb_minc, then data is bad sample and not used AWB operation.

< Group C >

(616~618) AWB weight & weight changing speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
616	68	awb_weight_c	21	15	00010101	RW	5	0	awb weight control
617	69	awb_weight_p	43	2B	00101011	RW	5	0	
618	6A	awb_wspeed	4	04	00000100	RW	5	0	

▷ **Awb_weight**

awb_weight_c : AWB center weight control register

awb_weight_p : AWB peripheral weight control register

caution) awb_weight_c & awb_weight_p should be, awb_weight_c + awb_weight_p = 64d

$$R/G/Bmean\_c/p = \frac{(\text{Sum. of R/G/B data in AWB window})\_c/p}{(\#\text{ of pixel in AWB window})\_c/p}$$

$$Weighted\_R/G/Bmean = \frac{(R/G/Bmean\_c \times ae\_weight\_c) + (R/G/Bmean\_p \times ae\_weight\_p)}{awb\_weight\_c + awb\_weight\_p}$$

▷ **Awb_wspeed**

awb_wspeed : AWB weight change speed control register

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(620~628) rg/bg ratio reference & rg/bg ratio

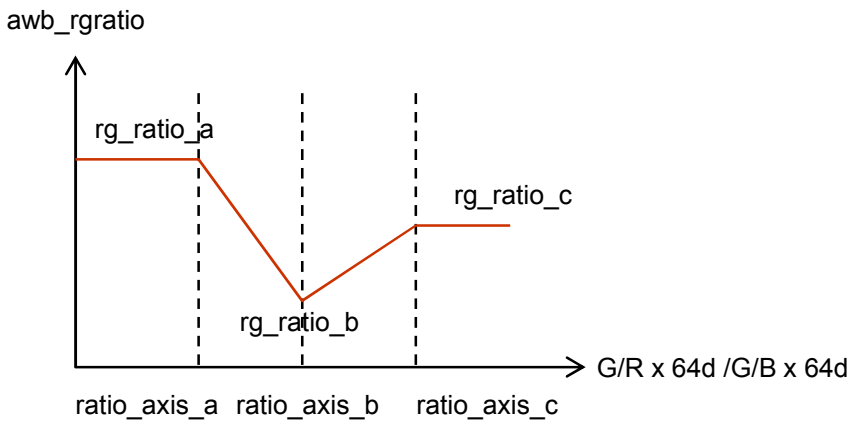
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
620	6C	rg_ratio_a	128	80	10000000	RW	5	0	Target awb ratio fitting reference
621	6D	bg_ratio_a	128	80	10000000	RW	5	0	
622	6E	rg_ratio_b	128	80	10000000	RW	5	0	
623	6F	bg_ratio_b	128	80	10000000	RW	5	0	
624	70	rg_ratio_c	128	80	10000000	RW	5	0	
625	71	bg_ratio_c	128	80	10000000	RW	5	0	
626	72	ratio_axis_a	64	40	01000000	RW	5	0	
627	73	ratio_axis_b	80	50	01010000	RW	5	0	
628	74	ratio_axis_c	96	60	01100000	RW	5	0	

▷ ***RG/BG_ratio_a/b/c***

These registers are used for changing AWB target with light source automatically.

If auto_control_3[7] is '1b', then automatic AWB target change function is enable.

If '0b', then function is disable.



User can select X-axis using auto_cotnrol_3[6]. (1b : G/B x 64 , 0b : G/R x 64).

Caution)

ratio_axis_a, ratio_axis_b and ratio_axis_c should be,

ratio_axis_a < ratio_axis_b < ratio_axis_c

< Group C >

(632~633) AWB lock range & speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
632	78	awb_lock	2	02	00000010	RW	5	0	Awb lock range
633	79	awb_speed	8	08	00001000	RW	5	0	Awb speed

▷ Awb_lock

awb_lock : used for AWB lock range control

(awb_lock range = | R/Bgain – R/Btarget | / R/Btarget)

▷ Awb_speed

awb_speed : used for AWB speed control.

Setting range of awb_speed is 01h to 10h. If awb_speed has high value, auto white balance speed will be faster. However, high awb_speed value may cause AWB oscillation.

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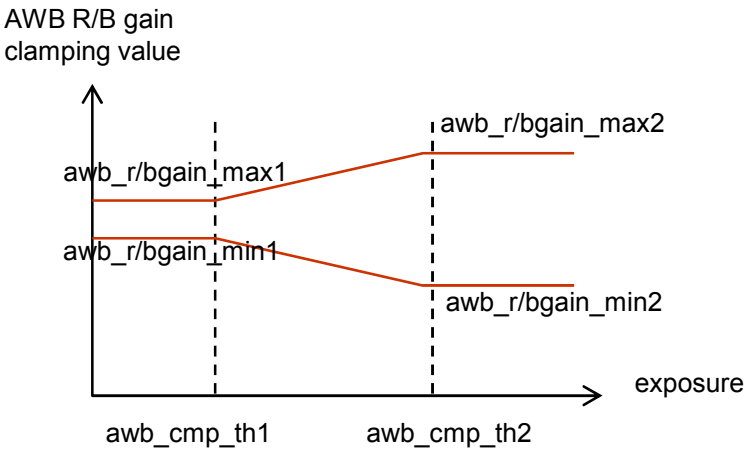
(635~646) AWB gain min/max clamping reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
635	7B	awb_rgain_min1	0	00	00000000	RW	5	0	Awb gain min / max clamping control reference
636	7C	awb_rgain_min2	0	00	00000000	RW	5	0	
637	7D	awb_rgain_max1	255	FF	11111111	RW	5	0	
638	7E	awb_rgain_max2	255	FF	11111111	RW	5	0	
639	7F	awb_bgain_min1	0	00	00000000	RW	5	0	
640	80	awb_bgain_min2	0	00	00000000	RW	5	0	
641	81	awb_bgain_max1	255	FF	11111111	RW	5	0	
642	82	awb_bgain_max2	255	FF	11111111	RW	5	0	
643	83	awb_cmp_th1_h	2	02	00000010	RW	5	0	
644	84	awb_cmp_th1_m	3	03	00000011	RW	5	0	
645	85	awb_cmp_th2_h	4	04	00000100	RW	5	0	
646	86	awb_cmp_th2_m	6	06	00000110	RW	5	0	

▷ **Awb_r/bgain_min/max**

These registers are used for AWB gain clamping control.



AWB R/B gain min/max clamping reference registers should be,

00h < awb_r/bgain_min1 < awb_r/bgain_max1 < FFh

00h < awb_r/bgain_min2 < awb_r/bgain_max2 < FFh

minexp < awb_cmp_th1 < awb_cmp_th2 < maxexp

Where, minexp/maxexp are register value.

< Group C >

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables (Detailed) : Group D

(768~825) Monitoring registers

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
768	00	DeviceID_H	128	80	10000000	RO	0	0	Device ID
769	01	DeviceID_L	48	30	00110000	RO	0	0	
770	02	RevNumber	0	00	00000000	RO	0	0	Revision number
771	03	bank	0	00	00000000	RW	5	0	Register group selector
772	04	m_tg_frameheight_H	0	00	00000000	RO	0	0	Tg framehieht monitoring
773	05	m_tg_frameheight_L	0	00	00000000	RO	0	0	
774	06	tgglbgain	0	00	00000000	RO	0	0	Tg globalgain monitoring
775	07	m_inttime_tgout_H	0	00	00000000	RO	0	0	Tg integration time monitoring
776	08	m_inttime_tgout_M	0	00	00000000	RO	0	0	
777	09	m_inttime_tgout_L	0	00	00000000	RO	0	0	
778	0A	tg_errors	0	00	00000000	RO	0	0	Tg error monitoring
792	18	num_center_byte2	0	00	00000000	RO	0	0	Number of pixel in ae center window
793	19	num_center_byte1	0	00	00000000	RO	0	0	
794	1A	num_center_byte0	0	00	00000000	RO	0	0	
795	1B	num_peri_byte2	0	00	00000000	RO	0	0	Number of pixel in ae peripheral window
796	1C	num_peri_byte1	0	00	00000000	RO	0	0	
797	1D	num_peri_byte0	0	00	00000000	RO	0	0	
798	1E	num_sat_c_byte2	0	00	00000000	RO	0	0	Number of saturation pixel in ae center window
799	1F	num_sat_c_byte1	0	00	00000000	RO	0	0	
800	20	num_sat_c_byte0	0	00	00000000	RO	0	0	
801	21	num_sat_peri_byte2	0	00	00000000	RO	0	0	Number of saturation pixel in ae peripheral window
802	22	num_sat_peri_byte1	0	00	00000000	RO	0	0	
803	23	num_sat_peri_byte0	0	00	00000000	RO	0	0	
804	24	sum_center_byte3	0	00	00000000	RO	0	0	Sumation of pixel in ae center window
805	25	sum_center_byte2	0	00	00000000	RO	0	0	
806	26	sum_center_byte1	0	00	00000000	RO	0	0	
807	27	sum_center_byte0	0	00	00000000	RO	0	0	
808	28	sum_peri_byte3	0	00	00000000	RO	0	0	Sumation of pixle in ae peripheral window
809	29	sum_peri_byte2	0	00	00000000	RO	0	0	
810	2A	sum_peri_byte1	0	00	00000000	RO	0	0	
811	2B	sum_peri_byte0	0	00	00000000	RO	0	0	
812	2C	auto_fcnt	0	00	00000000	RO	0	0	Auto frame counter monitoring
813	2D	monitor_sfcount	0	00	00000000	RO	0	0	Awb sfcounter monitoring
815	2F	awb_flag	0	00	00000000	RO	0	0	Awb flack monitoring
816	30	avg_r_c	0	00	00000000	RO	0	0	Average of rgb in awb center window
817	31	avg_g_c	0	00	00000000	RO	0	0	
818	32	avg_b_c	0	00	00000000	RO	0	0	
819	33	avg_r_p	0	00	00000000	RO	0	0	Average of rgb in awb peripheral window
820	34	avg_g_p	0	00	00000000	RO	0	0	
821	35	avg_b_p	0	00	00000000	RO	0	0	
822	36	m_awb_weight_c	0	00	00000000	RO	0	0	Current awb weight monitoring
823	37	m_awb_weight_p	0	00	00000000	RO	0	0	
825	39	monitor_proximity	0	00	00000000	RO	0	0	Proximity monitoring

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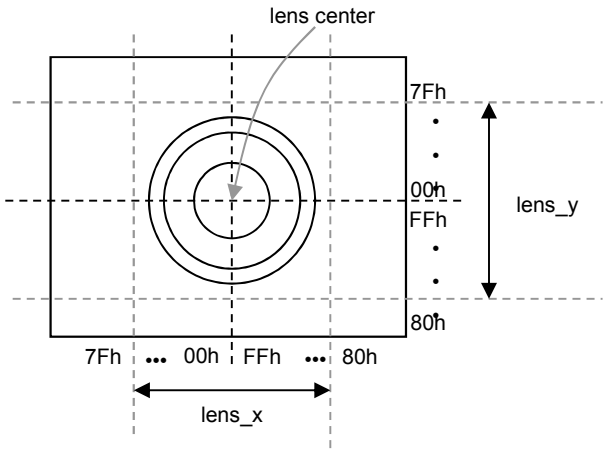
(841~842) Origin control of lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
841	49	lens_x	0	00	00000000	RW	5	0	Lens center position
842	4A	lens_y	0	00	00000000	RW	5	0	

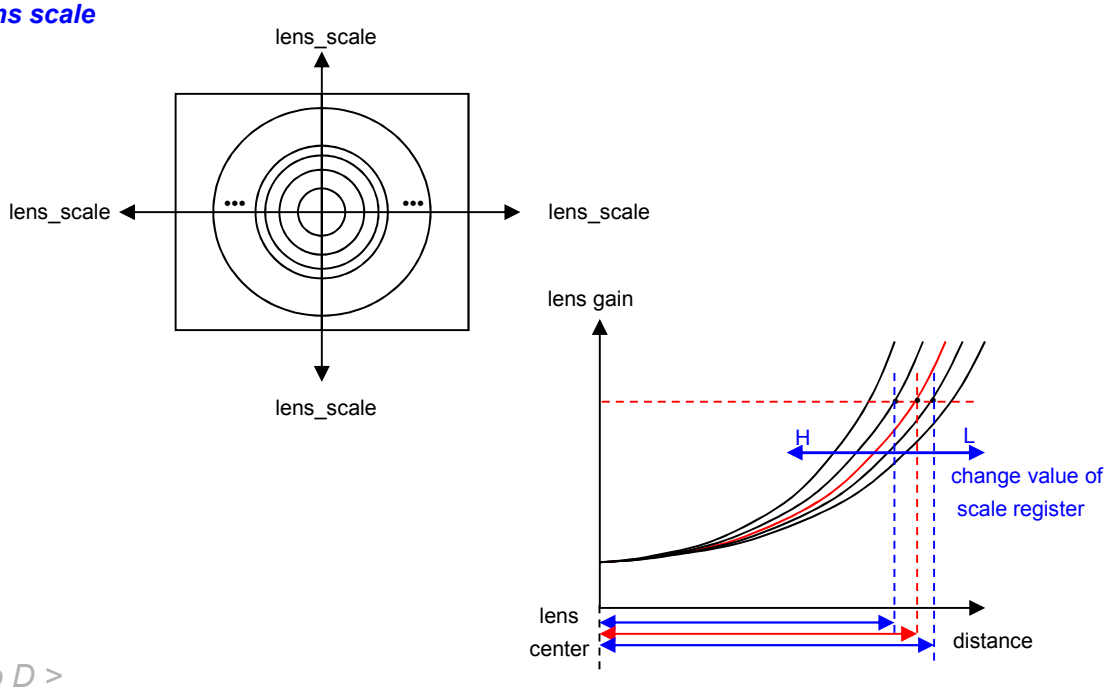
▷ **Lens shading origin control**



(843) Scale of lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
843	4B	lens_scale	81	51	01010001	RW	5	0	Lens scale

▷ **Lens scale**



< Group D >

(847~851) Frame restart

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
847	4F	cnt_init	0	00	00000000	RW	5	0	frame restart enable/disable
848	50	rcount_init_h	0	00	00000000	RW	5	0	Rcount reset value
849	51	rcount_init_l	0	00	00000000	RW	5	0	
850	52	ccount_init_h	0	00	00000000	RW	5	0	Ccount reset value
851	53	ccount_init_l	0	00	00000000	RW	5	0	

▷ Frame restart

To synchronize sensor operation, user set cnt_init register to '1'.

Then PO8030D restart counting from rcount_init and ccount_init to current frameheight & framewidth.

▶ cnt_init : Frame restart enable/disable register.

This register cleared internally.

▶ rcount_init : Row counter initialize value control register .

▶ ccount_init : Column counter initialize value control register .

(855~857) Dark y contrast fitting control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
855	57	dark_ycontrast0	64	40	01000000	RW	5	0	Dark Y contrast fitting control
856	58	dark_ycontrast1	64	40	01000000	RW	5	0	
857	59	dark_ycontrast2	64	40	01000000	RW	5	0	

▷ ***dark_ycontrast***

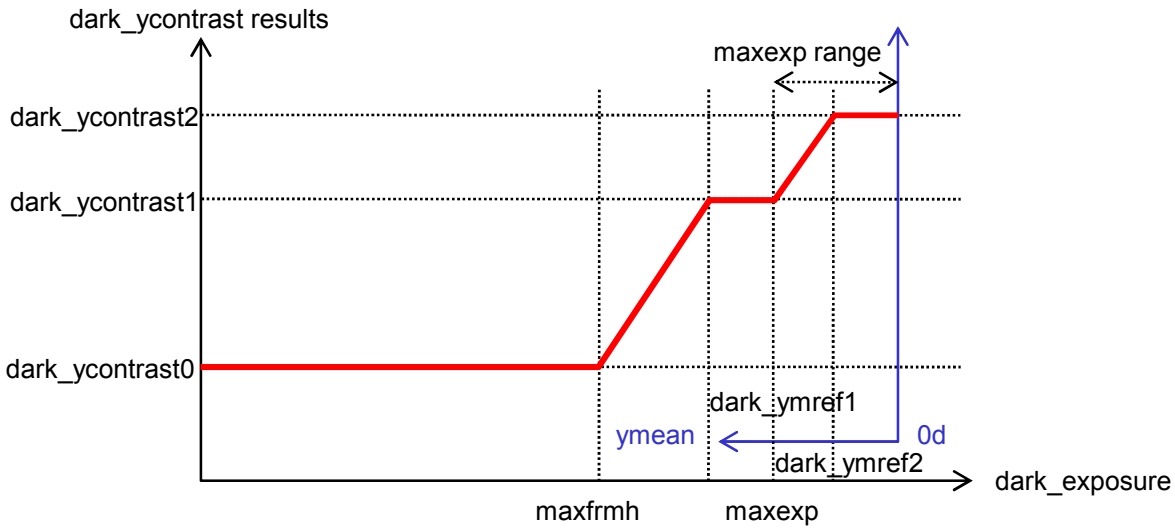
ycontrast control registers.

When auto_control3[0] = '0b', then user can program ycontrast manually.

Also, user can change ycontrast

★ ***dark_ycontrast conditions*** are given as

00h ≤ dark_ycontrast0 ≤ dark_ycontrast1 ≤ dark_ycontrast2 ≤ FFh



(859~861) Dark y brightness fitting control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
859	5B	dark_ybrightness0	0	00	00000000	RW	5	0	Dark Y brightness fitting control
860	5C	dark_ybrightness1	0	00	00000000	RW	5	0	
861	5D	dark_ybrightness2	0	00	00000000	RW	5	0	

▷ ***dark_ybrightness***

ybrightness control registers.

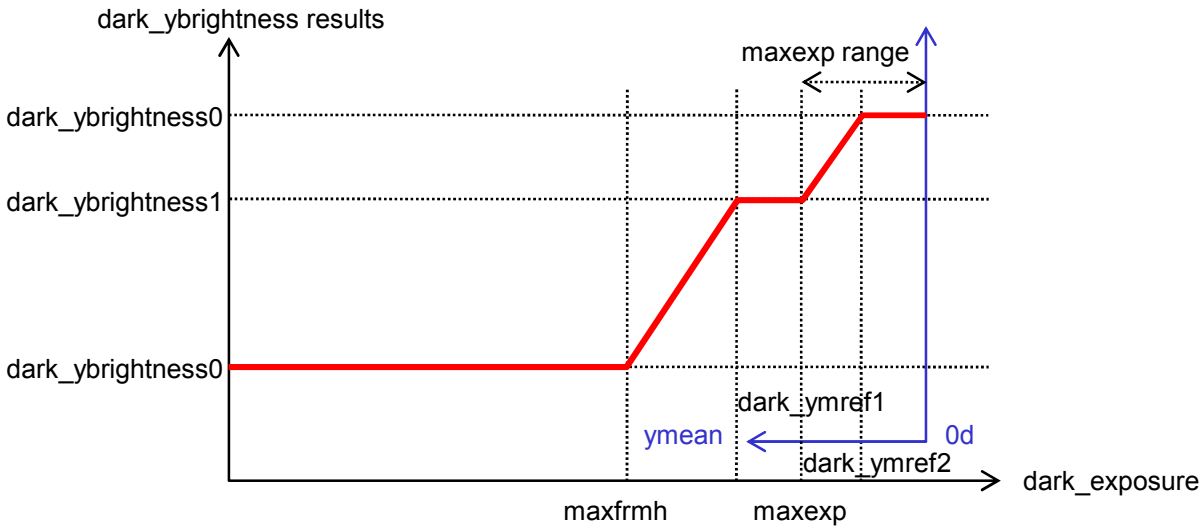
When auto_control3[0] = '0b', then user can program ybrightness manually.

Also, user can change ybrightness.

ybrightness is the two's complement binary numbers .

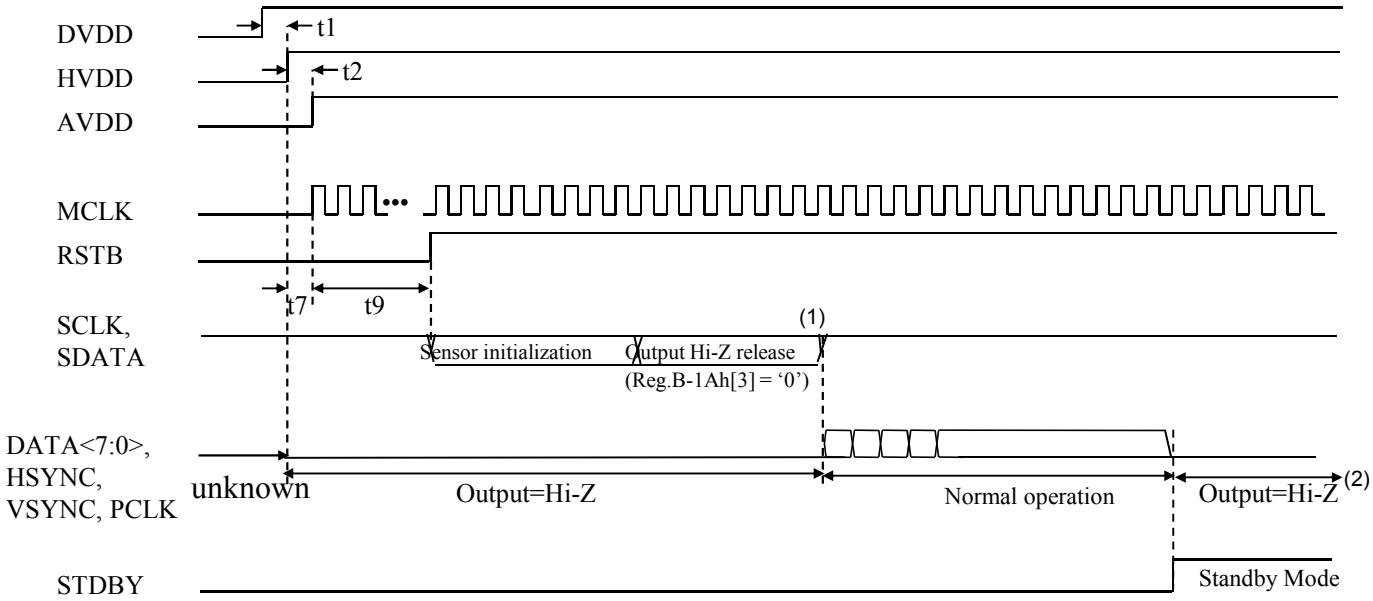
★ ***dark_ybrightness conditions*** are given as

80h ≤ dark_ybrightness0 ≤ dark_ybrightness1 ≤ dark_ybrightness2 ≤ 7Fh



< Group D >

Power-On Sequence



(1) Output state is Hi-Z in default. To release output Hi-Z state, set Reg.A-5Bh[6] to '0'

(2) To make output Hi-Z state in power-down mode, set Reg.A-5Bh[5] to '1' before starting power-down mode

Power-Off Sequence

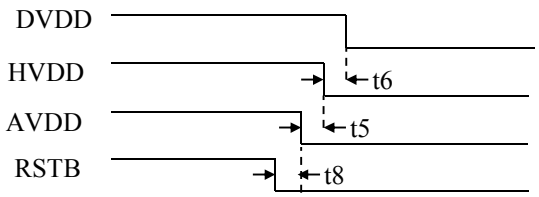


Table6. Recommended Power-On/Off sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From DVDD rising to HVDD rising	0			ns
t2	From HVDD rising to AVDD rising	0			ns
t5	From AVDD falling to HVDD falling	0			ns
t6	From HVDD falling to DVDD falling	0			ns
t7	From HVDD rising to initial mclk rising	0			ns
t8	From RSTB falling to AVDD falling	0			ns
t9	Minimum reset time	8 x MCLK period			