PNX8526

Programmable source decoder with integrated peripherials

Rev. 02 — 11 July 2005 Product data sheet

1. General description

The PNX8526 is a highly integrated media processor for use in Advanced Set Top Boxes (ASTB) and Digital Television (DTV) systems. The PNX8526 is targeted at the mid to high-end ASTB/DTV systems, decoding ‘all format’ HD and SD MPEG-2 source material with Standard Definition (SD), or double line-rate SD display capabilities. Although the PNX8526 can process high level input formats, its display capabilities are primarily targeted at NTSC, PAL and SECAM televisions. It is also intended for lower cost DTVs, those not considered high definition. Progressive output is also available for double line-rate television displays, or for high resolution graphic content to be displayed on a computer monitor. The PNX8526 is designed in a high performance 0.12 micron process.

The PNX8526 performs source decode functions, including conditional access, MPEG-2 transport stream demultiplexing, MPEG-2 video decode, audio decode and processing, graphics generation, video processing, and image composition and display. A 32-bit, 200 MHz VLIW processor, referred to as the TriMedia 3200 CPU core (TM32 CPU), carries out the majority of media processing operations performed by the PNX8526. Fixed function hardware will perform some operations that are not handled by the TM32 CPU. Additionally, the PNX8526 supports a number of peripheral interfaces such as I^2C-bus, USB, IDE and UART. Other interfaces such as IEEE-1284 and Ethernet may be supported via SuperI/O devices that reside on a PCI expansion bus. The expansion bus also provides for glueless interface to 8-bit wide slave devices, such as flash/ROM, DOCSIS modem, UARTs, etc.

An embedded MIPS processor (PR3940) running at 150 MHz is intended to run the OS. (There is no direct support for an external processor; however, a CPU of any type may be connected to the PNX8526 via the PCI interface.) This implies a complete CPU subsystem consisting of the CPU itself, local memory, and an interface to PCI. The MIPS processor is primarily responsible for control functions and graphics-intensive operating systems, while the TM32 CPU is responsible for running all real-time media processing functions. All resources supported within the PNX8526 are accessible by both the MIPS processor and the TM32 CPU. The software documentation of the PNX8526 provides more details on the interaction between the MIPS and the TM32 CPU.

The PNX8526 is intended to be used with a small companion IC, the PNX8510. This analog companion chip provides the majority of analog video and audio support for the output of the PNX8526. The PNX8510 companion is capable of simultaneously driving two video channels (six DACs) and two stereo audio channels (four DACs).

2. Features

- 200 MHz, 5-instruction/clock cycle, 32-bit VLIW processing core (TM32 CPU)
- 150 MHz, MIPS PR3940 processing core
- External CPU support via PCI
- Support for multiple digital video (D1) input streams
- Support for multiple MPEG-2 or DIRECTV transport streams (parallel format)
- On-chip conditional access for DVB, DES, MULTI2, CAM and DIRECTV
- On-chip copy protection support for OpenCable and ATSC (NRSS-B)
- Simultaneous decode of two SD streams (MPEG-2) or one HD MPEG stream (AFD style HD-SD decode)
- Simultaneous decode of two AC-3 or equivalent audio streams
- High performance 2D rendering and DMA capability
- Dual image composition/screen refresh engines: four layer primary output, two layer secondary output
- Multiple channel output to support watch/record and multi-room modes
- Embedded 1394 link layer with 5C copy protection
- Soft modem support via SSI interface
- 16 MB, 32 MB and 64 MB unified memory architecture implemented with high-speed SDRAM (166 MHz)
- System expansion capability via industry standard PCI bus
- Core peripherals (I^2C-bus, UART, USB, etc.) on the chip, other peripherals supported via third-party ‘SuperI/O’ chip.

3. Applications

- Advanced Set Top Box (ASTB)
- Digital Television (DTV)

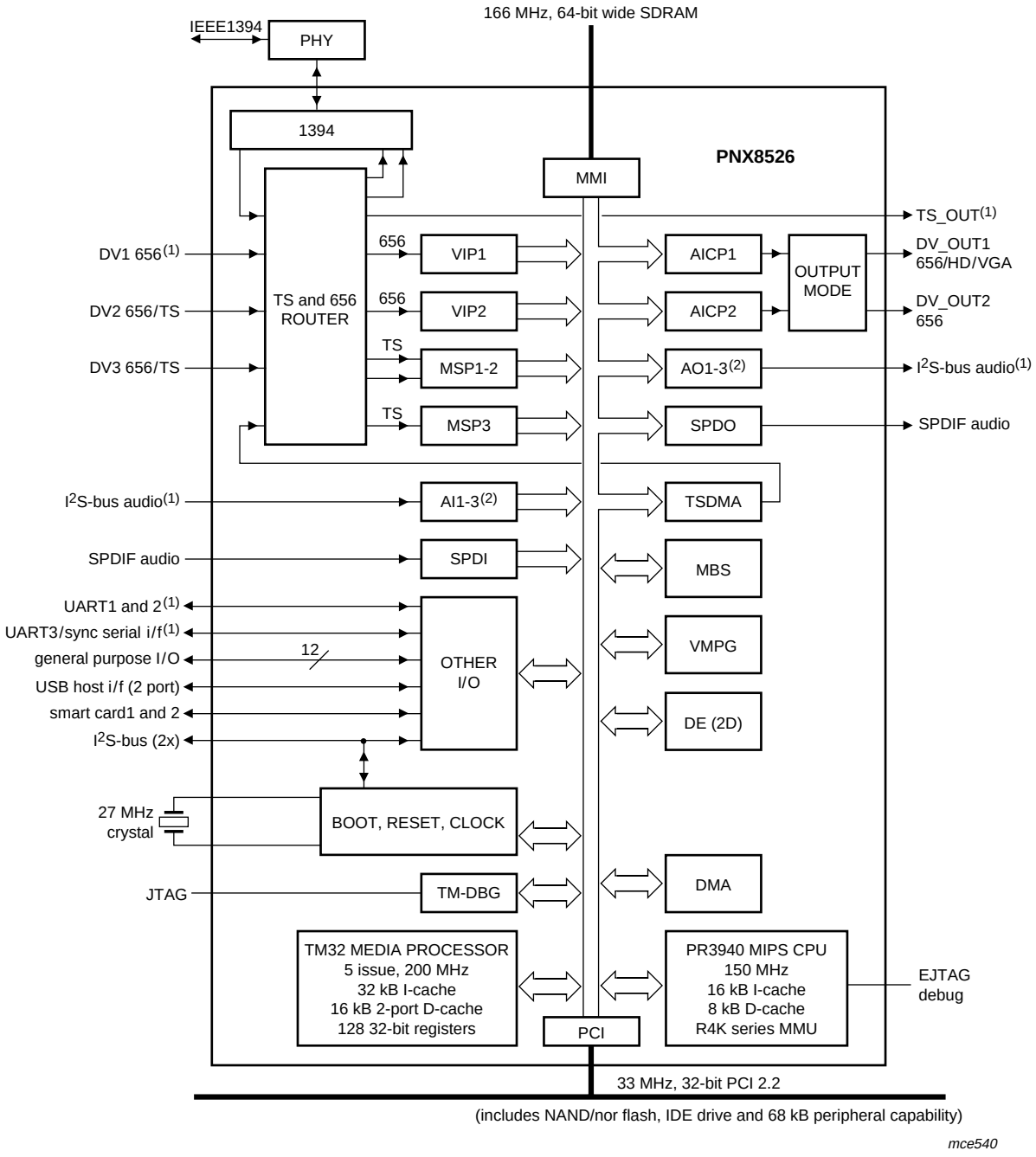
4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PNX8526EH/M0	HBGA456	plastic thermal enhanced ball grid array package; 456 balls; body 35 × 35 × 1.8 mm; heatsink	SOT610-1
PNX8526EH/M0/G	HBGA456 [1]	plastic thermal enhanced ball grid array package; 456 balls; body 35 × 35 × 1.8 mm; heatsink	SOT610-1

[1] Lead-free (Pb-free) package.

5. Block diagram



(1) I/O can also function as general purpose a serial input/output.

(2) Due to pin sharing, either AI1-3 or AO1-3 can be active, not both (audio input/output data bits S_IO_SD[3:0]).

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

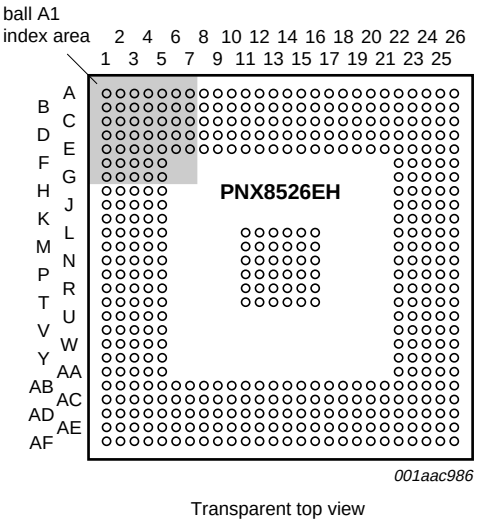


Fig 2. Pin configuration

6.2 Pin description

All pad inputs and input/output have built-in pull-up resistors (approximately 80 kΩ) and Schmitt trigger input thresholds. (See Table 18 for maximum ratings).

The following pins do not have pull-ups resistors:

XTALI, PCIx, analog pins, I^2C-bus, main memory interface, USB_DPx and USB_DMx.

The following pins do not have Schmitt trigger inputs:

XTALI, analog pins, USB_DPx and USB_DMx.

Table 2: Peripheral Controller Interface (PCI)

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
PCI_AD[31]	AB1	I/O	multiplexed address or data bit 31	
PCI_AD[30]	AB2	I/O	multiplexed address or data bit 30	
PCI_AD[29]	AB3	I/O	multiplexed address or data bit 29	
PCI_AD[28]	AB4	I/O	multiplexed address or data bit 28	
PCI_AD[27]	AC1	I/O	multiplexed address or data bit 27	
PCI_AD[26]	AC2	I/O	multiplexed address or data bit 26	
PCI_AD[25]	AC3	I/O	multiplexed address or data bit 25	
PCI_AD[24]	AD2	I/O	multiplexed address or data bit 24	
PCI_AD[23]	AE3	I/O	multiplexed address or data bit 23	
PCI_AD[22]	AF4	I/O	multiplexed address or data bit 22	

Table 2: Peripheral Controller Interface (PCI) *…continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
PCI_AD[21]	AE4	I/O	multiplexed address or data bit 21	
PCI_AD[20]	AD4	I/O	multiplexed address or data bit 20	
PCI_AD[19]	AE5	I/O	multiplexed address or data bit 19	
PCI_AD[18]	AD5	I/O	multiplexed address or data bit 18	
PCI_AD[17]	AC5	I/O	multiplexed address or data bit 17	
PCI_AD[16]	AC6	I/O	multiplexed address or data bit 16	
PCI_AD[15]	AD8	I/O	multiplexed address or data bit 15	
PCI_AD[14]	AC8	I/O	multiplexed address or data bit 14	
PCI_AD[13]	AF9	I/O	multiplexed address or data bit 13	
PCI_AD[12]	AE9	I/O	multiplexed address or data bit 12	
PCI_AD[11]	AD9	I/O	multiplexed address or data bit 11	
PCI_AD[10]	AC9	I/O	multiplexed address or data bit 10	
PCI_AD[9]	AF10	I/O	multiplexed address or data bit 9	
PCI_AD[8]	AE10	I/O	multiplexed address or data bit 8	
PCI_AD[7]	AC10	I/O	multiplexed address or data bit 7	
PCI_AD[6]	AF11	I/O	multiplexed address or data bit 6	
PCI_AD[5]	AE11	I/O	multiplexed address or data bit 5	
PCI_AD[4]	AD11	I/O	multiplexed address or data bit 4	
PCI_AD[3]	AC11	I/O	multiplexed address or data bit 3	
PCI_AD[2]	AE12	I/O	multiplexed address or data bit 2	
PCI_AD[1]	AD12	I/O	multiplexed address or data bit 1	
PCI_AD[0]	AC12	I/O	multiplexed address or data bit 0	
PCI_CBE[3]	AD1	I/O	multiplexed command or byte enable 3	
PCI_CBE[2]	AF5	I/O	multiplexed command or byte enable 2	
PCI_CBE[1]	AE8	I/O	multiplexed command or byte enable 1	
PCI_CBE[0]	AD10	I/O	multiplexed command or byte enable 0	
CLK	AA1	I	PCI bus clock	
PCI_DEVSEL	AF7	I/O	device select is asserted when a target address is decoded and remains asserted to indicate that a target device is selected	
PCI_FRAME	AF6	I/O	frame is asserted to indicate start of bus transaction and remains asserted until final data phase begins	
PCI_GNT	Y3	I/O	arbitration grant is asserted to indicate access to the bus has been granted; this pin is an input when an external arbiter is used and an output when using the internal arbiter	
PCI_GNT_A	Y4	I/O	auxiliary arbitration PCI_GNT_A is asserted to indicate bus access has been granted to an external PCI master; used where internal arbiter is configured	#

Table 2: Peripheral Controller Interface (PCI) *...continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
PCI_GNT_B	AA4	I/O	auxiliary arbitration grant PCI_GNT_B is asserted to indicate bus access has been granted to an external PCI master; used where internal arbiter is configured	#
IDSEL	AF3	I/O	initialization device select provides chip select during configuration read and write transactions	
PCI_INTA	V4	I/O	interrupt a is asserted to request an interrupt; this pin may be configured as an input if the internal pic is used, or as an output if the external interrupt controller is used; polarity in active low	
PCI_IRDY	AE6	I/O	initiator ready is asserted during writes to indicate valid data on AD[31:0]. also asserted during reads to indicate the target is prepared to accept data. wait states are inserted until PCI_IRDY and PCI_TRDY are both asserted	
PCI_PAR	AF8	I/O	parity supports even parity across the PCI address/data bus PCI_AD[31:0]) and command/ byte enable bus (PCI_CBE[3:0]); the bus master drives PCI_PAR for address and write data phases. the target drives PCI_PAR for the read data phases	
PCI_PERR	AD7	I/O	parity error indicates data parity errors during all PCI transactions except special cycle	
PCI_REQ	Y2	I/O	arbitration request on PCI bus; request is an output when using an external arbiter and an input when using an internal arbiter	
PCI_REQ_A	AA2	I/O	auxiliary arbitration PCI_REQ_A on PCI bus; used in modes where internal arbiter is configured	#
PCI_REQ_B	AA3	I/O	auxiliary arbitration PCI_REQ_B on PCI bus; used in modes where internal arbiter is configured	#
RESET_IN	W3	I	PCI bus global reset	
PCI_SERR	AC7	I/O	system error	
PCI_STOP	AE7	I/O	stop is asserted to indicate a request from the target for the master to stop the current transmission	
PCI_TRDY	AD6	I/O	target ready is asserted during reads to indicate valid data on AD[31:0]; it is asserted during writes to indicate the target is prepared to accept data; wait states are inserted until PCI_IRDY and PCI_TRDY are both asserted	

Table 3: Miscellaneous system interface (MISC)

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
XIO_A25	AE13	I/O	XIO address bit 25	#
XIO_ACK	AF13	I/O	XIO Acknowledge (EEPROM)	#
XIO_SEL[2]	AF12	I/O	external input/output select2	#
XIO_SEL[1]	AC13	I/O	external input/output select1	#
XIO_SEL[0]	AD13	I/O	external input/output select0	#
SYS_RSTN_OUT	Y1	O	system reset output	#

Table 4: Main Memory Interface (MMI)

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
MA[11]	C22	O	memory address bit 11	
MA[10]	B21	O	memory address bit 10	
MA[9]	A21	O	memory address bit 9	
MA[8]	C21	O	memory address bit 8	
MA[7]	A20	O	memory address bit 7	
MA[6]	C20	O	memory address bit 6	
MA[5]	D18	O	memory address bit 5	
MA[4]	D19	O	memory address bit 4	
MA[3]	C19	O	memory address bit 3	
MA[2]	D20	O	memory address bit 2	
MA[1]	B20	O	memory address bit 1	
MA[0]	D21	O	memory address bit 0	
MD[63]	M25	I/O	memory data bit 63	
MD[62]	M24	I/O	memory data bit 62	
MD[61]	M23	I/O	memory data bit 61	
MD[60]	L26	I/O	memory data bit 60	
MD[59]	L25	I/O	memory data bit 59	
MD[58]	L24	I/O	memory data bit 58	
MD[57]	L23	I/O	memory data bit 57	
MD[56]	K26	I/O	memory data bit 56	
MD[55]	K24	I/O	memory data bit 55	
MD[54]	K23	I/O	memory data bit 54	
MD[53]	J26	I/O	memory data bit 53	
MD[52]	J25	I/O	memory data bit 52	
MD[51]	J24	I/O	memory data bit 51	
MD[50]	J23	I/O	memory data bit 50	
MD[49]	H26	I/O	memory data bit 49	
MD[48]	H25	I/O	memory data bit 48	
MD[47]	H23	I/O	memory data bit 47	

Table 4: Main Memory Interface (MMI) *...continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
MD[46]	G26	I/O	memory data bit 46	
MD[45]	G25	I/O	memory data bit 45	
MD[44]	G24	I/O	memory data bit 44	
MD[43]	G23	I/O	memory data bit 43	
MD[42]	F26	I/O	memory data bit 42	
MD[41]	F25	I/O	memory data bit 41	
MD[40]	F24	I/O	memory data bit 40	
MD[39]	F23	I/O	memory data bit 39	
MD[38]	E25	I/O	memory data bit 38	
MD[37]	E24	I/O	memory data bit 37	
MD[36]	D25	I/O	memory data bit 36	
MD[35]	D26	I/O	memory data bit 35	
MD[34]	E23	I/O	memory data bit 34	
MD[33]	D24	I/O	memory data bit 33	
MD[32]	C25	I/O	memory data bit 32	
MD[31]	A18	I/O	memory data bit 31	
MD[30]	B18	I/O	memory data bit 30	
MD[29]	C18	I/O	memory data bit 29	
MD[28]	A19	I/O	memory data bit 28	
MD[27]	B17	I/O	memory data bit 27	
MD[26]	C17	I/O	memory data bit 26	
MD[25]	D17	I/O	memory data bit 25	
MD[24]	A16	I/O	memory data bit 24	
MD[23]	B16	I/O	memory data bit 23	
MD[22]	C16	I/O	memory data bit 22	
MD[21]	D16	I/O	memory data bit 21	
MD[20]	A15	I/O	memory data bit 20	
MD[19]	B15	I/O	memory data bit 19	
MD[18]	C15	I/O	memory data bit 18	
MD[17]	D15	I/O	memory data bit 17	
MD[16]	C14	I/O	memory data bit 16	
MD[15]	A14	I/O	memory data bit 15	
MD[14]	D14	I/O	memory data bit 14	
MD[13]	A13	I/O	memory data bit 13	
MD[12]	B13	I/O	memory data bit 12	
MD[11]	C13	I/O	memory data bit 11	
MD[10]	D13	I/O	memory data bit 10	
MD[9]	A12	I/O	memory data bit 9	
MD[8]	B12	I/O	memory data bit 8	

Table 4: Main Memory Interface (MMI) *...continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
MD[7]	C12	I/O	memory data bit 7	
MD[6]	A11	I/O	memory data bit 6	
MD[5]	B11	I/O	memory data bit 5	
MD[4]	D11	I/O	memory data bit 4	
MD[3]	A10	I/O	memory data bit 3	
MD[2]	C11	I/O	memory data bit 2	
MD[1]	B10	I/O	memory data bit 1	
MD[0]	C10	I/O	memory data bit 0	
MDQM[7]	K25	O	SDRAM control bit 7	
MDQM[6]	H24	O	SDRAM control bit 6	
MDQM[5]	E26	O	SDRAM control bit 5	
MDQM[4]	A24	O	SDRAM control bit 4	
MDQM[3]	A17	O	SDRAM control bit 3	
MDQM[2]	B14	O	SDRAM control bit 2	
MDQM[1]	D12	O	SDRAM control bit 1	
MDQM[0]	A9	O	SDRAM control bit 0	
MBA[1]	D22	O	SDRAM bank select	
MBA[0]	B22	O	SDRAM bank select	
MCKE	C23	O	memory clock enable	
MCLK[1]	C26	O	memory clock bit 1	
MCLK[0]	B19	O	memory clock bit 0	
MCS	A22	O	memory chip select	
MRAS	B23	O	EDODRAM row address strobe	
MCAS	A23	O	memory column address select	
MWE	B24	O	memory write enable	

Table 5: General Purpose Input/Output (GPIO)

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
GPIO[11]	N26	I/O	general purpose input/output bit 11	#
GPIO[10]	N24	I/O	general purpose input/output bit 10	#
GPIO[9]	N23	I/O	general purpose input/output bit 9	#
GPIO[8]	M26	I/O	general purpose input/output bit 8	
GPIO[7]	AE14	I/O	general purpose input/output bit 7	
GPIO[6]	AF14	I/O	general purpose input/output bit 6	
GPIO[5]	AD14	I/O	general purpose input/output bit 5	
GPIO[4]	AC14	I/O	general purpose input/output bit 4	
GPIO[3]	C5	I/O	general purpose input/output bit 3	

Table 5: General Purpose Input/Output (GPIO) *...continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
GPIO[2]	B4	I/O	general purpose input/output bit 2	#
GPIO[1]	D5	I/O	general purpose input/output bit 1	#
GPIO[0]	C4	I/O	general purpose input/output bit 0	#

Table 6: Serial communication (COM)

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
UA1_TX	U24	I/O	UART1 transmit	#
UA1_RX	U25	I/O	UART1 receive	#
UA2_TX	T23	I/O	UART2 transmit	#
UA2_RX	U26	I/O	UART2 receive	#
UA2_RTSN	T24	I/O	UART2 request to send	#
UA2_CTSN	T25	I/O	UART2 clear to send	#
SC1_DA	T26	I/O	smart card1 data	
SC1_CMD	R23	O	smart card1 command	
SC1_RST	R24	O	smart card1 reset	
SC1_OFFN	R25	I	smart card1 off	
SC1_SCCK	R26	O	smart card1 bit clock	
SC2_DA	P23	I/O	smart card2 data	
SC2_CMD	P24	O	smart card2 command	
SC2_RST	P26	O	smart card2 reset	
SC2_OFFN	P25	I	smart card2 off	
SC2_SCCK	N25	O	smart card2 bit clock	
SSI_SCLK_CTSN	V1	I/O	synchronous serial interface clock input	#
SSI_FS_RTSN	V2	I/O	synchronous serial interface frame sync	#
SSI_RXD	U4	I/O	synchronous serial interface receive	#
SSI_TXD	V3	I/O	synchronous serial interface transmit	#

Table 7: Universal Serial Bus (USB)

Symbol	Pin	Type	Description
USB_DP[1]	A5	I/O	data plus bit 1
USB_DP[0]	B6	I/O	data plus bit 0
USB_DM[0]	C6	I/O	data minus bit 0
USB_DM[1]	D7	I/O	data minus bit 1
USB_PWR	W1	O	USB port power on/off
			0 = power on
			1 = power off

Table 7: Universal Serial Bus (USB) *...continued*

Symbol	Pin	Type	Description
USB_OVRCUR	W2	I	indicates over current being drawn by a USB device
			0 = over current detected
			1 = no over current

Table 8: IEEE 1394 port

Symbol	Pin	Type	Description
PHY_D[7]	B9	I/O	PHY data bit 7; data is expected on ports 7:0 for 400 MB packets
PHY_D[6]	D10	I/O	PHY data bit 6; data is expected on ports 7:0 for 400 MB packets
PHY_D[5]	C9	I/O	PHY data bit 5; data is expected on ports 7:0 for 400 MB packets
PHY_D[4]	A8	I/O	PHY data bit 4; data is expected on ports 7:0 for 400 MB packets
PHY_D[3]	B8	I/O	PHY data bit 3; data is expected on ports 3:0 for 200 MB packets
PHY_D[2]	D9	I/O	PHY data bit 2; data is expected on ports 3:0 for 200 MB packets
PHY_D[1]	C8	I/O	PHY data bit 1; data is expected on ports 1:0 for 100 MB packets
PHY_D[0]	A7	I/O	PHY data bit 0; data is expected on ports 1:0 for 100 MB packets
PHY_CTL[1]	B7	I/O	PHY control bit 1; indicates the mode for data on the Din port
PHY_CTL[0]	C7	I/O	PHY control bit 0; indicates the mode for data on the Din port
PHY_LREQ	B5	O	used by the link to make bus requests and to access PHY registers; this is a serial bus; a train of pulses is sent on this signal
PHY_ISO_N	A6	I	signals which type of isolation mode is used at the PHY-Link interface
			0 = this is 1394-1995 annex J type isolation; enables differentiator circuitry
			1 = direct connection or single capacitor isolation mode; this will disable the differentiator circuitry
CLK_L1394	D8	I	system clock. 49.152 MHz input

Table 9: Serial communication port (I^2C-bus)

Symbol	Pin	Type	Description
I2C1_SCL	D6	I/O	serial communications port (I^2C-bus) clock
I2C1_SDA	A4	I/O	serial communications port (I^2C-bus) data
I2C2_SCL	H1	I/O	serial communications port (I^2C-bus) clock
I2C2_SDA	K4	I/O	serial communications port (I^2C-bus) data

Table 10: Audio and video interface

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
DV_OUT1[9]	M2	O	digital video output1; bit 9 for primary display channel from AICP	
DV_OUT1[8]	M1	O	digital video output1; bit 8 for primary display channel from AICP	
DV_OUT1[7]	N4	O	digital video output1; bit 7 for primary display channel from AICP	

Table 10: Audio and video interface *...continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
DV_OUT1[6]	N3	O	digital video output1; bit 6 for primary display channel from AICP	
DV_OUT1[5]	N1	O	digital video output1; bit 5 for primary display channel from AICP	
DV_OUT1[4]	N2	O	digital video output1; bit 4 for primary display channel from AICP	
DV_OUT1[3]	P2	O	digital video output1; bit 3 for primary display channel from AICP	
DV_OUT1[2]	P1	O	digital video output1; bit 2 for primary display channel from AICP	
DV_OUT1[1]	P4	O	digital video output1; bit 1 for primary display channel from AICP	
DV_OUT1[0]	P3	O	digital video output1; bit 0 for primary display channel from AICP	
DV_OUT2[9]	R2	O	digital video output2; bit 9 for secondary display channel from AICP	
DV_OUT2[8]	R4	O	digital video output2; bit 8 for secondary display channel from AICP	
DV_OUT2[7]	R3	O	digital video output2; bit 7 for secondary display channel from AICP	
DV_OUT2[6]	T1	O	digital video output2; bit 6 for secondary display channel from AICP	
DV_OUT2[5]	T2	O	digital video output2; bit 5 for secondary display channel from AICP	
DV_OUT2[4]	T3	O	digital video output2; bit 4 for secondary display channel from AICP	
DV_OUT2[3]	U1	O	digital video output2; bit 3 for secondary display channel from AICP	
DV_OUT2[2]	T4	O	digital video output2; bit 2 for secondary display channel from AICP	
DV_OUT2[1]	U2	O	digital video output2; bit 1 for secondary display channel from AICP	
DV_OUT2[0]	U3	O	digital video output2; bit 0 for secondary display channel from AICP	
DV_CLK1	M3	O	digital video clock1 for primary display channel from AICP	
DV_CLK2	R1	O	digital video clock2 for secondary display channel from AICP	
HSYNC	L1	O	horizontal sync for primary display	
VSYNC	L2	I/O	vertical sync for primary display	
BLANK	M4	O	blanking for primary display	
I2S_IN1_OSCLK	AD20	O	audio IN1oversample clock	
I2S_IN1_SCK	AC19	I/O	audio IN1 serial clock	
I2S_IN1_WS	AF21	I/O	audio IN1 word select	

Table 10: Audio and video interface *...continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
I2S_IN1_SD	AE21	I	audio IN1 data	
I2S_IN2_OSCLK	AD21	O	audio IN2 oversample clock	
I2S_IN2_SCK	AC20	I/O	audio IN2 serial clock	
I2S_IN2_WS	AF22	I/O	audio IN2 word select	
I2S_IN2_SD	AE22	I	audio IN2 data	
I2S_IO_OSCLK	AF15	I/O	audio input/output oversample clock	#
I2S_IO_SCK	AE15	I/O	audio input/output serial clock	#
I2S_IO_WS	AC15	I/O	audio input/output word select	#
I2S_IO_SD[3]	AD15	I/O	audio input/output data bit 3	#
I2S_IO_SD[2]	AF16	I/O	audio input/output data bit 2	#
I2S_IO_SD[1]	AE16	I/O	audio input/output data bit 1	#
I2S_IO_SD[0[	AD16	I/O	audio input/output data bit 0	#
I2S_OUT1_OSCLK	K3	O	audio out1 oversample clock	
I2S_OUT1_SCK	J1	I/O	audio out1 serial clock	
I2S_OUT1_WS	J3	I/O	audio out1 word select	
I2S_OUT1_SD	J2	O	audio out1 data	
I2S_OUT2_OSCLK	K2	O	audio out2 oversample clock	#
I2S_OUT2_SCK	L3	I/O	audio out2 serial clock	#
I2S_OUT2_WS	K1	I/O	audio out2 word select	#
I2S_OUT2_SD	L4	O	audio out2 data	#
SPDIF_IN	AF17	I	multi-channel/SPDIF input	
SPDIF_OUT	AC16	O	multi-channel/SPDIF output	

Table 11: Digital video bus

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
DV1_DATA[9]	AE17	I/O	ITU-656 VIP data bit 9 (most significant bit)	#
DV1_DATA[8]	AD17	I/O	ITU-656 VIP data bit 8	#
DV1_DATA[7]	AF18	I/O	ITU-656 VIP data bit 7	#
DV1_DATA[6]	AC17	I/O	ITU-656 VIP data bit 6	#
DV1_DATA[5]	AE18	I/O	ITU-656 VIP data bit 5	#
DV1_DATA[4]	AD18	I/O	ITU-656 VIP data bit 4	#
DV1_DATA[3]	AF19	I/O	ITU-656 VIP data bit 3	#
DV1_DATA[2]	AE19	I/O	ITU-656 VIP data bit 2	#
DV1_DATA[1]	AC18	I/O	ITU-656 VIP data bit 1	#
DV1_DATA[0]	AD19	I/O	ITU-656 VIP data bit 0 (least significant bit)	#
DV1_VALID	AF20	I/O	ITU-656 VIP data valid	#
DV1_CLK	AE20	I/O	ITU-656 VIP data clock	#
DV2_DATA[7]	AF23	I	digital video transport stream2 data bit 7	#

Table 11: Digital video bus *…continued*

 # indicates multiplexed signal, see Section 6.2.1 for more details.

Symbol	Pin	Type	Description	Alternate function
DV2_DATA[6]	AC21	I	digital video transport stream2 data bit 6	#
DV2_DATA[5]	AD22	I	digital video transport stream2 data bit 5	#
DV2_DATA[4]	AE23	I	digital video transport stream2 data bit 4	#
DV2_DATA[3]	AC22	I	digital video transport stream2 data bit 3	#
DV2_DATA[2]	AD23	I	digital video transport stream2 data bit 2	#
DV2_DATA[1]	AE24	I	digital video transport stream2 data bit 1	#
DV2_DATA[0]	AF24	I	digital video transport stream2 data bit 0	#
DV2_SOP	AD24	I	digital video transport stream2 start of packet	#
DV2_ERR	AD26	I	digital video transport stream2 error	#
DV2_VALID	AD25	I	digital video transport stream2 data valid	#
DV2_CLK	AC24	I	digital video transport stream2 clock	#
DV3_DATA[7]	W23	I	digital video transport stream3 data bit 7	#
DV3_DATA[6]	Y24	I	digital video transport stream3 data bit 6	#
DV3_DATA[5]	Y25	I	digital video transport stream3 data bit 5	#
DV3_DATA[4]	Y26	I	digital video transport stream3 data bit 4	#
DV3_DATA[3]	W24	I	digital video transport stream3 data bit 3	#
DV3_DATA[2]	V23	I	digital video transport stream3 data bit 2	#
DV3_DATA[1]	W25	I	digital video transport stream3 data bit 1	#
DV3_DATA[0]	W26	I	digital video transport stream3 data bit 0	#
DV3_SOP	V24	I	digital video transport stream3 start of packet	#
DV3_ERR	U23	I	digital video transport stream3 error	#
DV3_VALID	V25	I	digital video transport stream3 data valid	#
DV3_CLK	V26	I	digital video transport stream3 clock	#
TS_DATA[7]	AB23	I/O	transport stream data bit 7	#
TS_DATA[6]	AC25	I/O	transport stream data bit 6	#
TS_DATA[5]	AB24	I/O	transport stream data bit 5	#
TS_DATA[4]	AA23	I/O	transport stream data bit 4	#
TS_DATA[3]	AC26	I/O	transport stream data bit 3	#
TS_DATA[2]	AB25	I/O	transport stream data bit 2	#
TS_DATA[1]	AB26	I/O	transport stream data bit 1	#
TS_DATA[0]	Y23	I/O	transport stream data bit 0	#
TS_SOP	AA24	I/O	transport stream start of packet (parallel/serial)	#
TS_VALID	AA25	I/O	transport stream data valid (parallel/serial)	#
TS_CLK	AA26	I/O	transport stream clock (parallel/serial)	#

Table 12: Phase Lock Loop (PLL)

Symbol	Pin	Type	Description
XTALI	C2	I	PLL reference crystal input
XTALO	D3	O	PLL reference crystal feedback driver
PLL_OUT	W4	O	general purpose PLL clock output

Table 13: Analog and digital power (PWR)

Symbol	Pin	Description
V_{DDC1}	AB18	system 1.26 V
	AB17	system 1.26 V
	AB14	system 1.26 V
	AB13	system 1.26 V
	AB12	system 1.26 V
	AB9	system 1.26 V
	AB8	system 1.26 V
	N5	system 1.26 V
	P5	system 1.26 V
	U5	system 1.26 V
	V5	system 1.26 V
	K5	system 1.26 V
	J5	system 1.26 V
	E14	system 1.26 V
	E13	system 1.26 V
	E10	system 1.26 V
	E9	system 1.26 V
	E15	system 1.26 V
	E18	system 1.26 V
	E19	system 1.26 V
	U22	system 1.26 V
	V22	system 1.26 V
	P22	system 1.26 V
	N22	system 1.26 V
	K22	system 1.26 V
	J22	system 1.26 V
	D1	system 1.26 V
	E2	system 1.26 V
	E1	system 1.26 V
	G4	system 1.26 V
	F3	system 1.26 V
	F2	system 1.26 V
	F1	system 1.26 V
	H4	system 1.26 V
	G3	system 1.26 V

Table 13: Analog and digital power (PWR) *…continued*

Symbol	Pin	Description
V_{DDC2}	E4	system 1.26 V (analog power 1.728 GHz PLL)
	E3	system 1.26 V (analog power 1.728 GHz PLL)
V_{SS}	D2	system ground (analog ground 1.728 GHz PLL)
	F4	system ground (analog ground 1.728 GHz PLL)
V_{DD1}	AB6	system 3.3 V
	AB7	system 3.3 V
	AB10	system 3.3 V
	AB11	system 3.3 V
	AB16	system 3.3 V
	AB19	system 3.3 V
	AB20	system 3.3 V
	E12	system 3.3 V
	E11	system 3.3 V
	E8	system 3.3 V
	E7	system 3.3 V
	E16	system 3.3 V
	E17	system 3.3 V
	E20	system 3.3 V
	E21	system 3.3 V
	M22	system 3.3 V
	L22	system 3.3 V
	H22	system 3.3 V
	G22	system 3.3 V
	R22	system 3.3 V
	T22	system 3.3 V
	W22	system 3.3 V
	Y22	system 3.3 V
	T5	system 3.3 V
	R5	system 3.3 V
	M5	system 3.3 V
	L5	system 3.3 V
	W5	system 3.3 V
	Y5	system 3.3 V
V_{DD2}	G5	system 3.3 V (CAB)
	H5	system 3.3 V (CAB)
V_{DD3}	AB15	system 3.3 V (TM-PLL)
V_{SS}	AF25	system ground
	AF26	system ground
	AE26	system ground
	AE25	system ground
	AC23	system ground

Table 13: Analog and digital power (PWR) *…continued*

Symbol	Pin	Description
V_{SS}	AB22	system ground
	AB21	system ground
	AA22	system ground
	F22	system ground
	E22	system ground
	D23	system ground
	C24	system ground
	B25	system ground
	A25	system ground
	A26	system ground
	B26	system ground
	L15	system ground
	L14	system ground
	L13	system ground
	L12	system ground
	L11	system ground
	M11	system ground
	N11	system ground
	P11	system ground
	R11	system ground
	T11	system ground
	T12	system ground
	T13	system ground
	R13	system ground
	R14	system ground
	T14	system ground
	T15	system ground
	T16	system ground
	R16	system ground
	AA5	system ground
	AB5	system ground
	AC4	system ground
	AD3	system ground
	AE2	system ground
	AE1	system ground
	AF1	system ground
	AF2	system ground
	F5	system ground
	E5	system ground
	E6	system ground
	D4	system ground

Table 13: Analog and digital power (PWR) *…continued*

Symbol	Pin	Description
V_{SS}	B2	system ground
	A2	system ground
	A1	system ground
	B1	system ground
	R15	system ground
	R12	system ground
	P12	system ground
	P13	system ground
	N13	system ground
	N14	system ground
	P14	system ground
	P15	system ground
	P16	system ground
	N16	system ground
	N15	system ground
	N12	system ground
	M12	system ground
	M13	system ground
	M14	system ground
	L16	system ground
	M16	system ground
	M15	system ground

Table 14: Test

Symbol	Pin	Type	Description
DBG_TDI	A3	I	PR3940 debug port data in
DBG_TDO	B3	O	PR3940 debug port data out
DBG_TCK	C3	I	PR3940 debug port clock
DBG_TMS	C1	I	PR3940 debug port mode select
JTAG_TRST	G2	I	JTAG port reset
JTAG_TDI	J4	I	JTAG data in
JTAG_TDO	H2	O	JTAG data out
JTAG_TCK	G1	I	JTAG data clock
JTAG_TMS	H3	I	JTAG data mode select

Table 15: All pins (in alpha-numeric sequence)

Symbol	Pin	Group	Type	Description
V_{SS}	A1	PWR	-	system ground
	A2	PWR	-	system ground
DBG_TDI	A3	TEST	I	PR3940 debug port data in
I2C1_SDA	A4	I^2C-bus	I/O	serial communications port (I^2C-bus) data

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
USB_DP[1]	A5	USB	I/O	data plus bit 1
PHY_ISO_N	A6	1394	I	signals type of isolation mode used at the PHY-Link interface
				0 = 1394-1995 annex J type isolation; enables differentiator circuitry
				1 = direct connection or single capacitor isolation mode; this will disable the differentiator circuitry
PHY_D[0]	A7	1394	I/O	PHY data bit 0; data is expected on ports 1:0 for 100 MB packets
PHY_D[4]	A8	1394	I/O	PHY data bit 4; data is expected on ports 7:0 for 400 MB packets
MDQM[0]	A9	MMI	O	SDRAM control bit 0
MD[3]	A10	MMI	I/O	memory data bit 3
MD[6]	A11	MMI	I/O	memory data bit 6
MD[9]	A12	MMI	I/O	memory data bit 9
MD[13]	A13	MMI	I/O	memory data bit 13
MD[15]	A14	MMI	I/O	memory data bit 15
MD[20]	A15	MMI	I/O	memory data bit 20
MD[24]	A16	MMI	I/O	memory data bit 24
MDQM[3]	A17	MMI	O	SDRAM control bit 3
MD[31]	A18	MMI	I/O	memory data bit 31
MD[28]	A19	MMI	I/O	memory data bit 28
MA[7]	A20	MMI	O	memory address bit 7
MA[9]	A21	MMI	O	memory address bit 9
MCS	A22	MMI	O	memory chip select
MCAS	A23	MMI	O	memory column address select
MDQM[4]	A24	MMI	O	SDRAM control bit 4
V_{SS}	A25	PWR	-	system ground
	A26	PWR	-	system ground
	B1	PWR	-	system ground
	B2	PWR	-	system ground
DBG_TDO	B3	TEST	O	PR3940 debug port data out
GPIO[2]	B4	GPIO	I/O	general purpose input/output bit 2
PHY_LREQ	B5	1394	O	used by the link to make bus requests and to access PHY registers; this is a serial bus; a train of pulses is sent on this signal
USB_DP[0]	B6	USB	I/O	data plus bit 0
PHY_CTL[1]	B7	1394	I/O	PHY control bit 1; indicates the mode for data on the Din port
PHY_D[3]	B8	1394	I/O	PHY data bit 3; data is expected on ports 3:0 for 200 MB packets
PHY_D[7]	B9	1394	I/O	PHY data bit 7; data is expected on ports 7:0 for 400 MB packets

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
MD[1]	B10	MMI	I/O	memory data bit 1
MD[5]	B11	MMI	I/O	memory data bit 5
MD[8]	B12	MMI	I/O	memory data bit 8
MD[12]	B13	MMI	I/O	memory data bit 12
MDQM[2]	B14	MMI	O	SDRAM control bit 2
MD[19]	B15	MMI	I/O	memory data bit 19
MD[23]	B16	MMI	I/O	memory data bit 23
MD[27]	B17	MMI	I/O	memory data bit 27
MD[30]	B18	MMI	I/O	memory data bit 30
MCLK[0]	B19	MMI	O	memory clock bit 0
MA[1]	B20	MMI	O	memory address bit 1
MA[10]	B21	MMI	O	memory address bit 10
MBA[0]	B22	MMI	O	SDRAM bank select
MRAS	B23	MMI	O	EDODRAM row address strobe
MWE	B24	MMI	O	memory write enable
V_{SS}	B25	PWR	-	system ground
	B26	PWR	-	system ground
DBG_TMS	C1	TEST	I	PR3940 debug port mode select
XTALI	C2	PLL	I	PLL reference crystal input
DBG_TCK	C3	TEST	I	PR3940 debug port clock
GPIO[0]	C4	GPIO	I/O	general purpose input/output bit 0
GPIO[3]	C5	GPIO	I/O	general purpose input/output bit 3
USB_DM[0]	C6	USB	I/O	data minus bit 0
PHY_CTL[0]	C7	1394	I/O	PHY control bit 0; indicates the mode for data on the Din port
PHY_D[1]	C8	1394	I/O	PHY data bit 1; data is expected on ports 1:0 for 100 MB packets
PHY_D[5]	C9	1394	I/O	PHY data bit 5; data is expected on ports 7:0 for 400 MB packets
MD[0]	C10	MMI	I/O	memory data bit 0
MD[2]	C11	MMI	I/O	memory data bit 2
MD[7]	C12	MMI	I/O	memory data bit 7
MD[11]	C13	MMI	I/O	memory data bit 11
MD[16]	C14	MMI	I/O	memory data bit 16
MD[18]	C15	MMI	I/O	memory data bit 18
MD[22]	C16	MMI	I/O	memory data bit 22
MD[26]	C17	MMI	I/O	memory data bit 26
MD[29]	C18	MMI	I/O	memory data bit 29
MA[3]	C19	MMI	O	memory address bit 3
MA[6]	C20	MMI	O	memory address bit 6
MA[8]	C21	MMI	O	memory address bit 8
MA[11]	C22	MMI	O	memory address bit 11

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
MCKE	C23	MMI	O	memory clock enable
V_{SS}	C24	PWR	-	system ground
MD[32]	C25	MMI	I/O	memory data bit 32
MCLK[1]	C26	MMI	O	memory clock bit 1
V_{DDC}	D1	PWR	-	system 1.26 V
V_{SS}	D2	PWR	-	system ground (analog ground 1.728 GHz PLL)
XTALO	D3	PLL	O	PLL reference crystal feedback driver
V_{SS}	D4	PWR	-	system ground
GPIO[1]	D5	GPIO	I/O	general purpose input/output bit 1
I2C1_SCL	D6	I^2C-bus	I/O	serial communications port (I^2C-bus) clock
USB_DM[1]	D7	USB	I/O	data minus bit 1
CLK_L1394	D8	1394	I	system clock; 49.152 MHz input
PHY_D[2]	D9	1394	I/O	PHY data bit 2; data is expected on ports 3:0 for 200 MB packets
PHY_D[6]	D10	1394	I/O	PHY data bit 6; data is expected on ports 7:0 for 400 MB packets
MD[4]	D11	MMI	I/O	memory data bit 4
MDQM[1]	D12	MMI	O	SDRAM control bit 1
MD[10]	D13	MMI	I/O	memory data bit 10
MD[14]	D14	MMI	I/O	memory data bit 14
MD[17]	D15	MMI	I/O	memory data bit 17
MD[21]	D16	MMI	I/O	memory data bit 21
MD[25]	D17	MMI	I/O	memory data bit 25
MA[5]	D18	MMI	O	memory address bit 5
MA[4]	D19	MMI	O	memory address bit 4
MA[2]	D20	MMI	O	memory address bit 2
MA[0]	D21	MMI	O	memory address bit 0
MBA[1]	D22	MMI	O	SDRAM bank select
V_{SS}	D23	PWR	-	system ground
MD[33]	D24	MMI	I/O	memory data bit 33
MD[36]	D25	MMI	I/O	memory data bit 36
MD[35]	D26	MMI	I/O	memory data bit 35
V_{DDC1}	E1	PWR	-	system 1.26 V
	E2	PWR	-	system 1.26 V
V_{DDC2}	E3	PWR	-	system 1.26 V (analog power 1.728 GHz PLL)
	E4	PWR	-	system 1.26 V (analog power 1.728 GHz PLL)
V_{SS}	E5	PWR	-	system ground
	E6	PWR	-	system ground
V_{DD1}	E7	PWR	-	system 3.3 V
	E8	PWR	-	system 3.3 V

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
V_{DDC1}	E9	PWR	-	system 1.26 V
	E10	PWR	-	system 1.26 V
V_{DD1}	E11	PWR	-	system 3.3 V
	E12	PWR	-	system 3.3 V
V_{DDC1}	E13	PWR	-	system 1.26 V
	E14	PWR	-	system 1.26 V
	E15	PWR	-	system 1.26 V
V_{DD1}	E16	PWR	-	system 3.3 V
	E17	PWR	-	system 3.3 V
V_{DDC1}	E18	PWR	-	system 1.26 V
	E19	PWR	-	system 1.26 V
V_{DD1}	E20	PWR	-	system 3.3 V
	E21	PWR	-	system 3.3 V
V_{SS}	E22	PWR	-	system ground
MD[34]	E23	MMI	I/O	memory data bit 34
MD[37]	E24	MMI	I/O	memory data bit 37
MD[38]	E25	MMI	I/O	memory data bit 38
MDQM[5]	E26	MMI	O	SDRAM control bit 5
V_{DDC1}	F1	PWR	-	system 1.26 V
	F2	PWR	-	system 1.26 V
	F3	PWR	-	system 1.26 V
V_{SS}	F4	PWR	-	system ground (analog ground 1.728 GHz PLL)
	F5	PWR	-	system ground
	F22	PWR	-	system ground
MD[39]	F23	MMI	I/O	memory data bit 39
MD[40]	F24	MMI	I/O	memory data bit 40
MD[41]	F25	MMI	I/O	memory data bit 41
MD[42]	F26	MMI	I/O	memory data bit 42
JTAG_TCK	G1	TEST	I	JTAG data clock
JTAG_TRST	G2	TEST	I	JTAG port reset
V_{DDC1}	G3	PWR	-	system 1.26 V
	G4	PWR	-	system 1.26 V
V_{DD2}	G5	PWR	-	system 3.3 V (CAB)
V_{DD1}	G22	PWR	-	system 3.3 V
MD[43]	G23	MMI	I/O	memory data bit 43
MD[44]	G24	MMI	I/O	memory data bit 44
MD[45]	G25	MMI	I/O	memory data bit 45
MD[46]	G26	MMI	I/O	memory data bit 46
I2C2_SCL	H1	I^2C-bus	I/O	serial communications port (I^2C-bus) clock
JTAG_TDO	H2	TEST	O	JTAG data OUT
JTAG_TMS	H3	TEST	I	JTAG data mode select

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
V_{DDC1}	H4	PWR	-	system 1.26 V
V_{DD2}	H5	PWR	-	system 3.3 V (CAB)
V_{DD1}	H22	PWR	-	system 3.3 V
MD[47]	H23	MMI	I/O	memory data bit 47
MDQM[6]	H24	MMI	O	SDRAM control bit 6
MD[48]	H25	MMI	I/O	memory data bit 48
MD[49]	H26	MMI	I/O	memory data bit 49
I2S_OUT1_SCK	J1	AVIF	I/O	audio OUT1 serial clock
I2S_OUT1_SD	J2	AVIF	O	audio OUT1 data
I2S_OUT1_WS	J3	AVIF	I/O	audio OUT1 word select
JTAG_TDI	J4	TEST	I	JTAG data IN
V_{DDC1}	J5	PWR	-	system 1.26 V
	J22	PWR	-	system 1.26 V
MD[50]	J23	MMI	I/O	memory data bit 50
MD[51]	J24	MMI	I/O	memory data bit 51
MD[52]	J25	MMI	I/O	memory data bit 52
MD[53]	J26	MMI	I/O	memory data bit 53
I2S_OUT2_WS	K1	AVIF	I/O	audio OUT2 word select
I2S_OUT2_OSCLK	K2	AVIF	O	audio OUT2 oversample clock
I2S_OUT1_OSCLK	K3	AVIF	O	audio OUT1 oversample clock
I2C2_SDA	K4	I^2C-bus	I/O	serial communications port (I^2C-bus) data
V_{DDC1}	K5	PWR	-	system 1.26 V
	K22	PWR	-	system 1.26 V
MD[54]	K23	MMI	I/O	memory data bit 54
MD[55]	K24	MMI	I/O	memory data bit 55
MDQM[7]	K25	MMI	O	SDRAM control bit 7
MD[56]	K26	MMI	I/O	memory data bit 56
HSYNC	L1	AVIF	O	horizontal sync for primary display
VSYNC	L2	AVIF	I/O	vertical sync for primary display
I2S_OUT2_SCK	L3	AVIF	I/O	audio OUT2 serial clock
I2S_OUT2_SD	L4	AVIF	O	audio OUT2 Data
V_{DD1}	L5	PWR	-	system 3.3 V
V_{SS}	L11	PWR	-	system ground
	L12	PWR	-	system ground
	L13	PWR	-	system ground
	L14	PWR	-	system ground
	L15	PWR	-	system ground
	L16	PWR	-	system ground
V_{DD1}	L22	PWR	-	system 3.3 V
MD[57]	L23	MMI	I/O	memory data bit 57
MD[58]	L24	MMI	I/O	memory data bit 58

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
MD[59]	L25	MMI	I/O	memory data bit 59
MD[60]	L26	MMI	I/O	memory data bit 60
DV_OUT1[8]	M1	AVIF	O	digital video output1; bit 8 for primary display channel from AICP
DV_OUT1[9]	M2	AVIF	O	digital video output1; bit 9 for primary display channel from AICP
DV_CLK1	M3	AVIF	O	digital video clock1 for primary display channel from AICP
BLANK	M4	AVIF	O	blanking for primary display
V_{DD1}	M5	PWR	-	system 3.3 V
V_{SS}	M11	PWR	-	system ground
	M12	PWR	-	system ground
	M13	PWR	-	system ground
	M14	PWR	-	system ground
	M15	PWR	-	system ground
	M16	PWR	-	system ground
V_{DD1}	M22	PWR	-	system 3.3 V
MD[61]	M23	MMI	I/O	memory data bit 61
MD[62]	M24	MMI	I/O	memory data bit 62
MD[63]	M25	MMI	I/O	memory data bit 63
GPIO[8]	M26	GPIO	I/O	general purpose input/output Bit 8
DV_OUT1[5]	N1	AVIF	O	digital video output1; bit 5 for primary display channel from AICP
DV_OUT1[4]	N2	AVIF	O	digital video output1; bit 4 for primary display channel from AICP
DV_OUT1[6]	N3	AVIF	O	digital video output1; bit 6 for primary display channel from AICP
DV_OUT1[7]	N4	AVIF	O	digital video output1; bit 7 for primary display channel from AICP
V_{DDC1}	N5	PWR	-	system 1.26 V
V_{SS}	N11	PWR	-	system ground
	N12	PWR	-	system ground
	N13	PWR	-	system ground
	N14	PWR	-	system ground
	N15	PWR	-	system ground
	N16	PWR	-	system ground
V_{DDC1}	N22	PWR	-	system 1.26 V
GPIO[9]	N23	GPIO	I/O	general purpose input/output bit 9
GPIO[10]	N24	GPIO	I/O	general purpose input/output bit 10
SC2_SCCK	N25	COM	O	smart card2 bit clock
GPIO[11]	N26	GPIO	I/O	general purpose input/output bit 11
DV_OUT1[2]	P1	AVIF	O	digital video output1; bit 2 for primary display channel from AICP

Table 15: All pins (in alpha-numeric sequence) *...continued*

Symbol	Pin	Group	Type	Description
DV_OUT1[3]	P2	AVIF	O	digital video output1; bit 3 for primary display channel from AICP
DV_OUT1[0]	P3	AVIF	O	digital video output1; bit 0 for primary display channel from AICP
DV_OUT1[1]	P4	AVIF	O	digital video output1; bit 1 for primary display channel from AICP
V_{DDC1}	P5	PWR	-	system 1.26 V
V_{SS}	P11	PWR	-	system ground
	P12	PWR	-	system ground
	P13	PWR	-	system ground
	P14	PWR	-	system ground
	P15	PWR	-	system ground
	P16	PWR	-	system ground
V_{DDC1}	P22	PWR	-	system 1.26 V
SC2_DA	P23	COM	I/O	smart card2 data
SC2_CMD	P24	COM	O	smart card2 command
SC2_OFFN	P25	COM	I	smart card2 off
SC2_RST	P26	COM	O	smart card2 reset
DV_CLK2	R1	AVIF	O	digital video clock2 for secondary display channel from AICP
DV_OUT2[9]	R2	AVIF	O	digital video output2; bit 9 for secondary display channel from AICP
DV_OUT2[7]	R3	AVIF	O	digital video output2; bit 7 for secondary display channel from AICP
DV_OUT2[8]	R4	AVIF	O	digital video output2; bit 8 for secondary display channel from AICP
V_{DD1}	R5	PWR	-	system 3.3 V
V_{SS}	R11	PWR	-	system ground
	R12	PWR	-	system ground
	R13	PWR	-	system ground
	R14	PWR	-	system ground
	R15	PWR	-	system ground
	R16	PWR	-	system ground
V_{DD1}	R22	PWR	-	system 3.3 V
SC1_CMD	R23	COM	O	smart card1 command
SC1_RST	R24	COM	O	smart card1 reset
SC1_OFFN	R25	COM	I	smart card1 off
SC1_SCCK	R26	COM	O	smart card1 bit clock
DV_OUT2[6]	T1	AVIF	O	digital video output2; bit 6 for secondary display channel from AICP
DV_OUT2[5]	T2	AVIF	O	digital video output2; bit 5 for secondary display channel from AICP

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
DV_OUT2[4]	T3	AVIF	O	digital video output2; bit 4 for secondary display channel from AICP
DV_OUT2[2]	T4	AVIF	O	digital video output2; bit 2 for secondary display channel from AICP
V_{DD1}	T5	PWR	-	system 3.3 V
V_{SS}	T11	PWR	-	system ground
	T12	PWR	-	system ground
	T13	PWR	-	system ground
	T14	PWR	-	system ground
	T15	PWR	-	system ground
	T16	PWR	-	system ground
V_{DD1}	T22	PWR	-	system 3.3 V
UA2_TX	T23	COM	I/O	UART2 transmit
UA2_RTSN	T24	COM	I/O	UART2 request to send
UA2_CTSN	T25	COM	I/O	UART2 clear to send
SC1_DA	T26	COM	I/O	smart card1 data
DV_OUT2[3]	U1	AVIF	O	digital video output2; bit 3 for secondary display channel from AICP
DV_OUT2[1]	U2	AVIF	O	digital video output2; bit 1 for secondary display channel from AICP
DV_OUT2[0]	U3	AVIF	O	digital video output2; bit 0 for secondary display channel from AICP
SSI_RXD	U4	COM	I/O	synchronous serial interface receive
V_{DDC1}	U5	PWR	-	system 1.26 V
	U22	PWR	-	system 1.26 V
DV3_ERR	U23	DVB	I	digital video transport stream3 error
UA1_TX	U24	COM	I/O	UART1 transmit
UA1_RX	U25	COM	I/O	UART1 receive
UA2_RX	U26	COM	I/O	UART2 receive
SSI_SCLK_CTSN	V1	COM	I/O	synchronous serial interface clock
SSI_FS_RTSN	V2	COM	I/O	synchronous serial interface frame sync
SSI_TXD	V3	COM	I/O	synchronous serial interface transmit
PCI_INTA	V4	PCI	I/O	interrupt acknowledge is asserted to request an interrupt
V_{DDC1}	V5	PWR	-	system 1.26 V
	V22	PWR	-	system 1.26 V
DV3_DATA[2]	V23	DVB	I	digital video transport stream3 data bit 2
DV3_SOP	V24	DVB	I	digital video transport stream3 start of packet
DV3_VALID	V25	DVB	I	digital video transport stream3 data valid
DV3_CLK	V26	DVB	I	digital video transport stream3 clock

Table 15: All pins (in alpha-numeric sequence) *...continued*

Symbol	Pin	Group	Type	Description
USB_PWR	W1	USB	O	USB port power on/off
				0 = power on
				1 = power off
USB_OVRCUR	W2	USB	I	indicates over current being drawn by a USB device
				0 = over current detected
				1 = no over current
RESET_IN	W3	PCI	I	PCI bus global reset
PLL_OUT	W4	PLL	O	general purpose PLL clock output
V_{DD1}	W5	PWR	-	system 3.3 V
	W22	PWR	-	system 3.3 V
DV3_DATA[7]	W23	DVB	I	digital video transport stream3 data bit 7
DV3_DATA[3]	W24	DVB	I	digital video transport stream3 data bit 3
DV3_DATA[1]	W25	DVB	I	digital video transport stream3 data bit 1
DV3_DATA[0]	W26	DVB	I	digital video transport stream3 data bit 0
SYS_RSTN_OUT	Y1	MISC	O	system reset output
PCI_REQ	Y2	PCI	I/O	arbitration request on PCI bus; request is an output when using an external arbiter and an input when using an internal arbiter
PCI_GNT	Y3	PCI	I/O	arbitration grant is asserted to indicate access to the bus has been granted; this pin is an input when an external arbiter is used and an output when using the internal arbiter
PCI_GNT_A	Y4	PCI	I/O	auxiliary arbitration grant GNT_A is asserted to indicate bus access has been granted to an external PCI master; used where internal arbiter is configured
V_{DD1}	Y5	PWR	-	system 3.3 V
	Y22	PWR	-	system 3.3 V
TS_DATA[0]	Y23	DVB	I/O	transport stream data bit 0
DV3_DATA[6]	Y24	DVB	I	digital video transport stream3 data bit 6
DV3_DATA[5]	Y25	DVB	I	digital video transport stream3 data bit 5
DV3_DATA[4]	Y26	DVB	I	digital video transport stream3 data bit 4
CLK	AA1	PCI	I	PCI bus clock
PCI_REQ_A	AA2	PCI	I/O	auxiliary arbitration PCI_REQ_A on PCI Bus; used in modes where internal arbiter is configured
PCI_REQ_B	AA3	PCI	I/O	auxiliary arbitration PCI_REQ_B on PCI Bus; used in modes where internal arbiter is configured
PCI_GNT_B	AA4	PCI	I/O	auxiliary arbitration grant GNT_B is asserted to indicate bus access has been granted to an external PCI master; used where internal arbiter is configured

Table 15: All pins (in alpha-numeric sequence) *…continued*

Symbol	Pin	Group	Type	Description
V_{SS}	AA5	PWR	-	system ground
	AA22	PWR	-	system ground
TS_DATA[4]	AA23	DVB	I/O	transport stream data bit 4
TS_SOP	AA24	DVB	I/O	transport stream start of packet (parallel/serial)
TS_VALID	AA25	DVB	I/O	transport stream data valid (parallel/serial)
TS_CLK	AA26	DVB	I/O	transport stream clock (parallel/serial)
PCI_AD[31]	AB1	PCI	I/O	multiplexed address or data bit 31
PCI_AD[30]	AB2	PCI	I/O	multiplexed address or data bit 30
PCI_AD[29]	AB3	PCI	I/O	multiplexed address or data bit 29
PCI_AD[28]	AB4	PCI	I/O	multiplexed address or data bit 28
V_{SS}	AB5	PWR	-	system ground
V_{DD1}	AB6	PWR	-	system 3.3 V
	AB7	PWR	-	system 3.3 V
V_{DDC1}	AB8	PWR	-	system 1.26 V
	AB9	PWR	-	system 1.26 V
V_{DD1}	AB10	PWR	-	system 3.3 V
	AB11	PWR	-	system 3.3 V
V_{DDC1}	AB12	PWR	-	system 1.26 V
	AB13	PWR	-	system 1.26 V
	AB14	PWR	-	system 1.26 V
V_{DD1}	AB15	PWR	-	system 3.3 V (TM-PLL)
V_{DD3}	AB16	PWR	-	system 3.3 V
V_{DDC1}	AB17	PWR	-	system 1.26 V
	AB18	PWR	-	system 1.26 V
V_{DD1}	AB19	PWR	-	system 3.3 V
	AB20	PWR	-	system 3.3 V
V_{SS}	AB21	PWR	-	system ground
	AB22	PWR	-	system ground
TS_DATA[7]	AB23	DVB	I/O	transport stream data bit 7
TS_DATA[5]	AB24	DVB	I/O	transport stream data bit 5
TS_DATA[2]	AB25	DVB	I/O	transport stream data bit 2
TS_DATA[1]	AB26	DVB	I/O	transport stream data bit 1
PCI_AD[27]	AC1	PCI	I/O	multiplexed address or data bit 27
PCI_AD[26]	AC2	PCI	I/O	multiplexed address or data bit 26
PCI_AD[25]	AC3	PCI	I/O	multiplexed address or data bit 25
V_{SS}	AC4	PWR	-	system ground
PCI_AD[17]	AC5	PCI	I/O	multiplexed address or data bit 17
PCI_AD[16]	AC6	PCI	I/O	multiplexed address or data bit 16
PCI_SERR	AC7	PCI	I/O	system error
PCI_AD[14]	AC8	PCI	I/O	multiplexed address or data bit 14
PCI_AD[10]	AC9	PCI	I/O	multiplexed address or data bit 10

Table 15: All pins (in alpha-numeric sequence) *...continued*

Symbol	Pin	Group	Type	Description
PCI_AD[7]	AC10	PCI	I/O	multiplexed address or data bit 7
PCI_AD[3]	AC11	PCI	I/O	multiplexed address or data bit 3
PCI_AD[0]	AC12	PCI	I/O	multiplexed address or data bit 0
XIO_SEL[1]	AC13	MISC	I/O	external input/output select1
GPIO[4]	AC14	GPIO	I/O	general purpose input/output bit 4
I2S_IO_WS	AC15	AVIF	I/O	audio input/output word select
SPDIF_OUT	AC16	AVIF	O	multi-channel/SPDIF Output
DV1_DATA[6]	AC17	DVB	I/O	ITU-656 VIP data bit 6
DV1_DATA[1]	AC18	DVB	I/O	ITU-656 VIP data bit 1
I2S_IN1_SCK	AC19	AVIF	I/O	audio IN1 serial clock
I2S_IN2_SCK	AC20	AVIF	I/O	audio IN2 serial clock
DV2_DATA[6]	AC21	DVB	I	digital video transport stream2 data bit 6
DV2_DATA[3]	AC22	DVB	I	digital video transport stream2 data bit 3
V_{SS}	AC23	PWR	-	system ground
DV2_CLK	AC24	DVB	I	digital video transport stream2 clock
TS_DATA[6]	AC25	DVB	I/O	transport stream data bit 6
TS_DATA[3]	AC26	DVB	I/O	transport stream data bit 3
PCI_CBE[3]	AD1	PCI	I/O	multiplexed command or byte enable 3
PCI_AD[24]	AD2	PCI	I/O	multiplexed address or data bit 24
V_{SS}	AD3	PWR	-	system ground
PCI_AD[20]	AD4	PCI	I/O	multiplexed address or data bit 20
PCI_AD[18]	AD5	PCI	I/O	multiplexed address or data bit 18
PCI_TRDY	AD6	PCI	I/O	parity error indicates data parity errors during all PCI transactions except special cycle
PCI_PERR	AD7	PCI	I/O	parity error indicates data parity errors during all PCI transactions except special cycle
PCI_AD[15]	AD8	PCI	I/O	multiplexed address or data bit 15
PCI_AD[11]	AD9	PCI	I/O	multiplexed address or data bit 11
PCI_CBE[0]	AD10	PCI	I/O	multiplexed command or byte enable 0
PCI_AD[4]	AD11	PCI	I/O	multiplexed address or data bit 4
PCI_AD[1]	AD12	PCI	I/O	multiplexed address or data bit 1
XIO_SEL[0]	AD13	MISC	I/O	external input/output select0
GPIO[5]	AD14	GPIO	I/O	general purpose input/output bit 5
I2S_IO_SD[3]	AD15	AVIF	I/O	audio input/output data bit 3
I2S_IO_SD[0]	AD16	AVIF	I/O	audio input/output data bit 0
DV1_DATA[8]	AD17	DVB	I/O	ITU-656 VIP data bit 8
DV1_DATA[4]	AD18	DVB	I/O	ITU-656 VIP data bit 4
DV1_DATA[0]	AD19	DVB	I/O	ITU-656 VIP data bit 0 (least significant bit)
I2S_IN1_OSCLK	AD20	AVIF	O	audio IN1 oversample clock
I2S_IN2_OSCLK	AD21	AVIF	O	audio IN2 oversample clock
DV2_DATA[5]	AD22	DVB	I	digital video transport stream2 data bit 5

Table 15: All pins (in alpha-numeric sequence) *...continued*

Symbol	Pin	Group	Type	Description
DV2_DATA[2]	AD23	DVB	I	digital video transport stream2 data bit 2
DV2_SOP	AD24	DVB	I	digital video transport stream2 start of packet
DV2_VALID	AD25	DVB	I	digital video transport stream2 data valid
DV2_ERR	AD26	DVB	I	digital video transport stream2 error
V_{SS}	AE1	PWR	-	system ground
	AE2	PWR	-	system ground
PCI_AD[23]	AE3	PCI	I/O	multiplexed address or data bit 23
PCI_AD[21]	AE4	PCI	I/O	multiplexed address or data bit 21
PCI_AD[19]	AE5	PCI	I/O	multiplexed address or data bit 19
PCI_IRDY	AE6	PCI	I/O	initiator ready is asserted during writes to indicate valid data on PCI_AD[31:0]; also asserted during reads to indicate the target is prepared to accept data; wait states are inserted until PCI_IRDY and PCI_TRDY are both asserted
PCI_STOP	AE7	PCI	I/O	stop is asserted to indicate a request from the target for the master to stop the current transmission
PCI_CBE[1]	AE8	PCI	I/O	multiplexed command or byte enable 1
PCI_AD[12]	AE9	PCI	I/O	multiplexed address or data bit 12
PCI_AD[8]	AE10	PCI	I/O	multiplexed address or data bit 8
PCI_AD[5]	AE11	PCI	I/O	multiplexed address or data bit 5
PCI_AD[2]	AE12	PCI	I/O	multiplexed address or data bit 2
XIO_A25	AE13	MISC	I/O	XIO address bit 25
GPIO[7]	AE14	GPIO	I/O	general purpose input/output bit 7
I2S_IO_SCK	AE15	AVIF	I/O	audio input/output serial clock
I2S_IO_SD[1]	AE16	AVIF	I/O	audio input/output data bit 1
DV1_DATA[9]	AE17	DVB	I/O	ITU-656 VIP data bit 9 (most significant bit)
DV1_DATA[5]	AE18	DVB	I/O	ITU-656 VIP data bit 5
DV1_DATA[2]	AE19	DVB	I/O	ITU-656 VIP data bit 2
DV1_CLK	AE20	DVB	I/O	ITU-656 VIP data clock
I2S_IN1_SD	AE21	AVIF	I	audio IN1 data
I2S_IN2_SD	AE22	AVIF	I	audio IN2 data
DV2_DATA[4]	AE23	DVB	I	digital video transport stream2 data bit 4
DV2_DATA[1]	AE24	DVB	I	digital video transport stream2 data bit 1
V_{SS}	AE25	PWR	-	system ground
	AE26	PWR	-	system ground
	AF1	PWR	-	system ground
	AF2	PWR	-	system ground
IDSEL	AF3	PCI	I/O	initialization device select provides chip select during configuration read and write transactions
PCI_AD[22]	AF4	PCI	I/O	multiplexed address or data bit 22
PCI_CBE[2]	AF5	PCI	I/O	multiplexed command or byte enable 2

Table 15: All pins (in alpha-numeric sequence) *...continued*

Symbol	Pin	Group	Type	Description
PCI_FRAME	AF6	PCI	I/O	frame is asserted to indicate start of bus transaction and remains asserted until final data phase begins
PCI_DEVSEL	AF7	PCI	I/O	device select is asserted when a target address is decoded and remains asserted to indicate that a target device is selected
PCI_PAR	AF8	PCI	I/O	parity supports even parity across the PCI address/data bus AD[31:0]) and command/ byte enable bus (PCI_CBE[3:0]); bus master drives PCI_PAR for address and write data phases; target drives PCI_PAR for the read data phases
PCI_AD[13]	AF9	PCI	I/O	multiplexed address or data bit 13
PCI_AD[9]	AF10	PCI	I/O	multiplexed address or data bit 9
PCI_AD[6]	AF11	PCI	I/O	multiplexed address or data bit 6
XIO_SEL[2]	AF12	MISC	I/O	external input/output select2
XIO_ACK	AF13	MISC	I/O	XIO acknowledge (EEPROM)
GPIO[6]	AF14	GPIO	I/O	general purpose input/output bit 6
I2S_IO_OSCLK	AF15	AVIF	I/O	audio input/output oversample clock
I2S_IO_SD[2]	AF16	AVIF	I/O	audio input/output data bit 2
SPDIF_IN	AF17	AVIF	I	multi-channel/SPDIF input
DV1_DATA[7]	AF18	DVB	I/O	ITU-656 VIP data bit 7
DV1_DATA[3]	AF19	DVB	I/O	ITU-656 VIP data bit 3
DV1_VALID	AF20	DVB	I/O	ITU-656 VIP data valid
I2S_IN1_WS	AF21	AVIF	I/O	audio in1 word select
I2S_IN2_WS	AF22	AVIF	I/O	audio in2 word select
DV2_DATA[7]	AF23	DVB	I	digital video transport stream2 data bit 7
DV2_DATA[0]	AF24	DVB	I	digital video transport stream2 data bit 0
V_{SS}	AF25	PWR	-	system ground
	AF26	PWR	-	system ground

6.2.1 Multi-function pins

Table 16 identifies and describes alternate signals that are available in the PNX8526. In Section 6.2 alternate signals are also identified by a hash (#) within each functional group of signals.

Remark: The PNX8526 has a number of General Purpose Input Output (GPIO) pins. Some of these are dedicated pins, while others are configured as alternate signals on multifunction pins. The standard function of these pins may not be required in some system configurations.

For more details on GPIO functionality, see *"PNX8526 User Manual, Chapter 10"*.

Table 16: Multiplexed (MUX) pins

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
AF15	I2S_IO_OSCLK	I/O	audio input/output oversample clock
	GPIO[45]	I/O	general purpose input/output 45
AE15	I2S_IO_SCK	I/O	audio input/output serial clock
	GPIO[46]	I/O	general purpose input/output 46
AC15	I2S_IO_WS	I/O	audio input/output word select
	GPIO[47]	I/O	general purpose input/output 47
AD15	I2S_IO_SD[3]	I/O	audio input/output data bit 3
	GPIO[51]	I/O	general purpose input/output 51
AF16	I2S_IO_SD[2]	I/O	audio input/output data bit 2
	GPIO[50]	I/O	general purpose input/output 50
AE16	I2S_IO_SD[1]	I/O	audio input/output data bit 1
	GPIO[49]	I/O	general purpose input/output 49
AD16	I2S_IO_SD[0]	I/O	audio input/output data bit 0
	GPIO[48]	I/O	general purpose input/output 48
R2	DV_OUT2[9]	O	digital video output2, Bit 9 for secondary display channel from AICP
	SPY_OUT[9]	O	SPY micro-architecture output signal, Bit 9
R4	DV_OUT2[8]	O	digital video output2, bit 8 for secondary display channel from AICP
	SPY_OUT[8]	O	SPY micro-architecture output signal, bit 8
	DSU_TPC1	O	debug support unit1, tpc1
R3	DV_OUT2[7]	O	digital video output2, bit 7 for secondary display channel from AICP
	SPY_OUT[7]	O	SPY micro-architecture output signal, bit 7
	DSU_TPC0	O	debug support unit0, TPC0
T1	DV_OUT2[6]	O	digital video output2, bit 6 for secondary display channel from AICP
	SPY_OUT[6]	O	SPY micro-architecture output signal, bit 6
	DSU_PCST1[2]	O	program counter status1, bit 2
T2	DV_OUT2[5]	O	digital video output2, bit 5 for secondary display channel from AICP
	SPY_OUT[5]	O	SPY micro-architecture output signal, bit 5
	DSU_PCST1[1]	O	program counter status1, bit 1
T3	DV_OUT2[4]	O	digital video output2, bit 4 for secondary display channel from AICP
	SPY_OUT[4]	O	SPY micro-architecture output signal, bit 4
	DSU_PCST1[0]	O	program counter status1, bit 0
U1	DV_OUT2[3]	O	digital video output2, bit 3 for secondary display channel from AICP
	SPY_OUT[3]	O	SPY micro-architecture output signal, bit 3
	DSU_PCST0[2]	O	program counter status0, bit 2

Table 16: Multiplexed (MUX) pins *...continued*

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
T4	DV_OUT2[2]	O	digital video output2, bit 2 for secondary display channel from AICP
	SPY_OUT[2]	O	SPY micro-architecture output signal, bit 2
	DSU_PCST0[1]	O	program counter status0, bit 1
U2	DV_OUT2[1]	O	digital video output2, bit 1 for secondary display channel from AICP
	SPY_OUT[1]	O	SPY micro-architecture output signal, bit 1
	DSU_PCST0[0]	O	program counter status0, bit 0
U3	DV_OUT2[0]	O	digital video output2, bit 0 for secondary display channel from AICP
	SPY_OUT[0]	O	SPY micro-architecture output signal, bit 0
	DSU_CLK	O	debug support unit clock
K2	I2S_OUT2_OSCLK	O	audio out2 oversample clock
	DV_OUT[20]	O	AICP RGB data bit 20
	SPY_OUT[11]	O	SPY micro-architecture output signal, bit 11
L3	I2S_OUT2_SCK	I/O	audio OUT2 serial clock
	DV_OUT[21]	O	AICP RGB data bit 21
	SPY_OUT[10]	O	SPY micro-architecture output signal, bit 10
K1	I2S_OUT2_WS	I/O	audio OUT2 Word Select
	DV_OUT[22]	O	AICP RGB data bit 22
	DBG_EXT_STOP	I	external stop request signal
L4	I2S_OUT2_SD	O	audio OUT2 data
	DV_OUT[23]	O	AICP RGB data bit 23 (most significant bit)
	CLK_SPY	O	SPY micro-architecture clock output signal
AE17	DV1_DATA[9]	I	ITU-656 VIP data bit 9 (most significant bit)
	GPIO[42]	I/O	general purpose input/output 42
AD17	DV1_DATA[8]	I	ITU-656 VIP data bit 8
	GPIO[41]	I/O	general purpose input/output 41
AF18	DV1_DATA[7]	I	ITU-656 VIP data bit 7
	GPIO[40]	I/O	general purpose input/output 40
AC17	DV1_DATA[6]	I	ITU-656 VIP data bit 6
	GPIO[39]	I/O	general purpose input/output 39
AE18	DV1_DATA[5]	I	ITU-656 VIP data bit 5
	GPIO[38]	I/O	general purpose input/output 38
AD18	DV1_DATA[4]	I	ITU-656 VIP data bit 4
	GPIO[37]	I/O	general purpose input/output 37
AF19	DV1_DATA[3]	I	ITU-656 VIP data bit 3
	GPIO[36]	I/O	general purpose input/output 36
AE19	DV1_DATA[2]	I	ITU-656 VIP data bit 2
	GPIO[35]	I/O	general purpose input/output 35

Table 16: Multiplexed (MUX) pins *...continued*

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
AC18	DV1_DATA[1]	I	ITU-656 VIP data bit 1
	GPIO[34]	I/O	general purpose input/output 34
AD19	DV1_DATA[0]	I	ITU-656 VIP data bit 0 (least significant bit)
	GPIO[33]	I/O	general purpose input/output 33
AF20	DV1_VALID	I	ITU-656 VIP data valid
	GPIO[44]	I/O	general purpose input/output 44
AE20	DV1_CLK	I	ITU-656 VIP data clock
	GPIO[43]	I/O	general purpose input/output 43
AF23	DV2_DATA[7]	I	digital video transport stream2 data bit 7
	VIP[9]	I	ITU-656 VIP data bit 9 (most significant bit)
AC21	DV2_DATA[6]	I	digital video transport stream2 data bit 6
	VIP[8]	I	ITU-656 VIP data bit 8
	TSS_DATA2	I	digital video transport stream2 serial data2
AD22	DV2_DATA[5]	I	digital video transport stream2 data bit 5
	VIP[7]	I	ITU-656 VIP data bit 7
	TSS_SOP2	I	digital video transport stream2 serial start of packet2
AE23	DV2_DATA[4]	I	digital video transport stream2 data bit 4
	VIP[6]	I	ITU-656 VIP data bit 6
	TSS_ERR2	I	digital video transport stream2 serial error2
AC22	DV2_DATA[3]	I	digital video transport stream2 data bit 3
	VIP[5]	I	ITU-656 VIP data bit 5
	TSS_VALID2	I	digital video transport stream2 serial valid2
AD23	DV2_DATA[2]	I	digital video transport stream2 data bit 2
	VIP[4]	I	ITU-656 VIP data bit 4
	TSS_CLK2	I	digital video transport stream2 serial clock2
AE24	DV2_DATA[1]	I	digital video transport stream2 data bit 1
	VIP[3]	I	ITU-656 VIP data bit 3
AF24	DV2_DATA[0]	I	digital video transport stream2 data bit 0
	VIP[2]	I	ITU-656 VIP data bit 2
	TSS_DATA1	I	digital video transport stream2 serial data1
AD24	DV2_SOP	I	digital video transport stream2 start of packet
	VIP[1]	I	ITU-656 VIP data bit 1
	TSS_SOP1	I	digital video transport stream2 serial start of packet1
AD26	DV2_ERR	I	digital video transport stream2 error
	VIP[0]	I	ITU-656 VIP data bit 0 (least significant bit)
	TSS_ERR1	I	digital video transport stream2 serial error1
AD25	DV2_VALID	I	digital video transport stream2 data valid
	VIP_VALID	I	ITU-656 VIP data valid
	TSS_VALID1	I	digital video transport stream2 serial valid1

Table 16: Multiplexed (MUX) pins *...continued*

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
AC24	DV2_CLK	I	digital video transport stream2 clock
	VIP_CLK	I	ITU-656 VIP data clock
	TSS_CLK1	I	digital video transport stream2 serial clock1
W23	DV3_DATA[7]	I	digital video transport stream3 data bit 7
	VIP[9]	I	ITU-656 VIP data bit 9 (most significant bit)
Y24	DV3_DATA[6]	I	digital video transport stream3 data bit 6
	VIP[8]	I	ITU-656 VIP data bit 8
	TSS_DATA2	I	digital video transport stream3 serial data2
Y25	DV3_DATA[5]	I	digital video transport stream3 data bit 5
	VIP[7]	I	ITU-656 VIP data bit 7
	TSS_SOP2	I	digital video transport stream3 serial start of packet2
Y26	DV3_DATA[4]	I	digital video transport stream3 data bit 4
	VIP[6]	I	ITU-656 VIP data bit 6
	TSS_ERR2	I	digital video transport stream3 serial error2
W24	DV3_DATA[3]	I	digital video transport stream3 data bit 3
	VIP[5]	I	ITU-656 VIP data bit 5
	TSS_VALID2	I	digital video transport stream3 serial valid2
V23	DV3_DATA[2]	I	digital video transport stream3 data bit 2
	VIP[4]	I	ITU-656 VIP data bit 4
	TSS_CLK2	I	digital video transport stream3 serial clock2
W25	DV3_DATA[1]	I	digital video transport stream3 data bit 1
	VIP[3]	I	ITU-656 VIP data bit 3
W26	DV3_DATA[0]	I	digital video transport stream3 data bit 0
	VIP[2]	I	ITU-656 VIP data bit 2
	TSS_DATA1	I	digital video transport stream3 serial data1
V24	DV3_SOP	I	digital video transport stream3 start of packet
	VIP[1]	I	ITU-656 VIP data bit 1
	TSS_SOP1	I	digital video transport stream3 serial start of packet1
U23	DV3_ERR	I	digital video transport stream3 error
	VIP[0]	I	ITU-656 VIP data bit 0 (least significant bit)
	TSS_ERR1	I	digital video transport stream3 serial error1
V25	DV3_VALID	I	digital video transport stream3 data valid
	VIP_VALID	I	ITU-656 VIP data valid
	TSS_VALID1	I	digital video transport stream3 serial valid1
V26	DV3_CLK	I	digital video transport stream3 clock
	VIP_CLK	I	ITU-656 VIP data clock
	TSS_CLK1	I	digital video transport stream3 serial clock1
AB23	TS_DATA[7]	O	transport stream data bit 7
	GPIO[29]	I/O	general purpose input/output 29

Table 16: Multiplexed (MUX) pins *...continued*

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
AC25	TS_DATA[6]	O	transport stream data bit 6
	GPIO[28]	I/O	general purpose input/output 28
AB24	TS_DATA[5]	O	transport stream data bit 5
	GPIO[27]	I/O	general purpose input/output 27
AA23	TS_DATA[4]	O	transport stream data bit 4
	GPIO[26]	I/O	general purpose input/output 26
AC26	TS_DATA[3]	O	transport stream data bit 3
	GPIO[25]	I/O	general purpose input/output 25
AB25	TS_DATA[2]	O	transport stream data bit 2
	GPIO[24]	I/O	general purpose input/output 24
AB26	TS_DATA[1]	O	transport stream data bit 1
	GPIO[23]	I/O	general purpose input/output 23
Y23	TS_DATA[0]	O	transport stream data bit 0
	GPIO[22]	I/O	general purpose input/output 22
	TS_SD	O	transport stream serial data output
AA24	TS_SOP	O	transport stream start of packet (parallel/serial)
	GPIO[31]	I/O	general purpose input/output 31
AA25	TS_VALID	O	transport stream data valid (parallel/serial)
	GPIO[32]	I/O	general purpose input/output 32
AA26	TS_CLK	O	transport stream clock (parallel/serial)
	GPIO[30]	I/O	general purpose input/output 30
AA2	PCI_REQ_A [2]	I/O	auxiliary arbitration PCI_REQ_A on PCI bus; used in modes where internal arbiter is configured
	GPIO[57]	I/O	general purpose input/output 57
AA3	PCI_REQ_B [2]	I/O	auxiliary arbitration PCI_REQ_B on PCI bus; used in modes where internal arbiter is configured
	GPIO[58]	I/O	general purpose input/output 58
Y4	PCI_GNT_A [2]	I/O	auxiliary arbitration grant GNT_A is asserted to indicate bus access has been granted to an external PCI master; used where internal arbiter is configured
	GPIO[59]	I/O	general purpose input/output 59
AA4	PCI_GNT_B [2]	I/O	auxiliary arbitration grant GNT_B is asserted to indicate bus access has been granted to an external PCI master; used where internal arbiter is configured
	GPIO[60]	I/O	general purpose input/output 60
AF12	XIO_SEL[2] [2]	O	external MMIO select 2
	GPIO[54]	I/O	general purpose input/output 54
AC13	XIO_SEL[1] [2]	O	external MMIO select 1
	GPIO[53]	I/O	general purpose input/output 53
AD13	XIO_SEL[0] [2]	O	external MMIO select 0
	GPIO[52]	I/O	general purpose input/output 52

Table 16: Multiplexed (MUX) pins *...continued*

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
AF13	XIO_ACK [2]	I	XIO acknowledge (EEPROM)
	GPIO[55]	I/O	general purpose input/output 55
AE13	XIO_A25 [2]	O	XIO address bit 25
	GPIO[56]	I/O	general purpose input/output 56
U24	UA1_TX	O	UART1 transmit
	GPIO[12]	I/O	general purpose input/output 12
U25	UA1_RX	I	UART1 receive
	GPIO[13]	I/O	general purpose input/output 13
T23	UA2_TX	O	UART2 transmit
	GPIO[14]	I/O	general purpose input/output 14
U26	UA2_RX	I	UART2 receive
	ICAM1_SETVPP	O	ICAM1 VPP [3]
	GPIO[15]	I/O	general purpose input/output 15
T24	UA2_RTSN	O	UART2 request to send
	ICAM1_C8	I	ICAM1 C8 [3]
	GPIO[16]	I/O	general purpose input/output 16
T25	UA2_CTSN	I	UART2 clear to send
	ICAM1_C4	I/O	ICAM1 C4
	GPIO[17]	I/O	general purpose input/output 17
V1	SSI_SCLK_CTSN	I	synchronous serial interface clock input
	UART CTS	I	UART2 clear to send
	GPIO[21]	I/O	general purpose input/output 21
V2	SSI_FS_RTSN	I	synchronous serial interface frame sync
	UART RTS	O	UART2 request to send
	GPIO[20]	I/O	general purpose input/output 20
U4	SSI_RXD	I	synchronous serial interface receive
	GPIO[19]	I/O	general purpose input/output 19
V3	SSI_TXD	O	synchronous serial interface transmit
	GPIO[18]	I/O	general purpose input/output 18
N26	ICAM2_C4	I/O	ICAM2 C4
	GPIO[11]	I/O	general purpose input/output 11
N24	ICAM2_C8	I/O	ICAM2 C8
	GPIO[10]	I/O	general purpose input/output 10
N23	ICAM2_SETVPP	O	ICAM2 VPP
	GPIO[9]	I/O	general purpose input/output 9
B4	BOOTMODE[2]	I	select configuration bit 2 during system reset
	GPIO[2]	I/O	general purpose input/output 2
D5	BOOTMODE[1]	I	select configuration bit 1 during system reset
	GPIO[1]	I/O	general purpose input/output 1

Table 16: Multiplexed (MUX) pins *...continued*

Pin	MUX contacts primary signal and alternate function	Type [1]	Description
C4	BOOTMODE[0]	I	select configuration bit 0 during system reset
	GPIO[0]	I/O	general purpose input/output 0
P25	SC2_OFFN	I	smart card Off
	ICAM2_DETECT	I	ICAM2 detect
P24	SC2_CMD	O	smart card command
	ICAM2_SETVCC	O	ICAM2 V_{CC}
P26	SC2_RST	O	smart card reset
	ICAM2_RESET	O	ICAM2reset
N25	SC2_SCCK	O	smart card clock
	ICAM2_CLK	O	ICAM2 clock
P23	SC2_DA	I/O	smart card2 data
	ICAM2_C7	I/O	ICAM2 C7
R25	SC1_OFFN	I	smart card off
	ICAM1_DETECT	I	ICAM1 detect
R23	SC1_CMD	O	smart card command
	ICAM1_SETVCC	O	ICAM1 VCC
R24	SC1_RST	O	smart card reset
	ICAM1_RESET	O	ICAM1 reset
R26	SC1_SCCK	O	smart card clock
	ICAM1_CLK	O	ICAM1 clock
T26	SC1_DA	I/O	smart card1 data
	ICAM1_C7	I/O	ICAM1 C7

[1] In this table 'type' reflects MUX pin function only. A pin may have other 'type' capabilities as noted in its functional group.

[2] These pins are included in the XIO set. Refer to *"PNX8526 User Manual, Chapter 8"* for additional functions.

[3] The ICAM1_SETVPP and ICAM1_C8 signals are automatically selected when the ICAM function is selected. Refer to Table 17 (Offset 0x04 D600 IO_MUX_CTR). Selecting GPIO mode will disable this ICAM functionality.

7. Functional description

Figure 3 shows a block diagram of a typical PNX8526-based system. The system shown is a 'stand-alone system' which uses the internal MIPS host.

The PNX8526 runs on a single 27 MHz crystal from which all internal and external clocks are derived by on-chip synthesizers. The PNX8526 boots directly from attached flash memory or ROM. If desired, custom boot methods can be programmed using the optional I^2C-bus boot EEPROM.

The PNX8526 has three digital video inputs that accept digitized analog video (ITU-656), although only two ITU-656 streams can be processed simultaneously. Two of these inputs, DV2 and DV3, can also accept scrambled transport streams.

The DV inputs support parallel transport stream formats. In addition, a single incoming 1394 transport stream is supported. Two selected transport streams can undergo internal de-scrambling and decoding.

Based on the system implementation, one or both transport streams may pass through Point Of Deployment (POD) or Common Interface (CI) conditional access modules before transfer into the PNX8526. Either a single companion IC, such as the SCM microsystems CIMaX, or two CIMaX chips can be used. In the latter case, it is possible to handle dual decoding no matter which conditional access system is used.

The PNX8526 contains on-chip DVB, MULTI2 and DES hardware de-scramblers, as well as an ICAM verifier. The entitlement system for these de-scramblers is provided via two smart card interfaces.

The TM32 CPU does further processing on the result of the transport stream demultiplexing.

For MPEG-2 video, a slice level HL MPEG-2 video decoder performs the majority of the MPEG-2 algorithm. This MPEG decoder is capable of full-resolution decoding. The TM32 CPU does all MPEG-2 processing above the slice level. Two simultaneous SD streams or one HD stream may be processed.

All audio processing is done by the TM32 CPU. Compressed audio will be present in memory from either the transport stream de-multiplex or from the SPDIF input port. The SPDIF input port is intended primarily for DTV applications where a SPDIF source is available from an external source device, such as a DVD player. PCM (stereo sample) audio is present in memory from the I^2S-bus input ports or SPDIF input. Two AC-3 (or equivalent) compressed audio streams may be decoded simultaneously. The TM32 CPU may also process effects, enhancements and mix the audio data. Multi-channel compressed audio or down-mixed stereo PCM audio is transmitted over the SPDIF output interface. Multi-channel audio samples are Dolby Pro Logic down-mixed into the two stereo I^2S-bus interfaces to the PNX8510 companion IC. In addition to the two I^2S-bus inputs and two I^2S-bus outputs, a bidirectional I^2S-bus interface is provided. This allows connection of other audio inputs or outputs - headphones, for example. Note that there is not enough compute power to support encoding of multi-channel compressed audio simultaneous with video processing. So the multi-channel compressed audio transmitted over SPDIF must be from one of the original compressed sources.

Graphics rendering may be accomplished with the MIPS or the TM32 CPU by utilizing the 2D drawing and DMA engine. This engine can perform fast area fills, 3-operand bitblt, monochrome data expansion, and lines. It can also be used as a generic DMA engine to transfer data between memory locations on a byte-aligned basis. An alpha bitblt capability is also provided to allow for anti-aliased text and lines as well as source/destination blending operations.

Once all video and graphics data for specific fields or frames has been generated in memory, the video display pipeline starts processing those images for display. The video processing functions include 6-tap horizontal/vertical scaling, anti-flicker filtering, and de-interlacing (when progressive output is required). The processed images are then combined for each output. Up to four surfaces of any supported format may be combined to produce the primary display output. Up to two surfaces are combined to produce the

secondary output. Compositing of more surfaces for future video algorithms is possible by using the TM32 CPU and/or the memory based scaler prior to invoking the compositing/display engine. This is subject to CPU and memory bandwidth availability.

The PNX8526 contains a 1394 interface with 5C copy protection. The PNX8526 1394 can simultaneously transmit two transport streams while receiving one transport stream. The transmitted streams can be partial transport streams (created by PID filtering of an input) or one of the two streams can be software generated. In the case of receiving a scrambled 1394 transport stream input, the stream can either use the on-chip de-scramblers, or may be routed to the external companion CA IC for de-scrambling by the POD/CI CA module(s).

The PNX8526 contains a variety of peripheral interfaces to support both ASTB and DTV requirements. There are two smart card interfaces, two USB ports, two I^2C-bus ports, one IrDA data UART and two general purpose UARTs, one of which (UART3) is multiplexed with an SSI interface for soft modem support. The PNX8526 also contains an integrated IDE controller, which only requires an external isolation buffer to implement a full disk interface with sustained speeds up to 10 MB/s. A third-party PCI SuperI/O chip may be utilized to provide peripheral functionality not contained on the PNX8526. Functions such as IEEE-1284, 10/100 Ethernet, floppy drive support, UDMA66 IDE controllers and others are currently available in low-cost, commercially-available parts.

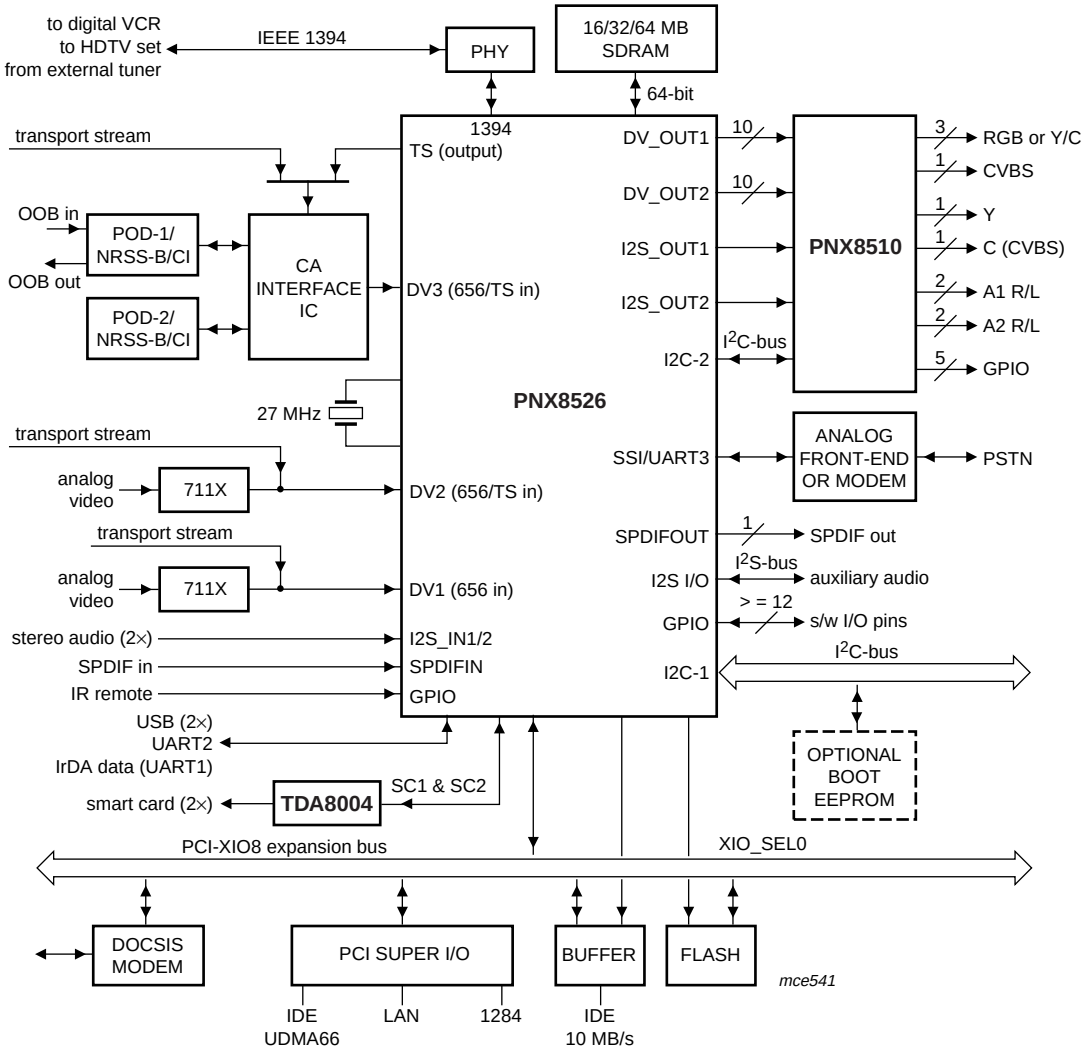


Fig 3. PNX8526-based system block diagram

8. I/O multiplexer control register

The I/O multiplexer control register is used to configure the multifunction pins to alternate functions as described in Table 16. Control is achieved via the global 2 register IO_MUX_CTRL Table 17.

Table 17: Global 2 registers

Bit	Symbol	Access	Value	Description
0x04 D600 IO_MUX_CTRL				
31, 15	not used			ignore during writes and read as zeros
14	AIO_MUX_SEL	R/W		I2S_IO audio mode
			0	select I2S_IO as audio output
			1	select I2S_IO as audio input

Table 17: Global 2 registers *...continued*

Bit	Symbol	Access	Value	Description
13	SSI_SEL	R/W		SSI or UART3 mode:
			0	select UART3
			1	select SSI
12	RGB24_SEL	R/W		audio Out2 or RGB mode:
			0	select audio Out2
			1	1select RGB (DV_OUT [23:20])
11:10	SMCRD2_MUX_CTRL[1:0]	R/W		ICAM or smart card2 mode:
			00	smart card1 module ports go to smart card2 pins
			01	smart card2 module ports go to smart card2 pins
			10	ICAM1 module ports go to smart card2 pins
			11	ICAM2 module ports go to smart card2 pins
9:8	SMCRD1_MUX_CTRL[1:0]	R/W		ICAM or smart card2 mode:
			00	smart card1 module ports go to smart card1 pins
			01	smart card2 module ports go to smart card1 pins
			10	ICAM1 module ports go to smart card1 pins
			11	ICAM2 module ports go to smart card1 pins
7	not used		-	ignore during writes and read as zeroes
6:4	VIP2_MUX_CTRL[2:0]	R/W		VIP2 module selection:
			000	VIP data from DV1 port
			001	VIP data from DV2 port
			010	VIP data from DV3 port
			011	VIP data from DV_OUT1 (AICP1) port
			100	1394 data from link core
3	not used		-	ignore during writes and read as zeroes
2:0	VIP1_MUX_CTRL[2:0]	R/W		VIP1 module selection:
			000	VIP data from DV1 port
			001	VIP data from DV2 port
			010	VIP data from DV3 port
			011	VIP data from DV_OUT2 (AICP2) port
			100	1394 data from link core

9. Power supply sequencing

Power application and power removal should obey the following rules:

9.1 Power-on sequence

- Apply power to V_{DDC} (1.26 V)
- Allow V_{DDC} (1.26 V) to stabilize (approximately 100 ms recommended)
- Apply power to V_{DD} (3.3 V).

9.2 Power-off sequence

- Power may be removed from V_{DD} (3.3 V) and V_{DDC} (1.26 V) at the same time
- Otherwise remove power from V_{DD} (3.3 V) followed by V_{DDC} (1.26 V).

10. Limiting values

Table 18: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	I/O pad DC supply voltage		3.0	3.6	V
V_{DDC}	logic core supply voltage		1.20	1.32	V
$V_{I/O}$	voltage on	with respect to V_{SS}			
	3 V I/O pins		–0.5	V_{DD} + 0.5	V
	5 V tolerant I/O pins		–0.5	+5.5	V
$V_{I(th)}$	voltage on I/O pins with non Schmitt trigger input voltage threshold		1.46	1.76	V
$V_{IL(ST)}$	LOW-level input voltage threshold on I/O pins with Schmitt trigger input		0.93	1.06	V
$V_{IH(ST)}$	HIGH-level input voltage threshold on I/O pins with Schmitt trigger input		1.66	1.79	V
V_{trt}	transient voltages on I/O pins		-	10	V
P_{tot}	total power dissipation				
	dynamic		-	2	W
	static	AICP off	-	1	W
T_{amb}	ambient temperature		0	70	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		-	100	°C
V_{esd}	electrostatic discharge voltage	human body model	-	± 1.5	kV

11. Thermal characteristics

PNX8526 can be used in different environments creating different junction temperatures.

The thermal resistance from junction to ambient ($R_{th(j-a)}$) of the PNX8526 in its HBGA456 package is approximately 11.7 K/W. This value is achieved using natural convection, no external heatsink and using a JEDEC-defined printed-circuit board with high thermal conduction (see *"JEDEC standards 51-2 and 51-7"* for details).

Given the power dissipation of the PNX8526 and the ambient temperature inside the enclosure, the expected junction temperature can be calculated using the following equation:

$$T_j = T_{amb} + P \times R_{th(j\text{-}a)} \quad (1)$$

In some applications the junction temperature may be judged too high, reducing the acceptable lifetime (see Section 13.2). However cooling can be improved by fitting an additional external heatsink, or increasing the airflow around the device. Table 19 shows the improvements that can be expected if these measures are taken.

Table 19: PNX8526 thermal data

Heatsink size = 37 mm × 37 mm × 10 mm.

PNX8526	Thermal resistance $R_{th(j\text{-}a)}$ (K/W)		
	Airflow		
	0 m/s	1 m/s	2 m/s
Standard	11.7	10.0	8.5
With external heatsink	9.5	7.6	6.3

12. Characteristics

The characteristics listed in the following tables apply to standard operating conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0 V, ground). Positive current flows into the referenced pin. The standard operating voltage range is V_{DD} = 3.3 V ± 0.3 V and V_{DDC} = 1.26 V ± 0.06 V. All digital input/output pins are 3.3 V tolerant.

In all cases described below, digital V_{DD} = 3.3 V ± 5 % and ambient temperature is 0 °C to 70 °C.

All AC timings are based on a 30 pF test load and are measured at a 1.6 V threshold (see Figure 4). Actual input/output voltage threshold is dependent on pad type, for example, Schmitt trigger input (see Section 6.1).

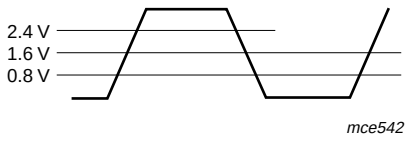


Fig 4. General AC characteristics

The AC voltage characteristics for active signal pins of the controller are listed in Table 20. Signal names for the PCI bus configuration are listed, as well as the minimum and maximum voltage, current, and capacitance for each pin.

Table 20: Digital AC/DC characteristics

V_{DD} = 3.3 V ± 5 %; T_{amb} = 0 °C to 70 °C; unless otherwise specified.

Symbol	Parameter	Conditions	[1]	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage			–0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.4	-	V_{DD} + 0.5	V
V_{OL}	LOW-level output voltage			0	-	0.4	V

Table 20: Digital AC/DC characteristics *...continued*

V_{DD} = 3.3 V ± 5 %; T_{amb} = 0 °C to 70 °C; unless otherwise specified.

Symbol	Parameter	Conditions	[1]	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage			2.4	-	-	V
I_{OL1}	LOW-level output current 1		[2]	-	-	5	mA
I_{OH1}	HIGH-level output current 1		[2]	-	-	–5	mA
I_{OL2}	LOW-level output current 2		[3]	-	-	8	mA
I_{OH2}	HIGH-level output current 2		[3]	-	-	–8	mA
I_{OL3}	LOW-level output current 3		[4]	-	-	12	mA
I_{OH3}	HIGH-level output current 3		[4]	-	-	–12	mA
I_{OL4}	LOW-level output current 4		[5]	-	-	14	mA
I_{OH4}	HIGH-level output current 4		[5]	-	-	–14	mA
I_{OZ}	3-state output leakage current			-	-	41	µA
C_{in}	input capacitance			-	-	3.5	pF
$I_{DD(core)}$	supply current; core			-	0.9	1.5	A
$I_{DD(periph)}$	supply current; peripherals			-	0.13	0.2	A

[1] The pin names used in the following notes are the primary names for PCI configurations. Output signals multiplexed on some pins have the same drive level.

[2] I_{OL1} (5 mA); I_{OH1} (–5 mA):
I2S_IN1_SCK, I2S_IN1_WS, I2S_IN2_SCK, I2S_IN2_WS, I2S_OUT1_SCK, I2S_OUT1_WS, I2S_OUT1_SD, I2S_OUT2_SD, DV1_DATA[9:0], DV1_VALID, DV1_CLK, DBG_TDO, JTAG_TDO, XTALO, UA1_TX, UA1_RX, UA2_TX, UA2_RX, UA2_RTS, UA2_CTS, SC1_DA, SC1_CMD, SC1_RST, SC1_SCCK, SC2_DA, SC2_CMD, SC2_RST, SC2_SCCK, SSI_SCLK_CTSN, SSI_FS_RTSN, SSI_RXD, SSI_TX, USB_DM[1:0], USB_DP[1:0], USB_PWR.

[3] I_{OL2} (8 mA); I_{OH2} (–8 mA):
DV_OUT1[9:0], DV_OUT2[9:0], DV_CLK1, DV_CLK2, HSYNC, VSYNC, I2S_IN1_OSCLK, I2S_IN2_OSCLK, I2S_IO_OSCLK, I2S_IO_SCK, I2S_IO_WS, I2S_IO_SD[3:0], I2S_OUT1_OSCLK, I2S_OUT2_OSCLK, I2S_OUT2_SCK, I2S_OUT2_WS, TS_DATA[7:0], TS_SOP, TS_VALID, TS_CLK, PHY_D[7:0], PHY_CTL[1:0], PHY_LREQ, MD[63:0], MDQM[7:0], MCKE, I2C1_SCL, I2C1_SDA, I2C2_SCL, I2C2_SDA, GPIO[11:0], SYS_RSTN_OUT, XIO_SEL[2:0], XIO_ACK, XIO_AD25.

[4] I_{OL3} (12 mA); I_{OH3} (–12 mA):
PCI_AD[31:0], PCI_CBE[3:0], PCI_DEVSEL, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_PERR, PCI_PAR, PCI_INTA, PCI_REQ, PCI_GNT, PCI_REQ_A, PCI_REQ_B, PCI_GNT_A, PCI_GNT_B, PCI_SERR,MWE, PLL_OUT.

[5] I_{OL4} (14 mA); I_{OH4} (–14 mA):
SPDIF_OUT, MCLK[1:0], MA[11:0], MBA[1:0], MCS, MRAS, MCAS.

12.1 Reset timing

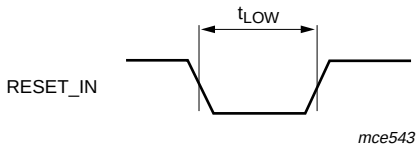


Fig 5. Reset timing

Table 21: Reset timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOW}	RESET_IN active pulse width	after stable power	400	-	-	µs

12.2 Peripheral Controller Interface (PCI) timing

For additional timing diagram information on XIO and IDE interfaces see *"PNX8526 User Manual, Chapter 8"*.

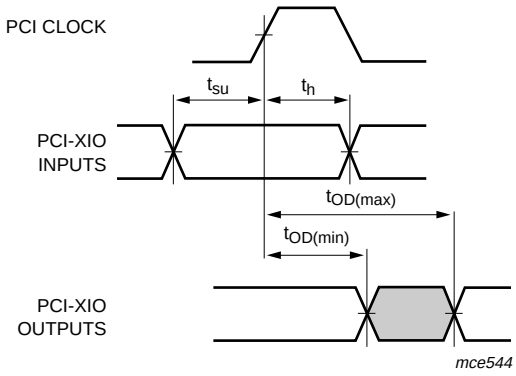


Fig 6. PCI timing

Table 22: PCI input timing (with reference to PCI clock)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	setup time on pins					
	PCI_AD[31:0], PCI_CBE[3:0], PCI_FRAME, PCI_IRDY		7	-	-	ns
	PCI_GNT		10	-	-	ns
t_h	hold time on pins					
	PCI_AD[31:0]		0	-	-	ns
	PCI_CBE[3:0], PCI_FRAME, PCI_IRDY, PCI_IDSEL		0	-	-	ns
	PCI_GNT		0	-	-	ns

Table 23: PCI output valid timing (with reference to PCI clock)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{OD(min)}$	minimum output delay on pins	[1]				
	PCI_AD[31:0], PCI_CBE[3:0]		2	-	-	ns
	PCI_DEVSEL, PCI_PAR		2	-	-	ns
	PCI_STOP		2	-	-	ns
	PCI_TRDY		2	-	-	ns
$t_{OD(max)}$	maximum output delay on pins	[2]				
	PCI_AD[31:0], PCI_CBE[3:0]		-	-	11	ns
	PCI_DEVSEL, PCI_PAR		-	-	11	ns
	PCI_STOP		-	-	11	ns
	PCI_TRDY		-	-	11	ns
	PCI_REQ		-	-	12	ns
	PCI_REQ		-	-	12	ns

[1] Minimum delay is the minimum time after the clock edge that a valid signal state from the previous cycle will begin transition to the next state (become invalid).

[2] Maximum delay is the maximum time after the clock edge that a signal state is valid for the next cycle.

12.3 Main Memory Interface (MMI) timing

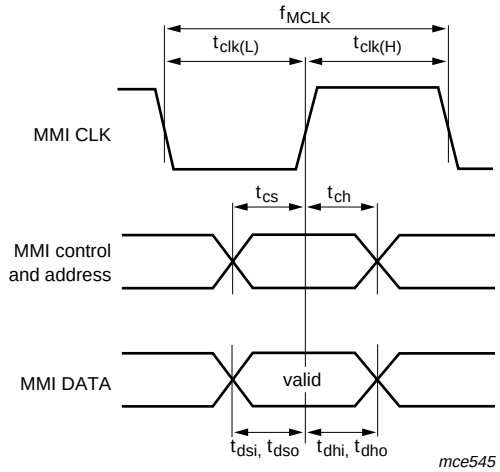


Fig 7. MMI timing

Table 24: MMI timing (with reference to MCLK)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{cs}	CS setup time		1.5	-	-	ns
t_{ch}	CS hold time		0.8	-	-	ns
t_{dso}	data output setup time	write cycle	1.5	-	-	ns
t_{dho}	data output hold time	write cycle	0.8	-	-	ns
t_{dsi}	data input setup time	read cycle	0	-	-	ns
t_{dhi}	data input hold time	read cycle	2.0	-	-	ns

Table 24: MMI timing (with reference to MCLK) *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{clk(L)}$	clock LOW time		2.9	-	-	ns
$t_{clk(H)}$	clock HIGH time		2.9	-	-	ns
f_{MCLK}	memory clock frequency (MCLK[1:0])			-	166	MHz

12.4 GPIO timing

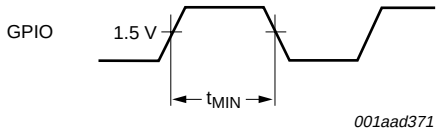


Fig 8. GPIO timing

Table 25: GPIO timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{MIN}	pulse width	GPIO as input	[1]	10	-	-	ns
		GPIO as output		75	-	-	ns

[1] If GPIO is to be time-stamped, the minimum pulse width is 75 ns.

12.5 UART timing

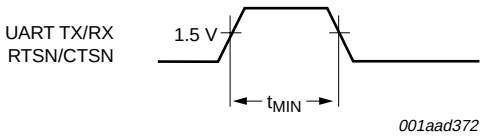


Fig 9. UART timing

Table 26: UART output timing (with reference to UART clock)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{MIN}	pulse width	UART TX	[1]	4.3	-	-	µs
		UART RX		4.3	-	-	µs
		UART RTSN		4.3	-	-	µs
		UART CTSN		4.3	-	-	µs

[1] Maximum baud rate: 230 kBd.

12.6 SSI timing

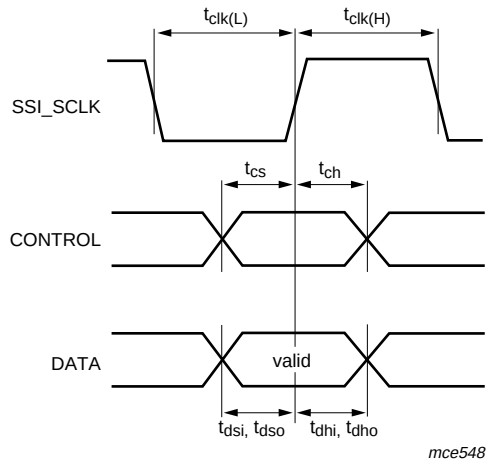


Fig 10. SSI timing

Table 27: SSI timing (with reference to MCLK)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{cs}	CS setup time		3	-	-	ns
t_{ch}	CS hold time		2	-	-	ns
t_{dso}	data output setup time		3	-	-	ns
t_{dho}	data output hold time		2	-	-	ns
t_{dsi}	data input setup time		1.0	-	-	ns
t_{dhi}	data input hold time		1.0	-	-	ns
$t_{clk(L)}$	clock LOW time		25	-	-	ns
$t_{clk(H)}$	clock HIGH time		25	-	-	ns

12.7 I²C-bus timing

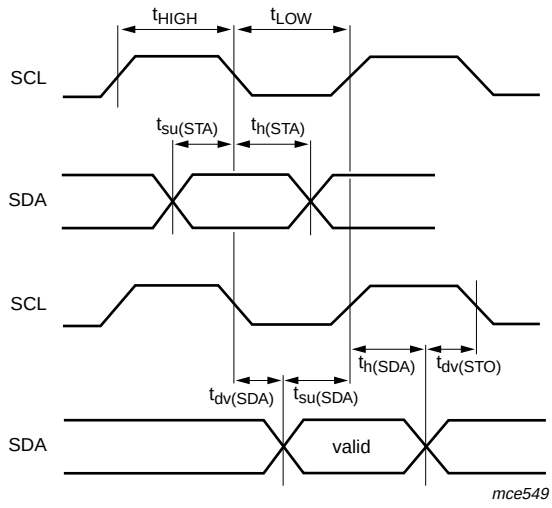


Fig 11. I²C-bus timing

Table 28: I²C-bus timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		-	-	400	kHz
$t_{su(STA)}$	start condition setup time		1	1	-	µs
$t_{h(STA)}$	start condition hold time		1	1	-	µs
t_{LOW}	SCL LOW time		1	1	-	µs
t_{HIGH}	SCL HIGH time		1	1	-	µs
$t_{su(SDA)}$	data setup time		100	100	-	ns
$t_{h(SDA)}$	data hold time		0	0	-	ns
$t_{dv(SDA)}$	SCL LOW to data out valid		-	-	0.5	µs
$t_{dv(STO)}$	SCL HIGH to data out		1	1	-	µs

12.8 IEEE 1394 Phy-Link interface

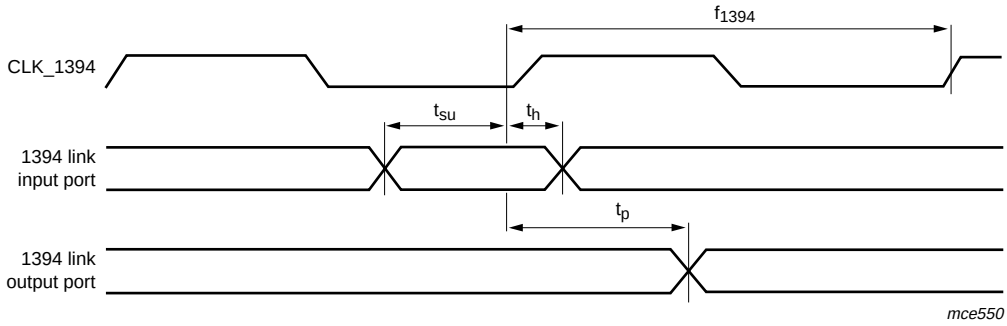


Fig 12. IEEE 1394 Phy-Link interface timing

Table 29: IEEE 1394 Phy-Link interface signals

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{1394}	CLK_1394 frequency		49.147	-	49.157	MHz
t_{su}	setup time for 1394 link input port	PHY_D[7:0]; PHY_CTL[1:0]	6	-	-	ns
t_h	input hold time		0	-	-	ns
t_p	output propagation delay for 1394 link output port	PHY_D[9:0]; PHY_LREQ; PHY_CTL[1:0]	-	-	9	ns

12.9 I²S-bus audio input and output timing

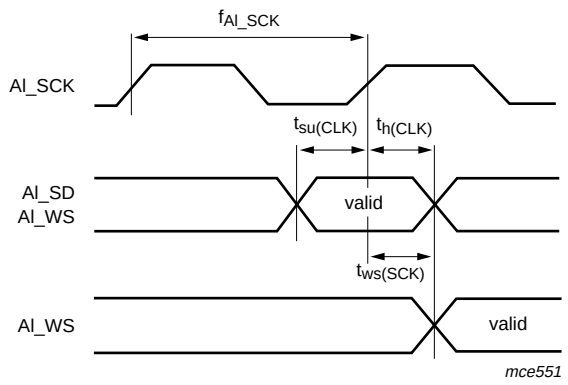


Fig 13. I²S-bus audio input timing

Table 30: I²S-bus audio input

Timing is with respect to the SCK clock edge. The PNX8526 is the source of AI_WS.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{AI_SCK}	audio-in clock AI_SCK frequency		-	-	20	MHz
$t_{su(CLK)}$	audio-in to AI_SCK setup time	audio interface as slave	3	-	-	ns
$t_{h(CLK)}$	audio-in from AI_SCK hold time	audio interface as slave	2	-	-	ns
$t_{ws(SCK)}$	audio-in clock AI_SCK to audio-in word-select AI_WS valid		2	-	10	ns

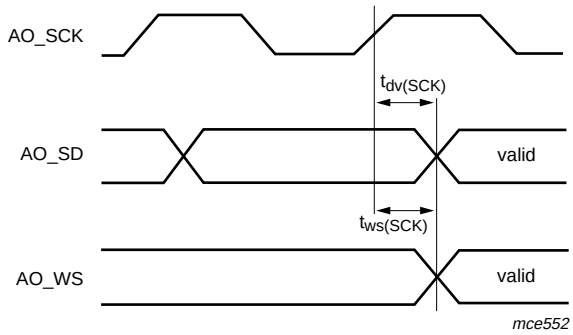


Fig 14. I²S-bus audio output timing

Table 31: I²S-bus audio output

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{AO_SCK}	audio-out clock AO_SCK frequency		-	-	20	MHz
$t_{dv(SCK)}$	audio-out clock AO_SCK to audio-out data AO_SD valid		2	-	-	ns
$t_{ws(SCK)}$	audio-out clock AO_SCK to audio-out word-select AO_WS valid		-	-	10	ns

12.10 SPDIF timing

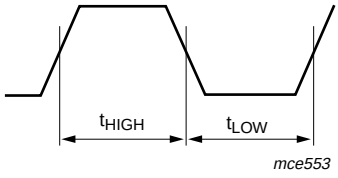


Fig 15. SPDIF clock

Table 32: SPDIF timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{HIGH}	clock HIGH time (PCI)		-	5.2	-	µs
t_{LOW}	clock LOW time (PCI)		-	5.2	-	µs

12.11 Digital video output (DV_OUT) timing

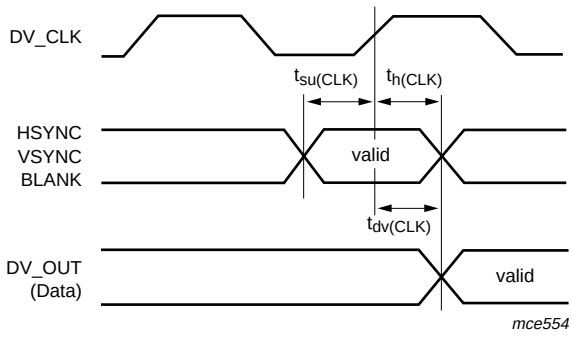


Fig 16. DV_OUT timing

Table 33: DV_OUT timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{DV_CLK}	video out clock DV_CLK frequency		[1]	27	-	-	MHz
$t_{dv(CLK)}$	video out clock DV_CLK to video out DV_OUT valid			–3.7	-	0	ns
$t_{su(CLK)}$	VSYNC to DV_CLK setup time	DV_CLK as input		3	-	-	ns
$t_{h(CLK)}$	CRT control from DV_CLK HSYNC, VSYNC, BLANK hold time			0	-	-	ns

[1] DV_CLK period is programmable via the internal PLL.

12.12 Digital video input (DV Input) timing

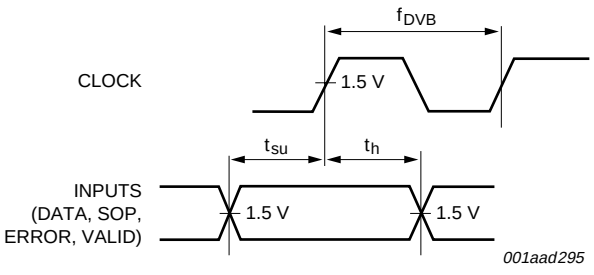


Fig 17. DV input timing

Table 34: DV input timing (referenced to input video clock)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{DVB}	DVB clock frequency		-	27	-	MHz
t_{su}	input data setup time		3	-	-	ns
t_h	input data hold time		3	-	-	ns

12.13 Transport Stream Output (TSO) timing

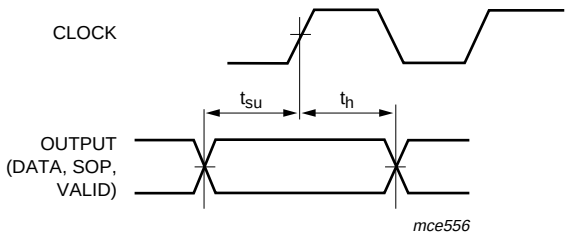


Fig 18. TSO timing

Table 35: TSO timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	data setup time		3	-	-	ns
t_h	data hold time		0	-	-	ns

13. Application information

13.1 Differences between PNX8525 and PNX8526

There are a number of differences between the PNX8525 and the PNX8526 with respect to the physical interfacing of the device. These differences are described in Table 36.

Table 36: Differences between PNX8525 and PNX8526

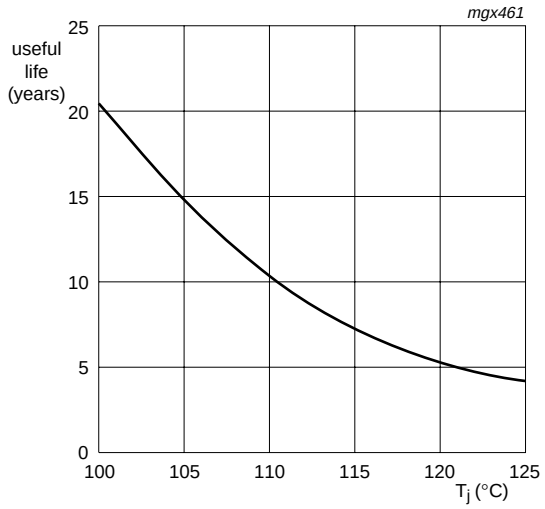
PNX8525	PNX8526
Core supply voltage	
1.8 V ± 5 %	1.26 V ± 0.06 V
I^2C-bus pads	
GPIO pads with Schmitt trigger and pull-ups	Special I^2C-bus pads designed to meet the I^2C-bus specification
IEEE-1394 pads	
GPIO pads with Schmitt trigger and pull-ups	Special IEEE-1394 pads designed to meet the IEEE-1394 link to Phy specification
PCI interface	
Supports 5 V tolerant interface with 3.3 V signalling	No 5 V tolerant interface, all signals limited to 3.3 V
System reset output (SYS_RSTN_OUT)	
Drive capability 12 mA	Drive capability 8 mA
Clock output (PLL_OUT)	
Drive capability 12 mA	Drive capability 8 mA
SPDIF output	
Drive capability 16 mA	Drive capability 14 mA
DV1 port, SSI, UART2, smart card1 and smart card2	
Drive capability 4 mA	Drive capability 5 mA, INputs support hysteresis
I^2S-bus CLK and WS	
Drive capability 4 mA	Drive capability 5 mA
TS interface and I^2S-bus data lines	
Hysteresis on inputs not supported	Hysteresis on inputs supported
SDRAM interface	
Supports 5 V tolerant signalling, with 3.3 V drive. (AD[11:0], CLK[1:0], RAS,CAS, CS and BA[1:0] drive capability 16 mA)	No 5 V tolerant signalling. Drive capability 14 mA
XIO SEL[2:0], ACK, A25	
Drive capability 12 mA	Drive capability 8 mA
Peripheral power supply	
Single connection on PCB for all V_{DD} bond pads	Requires separation of V_{DDC} into three segments, each segment filtered and star connected back to source [1]
Core power supply	
Single connection on PCB for all V_{DDC} bond pads	Requires separation of V_{DDC} into two segments, each segment filtered and star connected back to source [2]

[1] The new connections are:
   a) V_{DD1} - the input/output supply connection
   b) V_{DD2} - analog clock generation unit; Custom Analog Block (CAB)
   c) V_{DD3} - Trimedia clock generation PLL.

[2] The new connections are:
   a) V_{DDC1} - main core supply connection
   b) V_{DDC2} - 1.728GHz PLL supply connection.

13.2 Lifetime versus temperature

The relationship between operating (junction) temperature and the expected lifetime of a device is shown in Figure 19.



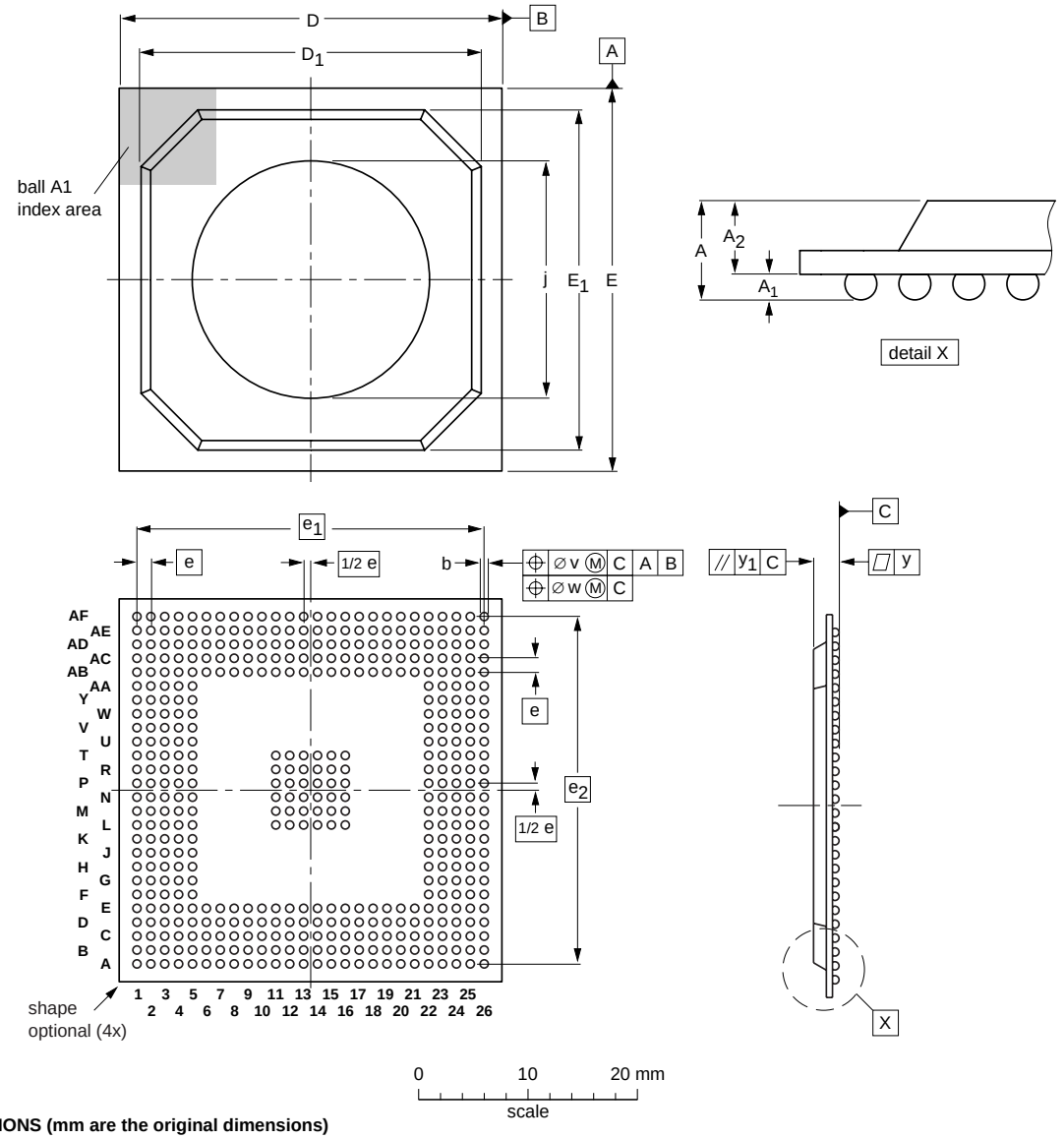
Useful life (years) as a function of junction temperature (°C); 1 % cumulative failures; 8 hours/day.

Fig 19. Lifetime dependency on temperature

As shown in Figure 19, at a junction temperature of 110 °C a 10 year lifetime can be expected (at 8 hours per day). If the junction temperature is increased to 125 °C, the lifetime can be reduced to 4 years. The junction temperature can be influenced by following the guidelines given in Section 11.

14. Package outline

HBGA456: plastic thermal enhanced ball grid array package; 456 balls; body 35 x 35 x 1.8 mm; heatsink **SOT610-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	D_1	E	E_1	e	e_1	e_2	j	v	w	y	y_1
mm	2.6	0.7 0.5	1.90 1.65	0.9 0.6	35.2 34.8	30.75 29.75	35.2 34.8	30.75 29.75	1.27	31.75	31.75	26 22	0.3	0.15	0.2	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT610-1	144E	MS-034	- - -			~~00-12-13~~ 02-01-30

Fig 20. Package outline SOT610-1 (HBGA456)

15. Soldering

15.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

15.2 Through-hole mount packages

15.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

15.3 Surface mount packages

15.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages

- for packages with a thickness ≥ 2.5 mm
- for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.

- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.4 Package related soldering information

Table 37: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package [1]	Soldering method		
		Wave	Reflow [2]	Dipping
Through-hole mount	CPGA, HCPGA	suitable	–	–
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable [3]	–	suitable
Through-hole-surface mount	PMFP [4]	not suitable	not suitable	–
Surface mount	BGA, HTSSON..T [5], LBGA, LFBGA, SQFP, SSOP..T [5], TFBGA, VFBGA, XSON	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [6]	suitable	–
	PLCC [7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended [7] [8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended [9]	suitable	–
	CWQCCN..L [10], WQCCN..L [10]	not suitable	not suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

16. Abbreviations

Table 38: Abbreviations

Acronym	Description
2D	two-dimensional
5C	5C digital copy protection technology
AC-3	Audio Coding version 3
ATSB	Advanced Set Top Box
ATSC	Advanced Television Systems Committee
AVIF	Audio and Video Interface
bitblt	bit-block transfer of color data
CI	Common Interface
CPU	Central Processor Unit
CRT	Cathode Ray Tube
DAC	Digital Analog Conversion
DES	Data Encryption Standard
DMA	Direct Memory Allocation
DVB	Digital Video Broadcast
DTV	Digital Television
DVD	Digital Video Disc
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input/Output
HBGA	Heat slug Ball Grid Array
HD	High Definition
I^2C-bus	Inter Integrated Circuit bus
I^2S-bus	Inter Integrated Circuit Sound bus
IC	Integrated Circuit
ICAM	Integrated Conditional Access Module
IDE	Integrated Drive Electronics
IEEE	Institute of Electrical and Electronic Engineers
JEDEC	Joint Electronic Device Engineering Council
MIPS	Million Instructions Per Second
MPEG	Motion Picture Experts Group
MULTI2	Security standard for Japanese market
NTSC	National TV Systems Committee
OS	Operating System
PAL	Phase Alternate Line
PCI	Peripheral Component Interconnect
PCM	Pulse Code Modulation
PID	Program Identifier
PLL	Phase-Locked Loop
RGB	Red Green Blue
ROM	Read Only Memory

Table 38: Abbreviations *...continued*

Acronym	Description
SD	Standard Definition
SDRAM	Synchronous Dynamic Random Access Memory
SECAM	Systeme Electronique Couleur Avec Memoire
SPDIF	Sony Philips Digital Interface
SSI	Synchronous Serial Interface
TSO	Transport Stream Output
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VLIW	Very Long Instruction Word
XIO	Extended Input Output

17. Revision history

Table 39: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PNX8526_2	20050711	Product data sheet	-	9397 750 15101	PNX8526_1
Modifications:	• Status changed to Product data sheet • Editorial improvements made.				
PNX8526_1	20040211	Preliminary data sheet	-	9397 750 11715	-

18. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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23. Contents

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