7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

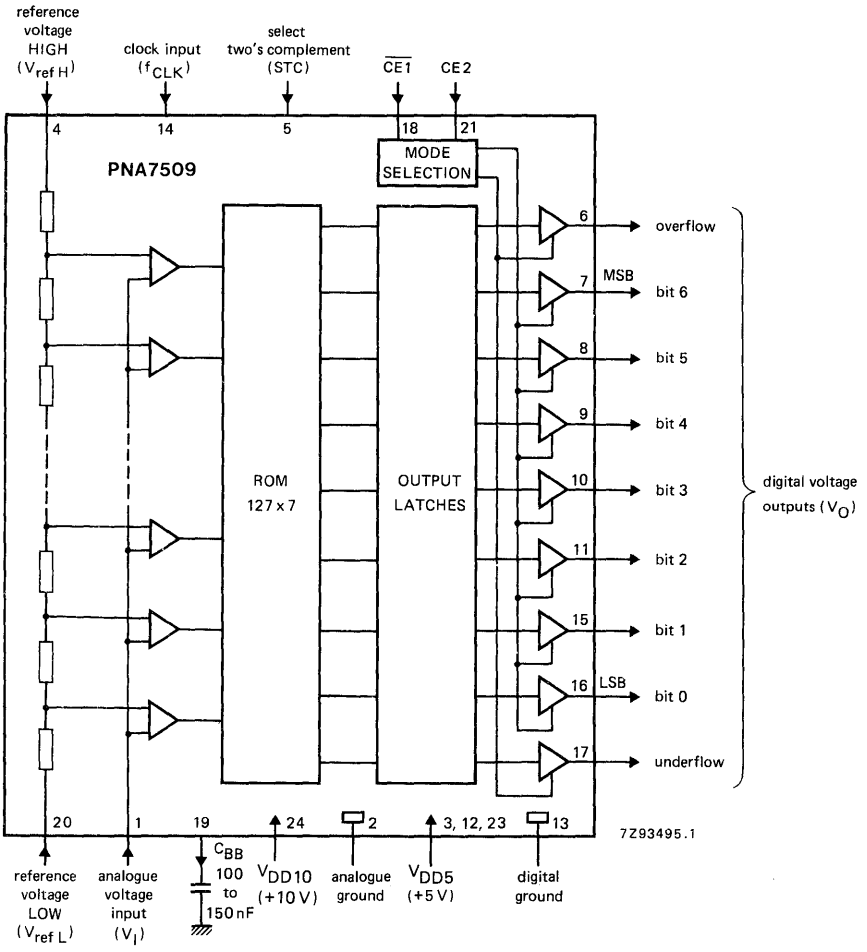
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)		V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)		V_{refH}	5,0	5,1	5,2	V
Non-linearity	f_i = 1,1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
–3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

DEVELOPMENT DATA

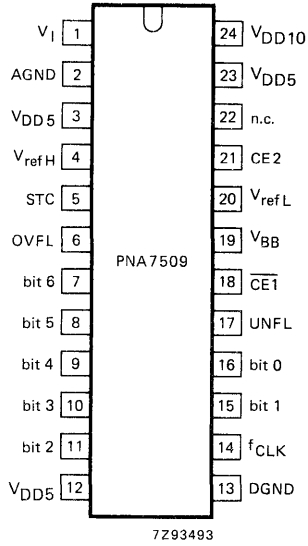


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE 2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0,5 to + 7	V
Supply voltage range (pin 24)	V_{DD10}	−0,5 to + 12	V
Input voltage range	V_I	−0,5 to + 7	V
Output current	I_O	5	mA
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4{,}5$ to 5,5 V; $V_{DD10} = V_{24-2} = 9{,}5$ to 10,5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)	V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH (note 1)	V_{IH}	3,0	–	V_{DD5}	V
Digital input levels (pins 5,18,21; note 2)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2,6	–	V
Input capacitance (note 3)	C_{1-2}	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5,0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0,4	V
Output voltage HIGH at $-I_O$ = 0,5 mA	V_{OL}	2,4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2,50 V; V_{refH} = 5,08 V)

step	$V_{1\text{-}2}$ (1)	UNFL	OVFL	binary bit 6 – bit 0							two's complement bit 6 – bit 0							
underflow	< 2,51	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
0	2,51	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
1	2,53	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	
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126	5,03	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	0	
127	5,05	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	
overflow	⩾ 5,07	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	

DEVELOPMENT DATA

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE\ 1}$	CE 2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13}$ = 4,5 V to 5,5 V; $V_{DD10} = V_{24-2}$ = 9,5 V to 10,5 V; V_{refL} = 2,5 V; V_{refH} = 5,1 V; f_{CLK} = 22 MHz; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C

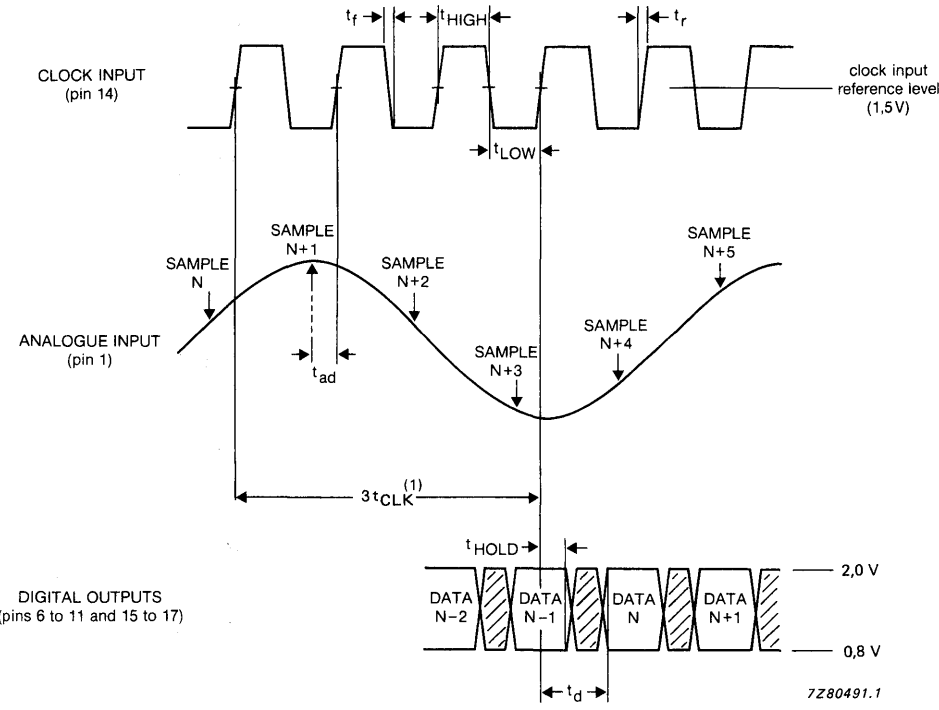
parameter	symbol	min.	max.	unit
Switching characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	3	ns
fall time	t_f	–	3	ns
Analogue input (note 1)				
Bandwidth (–3 dB)	B	11	–	MHz
Differential gain (note 2)	dG	–	± 5	%
Differential phase (note 2)	d_p	–	± 2,5	deg
Non-harmonic noise		–	–36	dB
Peak error (non-harmonic noise) (note 3)		–	3	LSB
Harmonics (full scale)				
fundamental (note 3)	f_0	–	0	dB
r.m.s. (2nd + 3rd harmonic)	$f_{2,3}$	–	–28	dB
r.m.s. (4th + 5th + 6th + 7th harmonic)	f_{4-7}	–	–35	dB

parameter	symbol	min.	max.	unit
Digital outputs (notes 1 and 4)				
Output hold time	t_{HOLD}	6	–	ns
Output delay time at C_L = 15 pF	t_d	–	38	ns
Output delay time at C_L = 50 pF	t_d	–	48	ns
3-state delay time	t_{dt}	–	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at f_i = 1,1 kHz				
integral	INL	–	± ½	LSB
differential	DNL	–	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sinewave (peak-to-peak value of the analogue input voltage at $V_{I(p-p)}$ = 1,8 V) combined with a sinewave voltage ($V_{I(p-p)}$ = 0,7 V) at f_i = 5 MHz.
3. Analogue frequency $f_{i(A)}$ = 5 MHz
   Amplitude $V_{i(A)}$ = 2.42 V (peak-to-peak value).
4. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

DEVELOPMENT DATA



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

DEVELOPMENT DATA

APPLICATION NOTE

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; V_{DD5} = 5 V, V_{DD10} = 10 V, T_{amb} = 22 °C.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1,5	LSB
Suppression of harmonics			
sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching).
Even a spike duration of less than 1 μs can destroy the device.

APPLICATION NOTE (continued)

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.

Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.

The successive processing completes the specific measurement (Fig. 5, 6, 7 and 8).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.

After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.

To calculate differential non-linearity a counter is used to count the frequency of each step. A histogram is calculated from the counter result to provide the basis for further computation (Fig. 7).

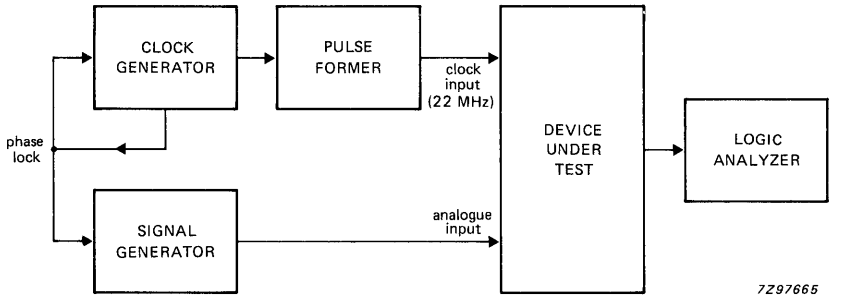
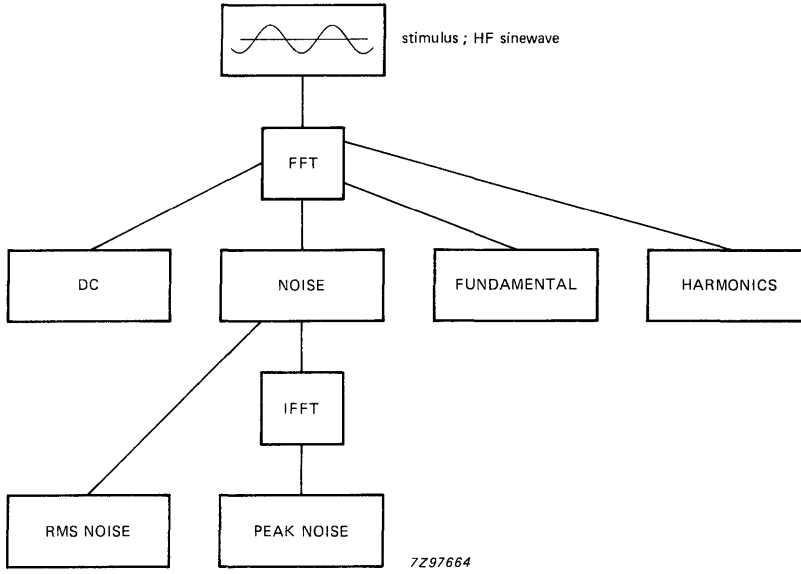


Fig. 4 Analogue-to-digital converter testing with locked signal source.



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.

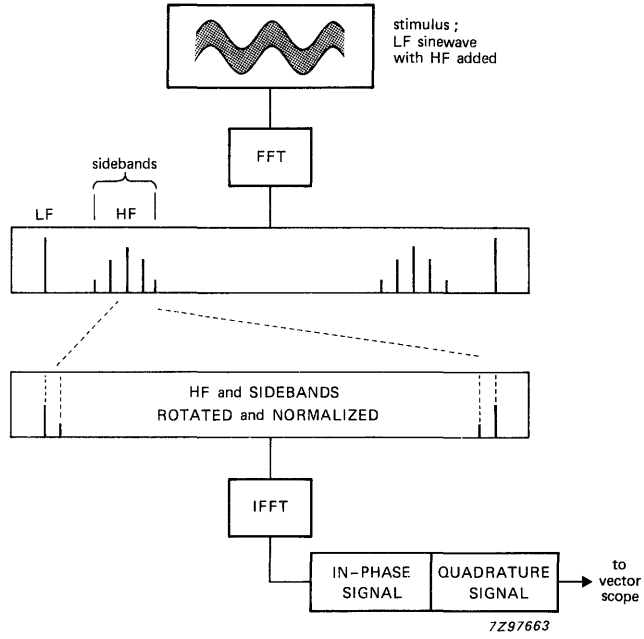
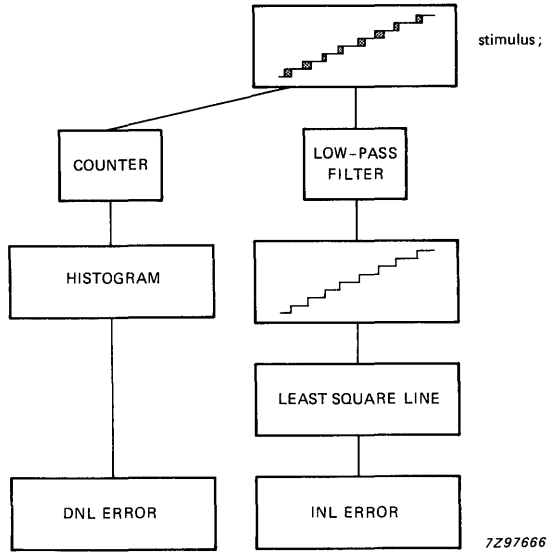


Fig. 6 Differential gain and phase.

APPLICATION NOTE (continued)



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 7 Low frequency ramp test; linearity.

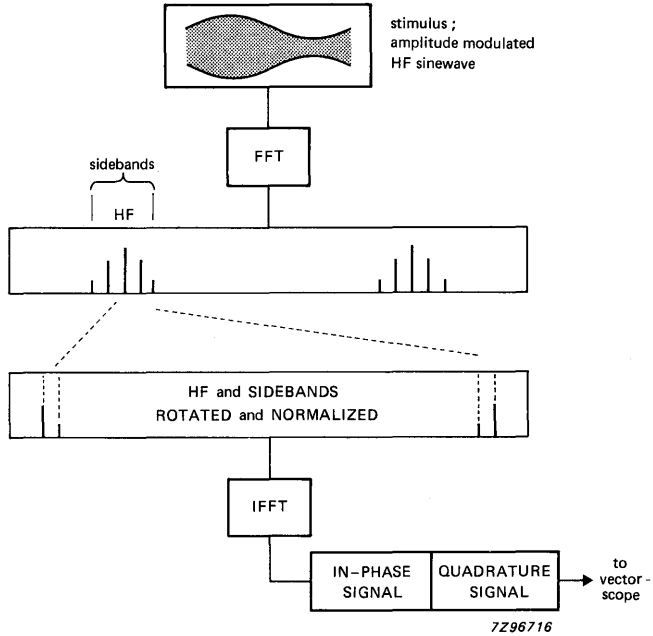


Fig. 8 Large signal phase error.