

PMCM440VNE

12 V, N-channel Trench MOSFET

7 April 2015

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a 4 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Ultra small package: $0.78 \times 0.78 \times 0.35$ mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	12	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-	5	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$		-	57	67	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

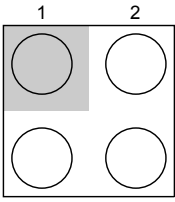
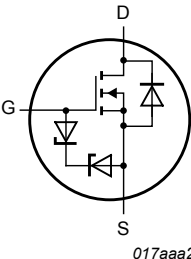


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	 <p>Transparent top view WLCSP4 (OL-PMCM440VNE)</p>	 <p>017aaa255</p>
A2	S	source		
B1	D	drain		
B2	S	source		

6. Ordering information

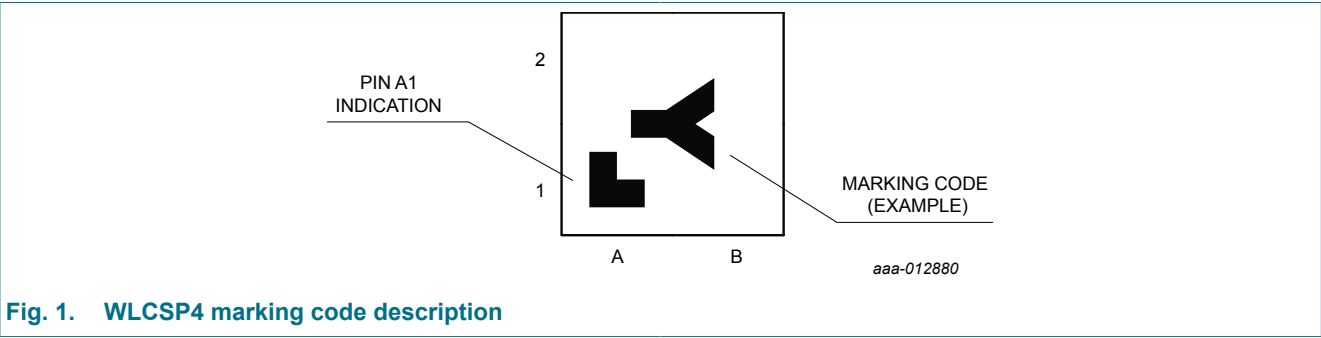
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCM440VNE	WLCSP4	WLCSP4: wafer level chip-size package; 4 bumps (2 x 2)	OL-PMCM440VNE

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM440VNE	M



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	12	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	5	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	3.9	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	15.5	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	16	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	400	mW
			[1]	-	1300	mW
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	12500	mW
T_j	junction temperature			-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.1	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .
- [2] Device mounted on an FR4 Printed Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

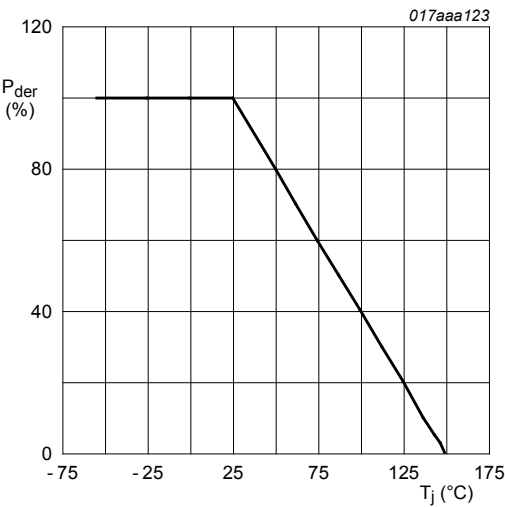


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

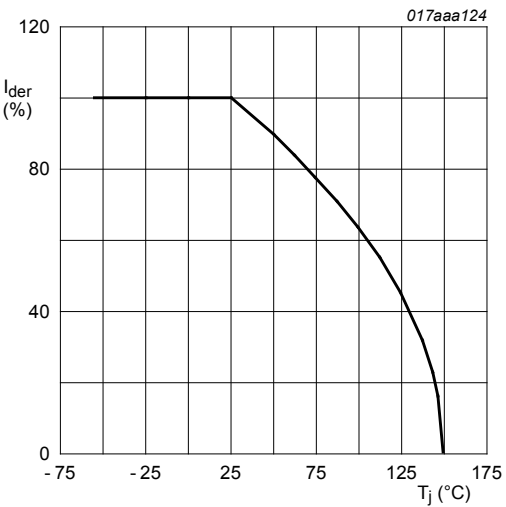


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

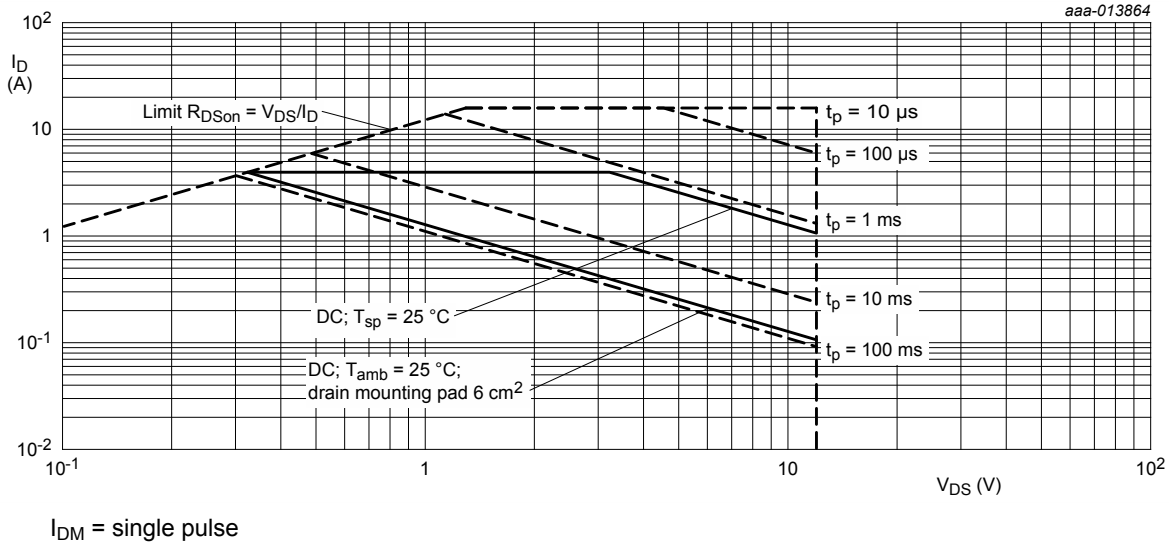


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	250	300	K/W
			[2]	-	70	85	K/W
			[3]	-	85	100	K/W
		in free air; $t \leq 5 s$	[3]	-	50	60	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	5	10	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain, 4-layer, 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

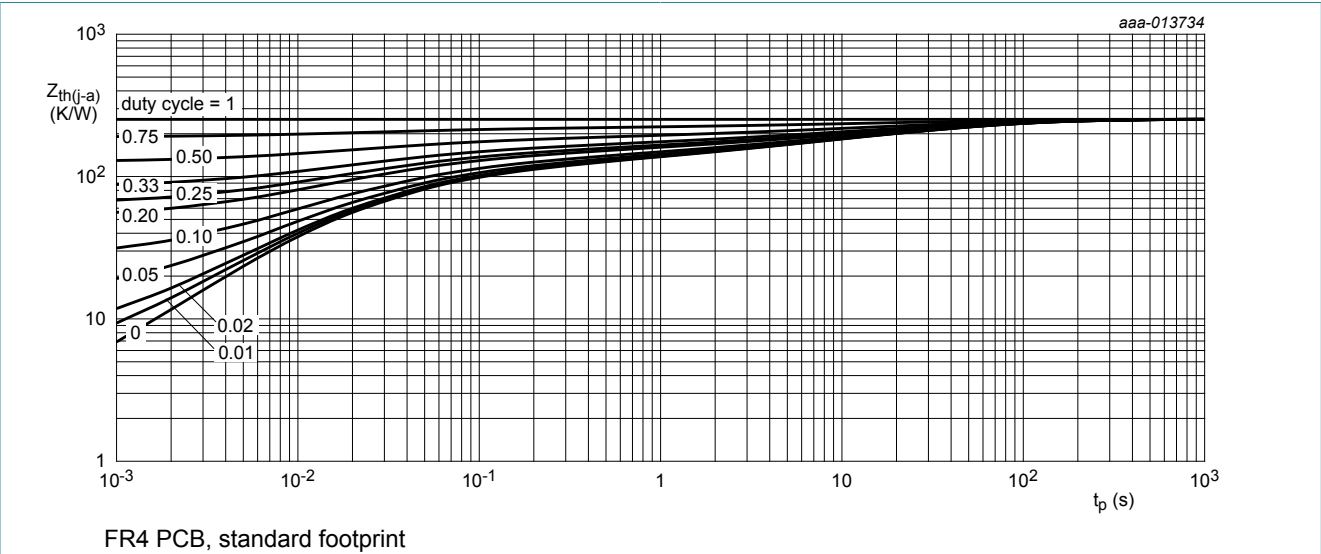


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

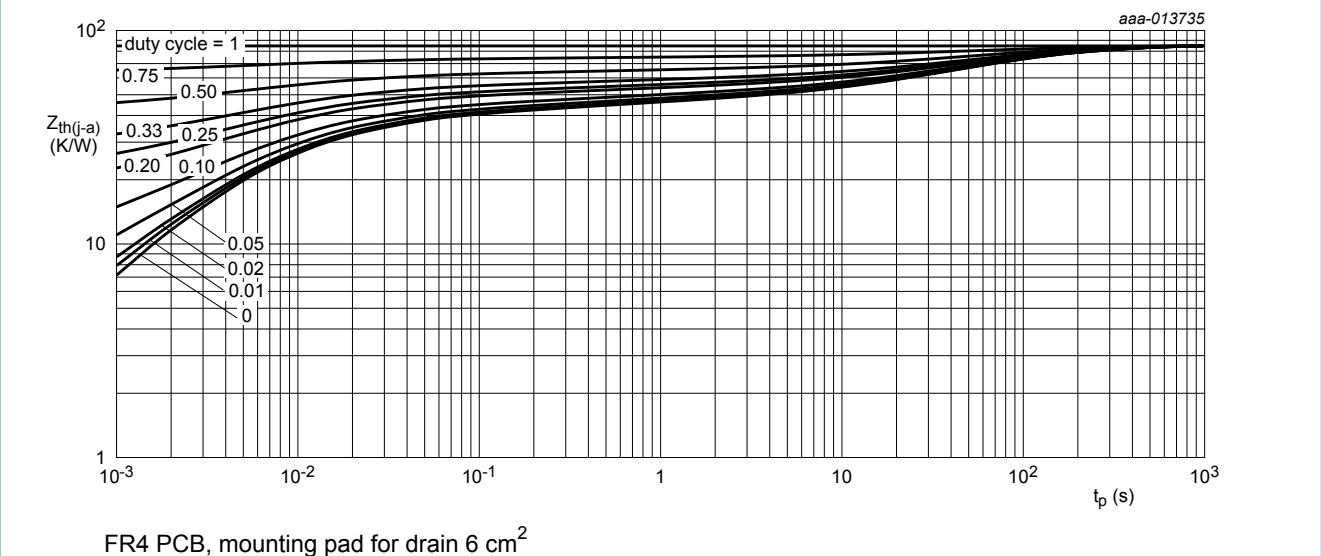


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	12	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250\ \mu A$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$	0.4	0.6	0.9	V
I_{DSS}	drain leakage current	$V_{DS} = 12\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	10	μA
		$V_{GS} = -8\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	-10	μA
		$V_{GS} = 4.5\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	5	μA
		$V_{GS} = -4.5\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	-5	μA
		$V_{GS} = 2.5\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	200	nA
		$V_{GS} = -2.5\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	-200	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 3\ A$; $T_j = 25\ ^\circ C$	-	57	67	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 3\ A$; $T_j = 150\ ^\circ C$	-	71	83	m Ω
		$V_{GS} = 2.5\ V$; $I_D = 3\ A$; $T_j = 25\ ^\circ C$	-	66	88	m Ω
		$V_{GS} = 1.8\ V$; $I_D = 1\ A$; $T_j = 25\ ^\circ C$	-	77	110	m Ω
		$V_{GS} = 1.5\ V$; $I_D = 0.1\ A$; $T_j = 25\ ^\circ C$	-	90	130	m Ω
g_{fs}	forward transconductance	$V_{DS} = 6\ V$; $I_D = 3\ A$; $T_j = 25\ ^\circ C$	-	17	-	S
R_G	gate resistance	$f = 1\ MHz$; $T_j = 25\ ^\circ C$	-	5.4	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 6\ V$; $I_D = 3\ A$; $V_{GS} = 4.5\ V$; $T_j = 25\ ^\circ C$	-	5.5	8.2	nC
Q_{GS}	gate-source charge		-	0.43	-	nC
Q_{GD}	gate-drain charge		-	1.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 6\ V$; $f = 1\ MHz$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	360	-	pF
C_{oss}	output capacitance		-	160	-	pF
C_{rss}	reverse transfer capacitance		-	140	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 6\ V$; $I_D = 3\ A$; $V_{GS} = 4.5\ V$; $R_{G(ext)} = 6\ \Omega$; $T_j = 25\ ^\circ C$	-	6.3	-	ns
t_r	rise time		-	24	-	ns
$t_{d(off)}$	turn-off delay time		-	27	-	ns
t_f	fall time		-	17	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.1\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	0.7	1.2	V

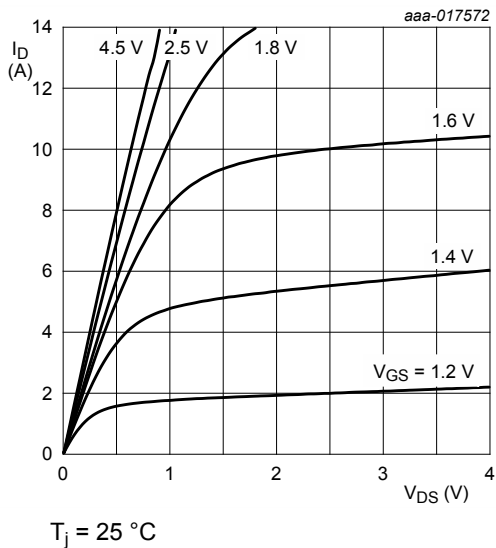


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

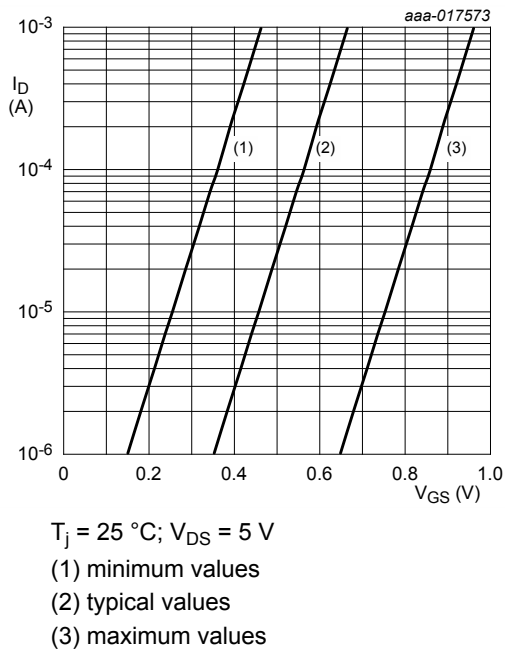


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

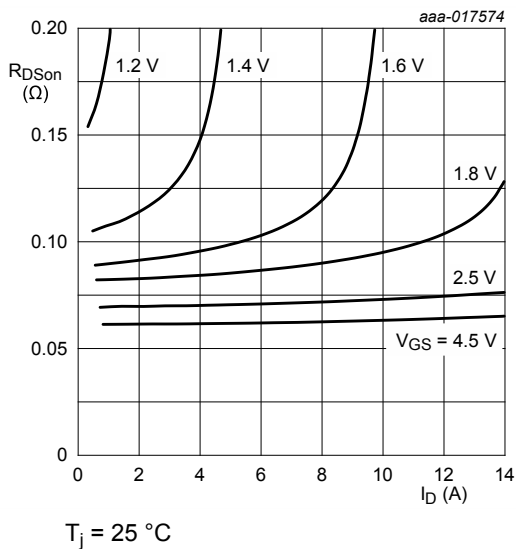


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

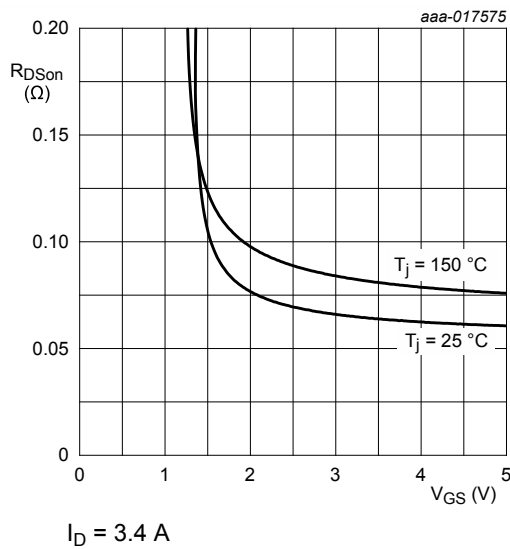


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

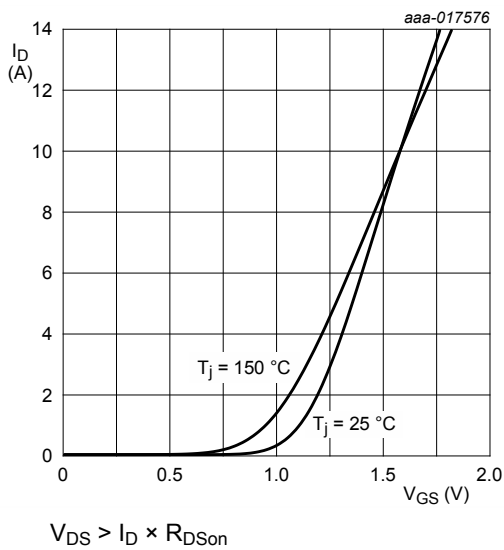


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

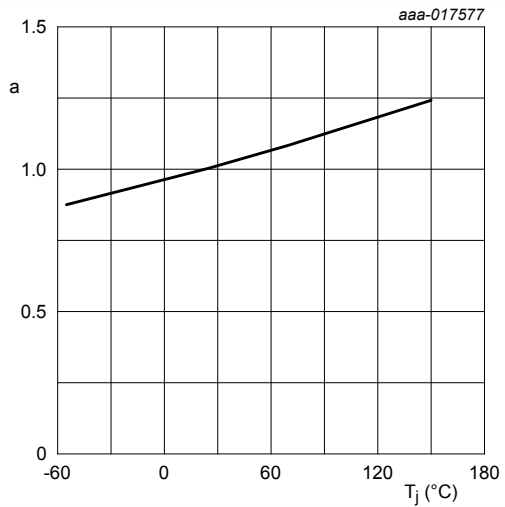
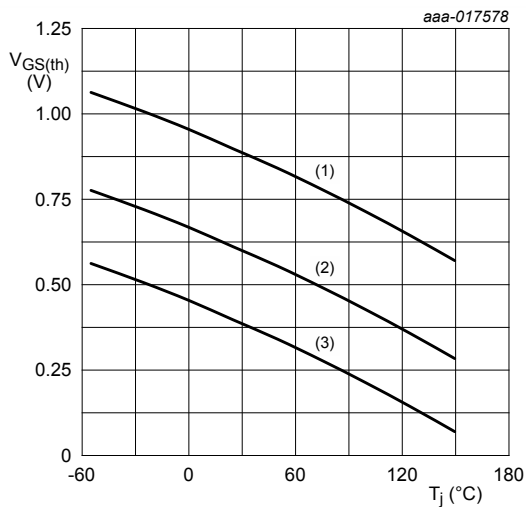


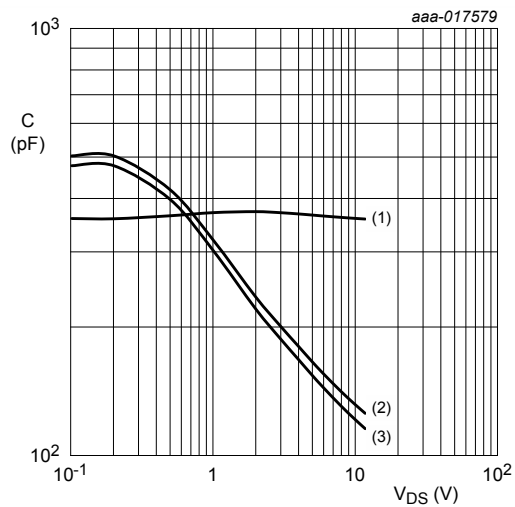
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$



$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$
(1) maximum values
(2) typical values
(3) minimum values

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
(1) C_{iss}
(2) C_{oss}
(3) C_{rss}

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

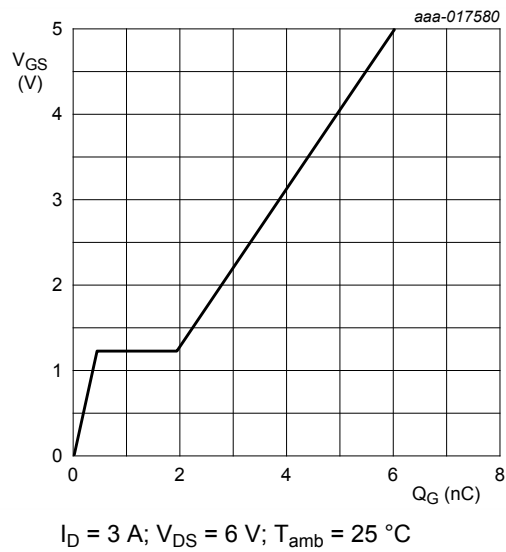


Fig. 15. Gate-source voltage as a function of gate charge; typical values

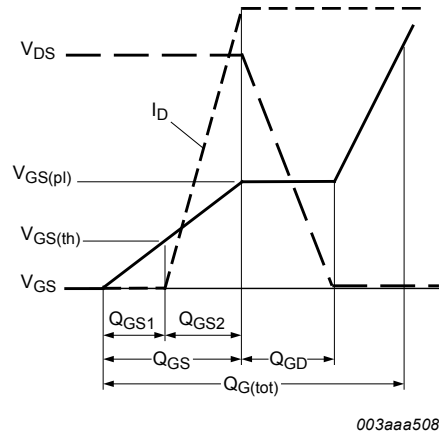


Fig. 16. MOSFET transistor: Gate charge waveform definitions

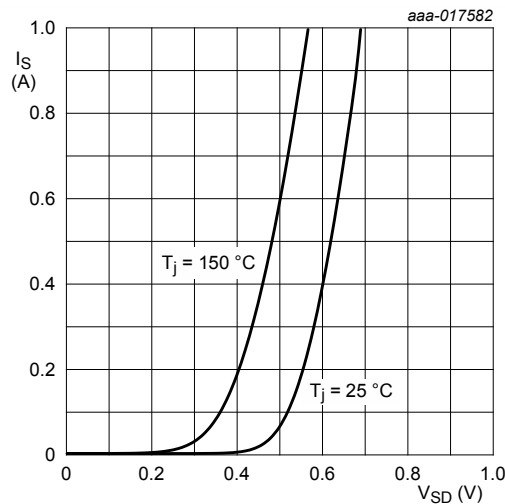


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

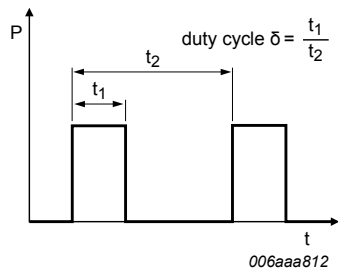


Fig. 18. Duty cycle definition

12. Package outline

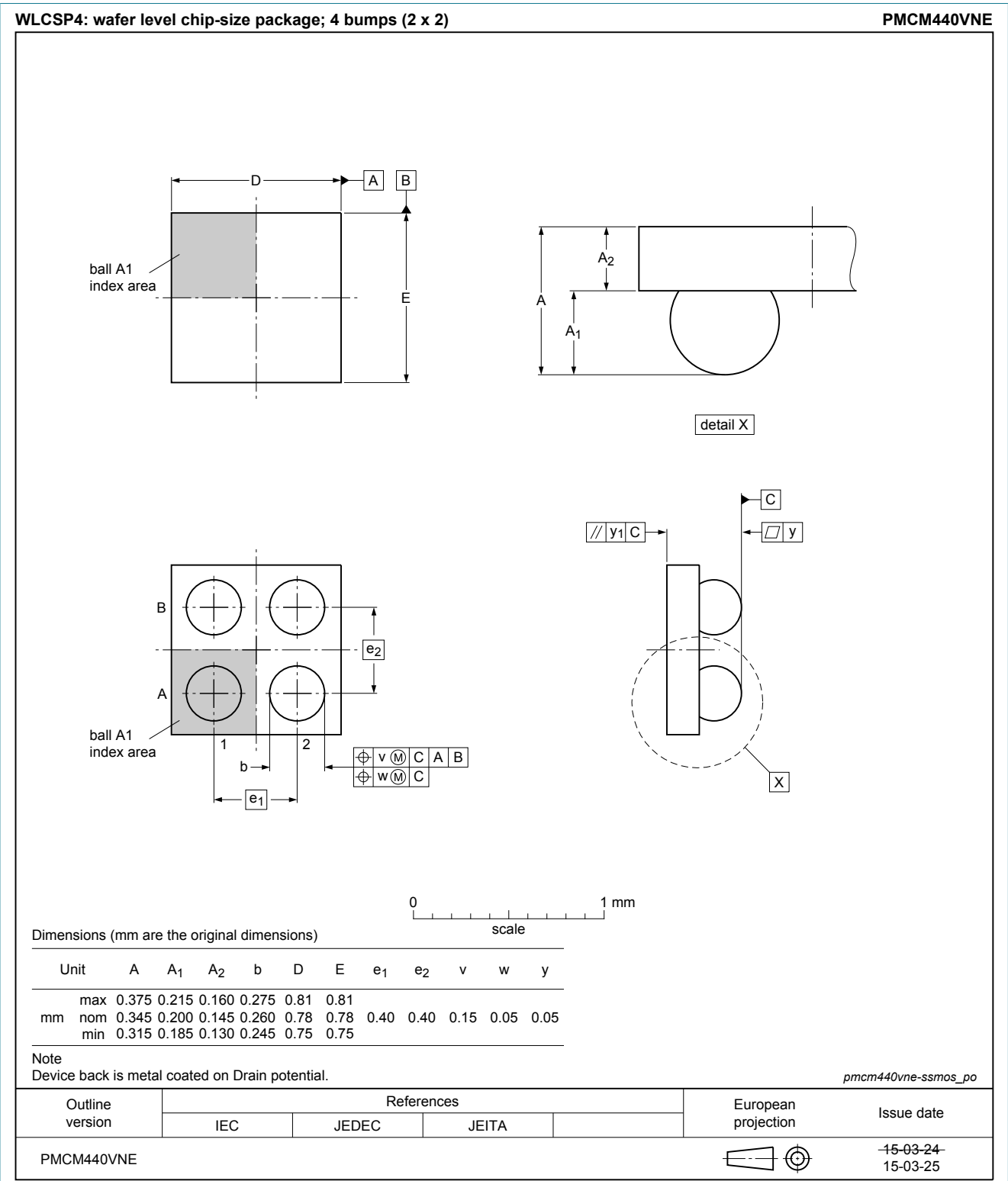
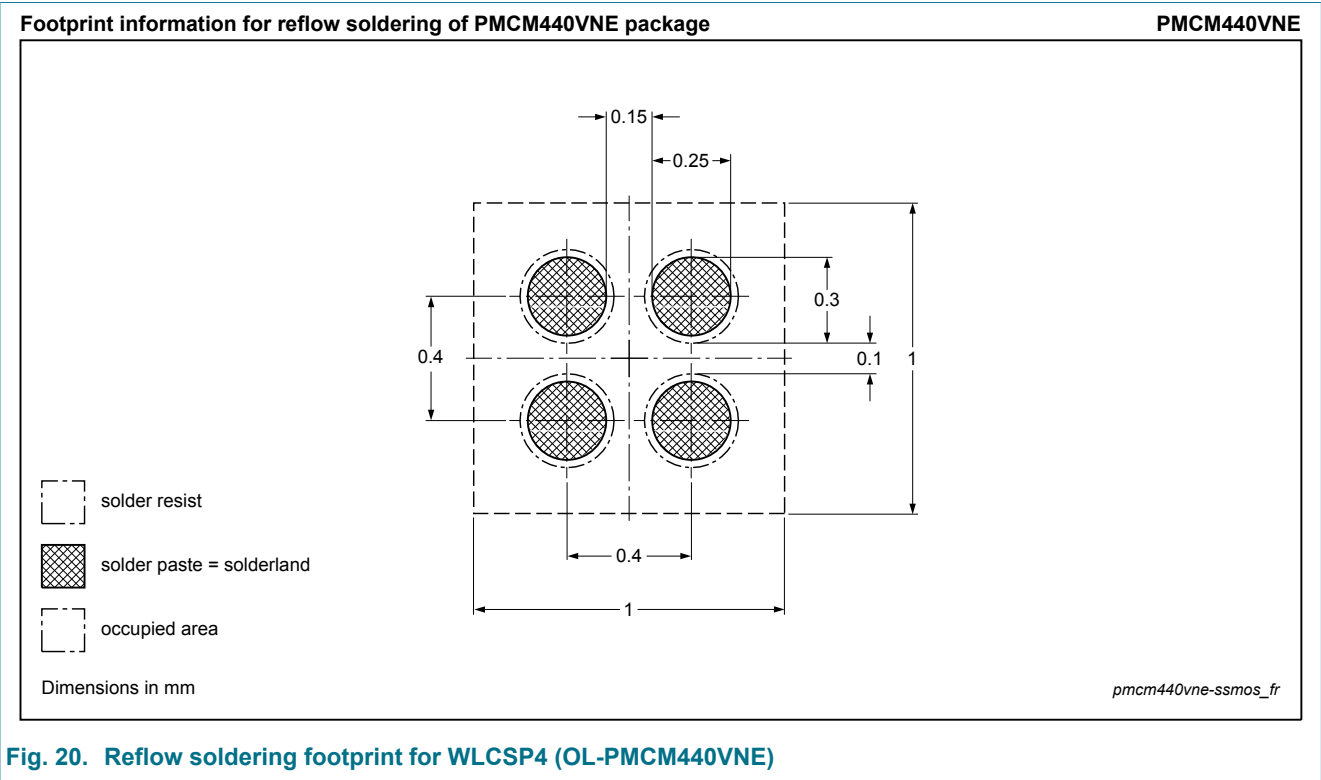


Fig. 19. Package outline WLCSP4 (OL-PMCM440VNE)

13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM440VNE v.1	20150407	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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