

# PM7830 BRIC

## Baseband Radio Interface Controller

Advance  
Product Brief

### PRODUCT OVERVIEW

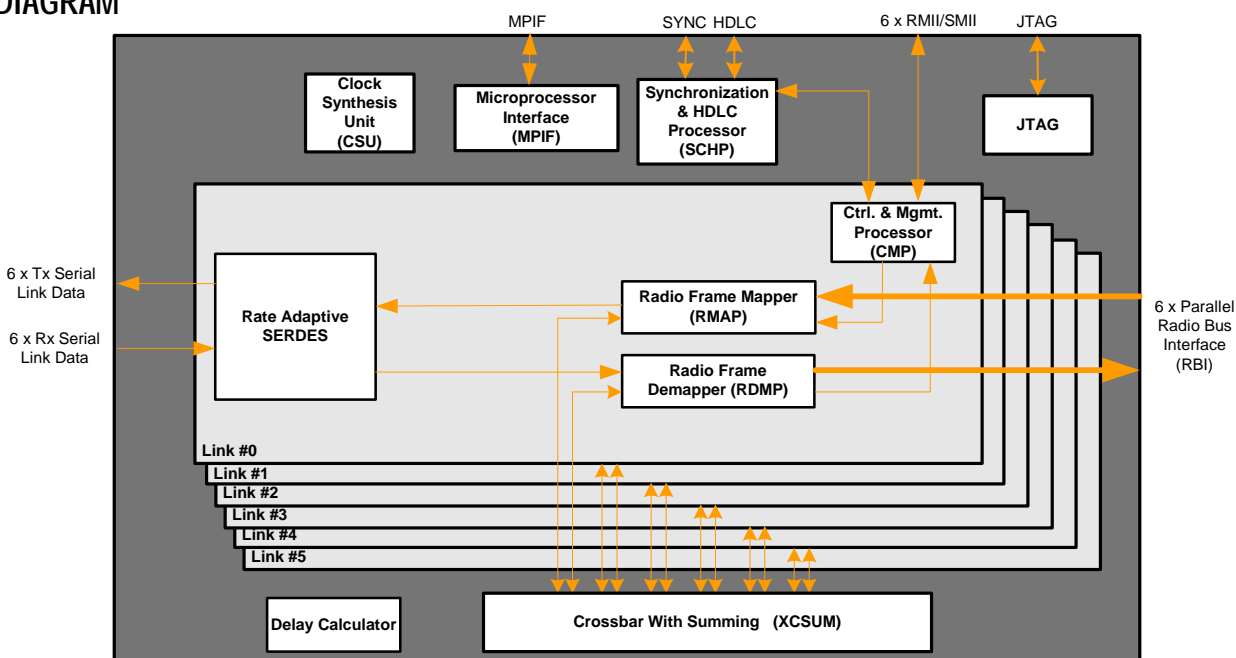
The PM7830 Baseband to Radio Interface Controller (BRIC) is a full-featured 6-port termination device that fully supports the CPRI specification for wireless base station interconnection. The BRIC provides integrated rate-adaptive SERDES links along with CPRI framing, mapping, switching, and combining functions.

When used in conjunction with the 2-port PM7832 BRIC-2, the BRIC and BRIC-2 can be used to flexibly create scalable CPRI-compliant distributed architectures.

### PRODUCT HIGHLIGHTS

- Operates in all of the following Baseband-to-RF interconnect topologies:
  - Local interconnect using a central combiner/distributor topology.
  - Local interconnect using a full mesh topology.
  - Remote interconnect using a point-to-point (P2P) star topology.
  - Remote interconnect using a tree and branch topology.
  - Remote interconnect using a chain topology.
  - Remote interconnect using a ring topology.
- Supports up to 6 serial channels running independently at CPRI line rates from 614.4 Mbit/s to 2457.6 Mbit/s with 8B/10B-encoded data.
- Supports up to 6 parallel Radio Bus Interfaces (RBIs) for output of user data.
- Supports CPRI start-up sequence and link-rate auto-negotiation for both REC and RE operating modes.
- Supports traffic switching at the CPRI Antenna Carrier (AxC) level.
- Supports IQ summing.
- Supports multiplexing and termination of control and synchronization sub-channels:
  - Up to 6 Ethernet Fast C&M channels.
  - Up to 6 HDLC Slow C&M channels.
- Measures round-trip delay on each CPRI link with an accuracy of  $\pm 1$  ns:
  - Provides programmable delay insertion to meet CPRI delay calibration requirements.
- Supports serial line protection switching.
- Supports configuration, control, monitoring and test capability on a per-channel basis.

### BLOCK DIAGRAM



## INTERFACES

- Line side high-speed serial outputs supporting simultaneous multiple CPRI line rates using a single reference clock input.
- System side parallel Radio Bus Interface (RBI) supporting parallel output of either:
  - Direct CPRI frame payload.
  - Unmapped IQ data to/from CPRI frame payload.
- 6-port RMII/SMII Ethernet interface for accessing Fast C&M channels.
- Multi-channel HDLC serial interface for accessing Slow C&M channels across all links.
- 16-bit microprocessor interface compatible with both Intel-like and Freescale-like processors.

## BENEFITS

- Provides all necessary functions for implementing CPRI-based Chain, Ring, Point-to-Point architectures, and more.
- Hitless protection switching, IQ summing, AxC switching & multicast functions enable single-device central switch/combiner architectures.

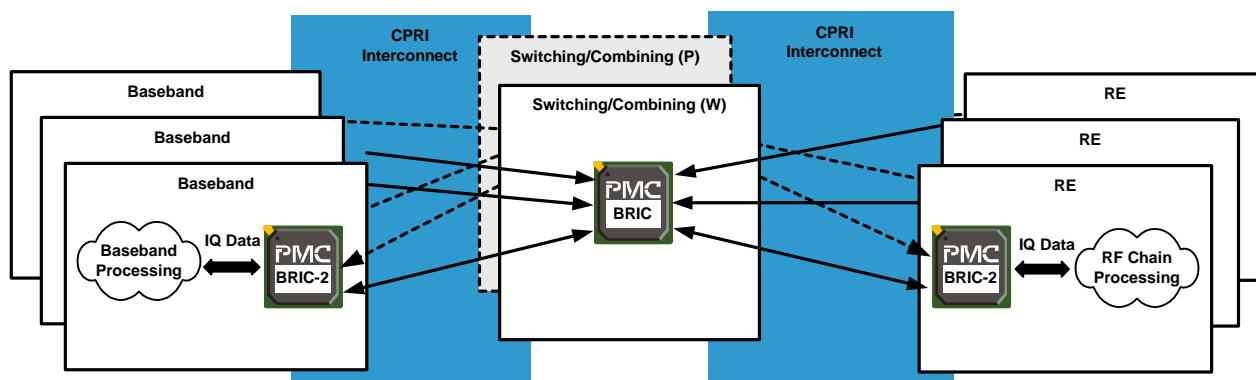
- Software-compatible BRIC and BRIC-2 allow complete CPRI solutions to be realized quickly and expanded as needed.
- Enables application-specific performance monitoring & OAM functions using in-band Ethernet/HDLC control & management sub-channels.
- Applicable for UMTS, CDMA, WiMAX solutions and beyond.
- Industry's most complete and low-risk solution with reuse from PM8358 QuadPHY 10GX SERDES and PM7831 BRIC-FP CPRI Framer.

## APPLICATIONS

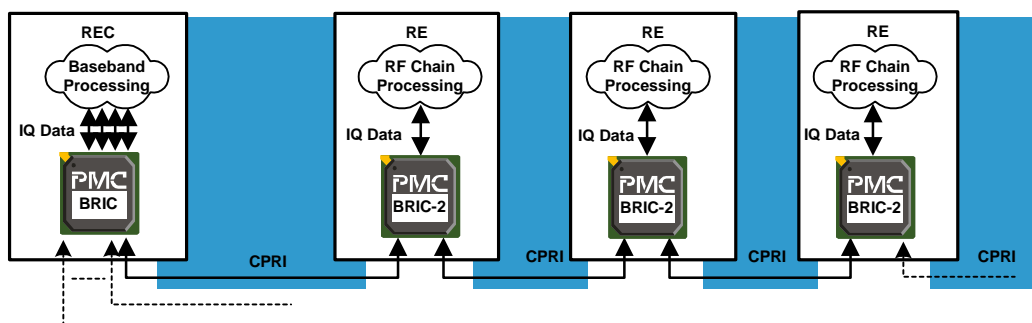
Two of the many possible architectural implementations using the BRIC and BRIC-2 are shown below:

- Central combiner-based CPRI architecture where the BRIC is used as a termination and switching device for the interconnect of BRIC-2-based REC and RE CPRI endpoints.
- Chain-based CPRI architecture where the BRIC is used to terminate one or more chains of remotely-located RE devices.

## CENTRAL COMBINER-BASED CPRI ARCHITECTURE



## CHAIN-BASED CPRI ARCHITECTURE



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