PhaseLink Laboratories, Inc.

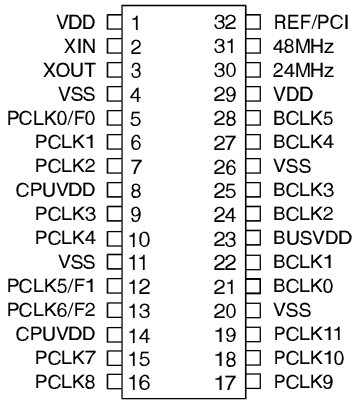
PLL52C61-23

Pentium/SDRAM Clock Generator for 2-DIMM

FEATURES

- Generates all clock frequencies for Pentium, AMD and Cyrix system requiring multiple CPU clocks (SDRAM, Shared memory architecture).
- Supports up to12 Synchronous CPU clocks.
- 6 PCI BUS clocks selectable between synchronous and asynchronous mode.
- One 14.318Mhz reference clock
- One 24Mhz floppy clock and one 48Mhz USB clock.
- Proven power-on strapping techniques to minimize four input pins. In any cases, no glitches will be produced from the output pins during power on.
- 3.3V and 5V operation.
- Available in 300mil 32 pin SOJ.

PIN INFORMATION



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DESCRIPTION

The PLL52C61-23 is a high performance system clock generator designed to support INTEL 430VX/TX PCIset motherboard with up to 2 DIMM Pentium based systems. All output clocks skew and jitter performance are designed to be fully compliant with INTEL Pentium CPU timing requirements.

TIMING SPECIFICATIONS

PCLK-PCLK skew	<250 ps
PCLK-BCLK skew	1~5 ns (PCLK leads)
PCLK,BCLK slew rate	> 1 V/ns (0.4 ~2.4V)
PCLK Jitter	±200 ps cycle-cycle

FREQUENCY SELECTION (MHz)

F2	F1	F0	PCLK (0:11)	BCLK(0:5)	
				PCI=1	PCI=0
0	0	0	50	25	32
0	0	1	60	30	32
0	1	0	66.6	33.3	32
0	1	1	Test	Test	Test
1	0	0	33	16.5	32
1	0	1	75	37.5	32
1	1	0	83.3	41.7	32
1	1	1	68.4	34.2	32

Note: F2,F1,F0 and PCI are selectable only during *Power-on*. They are HIGH by default and Low when 10K Ω pull-down is attached.

BLOCK DIAGRAM