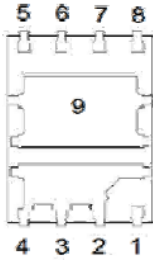
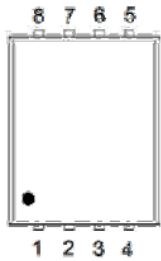


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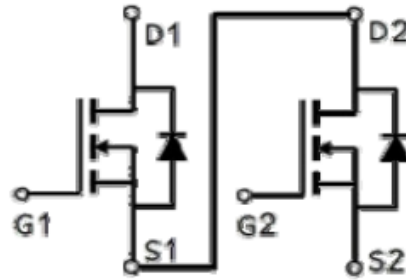
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D	CH.
30V	4.9mΩ @ $V_{GS} = 10V$	64A	Q2
30V	7.8mΩ @ $V_{GS} = 10V$	40A	Q1



1 : G1
2,3,4 : D1
5,6,7 : S2
8 : G2
9 : S1/D2

PDFN 5*6P



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ °C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	CH.	LIMITS	UNITS
Drain-Source Voltage		V _{DS}	Q2	30	V
			Q1	30	
Gate-Source Voltage		V _{GS}	Q2	±20	
			Q1	±20	
Continuous Drain Current ³	T _C = 25 °C	I _D	Q2	64	A
			Q1	40	
	T _C = 100 °C		Q2	40	
			Q1	25	
Pulsed Drain Current ¹		I _{DM}	Q2	150	
			Q1	90	
Continuous Drain Current	T _A = 25 °C	I _D	Q2	21	
			Q1	14	
	T _A = 70 °C		Q2	17	
			Q1	11	
Avalanche Current		I _{AS}	Q2	35	
			Q1	21	
Avalanche Energy	L = 0.1mH	E _{AS}	Q2	61	mJ
			Q1	22	
Power Dissipation	T _C = 25 °C	P _D	Q2	37	W
			Q1	24	
	T _C = 100 °C		Q2	15	
			Q1	9.6	

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Power Dissipation ⁴	T _A = 25 °C	P _D	Q2	4	W
	T _A = 70 °C		Q1	3.1	
			Q2	2.6	
			Q1	2	
Operating Junction & Storage Temperature Range		T _J , T _{STG}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	CH.	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$t \leq 10\text{s}$	$R_{\theta JA}$	Q2		30	$^{\circ}\text{C} / \text{W}$
			Q1		40	
	Steady-State	$R_{\theta JA}$	Q2		56	
			Q1		72	
Junction-to-Case		$R_{\theta JC}$	Q2		3.3	
			Q1		5.2	

¹Pulse width limited by maximum junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design.

³Package limitation current :Q1=25A,Q2=25A.

⁴The Power dissipation is based on $R_{\theta JA}$ $t \leq 10\text{s}$ value.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	CH.	LIMITS			UNITS
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 1mA$	Q2	30			V
		$V_{GS} = 0V, I_D = 250\mu A$	Q1	30			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	Q2	1.3	1.6	2.3	V
			Q1	1.27	1.36	2.3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q2			± 100	nA
			Q1			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$	Q2			0.5	mA
			Q1			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55^\circ C$	Q2			5	mA
			Q1			10	μA
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 16A$	Q2		3.4	5.1	m Ω
		$V_{GS} = 4.5V, I_D = 11A$	Q1		6.8	11	
		$V_{GS} = 10V, I_D = 20A$	Q2		2.7	4.9	
		$V_{GS} = 10V, I_D = 11A$	Q1		5.3	7.8	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$	Q2		70		S
		$V_{DS} = 5V, I_D = 11A$	Q1		66		

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DYNAMIC									
Input Capacitance	C _{iss}		V _{GS} = 0V, V _{DS} = 15V, f = 1MHz	Q2		2148		pF	
				Q1		853			
Output Capacitance	C _{oss}			Q2		402			
				Q1		149			
Reverse Transfer Capacitance	C _{rss}			Q2		255			
				Q1		109			
Gate Resistance	R _g		V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	Q2		1.6		Ω	
				Q1		0.8			
Total Gate Charge ²	Q _g	V _{GS} =10V	Q2 V _{DS} = 15V , V _{GS} = 10V, I _D = 20A Q1 V _{DS} = 15V , V _{GS} = 10V, I _D = 11A	Q2		44		nC	
				Q1		18			
		V _{GS} =4.5V		Q2		10.7			
				Q1		10			
Gate-Source Charge ²	Q _{gs}				Q2		5.4		
					Q1		2.1		
Gate-Drain Charge ²	Q _{gd}				Q2		11		
					Q1		4.8		
Turn-On Delay Time ²	t _{d(on)}		Q2 V _{DS} = 15V,I _D ≅ 20A, V _{GS} =10V, R _{GEN} = 6Ω Q1 V _{DS} = 15V ,I _D ≅ 11A, V _{GS} = 10V, R _{GEN} =6Ω	Q2		30		nS	
				Q1		25			
Rise Time ²	t _r			Q2		20			
				Q1		21			
Turn-Off Delay Time ²	t _{d(off)}			Q2		61			
				Q1		40			
Fall Time ²	t _f			Q2		22			
				Q1		20			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _j = 25 °C)									
Continuous Current ³	I _S			Q2			37	A	
				Q1			20		
Forward Voltage ¹	V _{SD}		I _F = 20A, V _{GS} = 0V	Q2			1	V	
			I _F = 11A, V _{GS} = 0V	Q1			1.2		
Reverse Recovery Time	t _{rr}		Q2 I _F = 20A, dl _F /dt = 100A /μS	Q2		21		nS	
				Q1		13.5			
Reverse Recovery Charge	Q _{rr}		Q1 I _F = 11A, dl _F /dt = 100A /μS	Q2		6.5		nC	
				Q1		4			

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

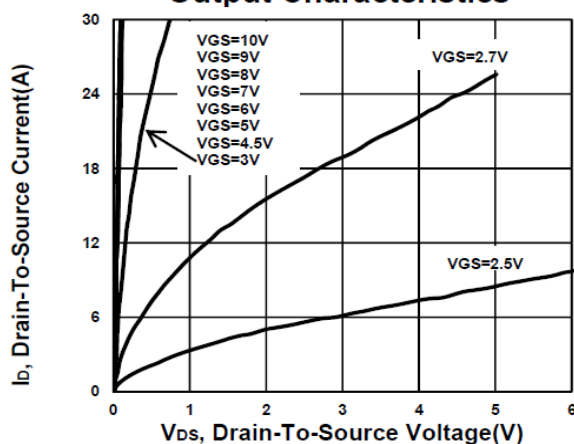
³Package limitation current :Q1=25A,Q2=25A.

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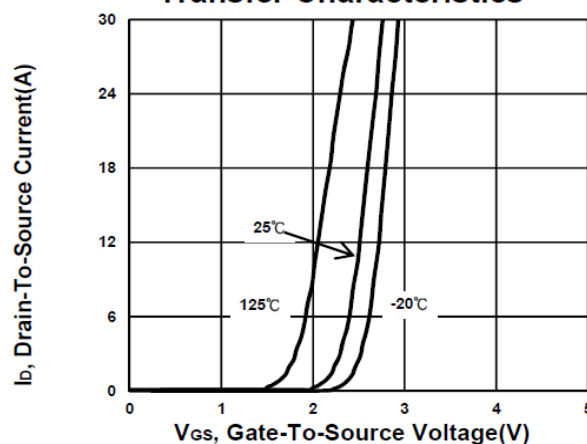
Dual N-Channel Enhancement Mode MOSFET

Q2

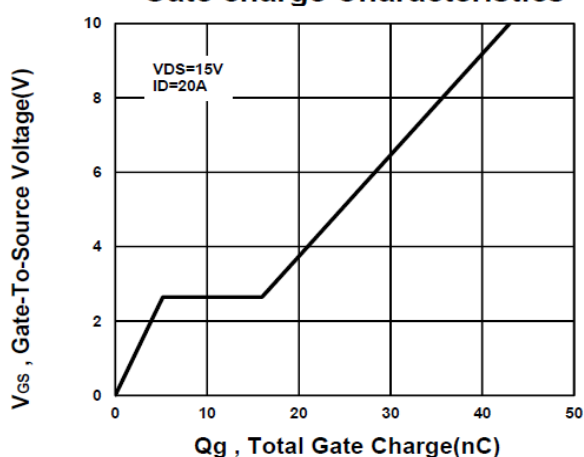
Output Characteristics



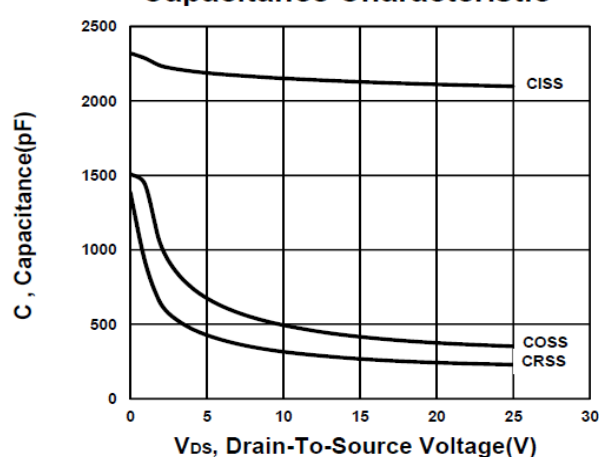
Transfer Characteristics



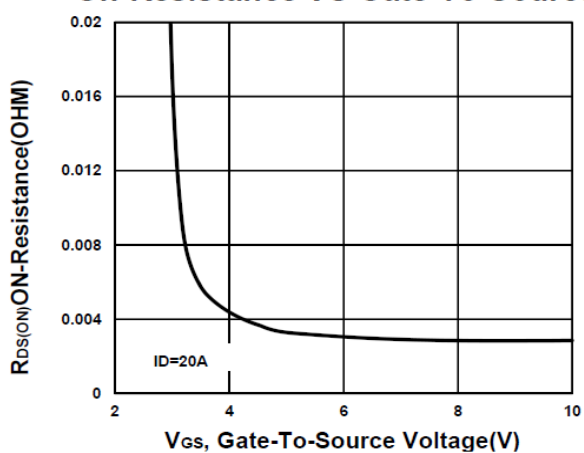
Gate charge Characteristics



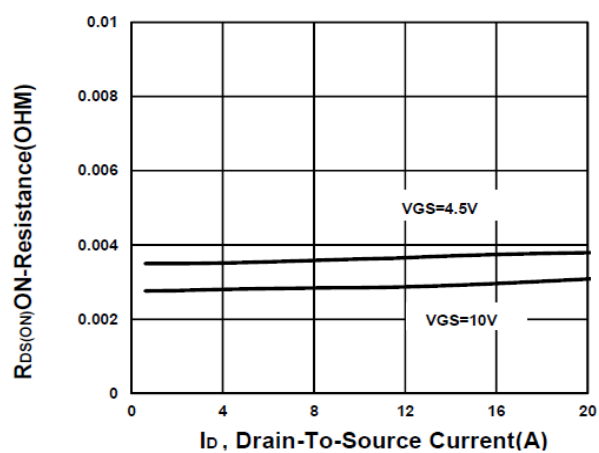
Capacitance Characteristic



On-Resistance VS Gate-To-Source



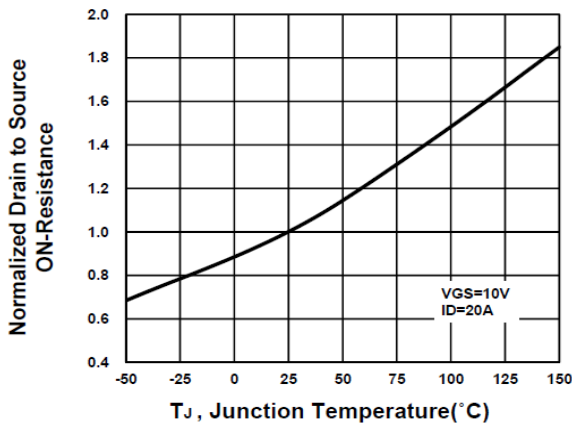
On-Resistance VS Drain Current



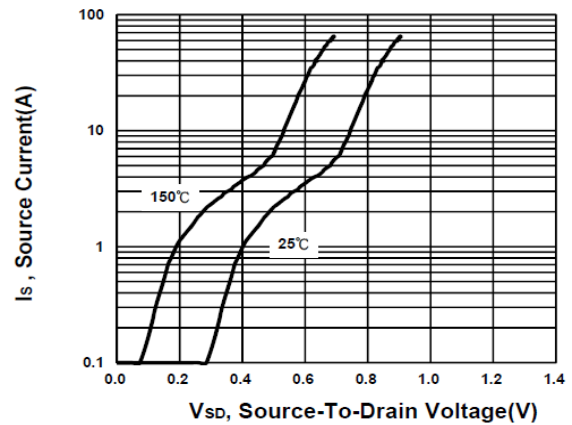
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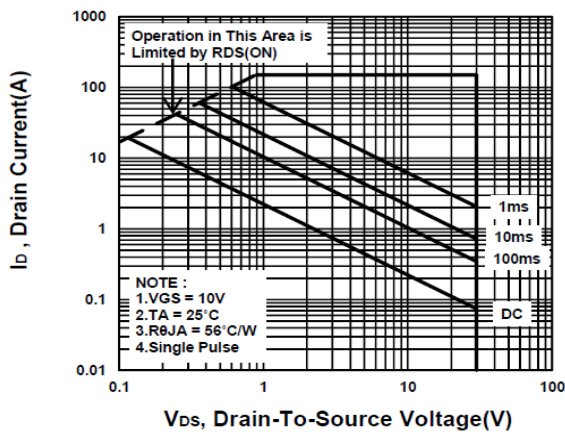
On-Resistance VS Temperature



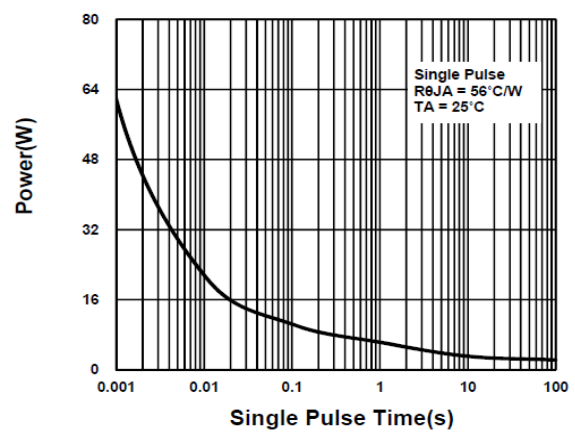
Source-Drain Diode Forward Voltage



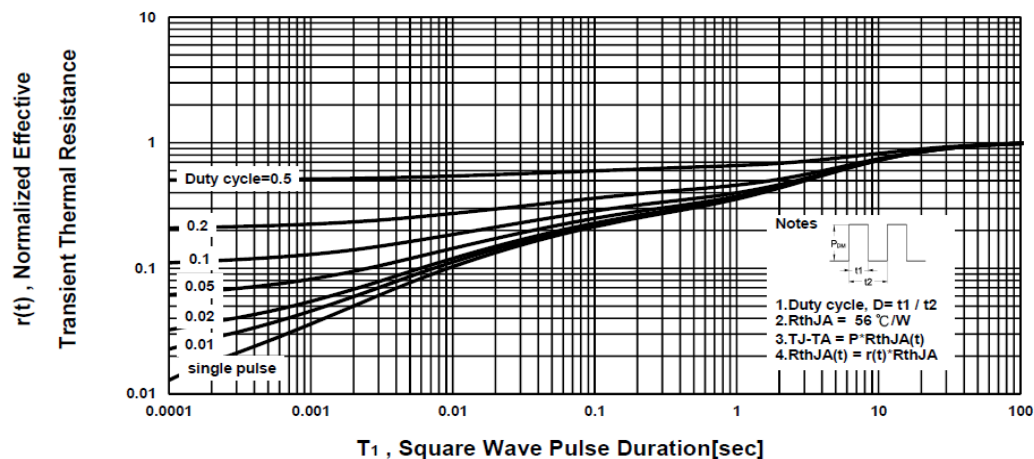
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

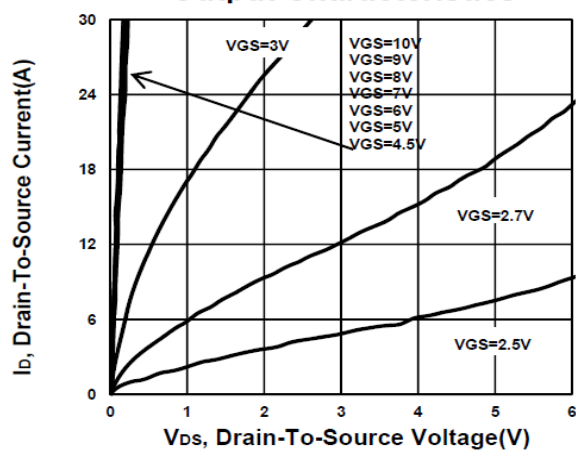


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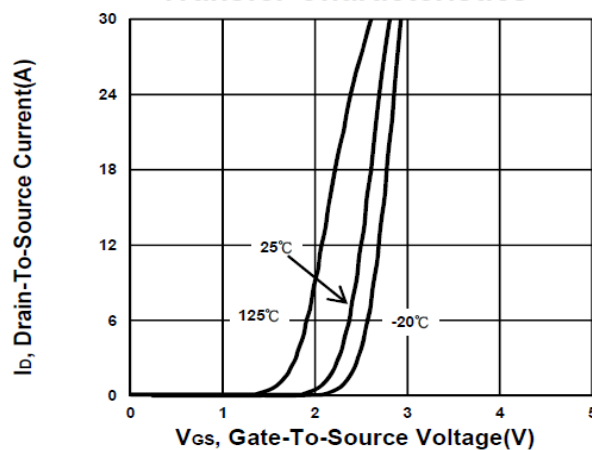
Dual N-Channel Enhancement Mode MOSFET

Q1

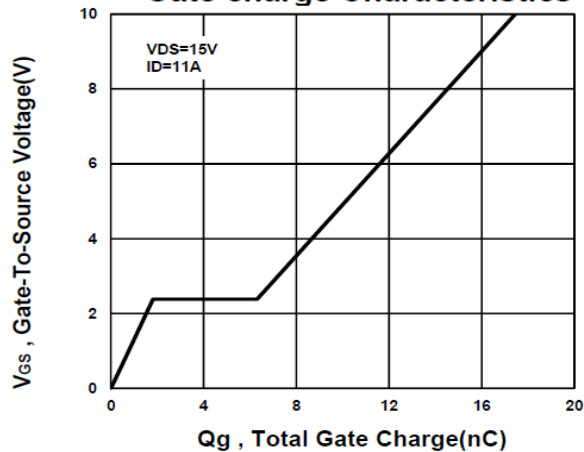
Output Characteristics



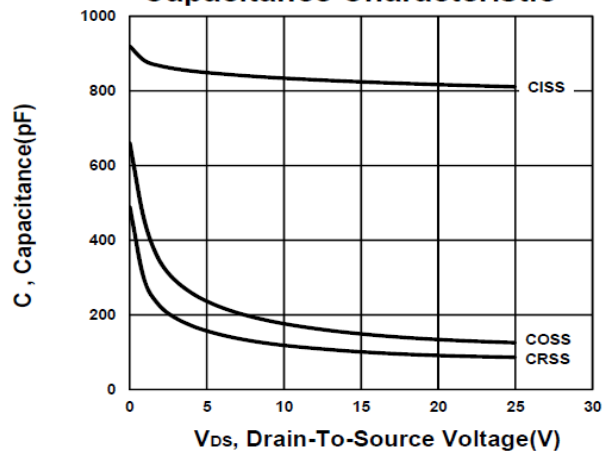
Transfer Characteristics



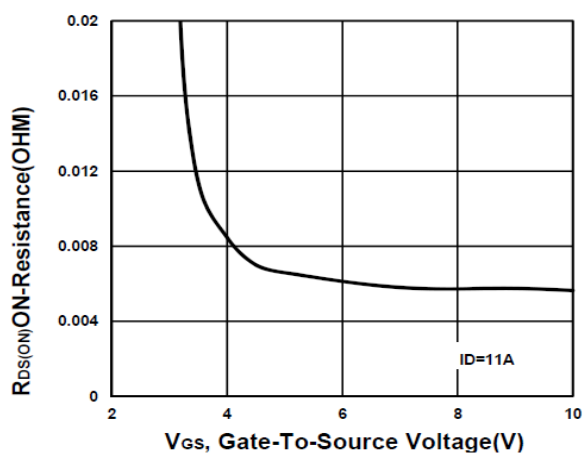
Gate charge Characteristics



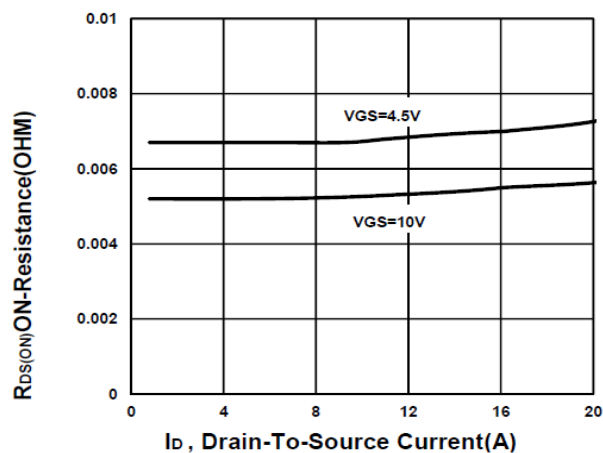
Capacitance Characteristic



On-Resistance VS Gate-To-Source



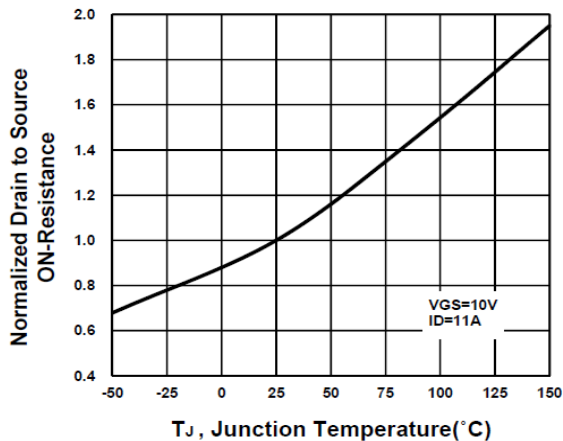
On-Resistance VS Drain Current



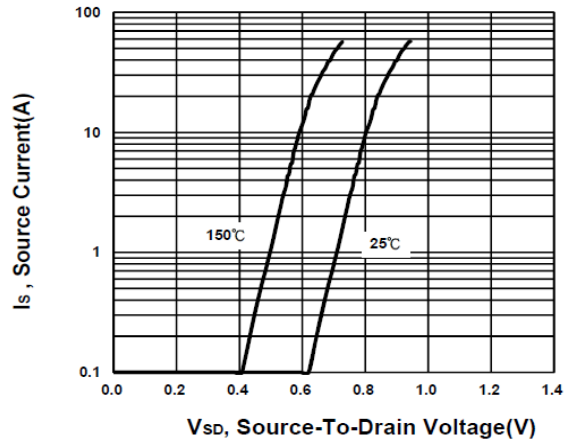
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Dual N-Channel Enhancement Mode MOSFET

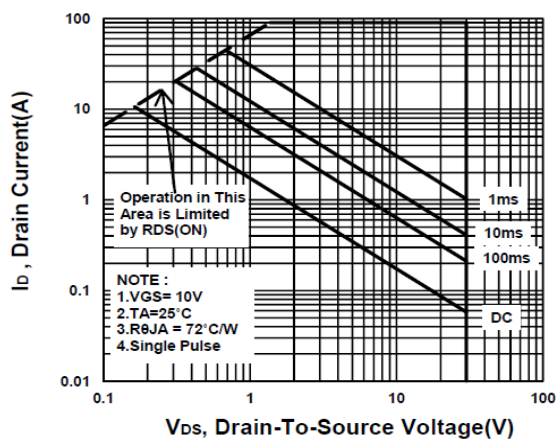
On-Resistance VS Temperature



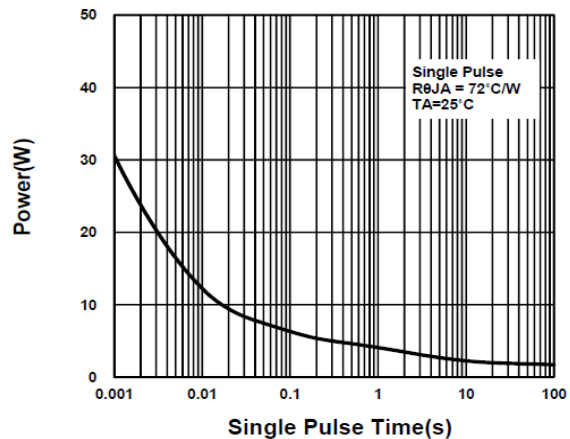
Source-Drain Diode Forward Voltage



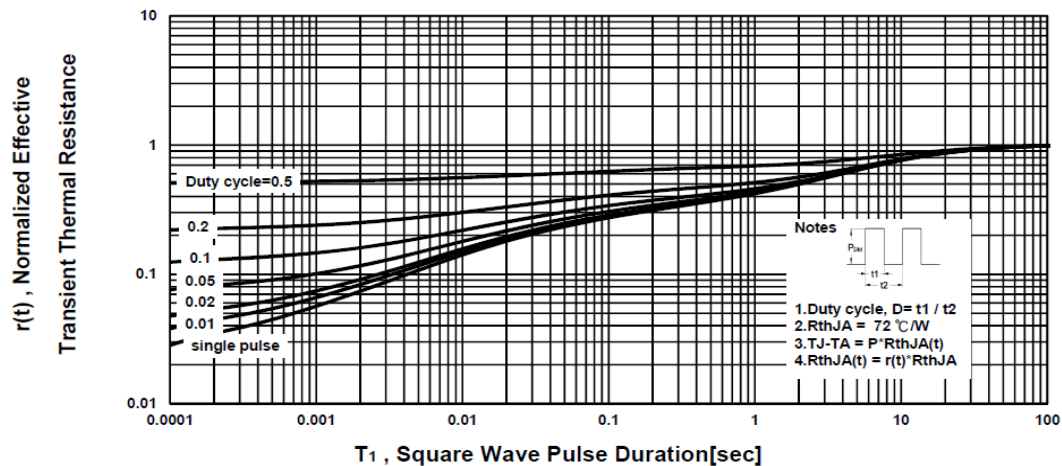
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



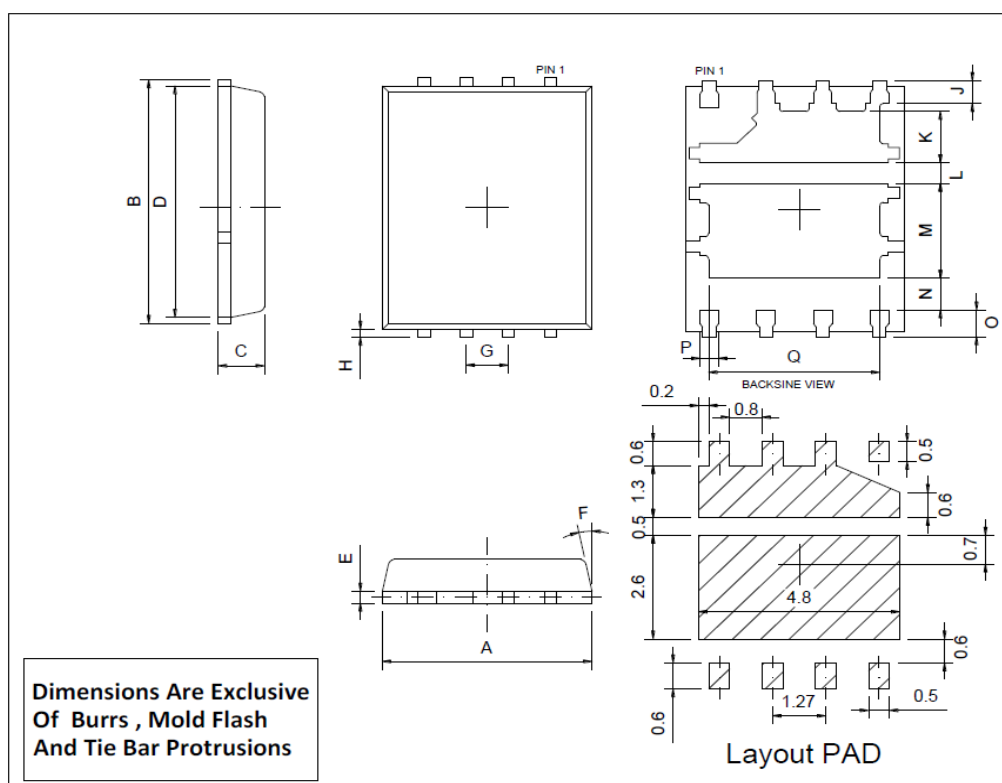
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Dual N-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P(上下 Dual) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	5	5.4	K	0.82	1.06	1.3
B	5.9	6.15	6.35	L	0.4	0.5	0.6
C	0.9	1	1.18	M	2.0	2.21	2.42
D	5.42	5.59	5.85	N	0.5	1	
E	0.15	0.25	0.35	O	0.42	0.56	0.71
F	0°	6°	12°	P	0.3	0.4	0.51
G	1.17	1.27	1.37	Q	3.61	4.05	4.5
H	0.06	0.21	0.36				
J	0.41	0.55	0.7				

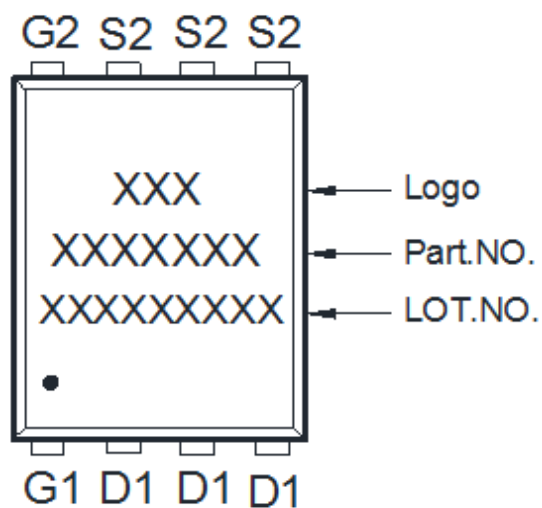


* 散热片形状会因为封装厂框架不同而有所差异。

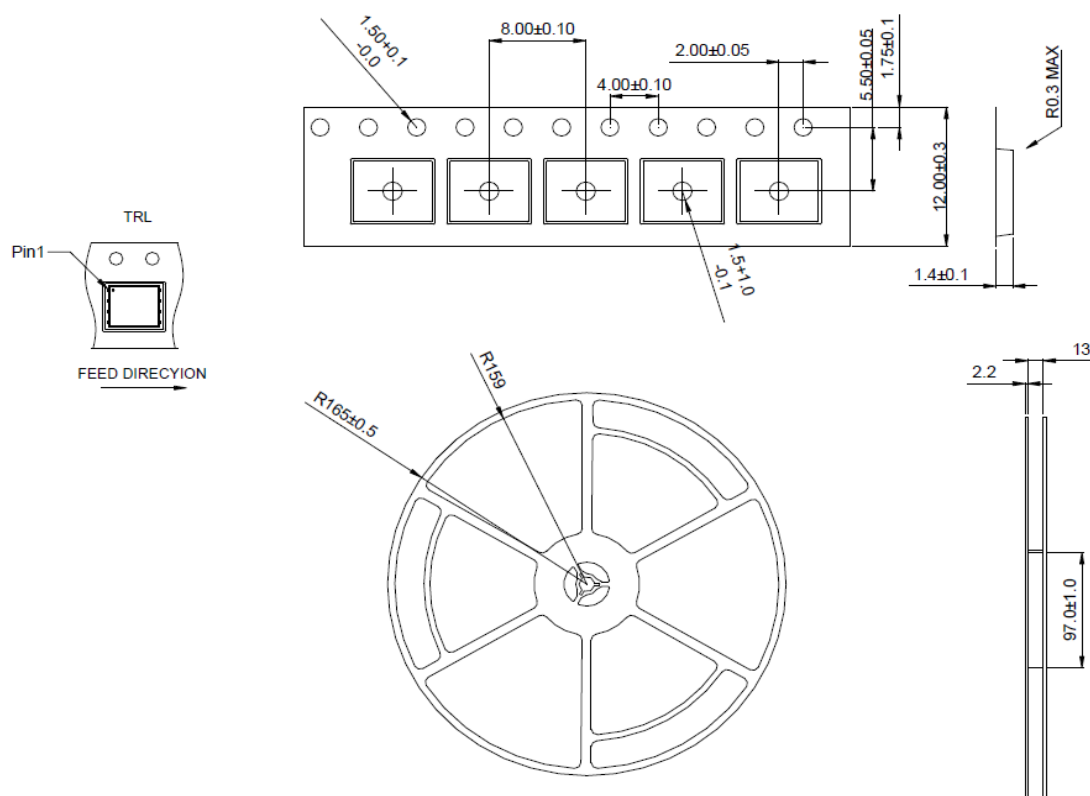
PK630HY

Dual N-Channel Enhancement Mode MOSFET

A. Marking Information



B. Tape&Reel Information:3000pcs/Reel

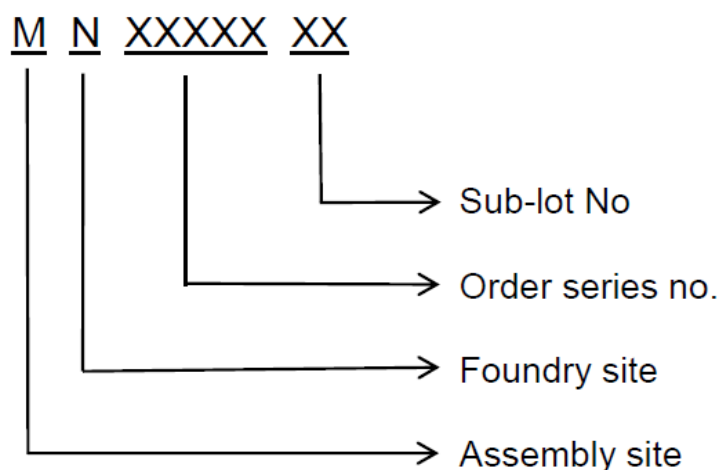


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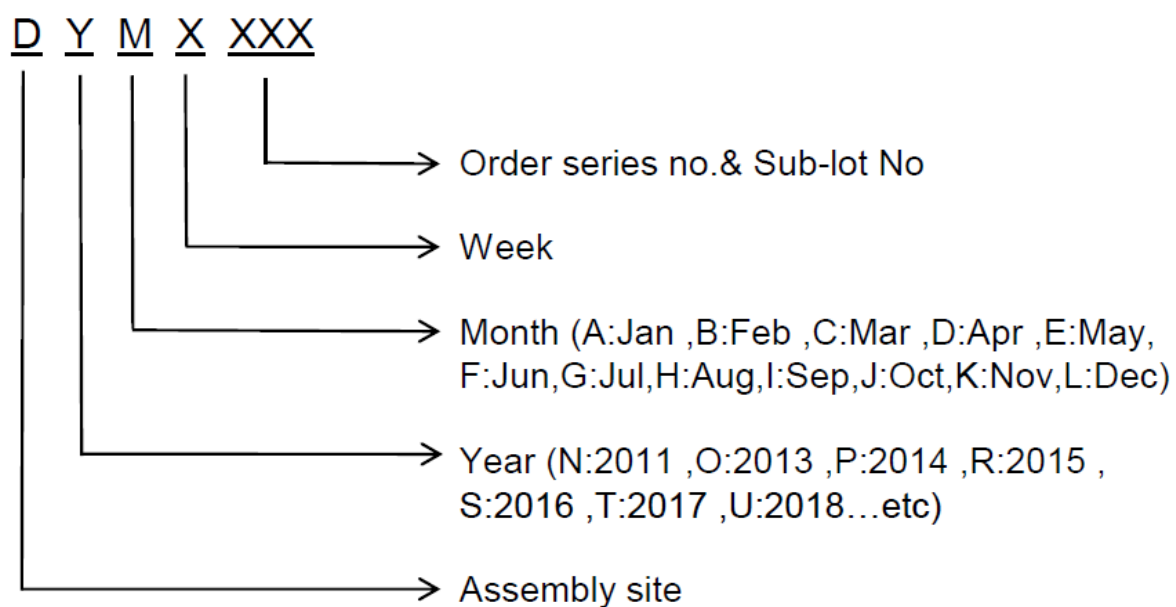
Dual N-Channel Enhancement Mode MOSFET

C. Lot No.&Date Code rule

1.Lot No.



2.Date Code



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Dual N-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G"和"Q"的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert " / " between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least