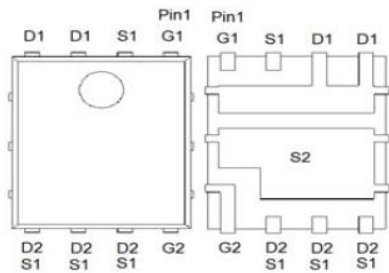


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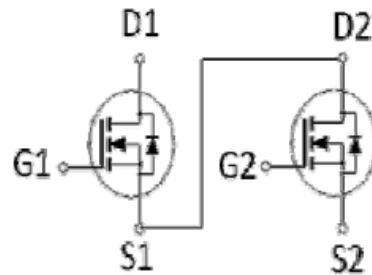
Dual N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D	CH.
30V	1.2m Ω @ $V_{GS} = 10V$	127A	Q2
30V	6.5m Ω @ $V_{GS} = 10V$	43A	Q1



PDFN 5*6P



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	CH.	LIMITS	UNITS
Drain-Source Voltage		V _{DS}	Q2	30	V
			Q1	30	
Gate-Source Voltage		V _{GS}	Q2	±20	
			Q1	±20	
Continuous Drain Current ³	T _C = 25 °C	I _D	Q2	127	A
	T _C = 100 °C		Q1	43	
			Q2	80	
			Q1	27	
Pulsed Drain Current ¹		I _{DM}	Q2	160	
			Q1	100	
Continuous Drain Current	T _A = 25 °C	I _D	Q2	32	
	T _A = 70 °C		Q1	11	
			Q2	25	
			Q1	9.4	
Avalanche Current		I _{AS}	Q2	68.6	
			Q1	25	
Avalanche Energy	L = 0.1mH	E _{AS}	Q2	235	mJ
			Q1	31	
Power Dissipation	T _C = 25 °C	P _D	Q2	39	W
	T _C = 100 °C		Q1	24	
			Q2	15	
			Q1	9.8	

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Dual N-Channel Enhancement Mode MOSFET

Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	Q2	2.5	W
			Q1	1.7	
	$T_A = 70\text{ }^{\circ}\text{C}$		Q2	1.6	
			Q1	1.1	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	CH.	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$	Q2		50	$^{\circ}\text{C} / \text{W}$
		Q1		70	
Junction-to-Case	$R_{\theta JC}$	Q2		3.2	
		Q1		5.1	

¹Pulse width limited by maximum junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design.

³Package limitation current :Q1=35A,Q2=35A.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	CH.	LIMITS			UNITS
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	Q2	30			V
			Q1	30			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	Q2	1.3	1.8	2.3	
			Q1	1.3	1.6	2.3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q2			± 100	nA
			Q1			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$	Q2			1	μA
			Q1			1	
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55\text{ }^{\circ}C$	Q2			10	
			Q1			10	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 16A$	Q2		1.2	1.6	mΩ
		$V_{GS} = 4.5V, I_D = 11A$	Q1		6	9.5	
		$V_{GS} = 10V, I_D = 20A$	Q2		0.85	1.2	
		$V_{GS} = 10V, I_D = 11A$	Q1		4.3	6.5	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$	Q2		68		S
		$V_{DS} = 5V, I_D = 11A$	Q1		50		

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Dual N-Channel Enhancement Mode MOSFET

DYNAMIC									
Input Capacitance	C _{iss}		V _{GS} = 0V, V _{DS} = 15V, f = 1MHz	Q2		4056		pF	
				Q1		888			
Output Capacitance	C _{oss}			Q2		782			
				Q1		171			
Reverse Transfer Capacitance	C _{rss}			Q2		456			
				Q1		99			
Gate Resistance	R _g		V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	Q2		1		Ω	
				Q1		1.1			
Total Gate Charge ²	Q _g	V _{GS} =10V	Q2 V _{DS} = 15V , V _{GS} = 10V, I _D = 20A Q1 V _{DS} = 15V , V _{GS} = 10V, I _D = 11A	Q2		81		nC	
				Q1		17.3			
		V _{GS} =4.5V		Q2		43			
Gate-Source Charge ²	Q _{gs}	Q1			9.3				
		Q2			12				
Gate-Drain Charge ²	Q _{gd}	Q1			2.5				
		Q2			19				
		Q1			4.7				
Turn-On Delay Time ²	t _{d(on)}			Q2 V _{DS} = 15V,I _D ≅ 20A, V _{GS} =10V, R _{GEN} = 6Ω Q1 V _{DS} = 15V ,I _D ≅ 11A, V _{GS} = 10V, R _{GEN} =6Ω	Q2		30		
		Q1			21				
Rise Time ²	t _r		Q2			19			
			Q1			15			
Turn-Off Delay Time ²	t _{d(off)}		Q2			61			
			Q1			46			
Fall Time ²	t _f		Q2			21			
			Q1			15			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _J = 25 °C)									
Continuous Current ³	I _S			Q2			39	A	
				Q1			20		
Forward Voltage ¹	V _{SD}		I _F = 20A, V _{GS} = 0V	Q2			1	V	
			I _F = 11A, V _{GS} = 0V	Q1			1.2		
Reverse Recovery Time	t _{rr}		Q2 I _F = 20A, dI _F /dt = 100A /μS	Q2		28		nS	
				Q1		8.2			
Reverse Recovery Charge	Q _{rr}		Q1 I _F = 11A, dI _F /dt = 100A /μS	Q2		15		nC	
				Q1		1.3			

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

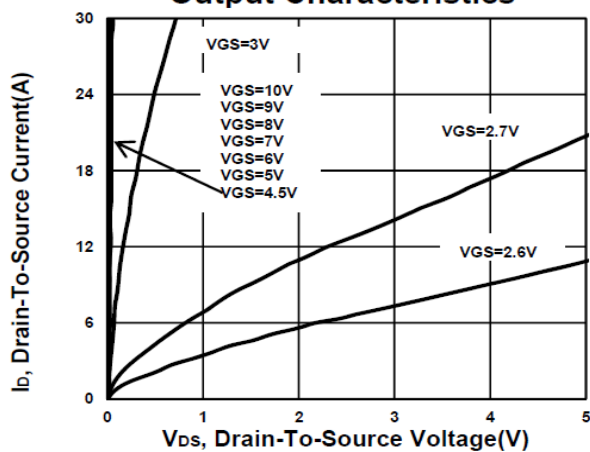
³Package limitation current :Q1=35A,Q2=35A.

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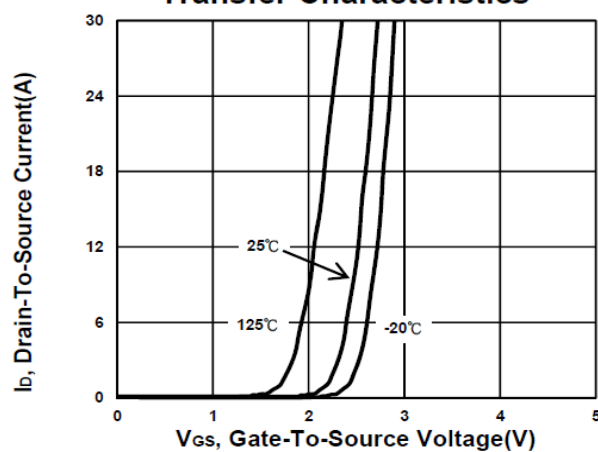
Dual N-Channel Enhancement Mode MOSFET

Q2

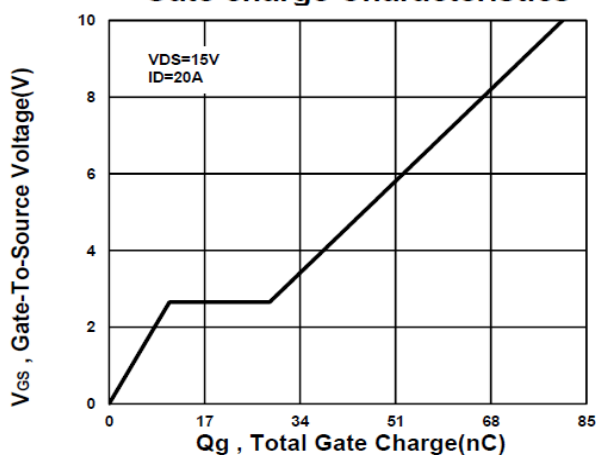
Output Characteristics



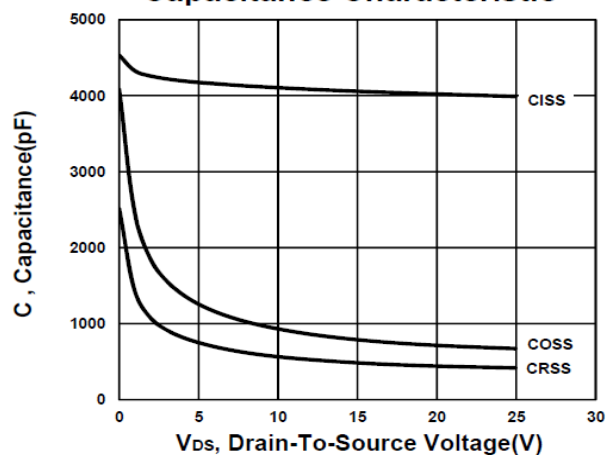
Transfer Characteristics



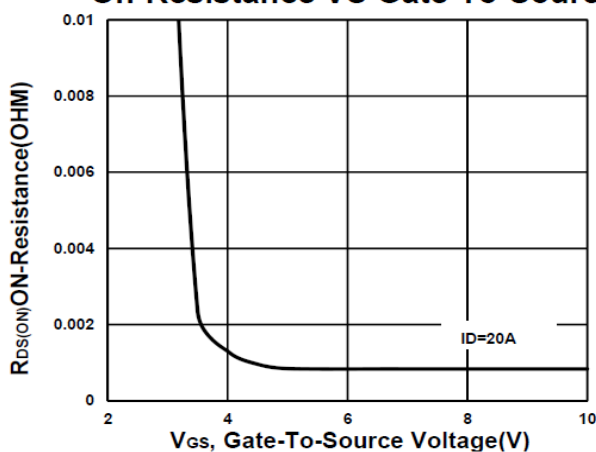
Gate charge Characteristics



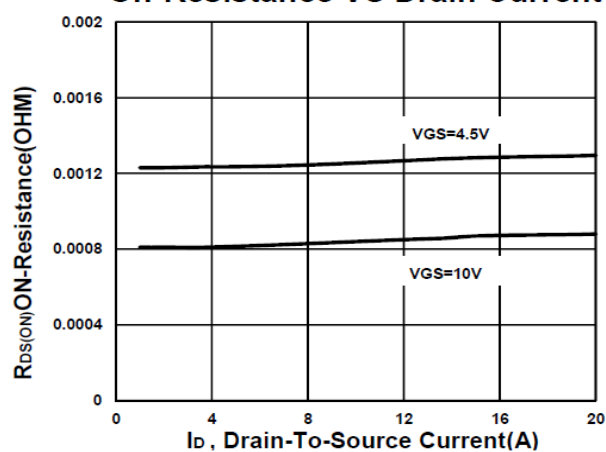
Capacitance Characteristic



On-Resistance VS Gate-To-Source



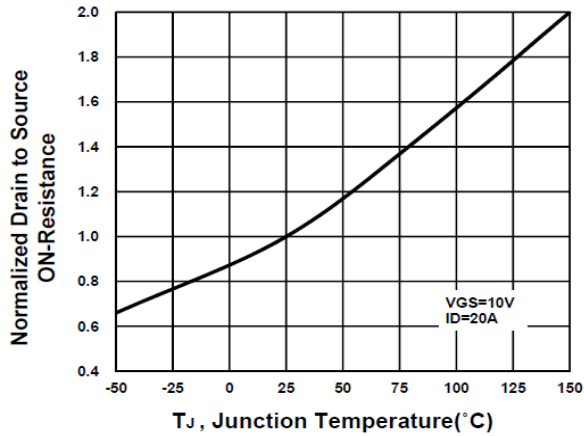
On-Resistance VS Drain Current



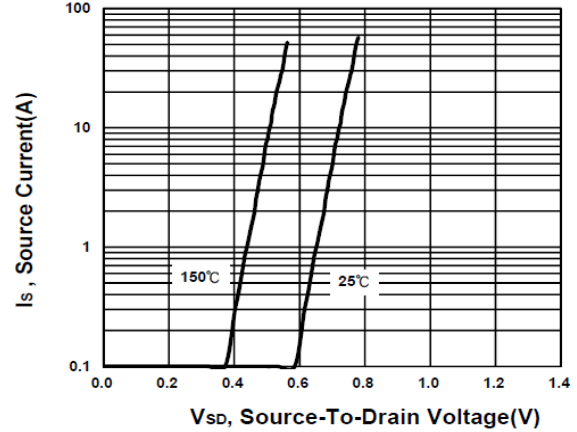
PK610DZ

Dual N-Channel Enhancement Mode MOSFET

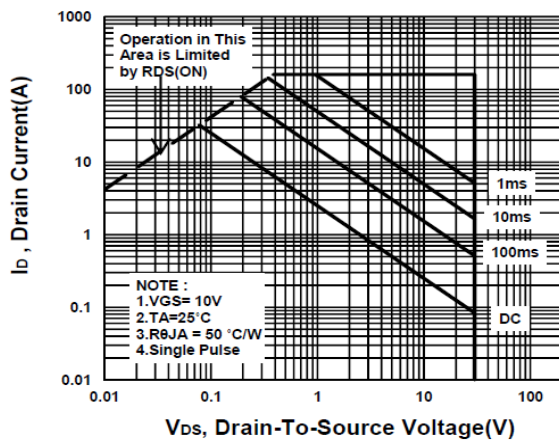
On-Resistance VS Temperature



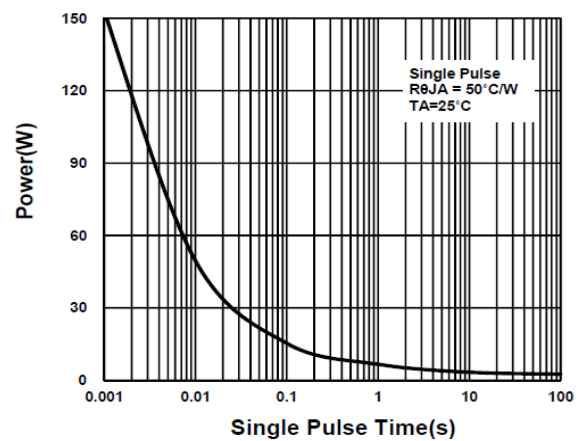
Source-Drain Diode Forward Voltage



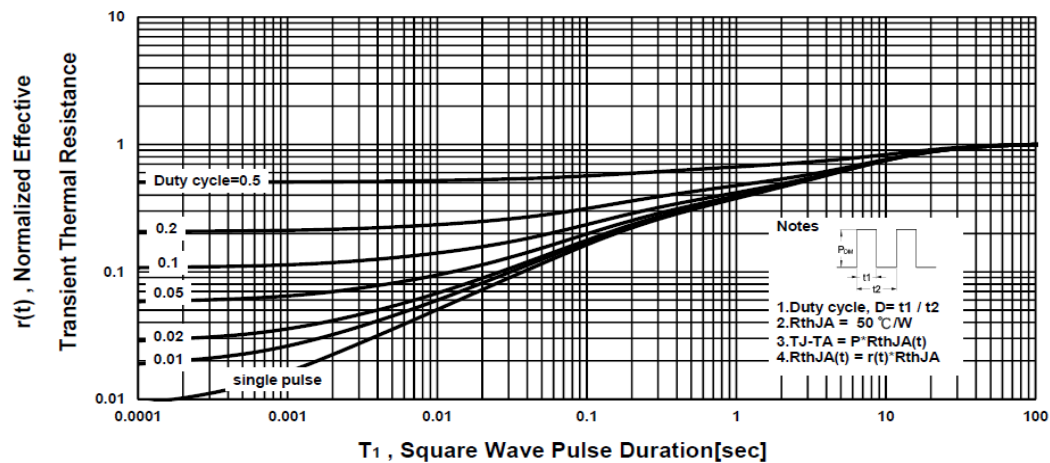
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

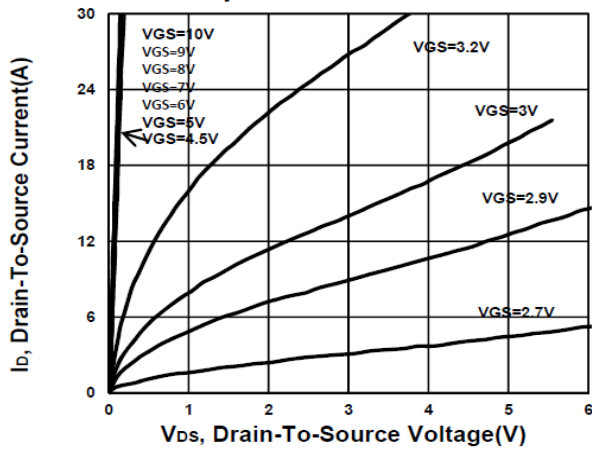


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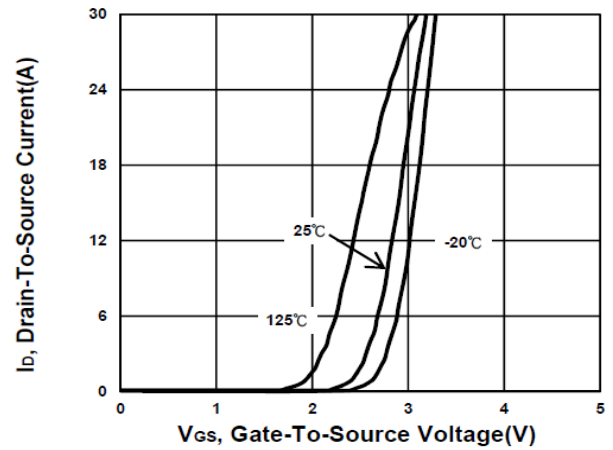
Dual N-Channel Enhancement Mode MOSFET

Q1

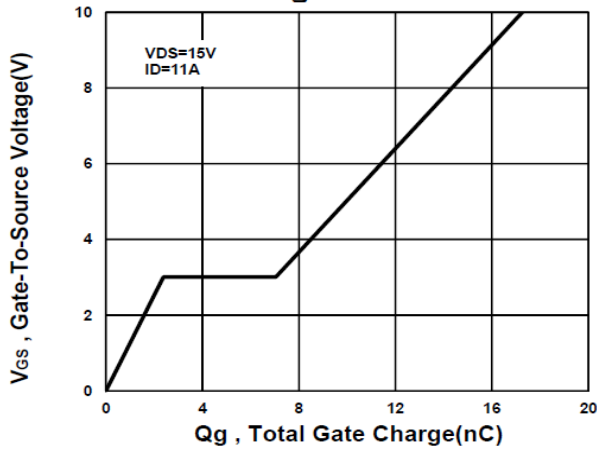
Output Characteristics



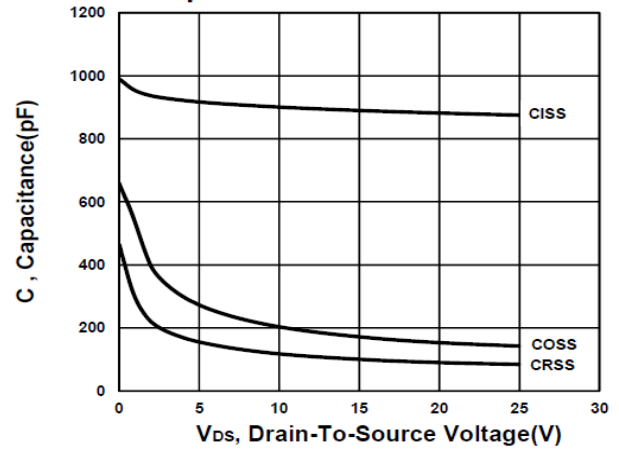
Transfer Characteristics



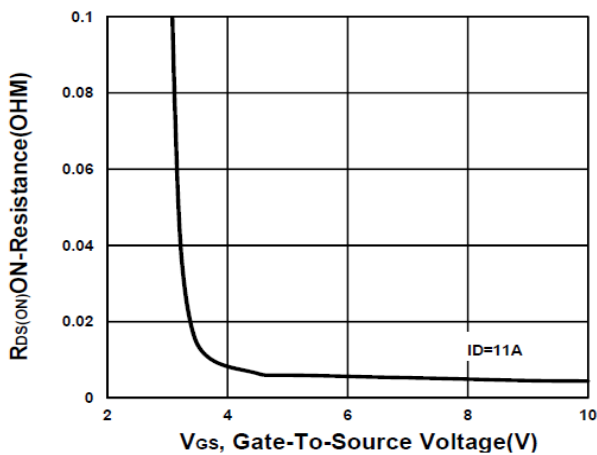
Gate charge Characteristics



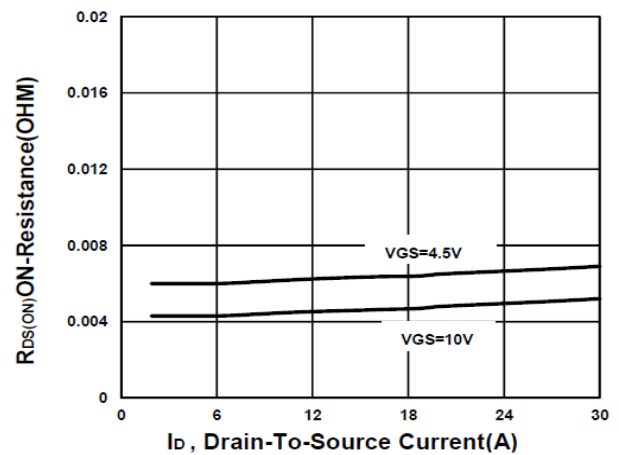
Capacitance Characteristic



On-Resistance VS Gate-To-Source



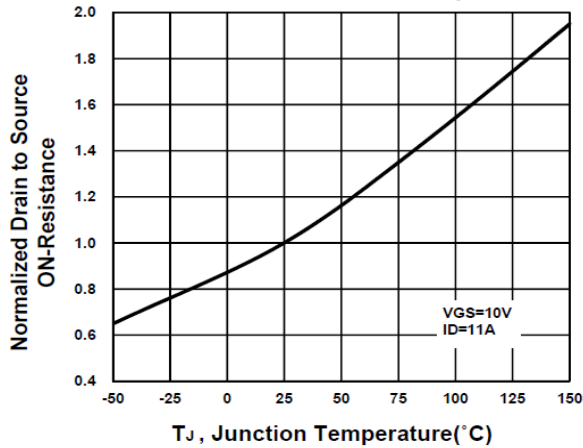
On-Resistance VS Drain Current



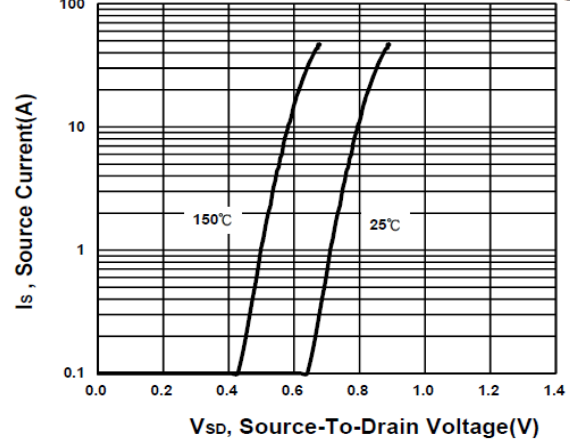
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Dual N-Channel Enhancement Mode MOSFET

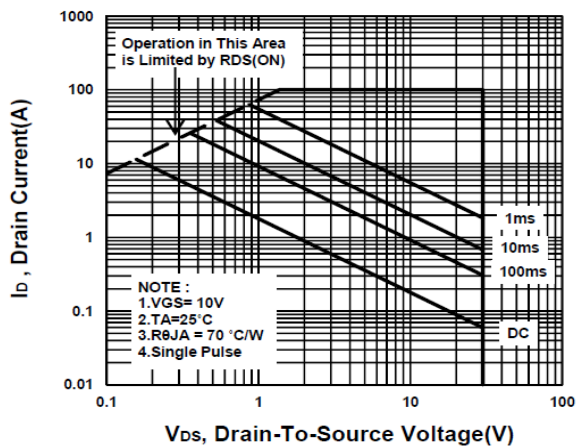
On-Resistance VS Temperature



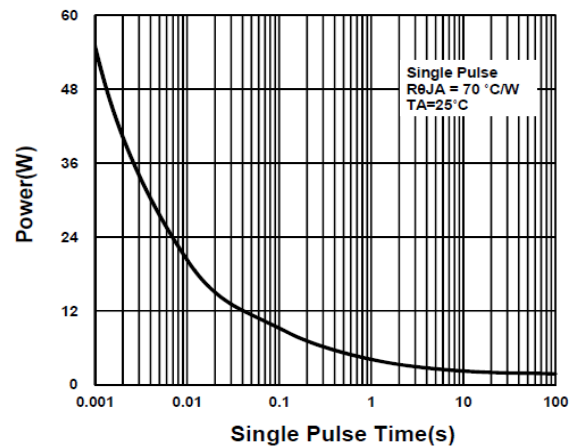
Source-Drain Diode Forward Voltage



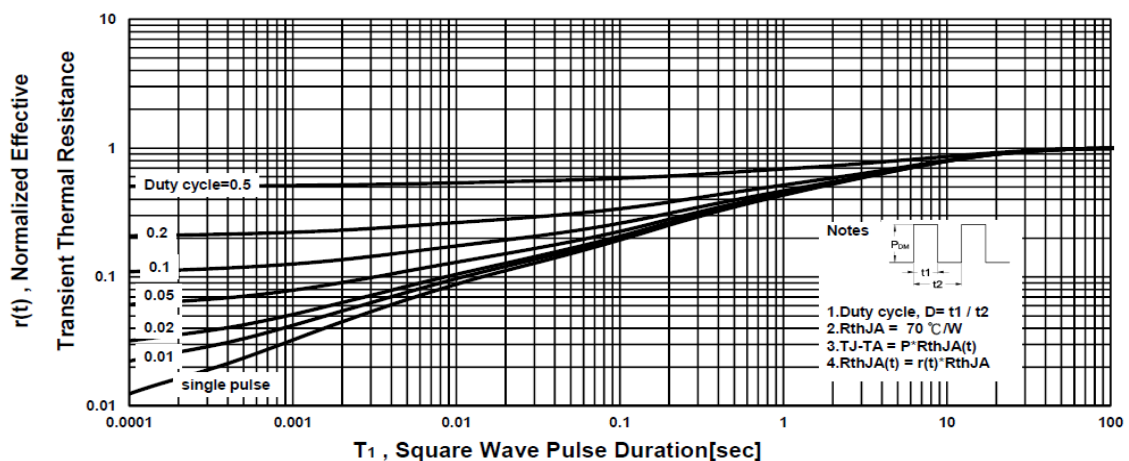
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



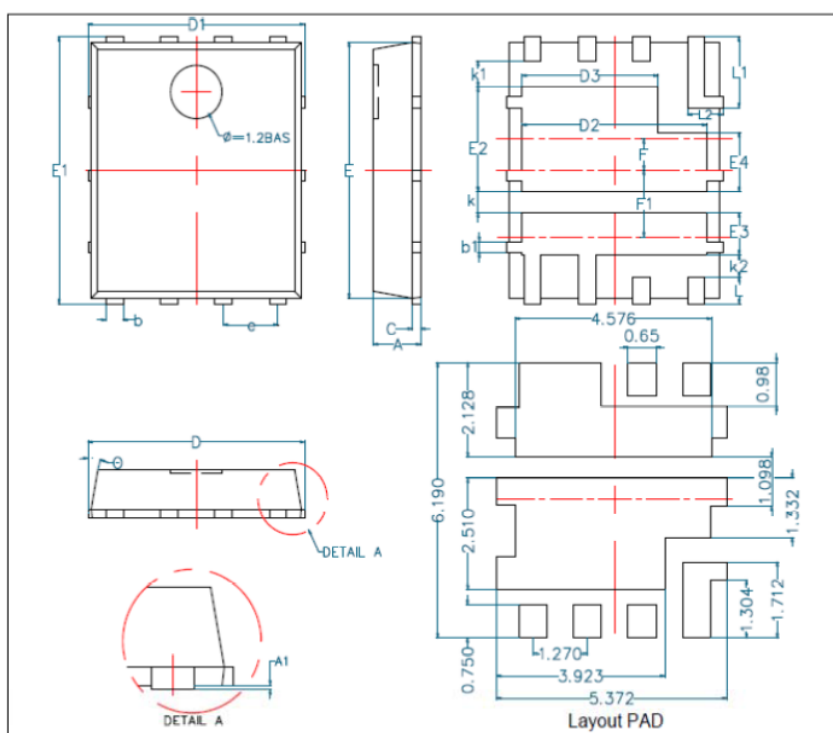
PK610DZ

Dual N-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P(Dual flip chip) MECHANICAL DATA

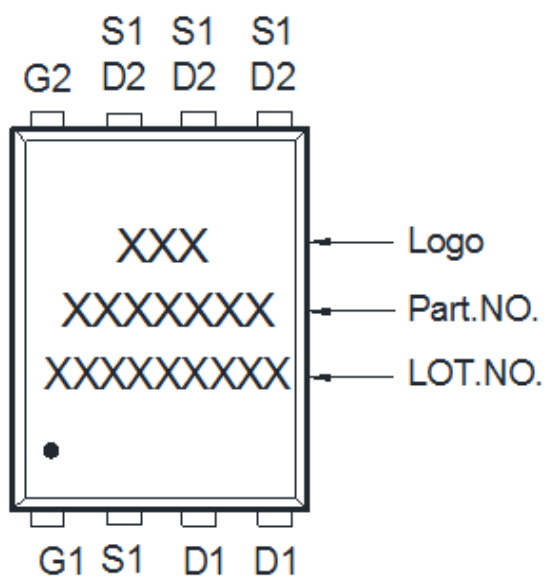
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.00		1.20	E3	0.85		1.15
A1	0.00		0.05	E4	1.23		1.53
b	0.30		0.50	e	1.27 BSC		
b1	0.15		0.35	Θ	10° REF		
c	0.15		0.25	L	0.40		0.60
D1	5.05 BSC			L1	1.50		1.70
D	4.80		5.00	L2	0.72		0.92
D2	4.15		4.45	K	0.47 BSC		
D3	3.02		3.32	K1	0.58 BSC		
E1	6.00 BSC			K2	0.50 BSC		
E	5.65		5.85	F	0.695 REF		
E2	2.30		2.60	F1	1.50REF		



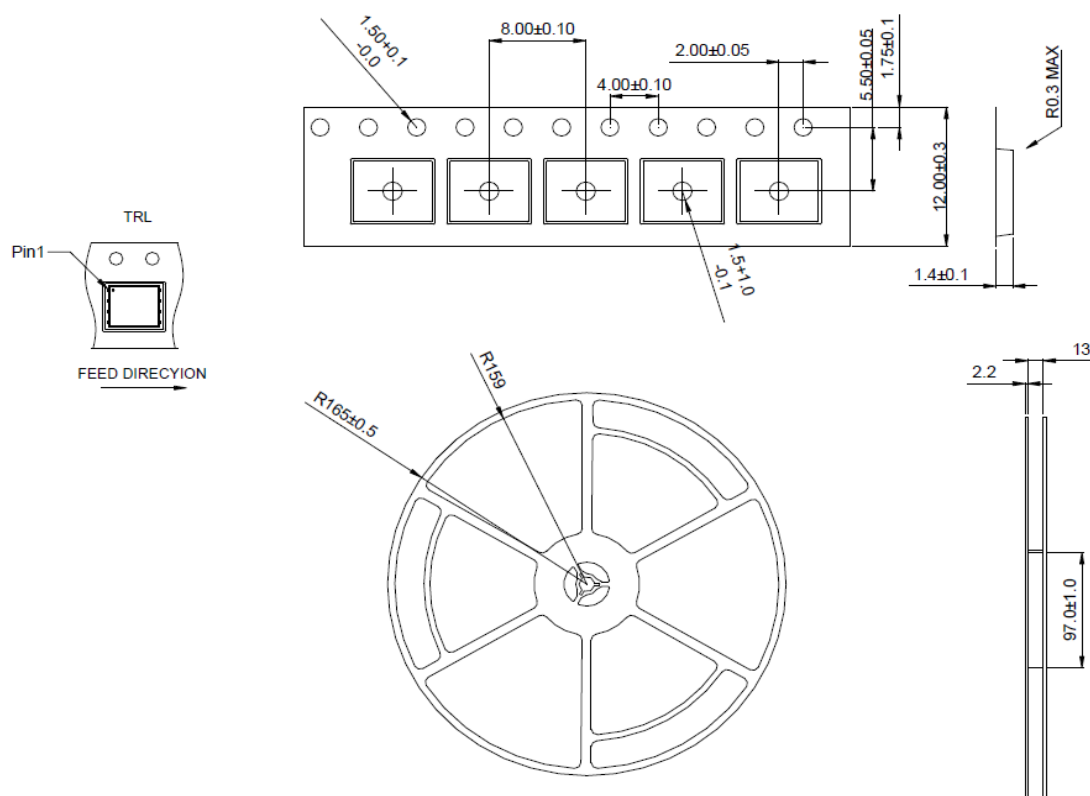
PK610DZ

Dual N-Channel Enhancement Mode MOSFET

A. Marking Information



B. Tape&Reel Information:3000pcs/Reel

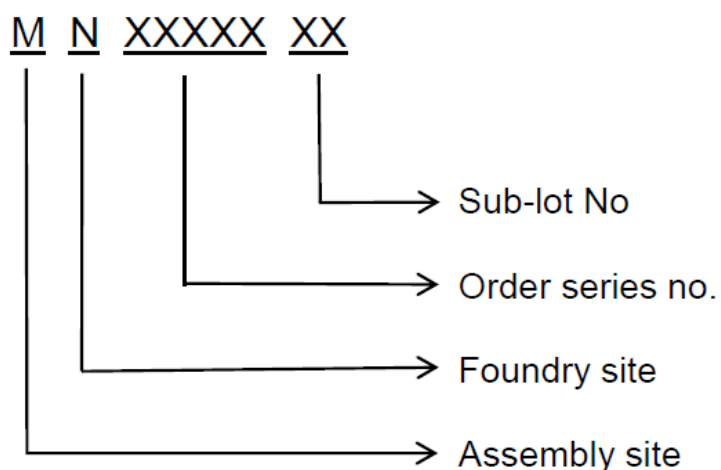


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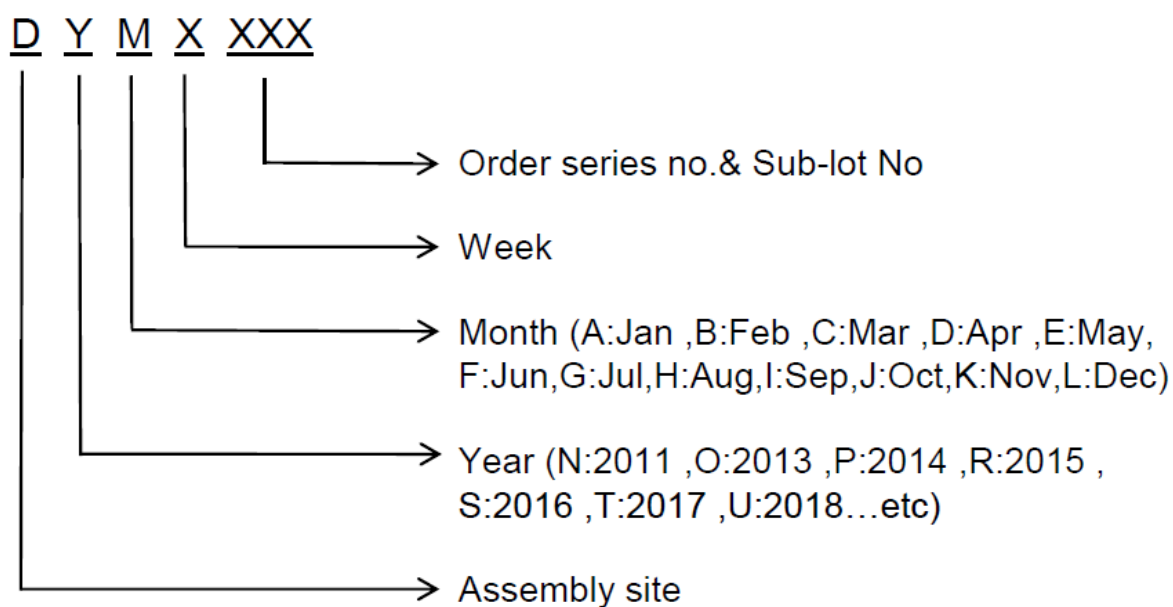
Dual N-Channel Enhancement Mode MOSFET

C. Lot No.&Date Code rule

1.Lot No.



2.Date Code



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Dual N-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G"和"Q"的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert " / " between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least