

QUAD TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

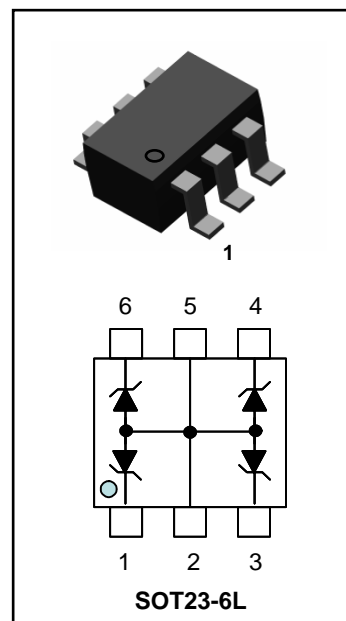
This Quad TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.

SPECIFICATION FEATURES

- 350W Power Dissipation (8/20 μ s Waveform)
- Low Leakage Current, Maximum of 5 μ A at rated voltage
- Very Low Clamping Voltage
- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- Industry Standard Surface Mount Package SOT23-6L
- 100% Tin Matte Finish (RoHS Compliance)

APPLICATIONS

- Personal Digital Assistant (PDA)
- SIM Card Port Protection (Mobile Phone)
- Portable Instrumentation
- Mobile Phones and Accessories
- Memory Card Port Protection



TVS	Marking Code
PJSM S05	M05
PJSM S12	M12
PJSM S15	M15
PJSM S24	M24

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20 μ s Waveform)	P _{pp}	350	W
ESD Voltage (HBM)	V _{ESD}	>25	kV
Operating Temperature Range	T _J	-50 to +125	°C
Storage Temperature Range	T _{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) T_j = 25°C

PJSM S05

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V _{WRM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 1mA	6			V
Reverse Leakage Current	I _R	V _R = 5V			5	μ A
Clamping Voltage (8/20 μ s)	V _C	I _{pp} = 5A			9.8	V
Clamping Voltage (8/20 μ s)	V _C	I _{pp} = 24A			13	V
Off State Junction Capacitance	C _j	0 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			225	pF
Off State Junction Capacitance	C _j	5 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			125	pF

ELECTRICAL CHARACTERISTICS (Per Device) $T_j = 25^\circ\text{C}$
PJSMS12

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1\text{mA}$	13.3			V
Reverse Leakage Current	I_R	$V_R = 12\text{V}$			1	μA
Clamping Voltage (8/20 μs)	V_c	$I_{pp} = 5\text{A}$			20	V
Clamping Voltage (8/20 μs)	V_c	$I_{pp} = 15\text{A}$			25	V
Off State Junction Capacitance	C_j	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2, 5			100	pF

PJSMS15

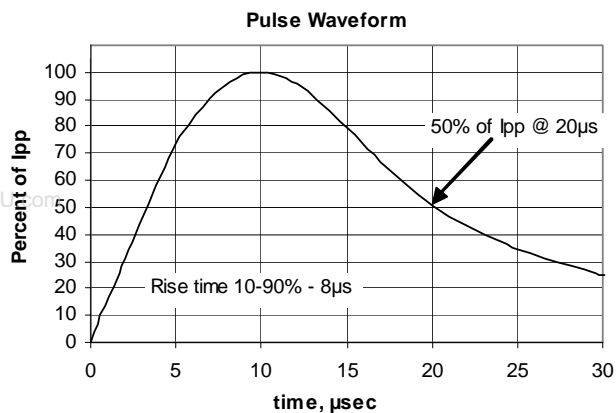
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1\text{mA}$	16.7			V
Reverse Leakage Current	I_R	$V_R = 15\text{V}$			1	μA
Clamping Voltage (8/20 μs)	V_c	$I_{pp} = 5\text{A}$			24	V
Clamping Voltage (8/20 μs)	V_c	$I_{pp} = 12\text{A}$			29	V
Off State Junction Capacitance	C_j	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2, 5			80	pF

PJSMS24

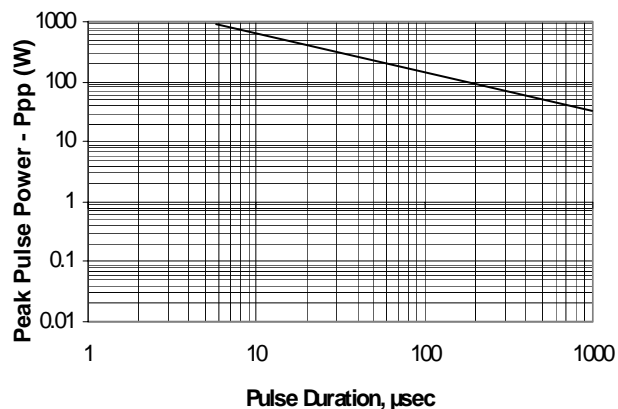
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1\text{mA}$	26.7			V
Reverse Leakage Current	I_R	$V_R = 24\text{V}$			1	μA
Clamping Voltage (8/20 μs)	V_c	$I_{pp} = 5\text{A}$			40	V
Clamping Voltage (8/20 μs)	V_c	$I_{pp} = 8\text{A}$			44	V
Off State Junction Capacitance	C_j	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2, 5			60	pF

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

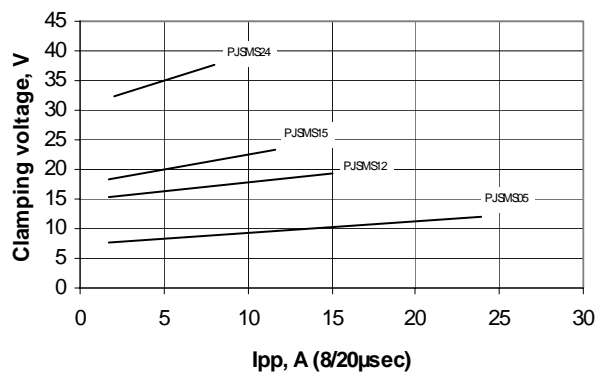
Surge Pulse Waveform Definition



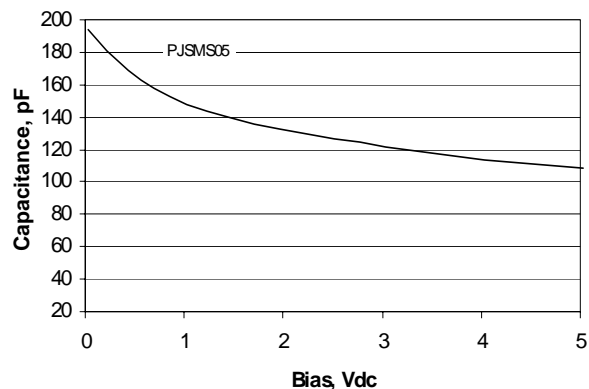
Non-Repetitive Peak Pulse Power vs Pulse Time



Clamping Voltage vs. Peak current

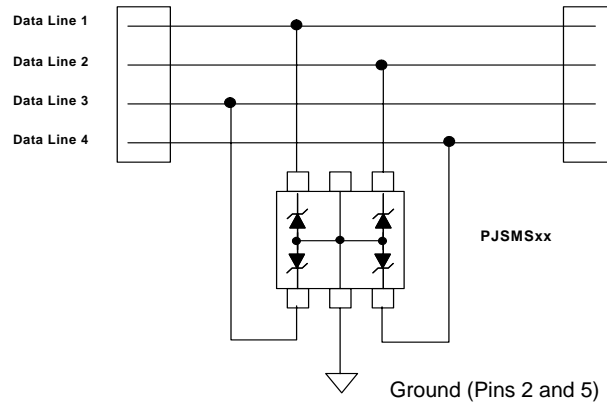


Off-State Capacitance per Device - 1MHz



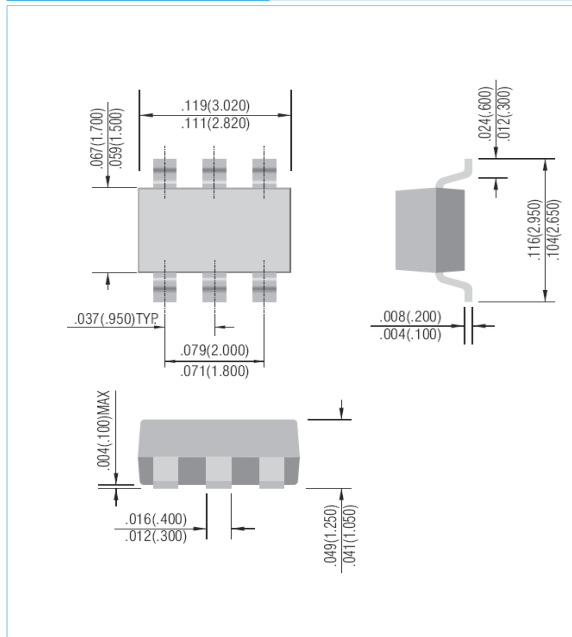


TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS



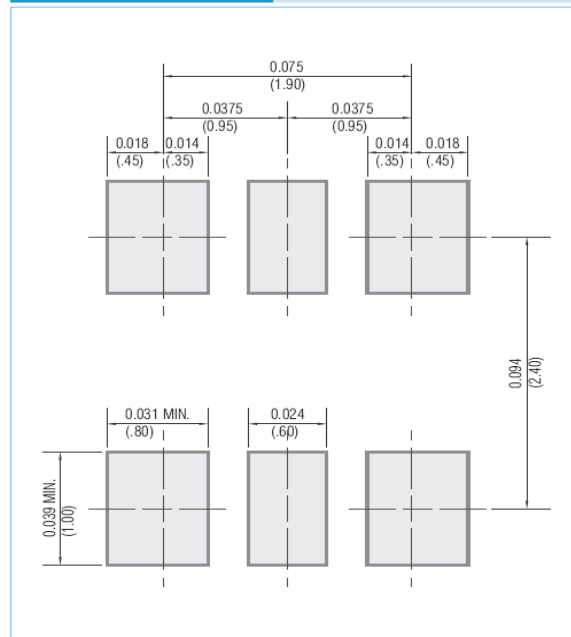
SOT-23-6L

Unit: inch (mm)



SOT23-6L

Unit: inch (mm)



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