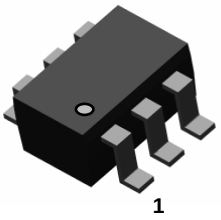
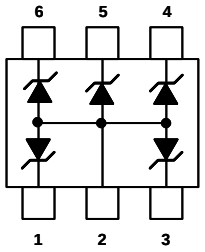
5-TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This 5-TVS/Zener Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry, operating at 3.3V and 5V, as well available for 12V, 15V, and 24V Systems. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.





SOT363

SPECIFICATION FEATURES

- **100W Power Dissipation (8/20µs Waveform)**
- **Low Leakage Current**
- **Very Low Clamping Voltage**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **Operating voltage options for 3.3V, 5V, 12V, 15V, and 24V**
- **Industry Standard SOT363 (SC70-6L) Package**

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APPLICATIONS

- **Personal Digital Assistant (PDA)**
- **SIM Card Port Protection (Mobile Phone)**
- **Portable Instrumentation**
- **Mobile Phones and Accessories**
- **Memory Card Port Protection**

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	100	W
ESD Voltage (HBM)	V_{ESD}	25	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to + 150	°C

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMF03LC

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				3.3	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 10 mA	4.7		5.6	V
Reverse Leakage Current	I_R	V_R = 3.3V			250	µA
Clamping Voltage (820µs)	V_C	I_{pp} = 5A			7.5	V
Clamping Voltage (8/20µs)	V_C	I_{pp} = 9A			9	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			160	pF
Off State Junction Capacitance	Cj	3.3 Vdc Bias f = 1MHz Between I/O pins and pin 2			90	pF

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ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMF05LC

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	6.2			V
Reverse Leakage Current	I_R	V_R = 5V			0.5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5A			10	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 9A			11	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			100	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 2			45	pF

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PJSMF12LC

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	13.3			V
Reverse Leakage Current	I_R	V_R = 12V			0.5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 3A			18	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5A			20	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			50	pF

PJSMF15LC

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	16.6			V
Reverse Leakage Current	I_R	V_R = 15V			0.5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 3A			23	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 4A			25	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			40	pF

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ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMF24LC

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	26.7			V
Reverse Leakage Current	I_R	V_R = 24V			0.5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 1A			35	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 2A			45	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			30	pF

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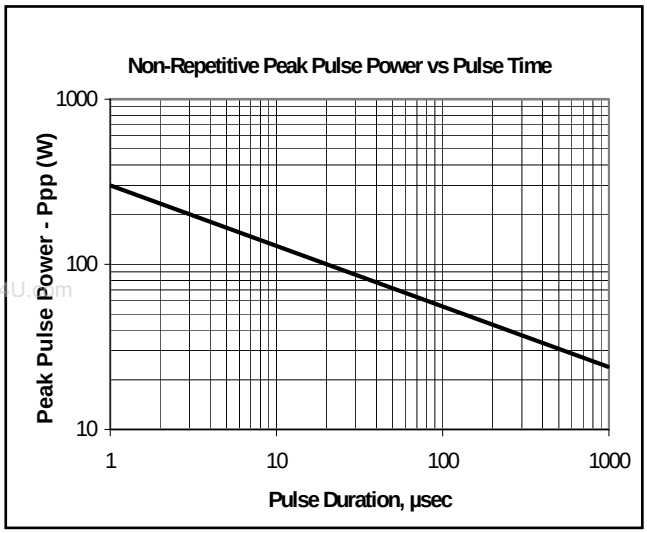
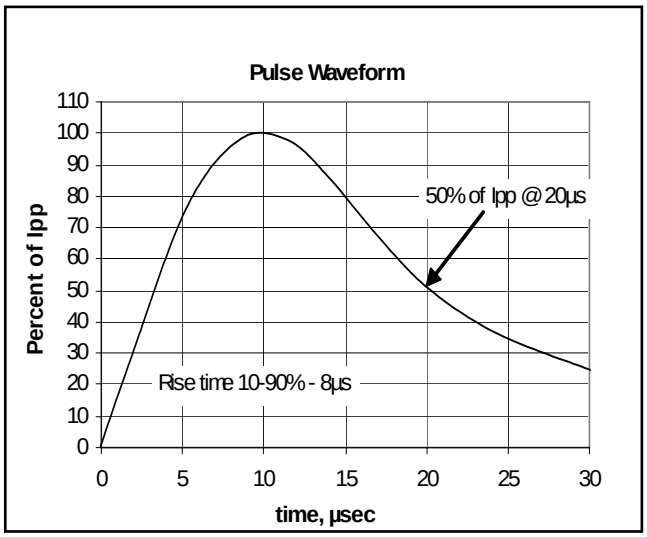
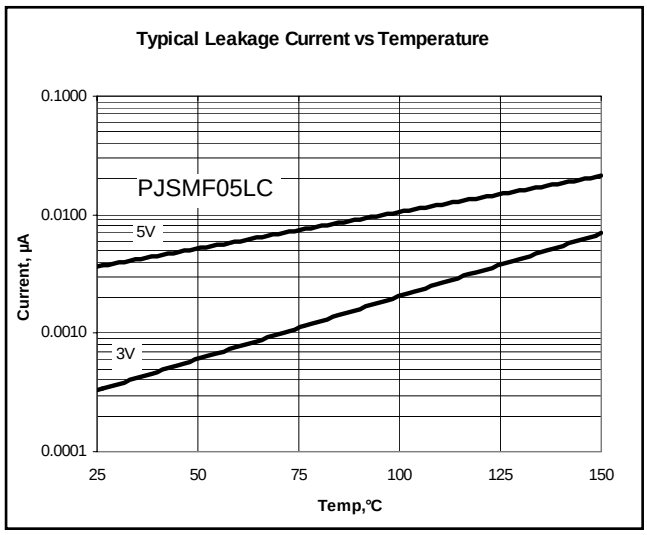
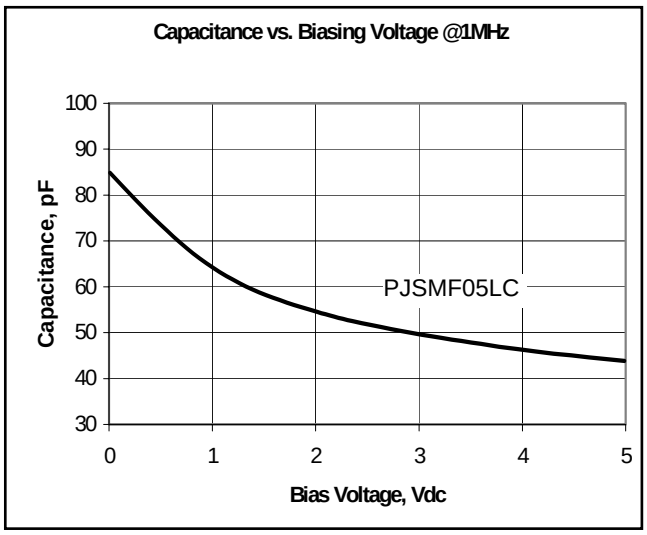
TYPICAL CHARACTERISTICS 25°C unless otherwise noted









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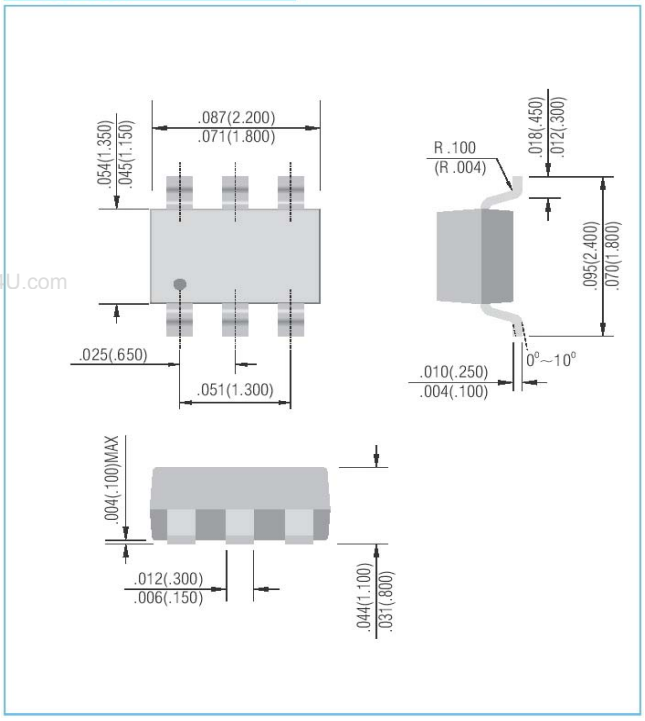
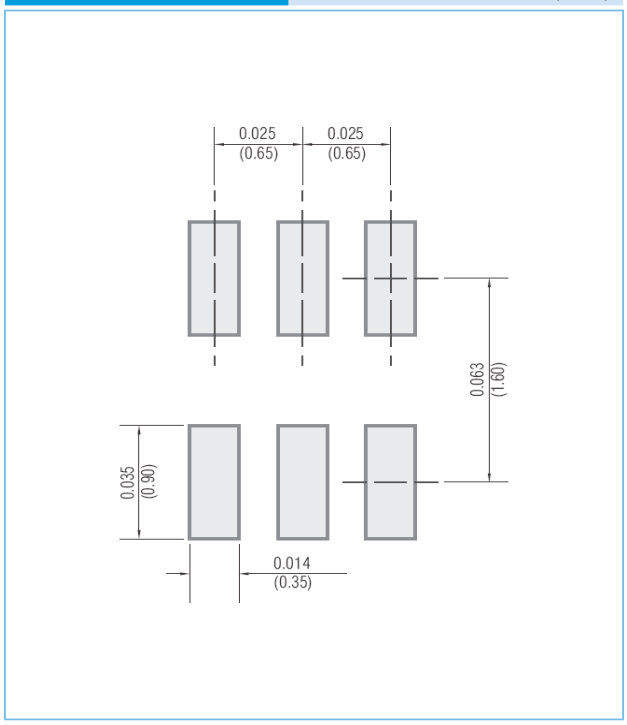
LAYOUT DIMENSIONS AND SUGGESTED PAD LAYOUT

SOT-363 Unit: inch (mm)



SOT-363 Unit: inch (mm)



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