



## FIVE BI-DIRECTIONAL TVS ARRAY FOR ESD PROTECTION

This Penta TVS Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.

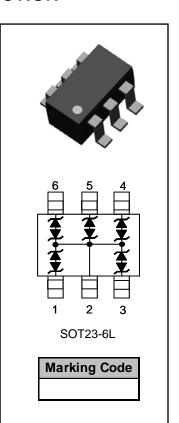
#### **SPECIFICATION FEATURES**

- 80W Power Dissipation (8/20µs Waveform)
- Low Leakage Current, Maximum of 1µA @ 5Vdc
- Very low Clamping voltage
- IEC61000-4-2 ESD 15kV air, 8kV Contact Compliance
- Industry standard SOT23-6L
- 100% Tin Matte Finish (RoHS Compliant)

#### **APPLICATIONS**

- Video I/O ports protection
- Set Top Boxes
- Portable Instrumentation





#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P <sub>pp</sub>	80	W
Peak Pulse Current (8/20µs Waveform)	I <sub>pp</sub>	5.0	А
ESD Voltage (HBM)	V <sub>ESD</sub>	>25	kV
Operating Temperature Range	TJ	-55 to +150	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

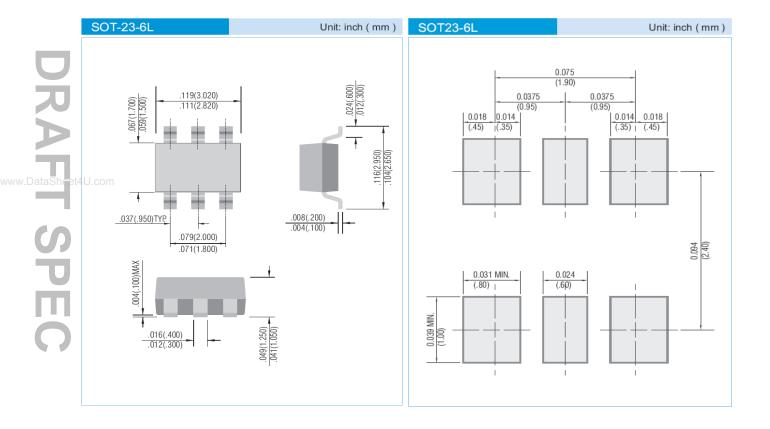
# **ELECTRICAL CHARACTERISTICS** Tj = 25°C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				5.0	V
Reverse Breakdown Voltage	$V_{BR}$	I <sub>BR</sub> =1mA	6.2		8.0	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>R</sub> =5V			1	μΑ
Clamping Voltage (8/20µs)	V <sub>c</sub>	I <sub>pp</sub> =1A			12	V
Clamping Voltage (8/20µs)	V <sub>c</sub>	1 <sub>pp</sub> = 4A			15	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			15	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 2			7	pF





### PACKAGE LAYOUT DIMENSIONS



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