

PJQ1821

20V P-Channel Enhancement Mode MOSFET

Voltage

-20 V

Current

-600mA

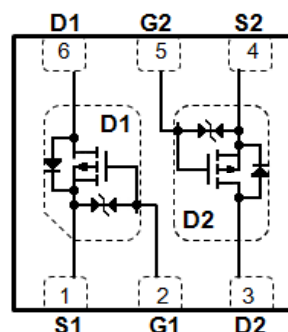
Features

- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN1010-6L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.000045 ounces, 0.0013 grams

DFN1010-6L



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V _{DS}	-20	V
Gate-Source Voltage		V _{GS}	±8	
Continuous Drain Current (Note 4)		I _D	-600	mA
Pulsed Drain Current (Note 1)		I _{DM}	-1200	
Power Dissipation	T _a =25°C	P _D	400	mW
	Derate above 25°C		3.2	mW/°C
Operating Junction and Storage Temperature Range		T _J ,T _{STG}	-55~150	°C
Typical Thermal Resistance		R _{θJA}	312	°C/W
- Junction to Ambient (Note 3,4)				

- Limited only By Maximum Junction Temperature



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.3	-0.6	-1	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-300mA	-	470	600	mΩ
		V _{GS} =-2.5V, I _D =-200mA	-	630	850	
		V _{GS} =-1.8V, I _D =-100mA	-	810	1200	
		V _{GS} =-1.5V, I _D =-100mA	-	1020	1600	
		V _{GS} =-1.2V, I _D =-100mA	-	1670	3000	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>±</u> 8V, V _{DS} =0V	-	-	<u>±</u> 10	
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-200mA, V _{GS} =-4.5V (Note 2)	-	1.1	-	nC
Gate-Source Charge	Q _{gs}		-	0.2	-	
Gate-Drain Charge	Q _{gd}		-	0.1	-	
Input Capacitance	C _{iSS}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ	-	51	-	pF
Output Capacitance	C _{oSS}		-	15	-	
Reverse Transfer Capacitance	C _{rSS}		-	2.2	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =-10V, I _D =-200mA, V _{GS} =-4.5V, R _G =6Ω (Note 2)	-	4.3	-	ns
Turn-On Rise Time	t _r		-	20	-	
Turn-Off Delay Time	t _{d(off)}		-	33	-	
Turn-Off Fall Time	t _f		-	25	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	-200	mA
Diode Forward Voltage	V _{SD}	I _S =-200mA, V _{GS} =0V	-	-0.85	-1	V

NOTES:

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

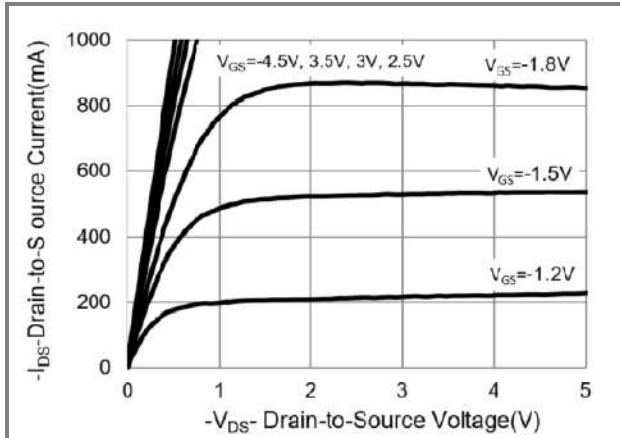


Fig.1 On-Region Characteristics

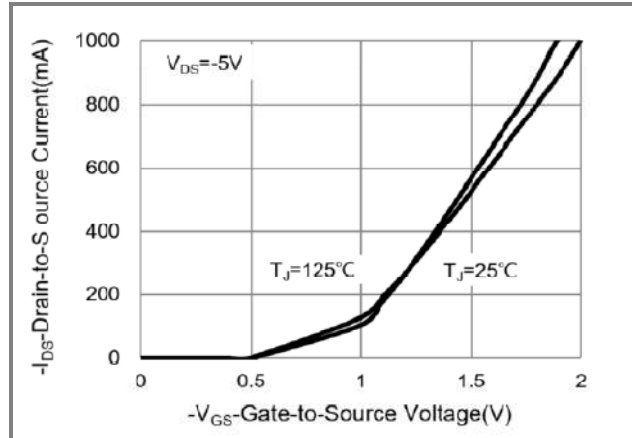


Fig.2 Transfer Characteristics

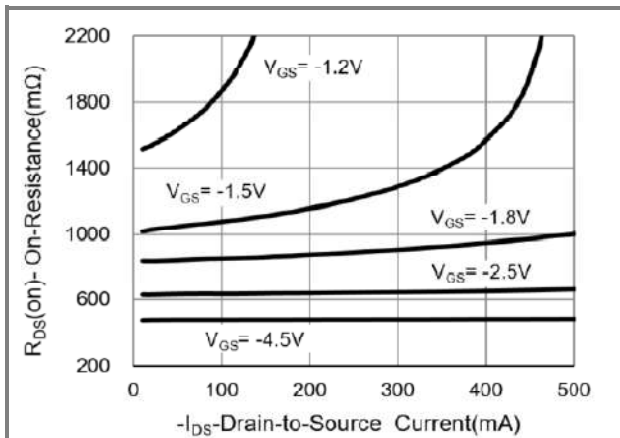


Fig.3 On-Resistance vs. Drain Current

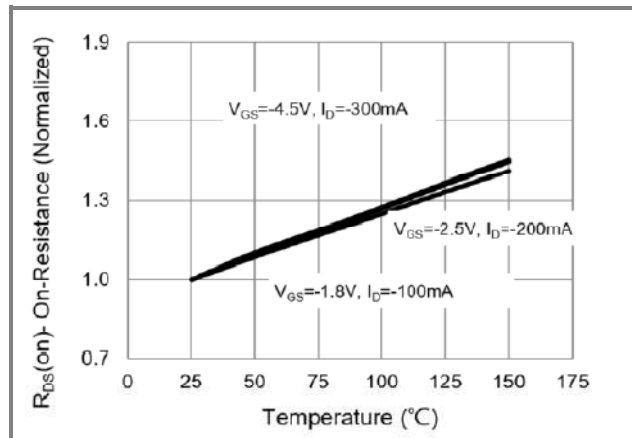


Fig.4 On-Resistance vs. Junction temperature

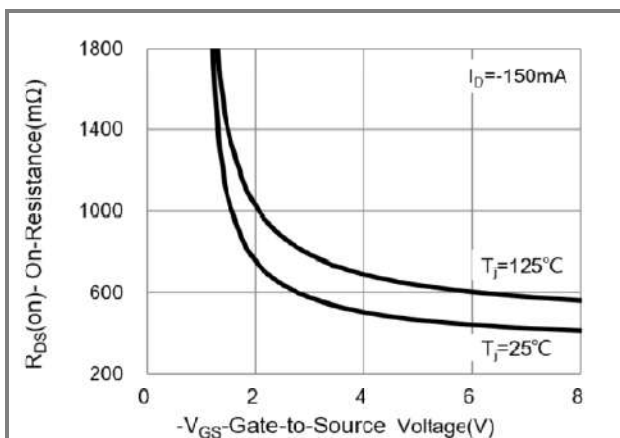


Fig.5 On-Resistance Variation with V_{GS}

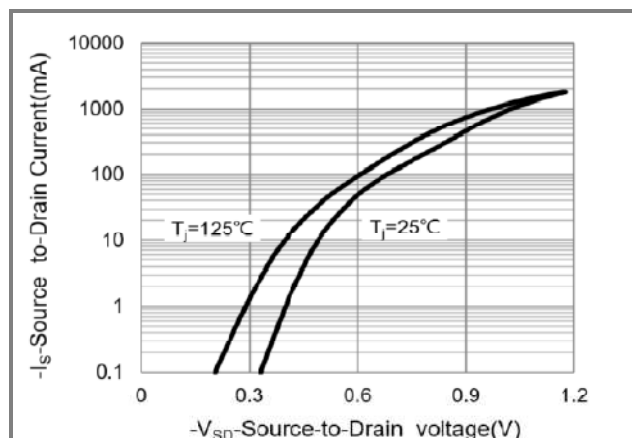


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

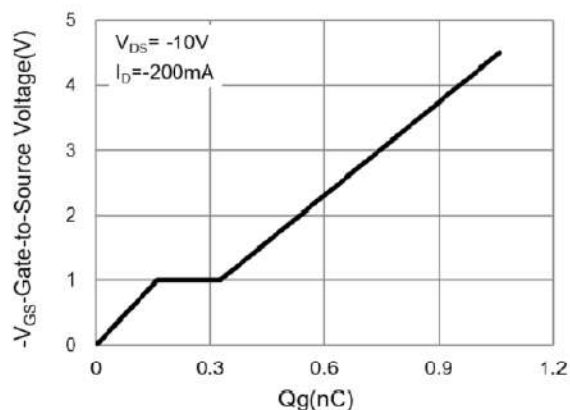


Fig.7 Gate-Charge Characteristics

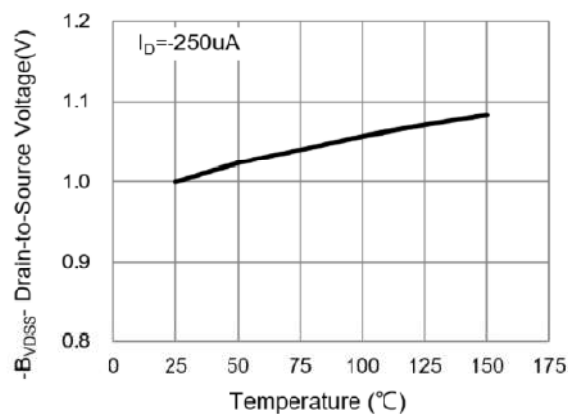


Fig.8 Breakdown Voltage Variation vs. Temperature

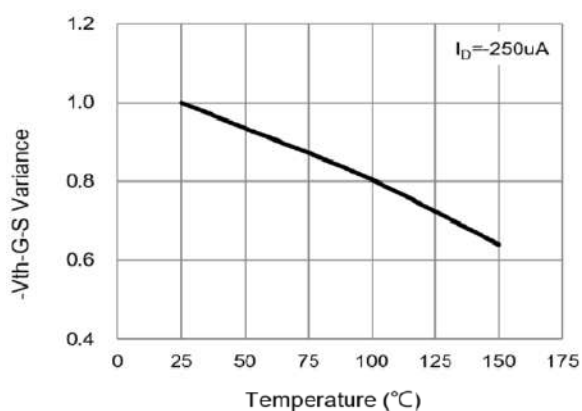


Fig.9 Threshold Voltage Variation with Temperature

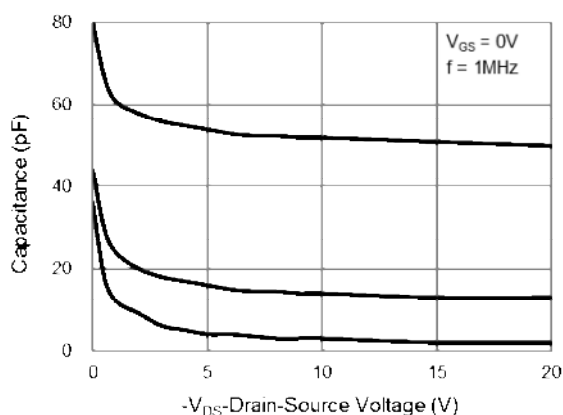


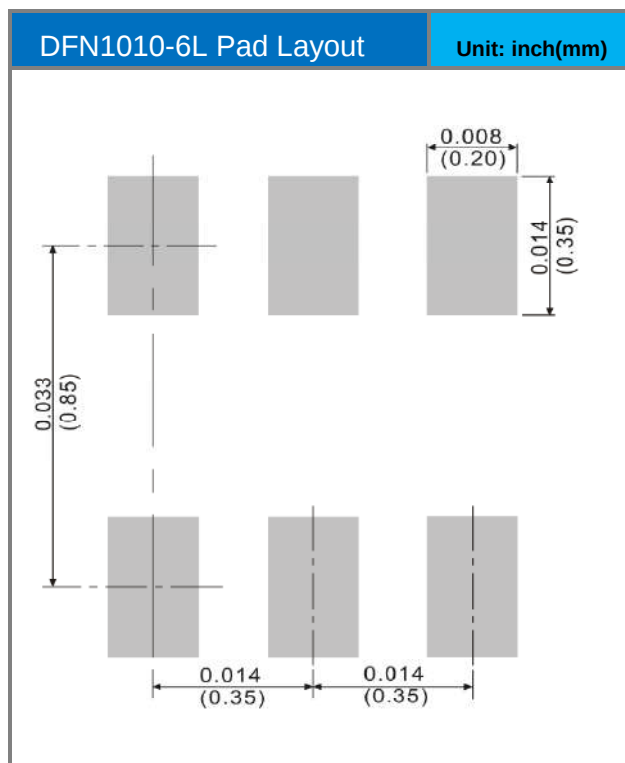
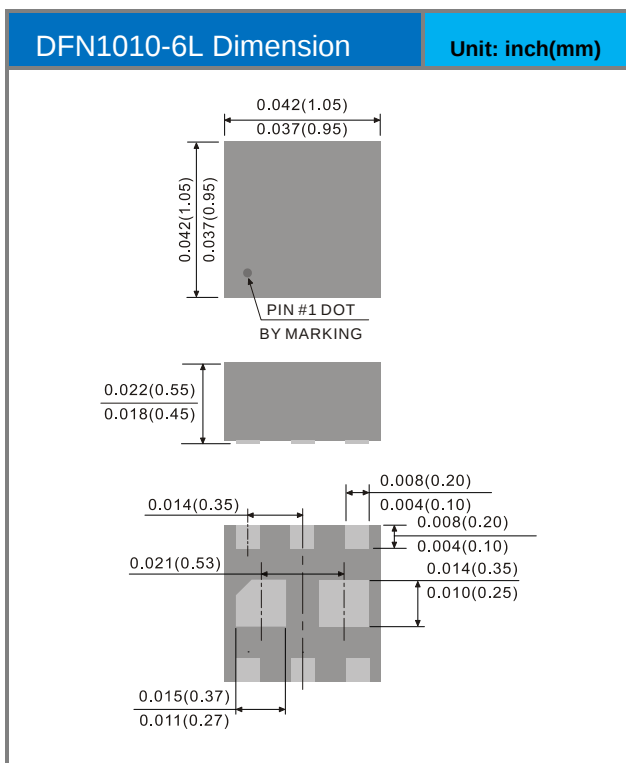
Fig.10 Capacitance vs. Drain-Source Voltage

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Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ1821_R1_00001	DFN1010-6L	5K pcs / 7" reel	821	Halogen free

Packaging Information & Mounting Pad Layout





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