

PJL9454A

100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	Current	5 A
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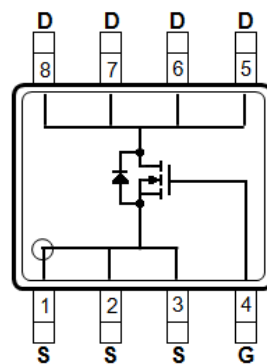
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@5A<50m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@3A<55m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9454A

SOP-8



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V _{DS}	100	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A =25°C	I _D	5	A
	T _A =70°C		4	
Pulsed Drain Current ^(Note 1)		I _{DM}	20	A
Power Dissipation	T _A =25°C	P _D	2.5	W
	T _A =70°C		1.6	
Single Pulse Avalanche Energy ^(Note 5)		E _{AS}	5	mJ
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~150	°C
Typical Thermal resistance		R _{θJA}	50	°C/W
- Junction to Ambient, t ≤ 10s ^(Note 6)				



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

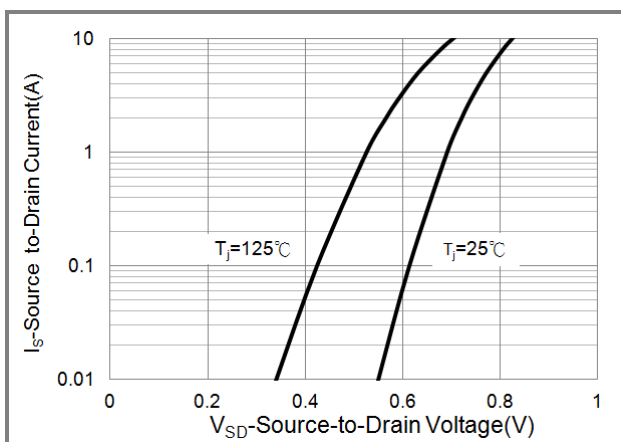
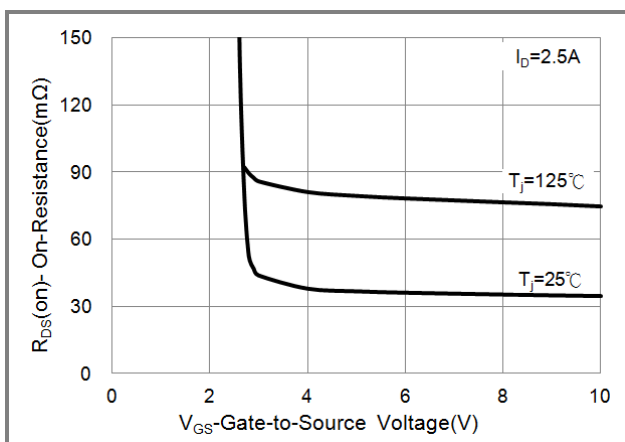
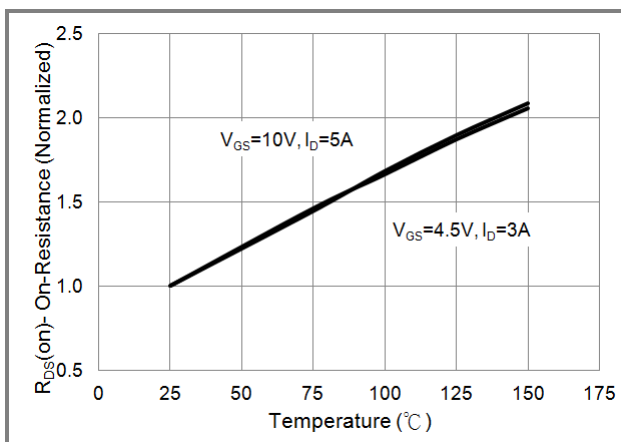
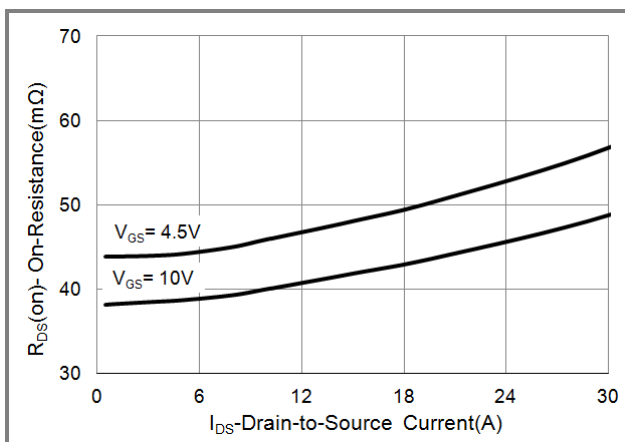
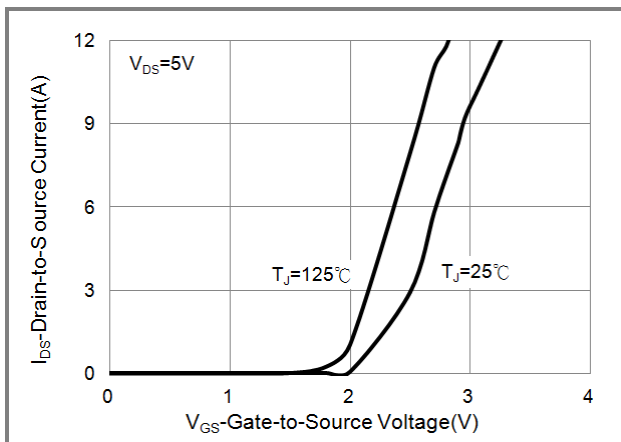
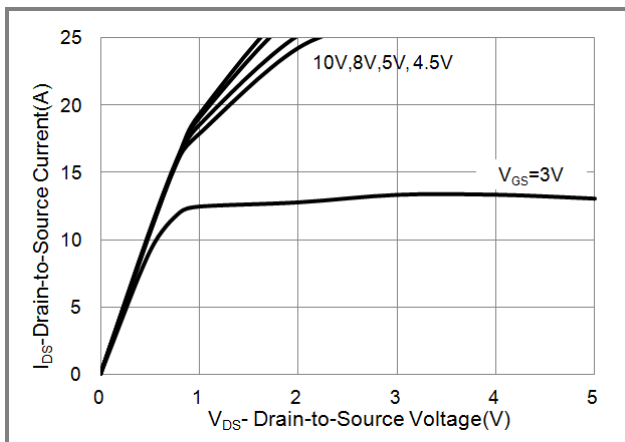
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	100	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =5A	-	37	50	mΩ
		V _{GS} =4.5V, I _D =3A	-	38	55	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1.0	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 7)						
Total Gate Charge	Q _g	V _{DS} =80V, I _D =5A, V _{GS} =10V (Note 1,2)	-	55	-	nC
Gate-Source Charge	Q _{gs}		-	7.9	-	
Gate-Drain Charge	Q _{gd}		-	10	-	
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1.0MHZ	-	3601	-	pF
Output Capacitance	C _{oss}		-	133	-	
Reverse Transfer Capacitance	C _{rss}		-	65	-	
Turn-On Delay Time	td _(on)	V _{DD} =50V, I _D =5A, V _{GS} =10V, R _G =3Ω (Note 1,2)	-	14	-	ns
Turn-On Rise Time	tr		-	45	-	
Turn-Off Delay Time	td _(off)		-	57	-	
Turn-Off Fall Time	tf		-	16	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	5.0	A
Diode Forward Voltage	V _{SD}	I _S =1.0A, V _{GS} =0V	-	0.7	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
4. The maximum current rating is package limited.
5. The test condition is $L=0.1\text{mH}$, $I_{AS}=10A$, $V_{DD}=50V$, $V_{GS}=10V$
6. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.

PJL9454A

TYPICAL CHARACTERISTIC CURVES



PJL9454A

TYPICAL CHARACTERISTIC CURVES

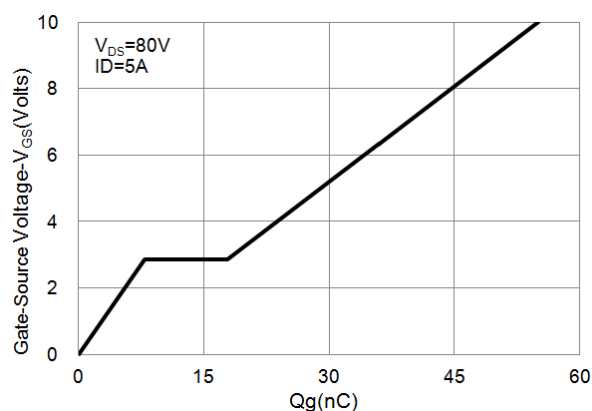


Fig.7 Gate-Charge Characteristics

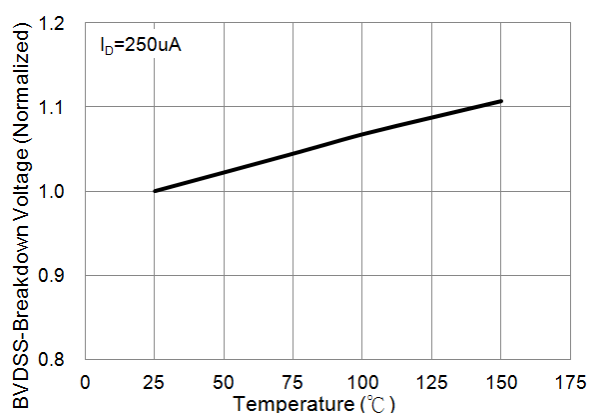


Fig.8 Breakdown Voltage Variation vs. Temperature

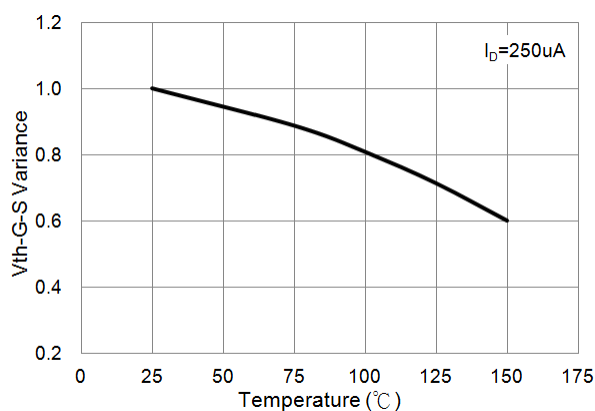


Fig.9 Threshold Voltage Variation with Temperature.

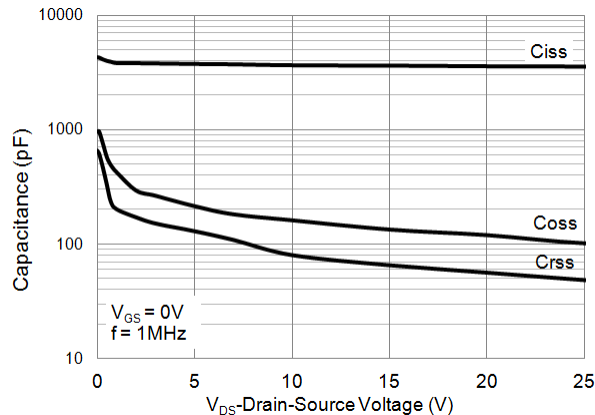


Fig.10 Capacitance vs. Drain-Source Voltage.

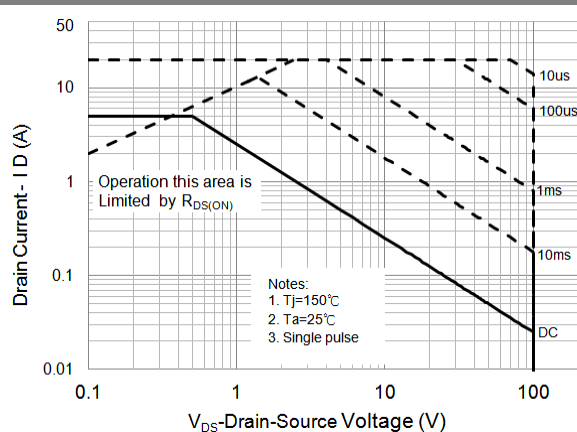


Fig.11 Maximum Safe Operating Area



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TYPICAL CHARACTERISTIC CURVES

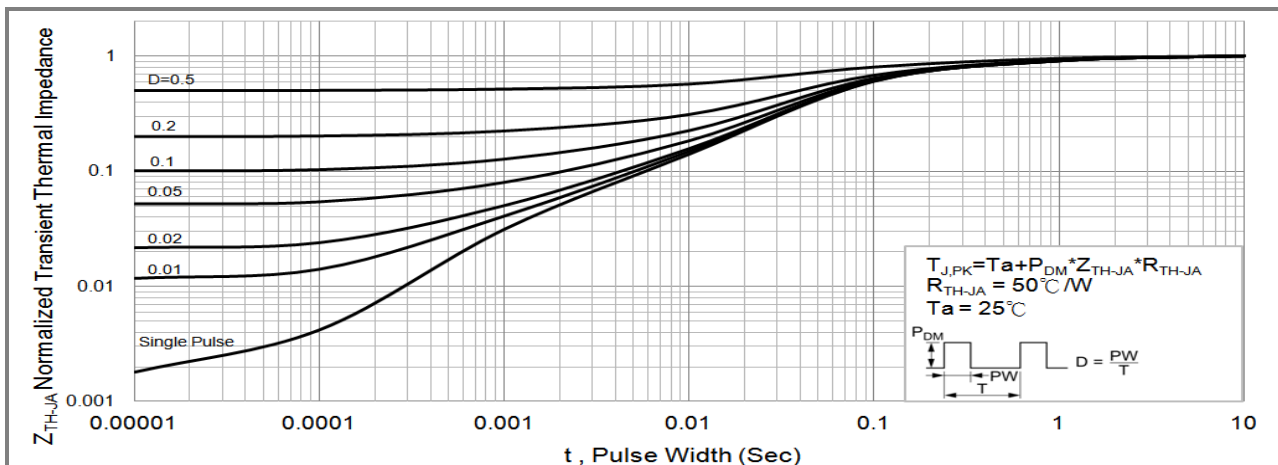


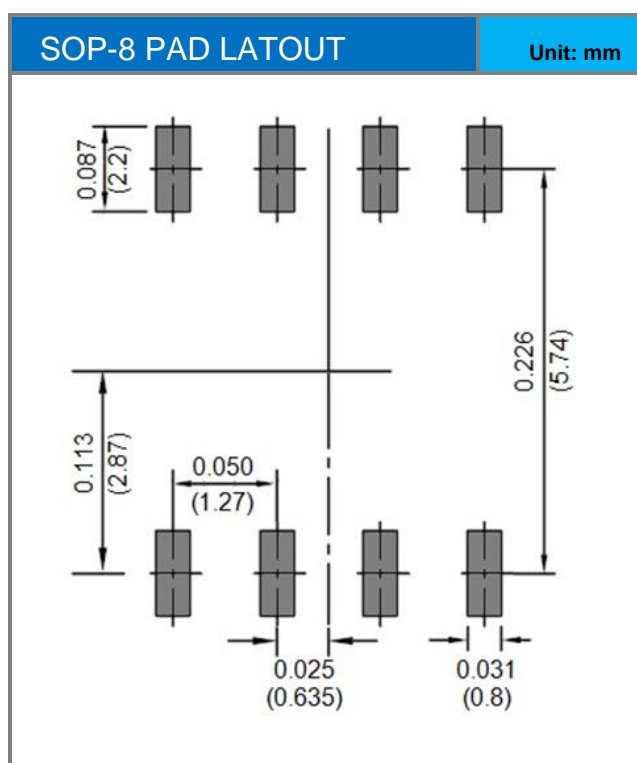
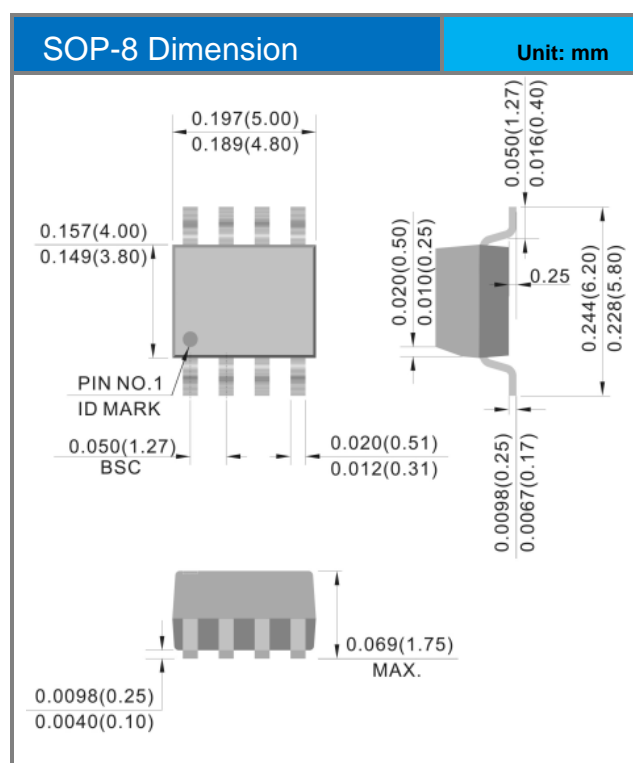
Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

PJL9454A

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9454A_R2_00001	SOP-8	2.5K pcs / 13" reel	L9454A	Halogen free

Packaging Information & Mounting Pad Layout





PJL9454A

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