

PJ6694

25V N-Channel Enhancement Mode MOSFET

FEATURES

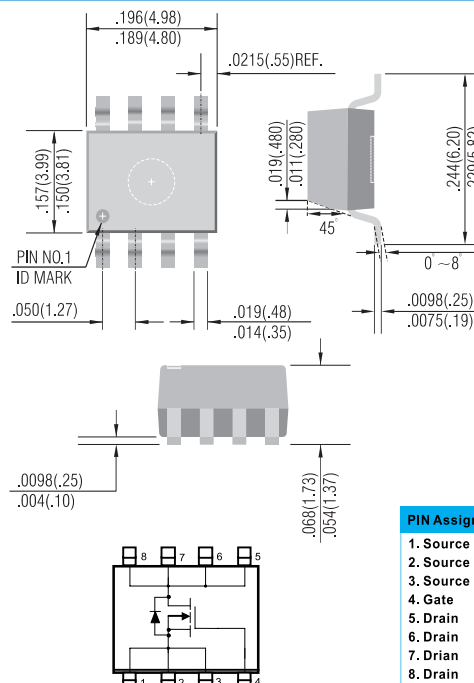
- $R_{DS(ON)}$, $V_{GS}@10V, I_{DS}@12A=12m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V, I_{DS}@10A=22m\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters
- Fully Characterized Avalanche Voltage and Current
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICAL DATA

- Case: SOIC-08 Package
- Terminals : Solderable per MIL-STD-750D, Method 1036.3
- Marking : 6694

SOIC-08

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	12	A
Pulsed Drain Current ¹⁾	I_{DM}	50	A
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$ 2.5 $T_A=75^\circ\text{C}$ 1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$
Avalanche Energy with Single Pulse $I_D=23A, V_{DD}=25V, L=0.5mH$	E_{AS}	130	mJ
Junction-to Ambient Thermal Resistance(PCB mounted) ²	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Note: 1. Maximum DC current limited by the package

2. Surface mounted on FR4 board, $t \leq 10$ sec

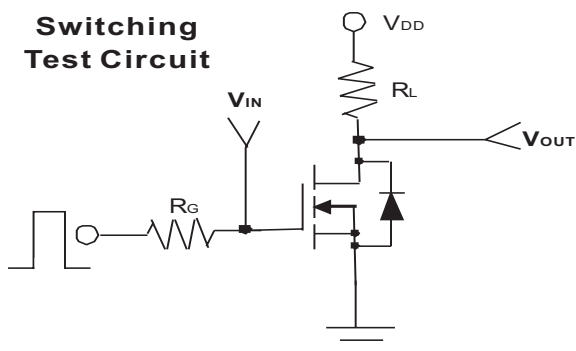
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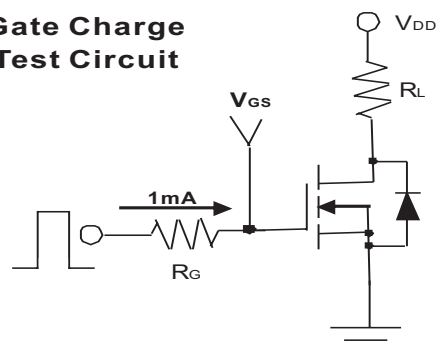
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	25	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =10A	-	17.5	22.0	mΩ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =12A	-	9.2	12.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =25V, V _{GS} =0V	-	-	1	uA
Gate Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Forward Transconductance	g _{fS}	V _{DS} =10V, I _D =12A	25	-	-	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, I _D =12A, V _{GS} =5V	-	15.0	-	nC
		V _{DS} =15V, I _D =12A V _{GS} =10V	-	26.5	-	
Gate-Source Charge	Q _{gs}		-	5.2	-	
Gate-Drain Charge	Q _{gd}		-	5.7	-	
Turn-On Delay Time	T _{d(on)}	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V R _G =3.6Ω	-	12	14	ns
Turn-On Rise Time	t _{rr}		-	10	12.5	
Turn-Off Delay Time	t _{d(off)}		-	32	37.5	
Turn-Off Fall Time	t _f		-	6.5	8	
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1.0MH _z	-	1450	-	pF
Output Capacitance	C _{oss}		-	260	-	
Reverse Transfer Capacitance	C _{rss}		-	150	-	
Source-Drain Diode						
Max. Diode Forward Current	I _s	-	-	-	2.5	A
Diode Forward Voltage	V _{SD}	I _S =2.5A , V _{GS} =0V	-	0.75	1.2	V

Switching Test Circuit



Gate Charge Test Circuit



PJ6694

Typical Characteristics Curves ($T_J=25^\circ\text{C}$, unless otherwise noted)

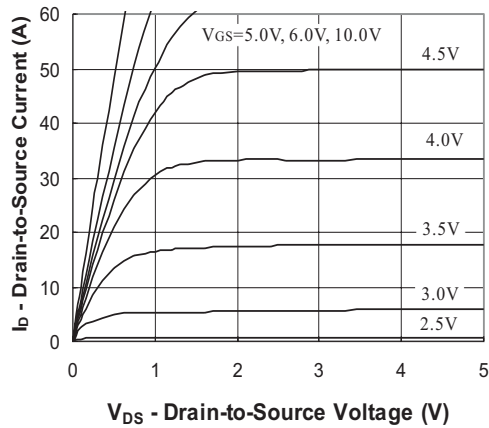


FIG.1- Output Characteristic

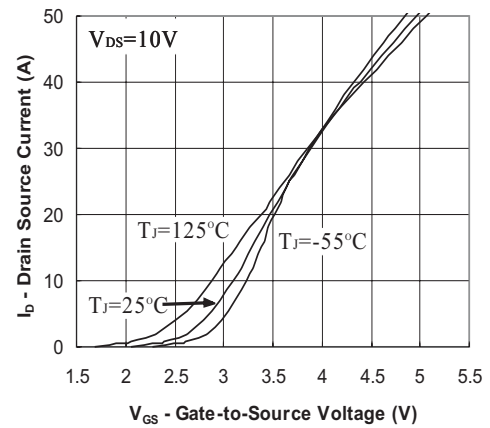


FIG.2- Transfer Characteristic

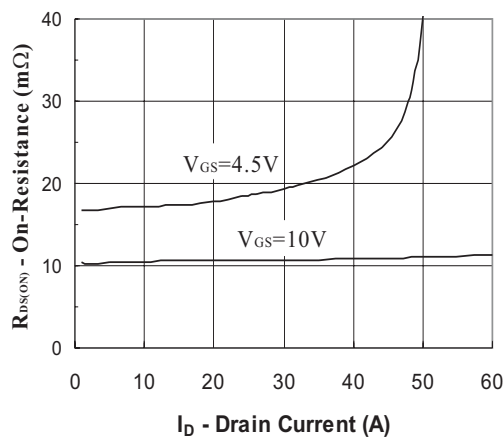


FIG.3- On Resistance vs Drain Current

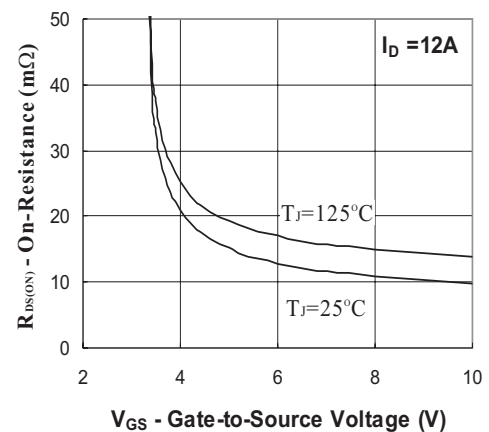


FIG.4- On Resistance vs Gate to Source Voltage

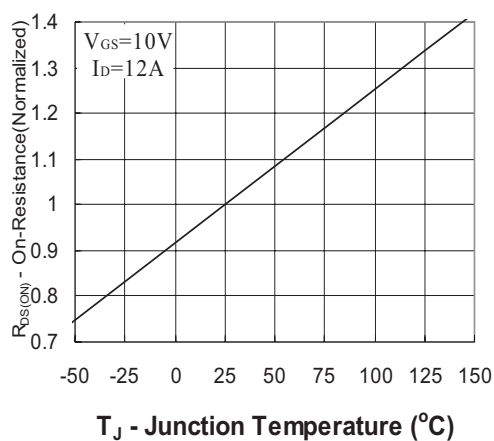


FIG.5- On Resistance vs Junction Temperature

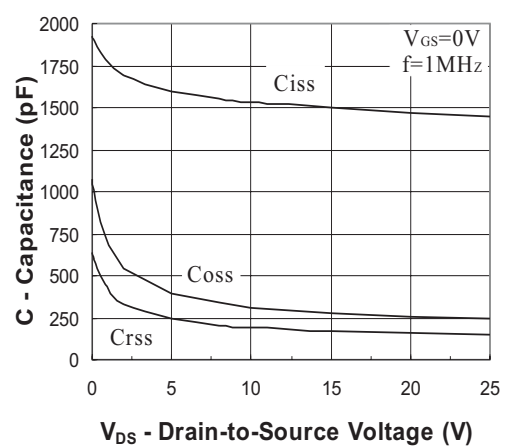


FIG.6- Capacitance

PJ6694

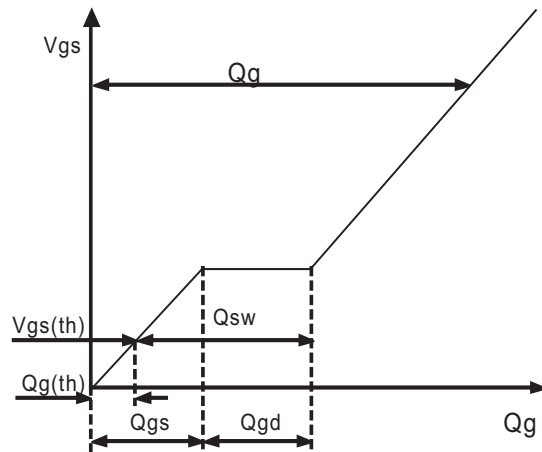


Fig.7 - Gate Charge Waveform

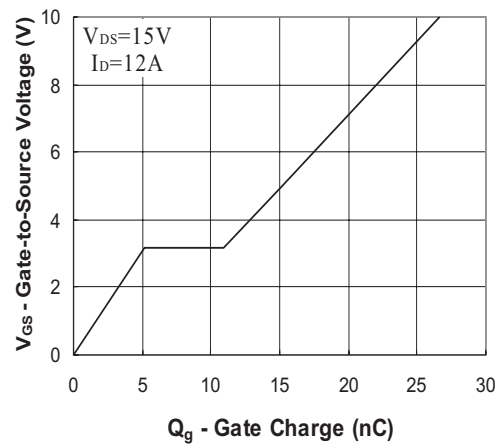


Fig.8 - Gate Charge

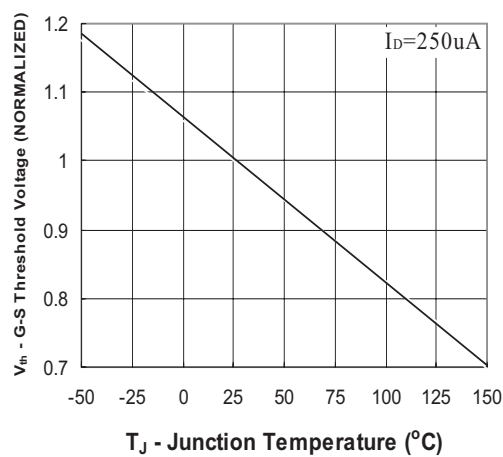


Fig.9 - Threshold Voltage vs Temperature

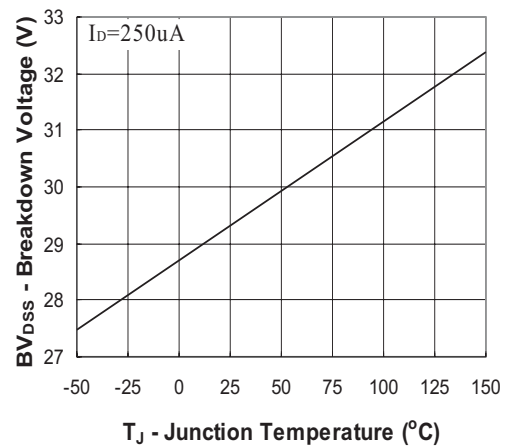


Fig.10 - Breakdown Voltage vs Junction Temperature

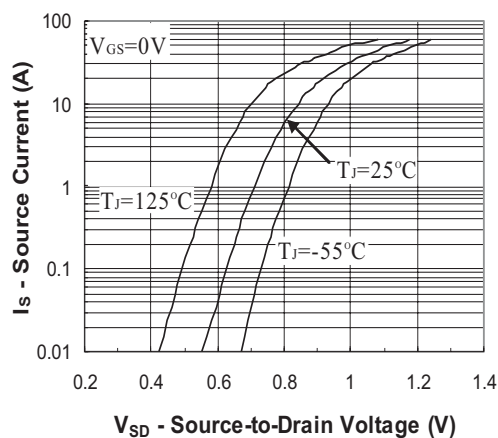


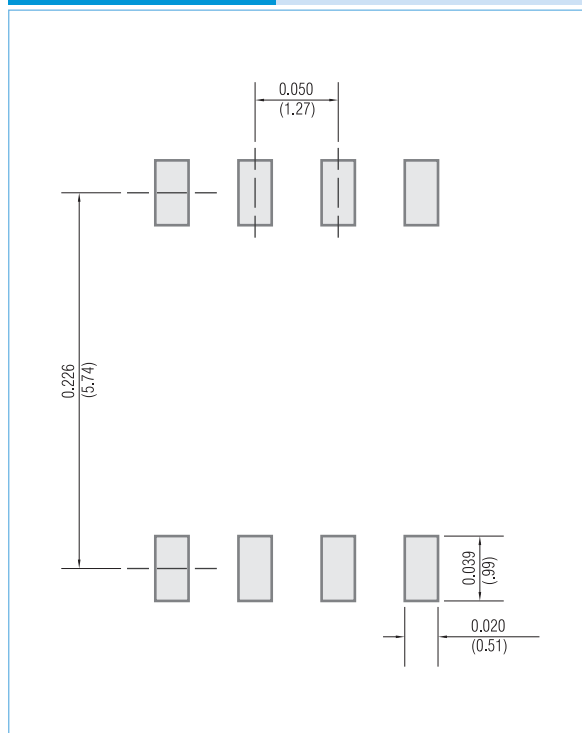
Fig.11 - Source-Drain Diode Forward Voltage

PJ6694

MOUNTING PAD LAYOUT

SOIC-08

Unit: inch (mm)



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ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

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