

PJ6676

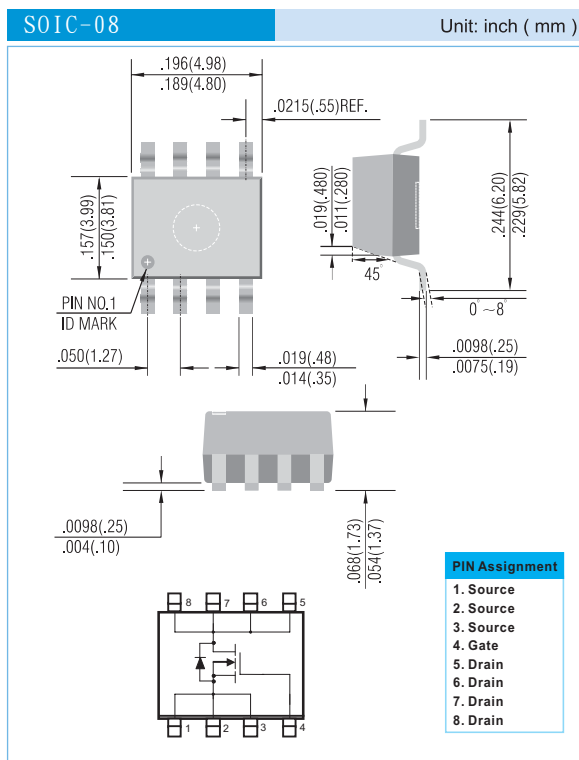
25V N-Channel Enhancement Mode MOSFET

FEATURES

- $R_{DS(ON)}, V_{GS}@10V, I_{DS}@15A=8m\Omega$
- $R_{DS(ON)}, V_{GS}@4.5V, I_{DS}@13A=12m\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters
- Fully Characterized Avalanche Voltage and Current
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICAL DATA

- Case: SOIC-08 Package
- Terminals : Solderable per MIL-STD-750D,Method 1036.3
- Marking : 6676



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	15	A
Pulsed Drain Current ¹⁾	I_{DM}	50	A
Maximum Power Dissipation $T_A=25^{\circ}C$ $T_A=75^{\circ}C$	P_D	2.5 1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^{\circ}C$
Avalanche Energy with Single Pulse ID=40A, VDD=25V, L=0.5mH	E_{AS}	400	mJ
Junction-to Ambient Thermal Resistance(PCB mounted) ²⁾	$R_{\theta JA}$	50	$^{\circ}C/W$

Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, $t \leq 10$ sec

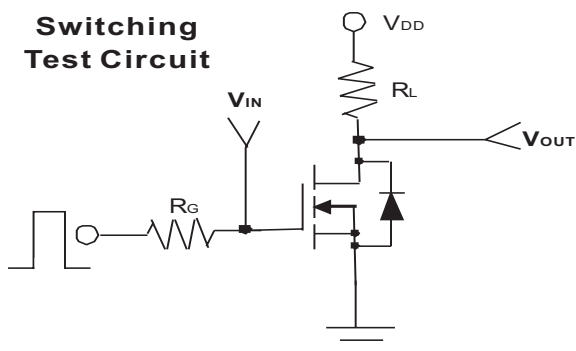
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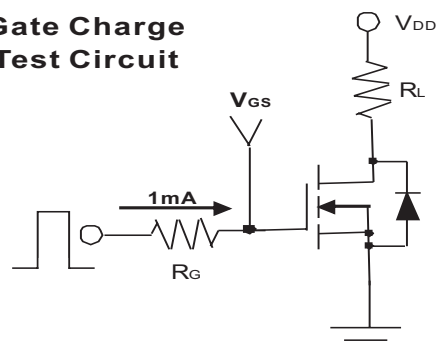
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	25	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =13A	-	9.6	12.0	mΩ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =15A	-	6.0	8.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =25V, V _{GS} =0V	-	-	1	uA
Gate Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =15A	30	-	-	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, I _D =15A, V _{GS} =5V	-	39	-	nC
		V _{DS} =15V, I _D =15A V _{GS} =10V	-	74	-	
Gate-Source Charge	Q _{gs}		-	8.3	-	
Gate-Drain Charge	Q _{gd}		-	14.2	-	
Turn-On Delay Time	T _{d(on)}	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V R _G =3.6Ω	-	17.2	21	ns
Turn-On Rise Time	t _{rr}		-	15	17	
Turn-Off Delay Time	t _{d(off)}		-	78	90	
Turn-Off Fall Time	t _f		-	30	42	
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1.0MH _z	-	3750	-	pF
Output Capacitance	C _{oss}		-	650	-	
Reverse Transfer Capacitance	C _{rss}		-	500	-	
Source-Drain Diode						
Max. Diode Forward Current	I _s	-	-	-	2.5	A
Diode Forward Voltage	V _{SD}	I _S =2.5A , V _{GS} =0V	-	0.73	1.2	V

Switching Test Circuit



Gate Charge Test Circuit



PJ6676

Typical Characteristics Curves ($T_J=25^\circ\text{C}$, unless otherwise noted)

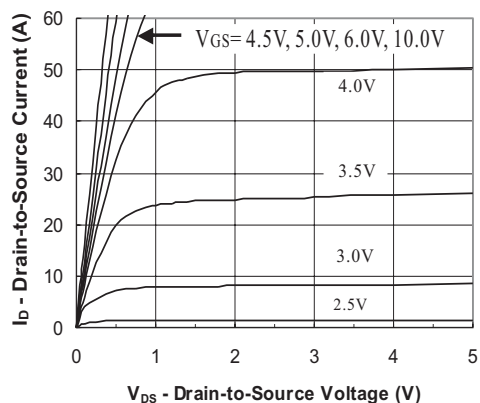


FIG.1- Output Characteristic

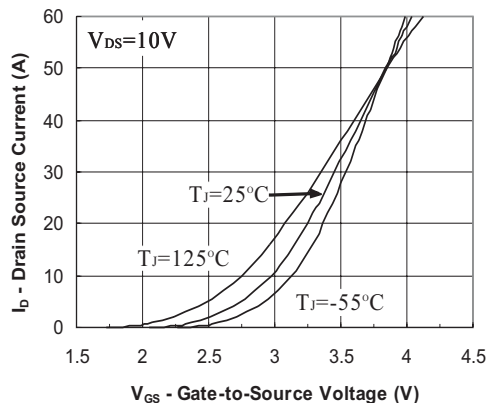


FIG.2- Transfer Characteristic

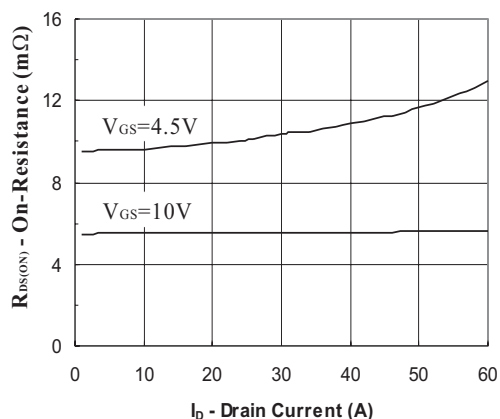


FIG.3- On Resistance vs Drain Current

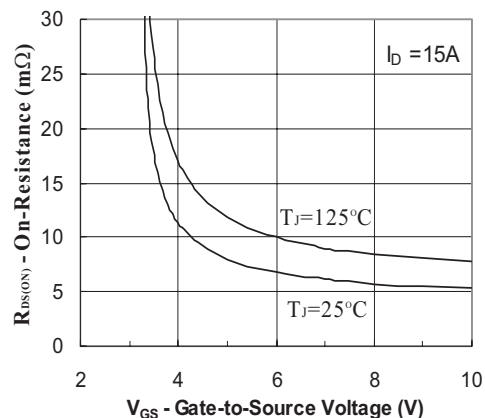


FIG.4- On Resistance vs Gate to Source Voltage

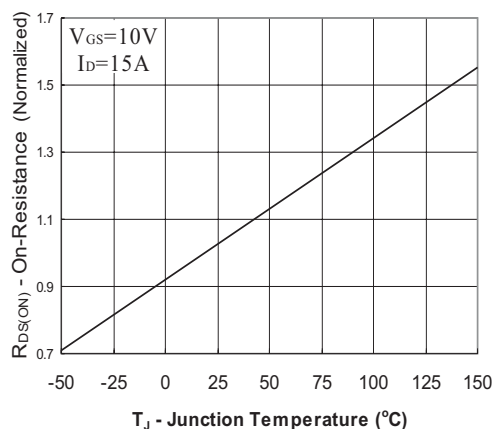


FIG.5- On Resistance vs Junction Temperature

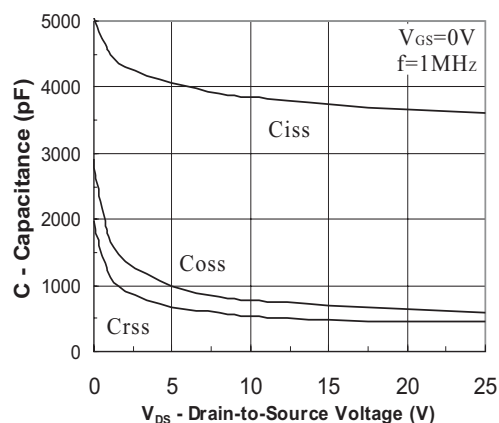
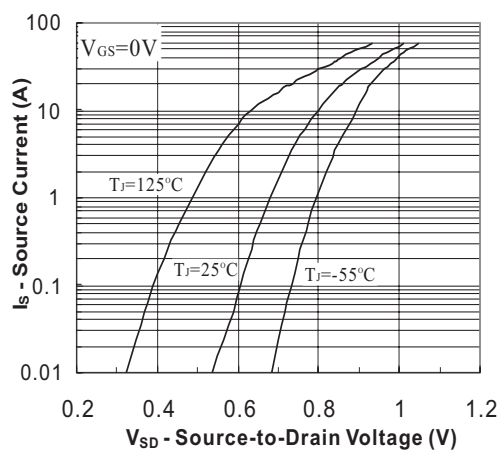
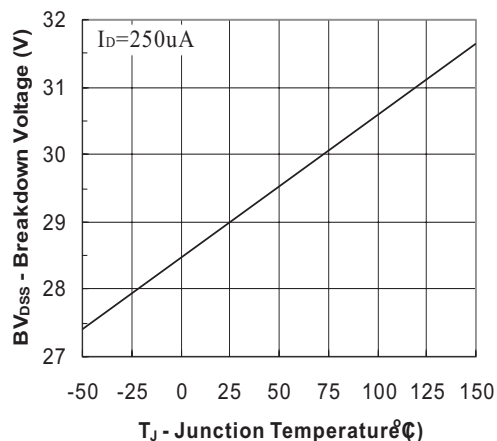
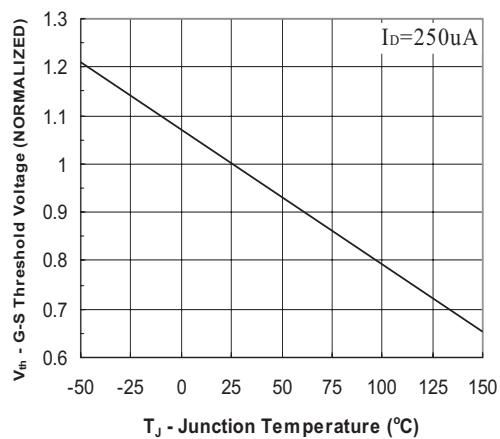
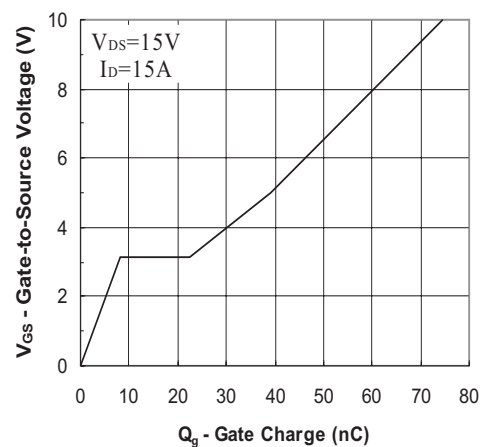
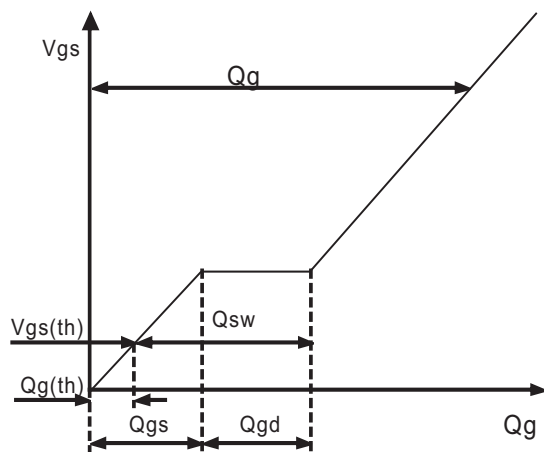


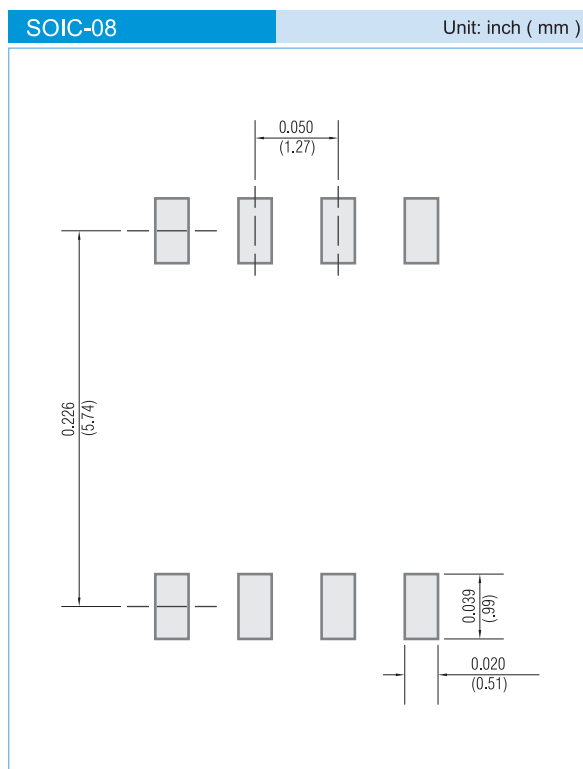
FIG.6- Capacitance

PJ6676



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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

LEGAL STATEMENT

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