

PJ2306

30V N-Channel Enhancement Mode MOSFET - ESD Protected

FEATURES

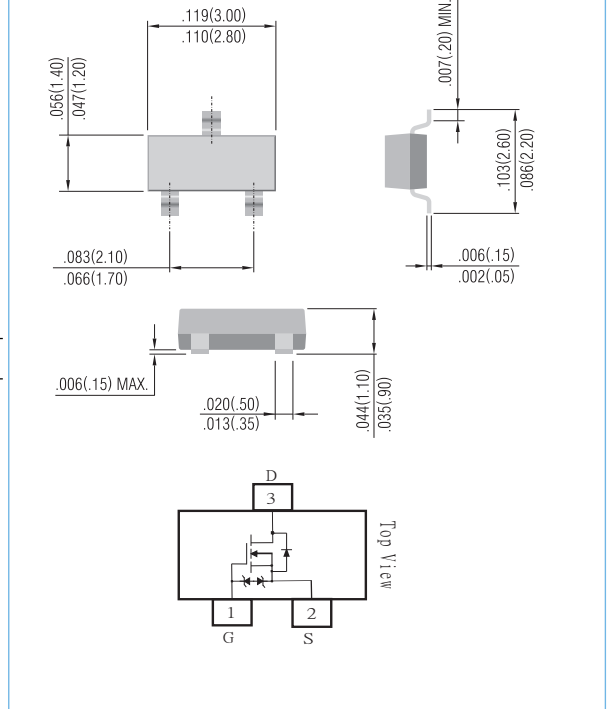
- $R_{DS(ON)}, V_{GS}@10V, I_{DS}@3.2A=65m\Omega$
- $R_{DS(ON)}, V_{GS}@4.5V, I_{DS}@2.8A=85m\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Load Switch, PWM Applications
- ESD Protected
- Component are in compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case: SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Marking : 06

SOT-23

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	3.2	A
Pulsed Drain Current ¹⁾	I _{DM}	16	A
Maximum Power Dissipation	P _D	T _A =25°C: 1.25 T _A =75°C: 0.75	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to + 150	°C
Junction-to Ambient Thermal Resistance(PCB mounted) ²	R _{θJA}	100	°C/W

Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, t ≤ 5 sec

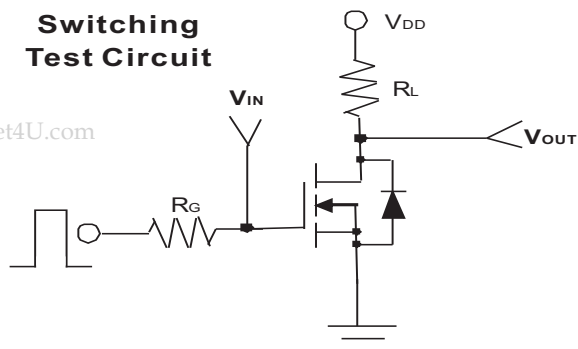
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ELECTRICAL CHARACTERISTICS

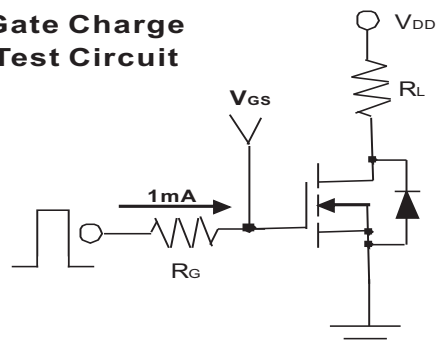
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=2.8A$		72	85	mΩ
	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.2A$		55	65	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	μA
Gate Body Leakage	I_{GSS}	$V_{GS}=\pm 16V, V_{DS}=0V$			±10	μA
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.8A$	3			S
Diode Forward Voltage	V_{SD}	$I_S=2.8A, V_{GS}=0V$		0.88	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=3.2A, V_{GS}=5V$		2.8	3.5	nC
				5.0	6.5	
Gate-Source Charge	Q_{gs}	$V_{DS}=15V, I_D=3.2A$ $V_{GS}=10V$		0.5		
Gate-Drain Charge	Q_{gd}			1.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=1A, V_{GEN}=10V$ $R_G=6\Omega$		8.6	11.2	ns
Rise Time	t_r			12.8	16.8	
Turn-Off Delay Time	$t_{d(off)}$			18.6	26	
Fall Time	t_f			1.9	2.6	
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1.0MHz$		270		pF
Output Capacitance	C_{oss}			45		
Reverse Transfer Capacitance	C_{rss}			30		

NOTE : Plus Test : Pluse Width ≤ 300us, Duty Cycle ≤ 2%.

Switching Test Circuit

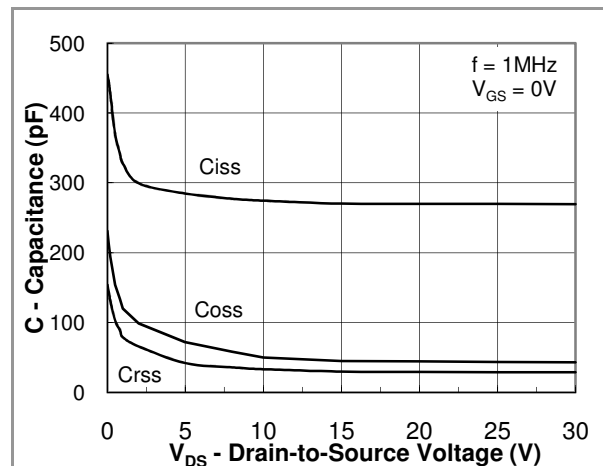
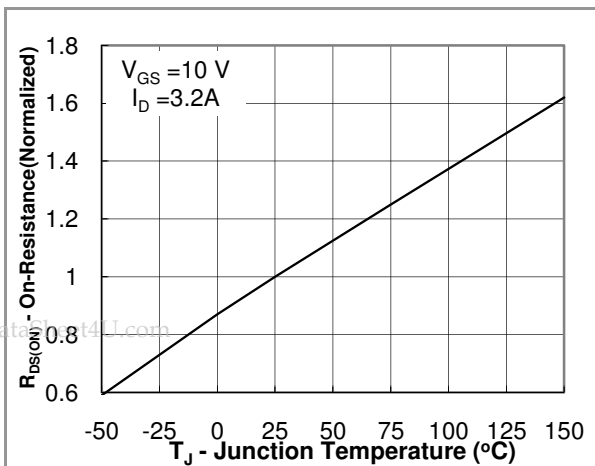
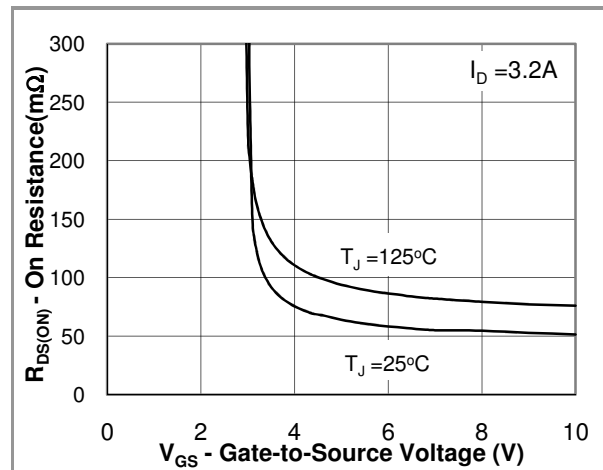
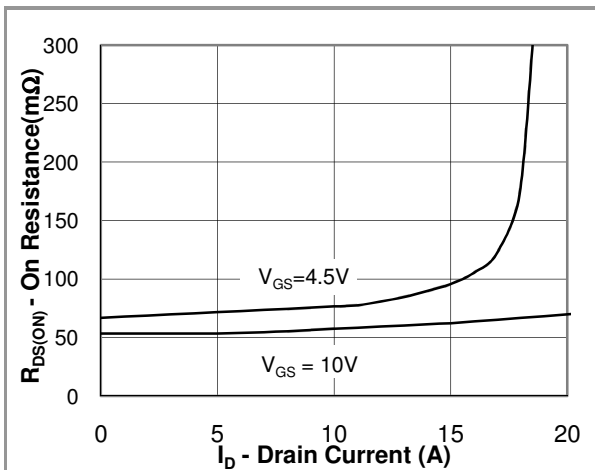
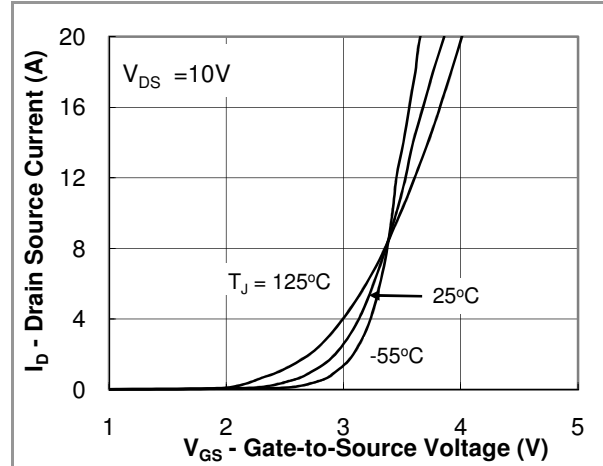
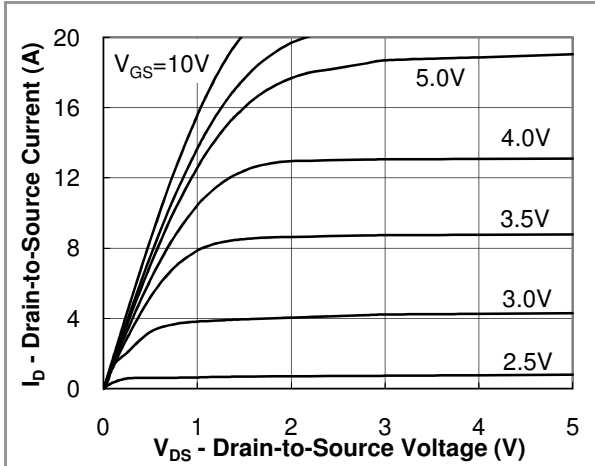


Gate Charge Test Circuit



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Typical Characteristics Curves ($T_a=25^{\circ}\text{C}$, unless otherwise noted)



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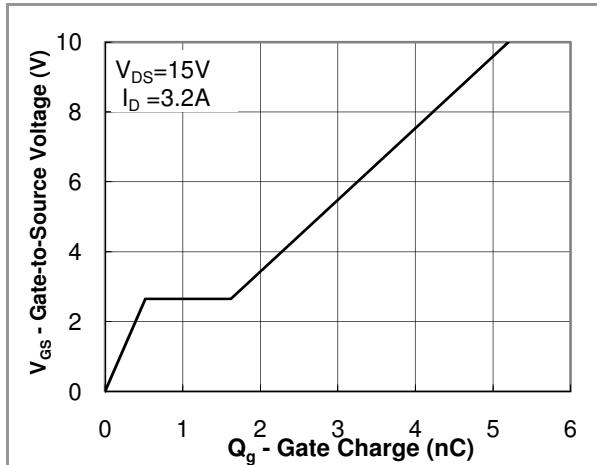


Fig. 7 Gate Charge Waveform

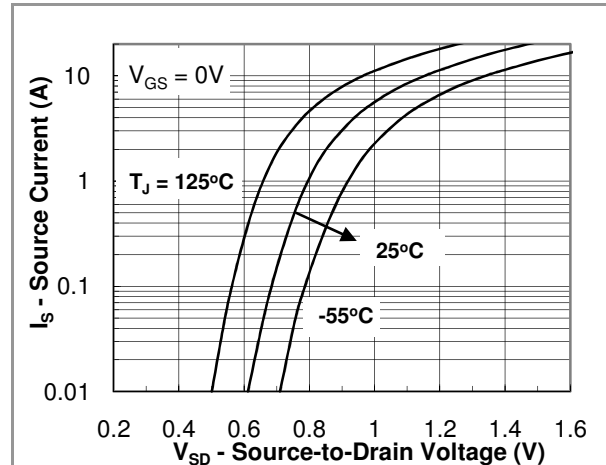


Fig. 8 Source-Drain Diode Forward Voltage

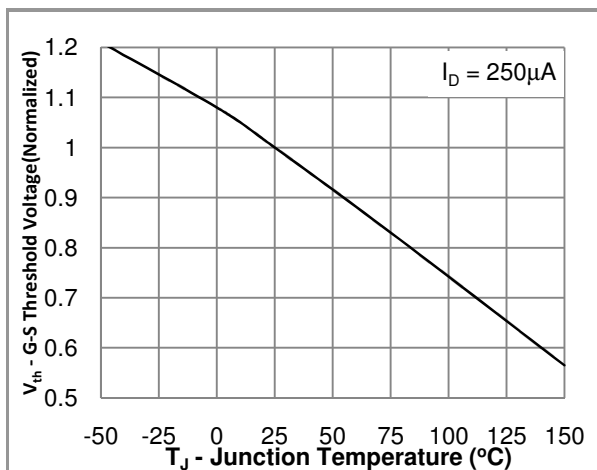


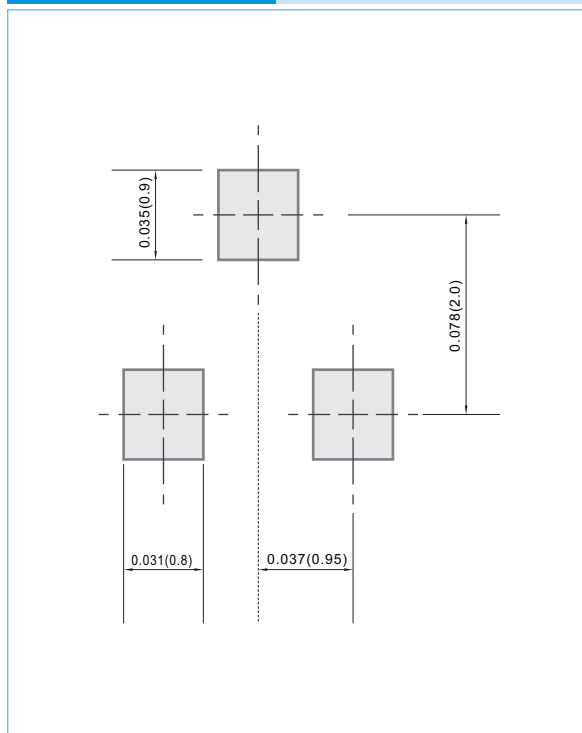
Fig. 9 Breakdown Voltage vs Junction Temperature

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MOUNTING PAD LAYOUT

SOT-23

Unit: inch (mm)



ORDER INFORMATION

- Packing information
T/R - 3K per 7" plastic Reel

LEGAL STATEMENT

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