Lead-free Green

PI7C9X130

PCI Express to PCI-X Reversible Bridge

DATASHEET

Revision 8

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A Product Line of Diodes Incorporated

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REVISION HISTORY

Date	Revision Number	Description
02/24/2006	0.1	First Draft of PI7C9X130 Data Sheet
03/20/2006	0.2	Correct INTA, B, C, D buffer type Update configuration map and registers Update JTAG chain order Add PCI/PCI-X selection information
04/07/2006	0.3	Update on configuration register bit definitions. 1) Bit [10, 7:2] of offset 40h 2) Bit [31:30] of offset 68h 3) Bit [0] of offset 70h 4) Bit [23:22] of offset 94h 5) Bit [7:1] of offset 164h Correct typo of pin CLKRUN_L in pin assignment and JTAG section.
06/07/2006	0.4	Add Absolute Maximum Ratings Correct pin description: 1. REQ_L as GPI and GNT_L as GPO 2. CLKOUT [8:0] as CLKOUT [6:0]
06/19/2006	0.5	Correct default setting for bit [31:30] of offset 68h
03/26/2007	0.6	
04/18/2007	0.7	Completed non-transparent function for address 28h – 2Bh in the Configuration Register Map – section 7.1 Corrected pin HSEN (R3) in section 2.6 – Miscellaneous Signals. Should read tie LOW if Hot Swap is not used instead of tie HIGH
05/02/2007	0.8	Revised table 8-1 in section 8 Address bit[5] corrected to equal 0 Address bit[4] corrected to equal GPIO[3]
05/15/2007	0.9	Revised PCIe Base Specification Compliancy from 1.0a to 1.1
06/08/2007	0.91	Corrected pin HSSW (T3) in section 2.6 – Miscellaneous Signals. Remove "Tied high if hot swap function is not used."
07/13/2007	1.0	Corrected bit[13] offset 110h from reserved to "Advisory Non-Fatal Error Status" Changed Logos and some font types
08/07/2007	1.1	Corrected Pin #'s of GNT_L[1], GNT_L[2], GNT_[3], GNT_[4], GNT_[5] on Table 14-1JTAG Boundary Scan Register Definition
09/28//2007	1.2	Recommendation of Pull-up Resistor for PI7C9X130 Control Signals added to section 16.3 of PI7C9X130 Datasheets; pin numbers of SMBCLK and SMBDAT are corrected under section 5.2. Added PCIX Clock Detection to Chapter 9, Clock Scheme.
01/03/2008	1.3	Revised Ambient Temperature Maximum Ratings Compliancy
04/21/2008	1.4	Updated to revision D
04/24/2008	1.5	Added package thermal data. RREF pin description change. Removed CDM information
08/08/2008	1.6	Added Power-Up Sequencing Description
10/30/2008	1.7	Revised Product Ordering Info
07/01/2009	1.8	Added Extended Configuration Access / Data Register under section 7.1 and 7.4
01/20/2010	1.9	Added Asynchronous Clock Support to Section 19
03/29/2010	2.0	Revised configuration register definitions: 1) 7.4.31 bit[5:4] and bit[7:6] of PCI Data Buffering Control Register)Offset 40h) 2) 7.4.87 Extended Configuration Access Address Register (Offset E0h) 3) 7.4.88 Extended Configuration Access Data Register (Offset E4h) 4) 7.4.129 bit[30] of Replay and Acknowledge Latency Timers (Offset 310h) 5) 7.5.24 bit[5:4] and bit[7:6] of PCI Data Buffering Control Register)Offset 40h) 6) 7.5.135 bit[30] of Replay and Acknowledge Latency Timers (Offset 310h) Revised Section 9 Clock Scheme
04/27/2011	2.1	Updated Section 2.2 PCI Express Signals

06/29/2011	2.2	Updated Section 2.3 PCI Signals (REQ_L [3:0], GNT_L [3:0]) Updated Section 7.5.9, 7.5.11, 7.5.12, 7.5.13, 7.5.34, 7.5.36, 7.5.37, 7.5.38 (bit[31:12]).
09/17/2012	2.3	Updated Section 7.4.70 Device Capability Register (bit[2:0]) Updated Section 7.5.76 Device Capability Register (bit[2:0])
04/15/2015	2.4	Updated Section 7.4 PCI Configuration Registers For Transparent Bridge Mode Updated Section 7.5 PCI Configuration Registers For Non-Transparent Bridge Mode
04/20/2016	2.5	Updated Section 7.4 PCI Configuration Registers For Transparent Bridge Mode Updated Section 7.5 PCI Configuration Registers For Non-Transparent Bridge Mode Updated Section 2.5 JTAG Boundary Scan Signals
06/02/2017	2.6	Updated Section 16.1 Absolute Maximum Ratings Updated Section 16.2 DC SPECIFICATIONS Added Table 16-4 PCIe Reference Clock Timing Parameters Added Table 16-5 PCI Express Interface - Differential Transmitter (TX) Output Characteristics Added Table 16-6 PCI Express Interface - Differential Receiver (RX) Input Characteristics Added Section 16.5 Operating Ambient Temperature
09/27/2017	3	Added Section 16 Power Sequencing Updated Section 19 Ordering Information Revision numbering system changed to whole number
03/16/2018	4	Updated Section 19 Ordering Information Added Figure 18-4 PART MARKING
07/30/2018	5	Updated Section 1.3 General Features Updated Section 2.6 Miscellaneous Signals Updated Section 19 Ordering Information
04/09/2020	6	Updated Section 16 Power Sequencing
09/14/2020	7	Updated Part Marking
01/07/2021	8	Updated Section 16 Power Sequencing Updated Figure 16-1 and 16-2

PREFACE

The datasheet of PI7C9X130 will be enhanced periodically when updated information is available. The technical information in this datasheet is subject to change without notice. This document describes the functionalities of PI7C9X130 (PCI Express Bridge) and provides technical information for designers to design their hardware using PI7C9X130.

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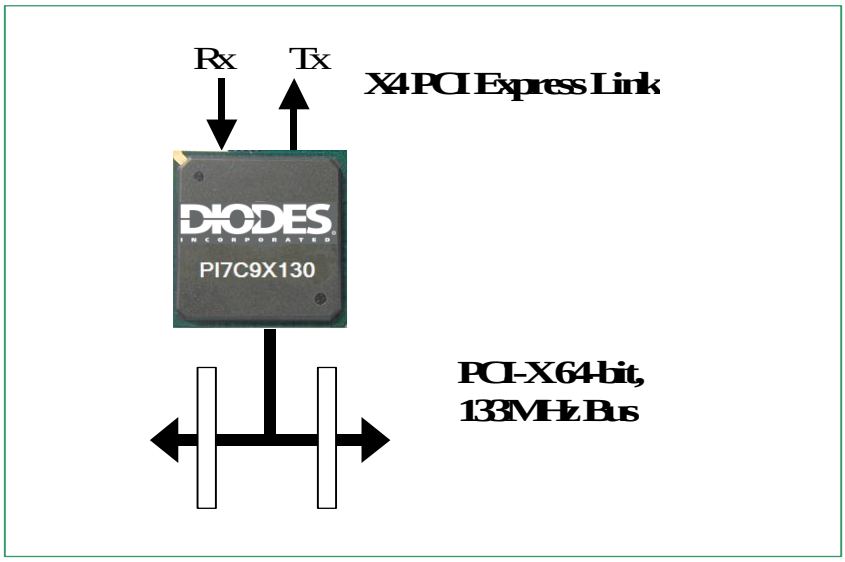
1 INTRODUCTION

PI7C9X130 is a PCIe-to-PCI/PCI-X bridge. PI7C9X130 is compliant with the *PCI Express Base Specification*, Revision 1.1, the *PCI Express Card Electromechnical Specification*, Revision 1.1, the *PCI Local Bus Specification*, Revision 3.0 and *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. PI7C9X130 supports transparent and non-transparent mode of operations. Also, PI7C9X130 supports forward and reverse bridging. In forward bridge mode, PI7C9X130 has an x4 PCI Express upstream port and a 64-bit PCI/PCI-X downstream port. The 64-bit PCI-X downstream port is 133MHz capable (see). In reverse bridge mode, PI7C9X130 has a 64-bit PCI-X upstream port and an x4 PCI Express downstream port. PI7C9X130 configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software and firmware is needed for the original operation.

Figure 1-1 PI7C9X130 Topology



1.1 PCI EXPRESS FEATURES

- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express Card Electromechnical Specification, Revision 1.1
- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Physical Layer interface (x4 link with 2.5Gb/s data rate)
- Lane polarity toggle
- Virtual isochronous support (upstream TC1-7 generation, downstream TC1-7 mapping)
- ASPM support
- Beacon support
- CRC (16-bit), LCRC (32-bit)
- ECRC and advanced error reporting
- PRBS (Pseudo Random Bit Sequencing) generator/checker for chip testing
- Maximum payload size to 512 bytes

1.2 PCI/PCI-X FEATURES

- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Bus PM Interface Specification, Revision 1.1
- Compliant with PCI Hot-Plug Specification, Revision 1.1
- Compliant with PCI Mobile Design Guide, Version 1.1
- Compliant with PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a
- PME support
- 3.3V PCI signaling with 5V I/O tolerance
- Provides two level arbitration support for six PCI Bus masters
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support

1.3 GENERAL FEATURES

- Compliant with Advanced Configuration and Power Interface Specification (ACPI), Revision 2.0b
- Compliant with System Management (SM) Bus, Version 2.0
- Forward bridging (PCI Express as primary bus, PCI as secondary bus)
- Reverse bridging (PCI as primary bus, PCI Express as secondary bus)
- Transparent mode support
- Non-transparent mode Support
- GPIO support (4 bi-directional pins)
- Power Management (including ACPI, CLKRUN_L, PCI_PM)
- Masquerade Mode (pre-loadable vendor, device, and revision IDs)
- EEPROM (I2C) Interface
- Industril Temp Compliant (-40˚C ~ +85˚C)
- SM Bus Interface
- Auxiliary powers (VAUX, VDDAUX, VDDCAUX) support
- Power consumption at about 1.5 Watt in typical condition
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

2 PIN DEFINITION

2.1 SIGNAL TYPES

TYPE OF SIGNAL	DESCRIPTION
B	Bi-directional
I	Input
IU	Input with pull-up
ID	Input with pull-down
IOD	Bi-directional with open drain output
OD	Open drain output
O	Output
P	Power
G	Ground

"_L" in signal name indicates Active LOW signal

2.2 PCI EXPRESS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
REFCLKP REFCLKN	D2, D1	I	**Reference Clock Input s:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors.
RAP RAN	F2, F1	I	**PCI Express data input s:** Differential data receiver input signals for lane A
RBP RBN	H2, H1	I	**PCI Express data input s:** Differential data receiver input signals for lane B
RCP RCN	K2, K1	I	**PCI Express data input s:** Differential data receiver input signals for lane C
RDP RDN	M2, M1	I	**PCI Express data input s:** Differential data receiver input signals for lane D
TAP TAN	E4, E3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane A
TBP TBN	G4, G3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane B
TCP TCN	J4, J3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane C
TDP TDN	L4, L3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane D
RREF	H4	I	**Resistor Reference:** It is used to connect an external resistor (2.1K Ohm +/- 1%) to VSS to provide a reference current for the driver and equalization circuit.
PERST_L	P1	B	**PCI Express Fundamental Reset:** PI7C9X130 uses this reset to initialize the internal state machines.

2.3 PCI SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
AD [31:0]	D5, A6, B6, C6, D6, A7, B7, C7, A8, B8, C8, D8, A9, B9, C9, D9, G16, G15, G14, G13, H16, H15, H14, H13, J15, J14, J13, K16, K15, K14, K13, L16	B	**Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of FBCLKIN when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X130 drives AD [31:0] to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
AD [63:32]	N11, P11, R11, T11, N12, P12, R12, T12, R13, T13, P14, R14, T14, T15, R15, R16, D16, C15, C16, B16, B15, A15, C14, B14, C13, B13, A13, D12, C12, B12, A12, D11	B	**Upper 32-bit Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of FBCLKIN when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X130 drives AD [63:32] to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
CBE [3:0]	D7, A10, F13, J16	B	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X130 drives CBE [3:0] signals to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
CBE [7:4]	P13, P15, A14, C11	B	**Upper 4-bit Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X130 drives CBE [7:4] signals to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
PAR	F14	B	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [31:0], CBE [3:0]. If PI7C9X130 is an initiator with a write transaction, PI7C9X130 will tri-state PAR. If PI7C9X130 is a target and a write transaction, PI7C9X130 will drive PAR one clock after the address or data phase. If PI7C9X130 is a target and a read transaction, PI7C9X130 will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X130 drives PAR to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
PAR64	D15	B	**Parity Bit for Upper 32-bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [63:32], CBE [7:4]. If PI7C9X130 is an initiator with a write transaction, PI7C9X130 will tri-state PAR64. If PI7C9X130 is a target and a write transaction, PI7C9X130 will drive PAR64 one clock after the address or data phase. If PI7C9X130 is a target and a read transaction, PI7C9X130 will drive PAR64 one clock after the address phase and tri-state PAR64 during data phases. PAR64 is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X130 drives PAR64 to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
FRAME_L	B10	B	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME_L indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
IRDY_L	C10	B	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
TRDY_L	D10	B	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
DEVSEL_L	A11	B	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, PI7C9X130 waits for the assertion of this signal within 5 cycles of FRAME_L assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.
STOP_L	B11	B	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a de-asserted state for one cycle.
LOCK_L	E13	B	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. PI7C9X130 does not support any upstream LOCK transaction.
IDSEL	M13	I	**Initialization Device Select:** Used as a chip select line for Type 0 configuration access to bridge's configuration space.
PERR_L	F16	B	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
SERR_L	F15	IOD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error condition. If SERR control is enabled, PI7C9X130 will drive this pin on: ▪ Address parity error ▪ Posted write data parity error on target bus ▪ Master abort during posted write transaction ▪ Target abort during posted write transaction ▪ Posted write transaction discarded ▪ Delayed write request discarded ▪ Delayed read request discarded ▪ Delayed transaction master timeout ▪ Errors reported from PCI Express port (advanced error reporting) in transparent mode. This signal is an open drain buffer that requires an external pull-up resistor for proper operation.
REQ_L [5:0]	P3, N3, T2, R2, P2, R1	I	**Request (Active LOW):** REQ_Ls are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ_Ls for at least 2 PCI clock cycles before asserting them again. If the device is in reverse mode or if external arbiter is selected (CFN_L=1), REQ_L [0] will be the bus grant input to PI7C9X130. Also, REQ_L [5:2] will become the GPI [3:0].
GNT_L [5:0]	T5, R5, P5, N5, T4, R4	O	**Grant (Active LOW):** PI7C9X130 asserts GNT_Ls to release PCI bus control to bus master devices. During idle and all GNT_Ls are de-asserted and arbiter is parking to PI7C9X130, PI7C9X130 will drive AD, CBE, and PAR to valid logic levels. If the device is in reverse mode or if external arbiter is selected (CFN_L=1), GNT_L [0] will be the bus request from PI7C9X130 to external arbiter. Also, GNT_L [5:2] will become the GPO [3:0].
REQ64_L	D14	B	**Request for 64-bit transfer (Active LOW):** PI7C9X130 asserts REQ64_L to request for 64-bit transactions on the PCI bus when PI7C9X130 is the bus master. REQ64_L is an input when PI7C9X130 is a target device.
ACK64_L	E16	B	**Acknowledge for 64-bit transfer (Active LOW):** When PI7C9X130 is a target device and drives ACK64_L to signal the bus master to use 64-bit transfer. When PI7C9X130 is the bus master, ACK64_L is an input.
CLKOUT [6:0]	N10, T9, R9, P9, N9, T8, R8	O	**PCI Clock Outputs:** PCI clock outputs are derived from the CLKIN and provide clocking signals to external PCI Devices.
RESET_L	N7	B	**RESET_L (Active LOW):** When RESET_L active, all PCI signals should be asynchronously tri-stated.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
INTA_L INTB_L INTC_L INTD_L	P4 R6 T10 N15	IOD	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA_L, INTB_L, INTC_L, INTD_L signals are inputs and asynchronous to the clock in the forward mode. In reverse mode, INTA_L, INTB_L, INTC_L, and INTD_L are open drain buffers for sending interrupts to the host interrupt controller.
FBCLKIN	B4	I	**Feedback Clock Input:** It connects to one of the CLKOUT [6:0] Output Signals and provides internal clocking to PI7C9X130 PCI bus interface.
CLKIN / M66EN	T6	I	**PCI Clock Input:** PCI Clock Input Signal connects to an external clock source. The PCI Clock Outputs CLKOUT [6:0] pins are derived from CLKIN Input. **M66EN Input:** It is driven high or low to enable the internal clock generator to provide clock outputs to CLKOUT[6:0] pins.

2.4 MODE SELECT AND STRAPPING SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TM2	P16	I	**Mode Select 2:** TM2 is a strapping pin. When TM2 is strapped low for normal operations and strapped high for testing functions. See table 3-1 for mode selection and 3-2 for strapping control for details.
TM1	A3	I	**Mode Select 1:** Mode Selection Pin to select EEPROM or SM Bus. TM1=0 for EEPROM (I2C) support and TM1=1 for SM Bus support. TM1 is also a strapping pin. See table 3-1 mode selection and 3-2 for strapping control.
TM0	A2	I	**Mode Select 0:** Mode Selection Pin to select transparent or non-transparent mode. TM0=0 for transparent bridge function mode and TM0=1 for non-transparent bridge function mode. TM0 is also a strapping pin. See table 3-1 for mode selection and 3-2 for strapping control.
MSK_IN	N16	I	**Mask Input for CLKOUT:** When it is strapped to high, hot-plug is enabled. See table 3-2 for strapping control.
REVRSB	N14	I	**Forward or Reverse Bridging Pin:** REVRSB pin controls the Forward (REVRSB=0) or Reverse (REVRSB=1) Bridge Mode of PI7C9X130. This pin is also a strapping pin. See table 3-1 for mode selection.
CFN_L	P7	ID	**Bus Central Function Control Pin (Active Low):** To enable the internal arbiter, CFN_L pin should be tied low. When it's tied high, an external arbiter is required to arbitrate the bus. In external arbiter mode, REQ_L [0] is re-configured to be the secondary bus grant input, and GNT_L [0] is reconfigured to be the secondary bus request output. Also, REQ_L [5:2] and GNT_L [5:2] become GPI [3:0] and GPO [3:0] respectively if external arbiter is selected. CFN_L has a weak internal pull-down resistor. See table 3-1 for mode selection.

2.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TCK	L13	IU	**Test Clock:** TCK is the test clock to synchronize the state information and data on the PCI bus side of PI7C9X130 during boundary scan operation. At normal operation mode, this pin should be left open (NC).
TMS	M16	IU	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.
TDO	M14	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. At normal operation mode, this pin should be left open (NC).

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TDI	M15	IU	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the PCI side of PI7C9X130. At normal operation mode, this pin should be left open (NC).
TRST_L	L14	IU	**Test Reset (Active LOW):** TRST_L is the test reset to initialize the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.

2.6 MISCELLANEOUS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
GPIO [6:0]	L15, R10, P10, R7, T7, N8, P8	B	**General Purpose I/O Data Pins:** The 7 general-purpose signals are programmable as either input-only or bi-directional signals by writing the GPIO output enable control register in the configuration space. See chapter 8 for more information.
SMBCLK / SCL	B5	B	**SMBUS / EEPROM Clock Pin:** When EEPROM (I2C) interface is selected (TM1=0), this pin is an output of SCL clock and connected to EEPROM clock input. When SMBUS interface is selected (TM1=1), this pin is an input for the clock of SMBUS.
SMBDAT / SDA	A5	B/IOD	**SMBUS / EEPROM Data Pin:** Data Interface Pin to EERPOM or SMBUS. When EEPROM (I2C) interface is selected (TM1=0), this pin is a bi-directional signal. When SMBUS interface is selected (TM1=1), this pin is an open drain signal.
PME_L	C5	B	**Power Management Event Pin:** Power Management Event Signal is asserted to request a change in the device or link power state.
CLKRUN_L	C4	B	**Clock Run Pin (Active LOW):** The Clock Run signal, for mobile environment, is asserted and de-asserted to indicate the status of the PCI Clock.
PCIXCAP	A4	I	**PCI-X Capability Pin:** PI7C9X130 can be forced to PCI mode if PCIXCAP is tied to ground with a capacitor (0.01uF) in parallel. If PCIXCAP is connected to ground through a capacitor (0.01uF), PI7C9X130 will be in 133MHz PCI-X mode. If PCIXCAP is connected to ground through a resistor (10K Ohm) with a capacitor (0.01uF) in parallel, PI7C9X130 will be in 66MHz PCI-X mode.
PCIXUP	B3	O	**PCIXCAP Pull-up driver:** PI7C9X130 drives this pin for PCI-X mode detection.
DEV64	E15	I	**Control 64-bit bus width:** PI7C9X130 operates with 64-bit bus when DEV64=1. When DEV64=0, PI7C9X130 operates with 32-bit bus.
SEL100	E14	I	**Select 100MHz frequency:** When SEL100=1, PI7C9X130 expects to run at 100MHz clock. When SEL100=0, PI7C9X130 expects to run at 133MHz..
HSEN	R3	I	**Hot Swap Enable:** PI7C9X130 supports hot swap when HSEN is set to high. Tie LOW if hot swap function is not used.
HSSW	T3	I	**Hot Swap Switch:** PI7C9X130 detects HSSW input to monitor the insertion or impending extraction of a board.
LOO	N6	O	**LED On/Off:** PI7C9X130 drives LOO for LED illumination that signals the operator to extract the board.
ENUM_L	P6	OD	**ENUM_L signal:** PI7C9X130 drives ENUM_L to notify the system host that either a board has been freshly inserted or is about to be extracted.

2.7 POWER AND GROUND PINS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDA	E2, J1, J2, H3	P	**Analog Voltage Supply for PCI Express Interface:** Connect to the 1.8V Power Supply.
VDDP	G2, F3, J5, M3, N2	P	**Digital Voltage Supply for PCI Express Interface:** Connect to the 1.8V Power Supply.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDAUX	F4, L1	P	**Auxiliary Voltage Supply for PCI Express Interface:** Connect to the 1.8V Power Supply.
VTT	G1, L5	P	**Termination Supply Voltage for PCI Express Interface:** Connect to the 1.8V Power Supply.
VDDA_PLL	D3	P	**Analog Voltage Supply for PLL at PCI Interface:** Connect to the 1.8V Power Supply.
VDDP_PLL	C2	P	**Digital Voltage Supply for PLL at PCI Interface:** Connect to the 1.8V Power Supply.
VDDC	M5, M6, M11, M12, J11, H11, E11, E10, K5, A1	P	**Core Supply Voltage:** Connect to the 1.8V Power Supply.
VDDCAUX	H5	P	**Auxiliary Core Supply Voltage:** Connect to the 1.8V Power Supply.
VD33	T1, N4, M7, M8, M9, L10, L11, M10, T16, N13, L12, K12, K11, J12, H12, G11, G12, F12, A16, D13, E12, F11, E9, E8, E7, E6, E5	P	**I/O Supply Voltage for PCI Interface:** Connect to the 3.3V Power Supply for PCI I/O Buffers.
VAUX	B2	P	**Auxiliary I/O Supply Voltage for PCI interface:** Connect to the 3.3V Power Supply.
VSS	B1, C1, C3, D4, F5, E1, G5, K3, K4, L2, N1, M4, L6, K6, L7, K7, L8, L9, K8, K9, K10, J6, J7, J8, J9, J10, H8, H9, H10, G10, F10, F9, F8, F7, F6, G9, G8, G7, G6, H7, H6	P	**Ground:** Connect to Ground.

2.8 PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VDDC	E1	VSS	J1	VDDA	N1	VSS
A2	TM0	E2	VDDA	J2	VDDA	N2	VDDP
A3	TM1	E3	TAN	J3	TCN	N3	REQ_L[4] / GPI[2]
A4	PCIXCAP	E4	TAP	J4	TCP	N4	VD33
A5	SMBDAT / SDA	E5	VD33	J5	VDDP	N5	GNT_L[2] / GPO[0]
A6	AD[30]	E6	VD33	J6	VSS	N6	LOO
A7	AD[26]	E7	VD33	J7	VSS	N7	RESET_L
A8	AD[23]	E8	VD33	J8	VSS	N8	GPIO[1]
A9	AD[19]	E9	VD33	J9	VSS	N9	CLKOUT[2]
A10	CBE[2]	E10	VDDC	J10	VSS	N10	CLKOUT[6]
A11	DEVSEL_L	E11	VDDC	J11	VDDC	N11	AD[63]
A12	AD[33]	E12	VD33	J12	VD33	N12	AD[59]
A13	AD[37]	E13	LOCK_L	J13	AD[5]	N13	VD33
A14	CBE[5]	E14	SEL100	J14	AD[6]	N14	REVRSB
A15	AD[42]	E15	DEV64	J15	AD[7]	N15	INTD_L
A16	VD33	E16	ACK64_L	J16	CBE[0]	N16	MSK_IN
B1	VSS	F1	RAN	K1	RCN	P1	PERST_L
B2	VAUX	F2	RAP	K2	RCP	P2	REQ_L[1]
B3	PCIXUP	F3	VDDP	K3	VSS	P3	REQ_L[5] / GPI[3]
B4	FBCLKIN	F4	VDDAUX	K4	VSS	P4	INTA_L
B5	SMBCLK / SCL	F5	VSS	K5	VDDC	P5	GNT_L[3] / GPO[1]
B6	AD[29]	F6	VSS	K6	VSS	P6	ENUM_L

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B7	AD[25]	F7	VSS	K7	VSS	P7	CFN_L
B8	AD[22]	F8	VSS	K8	VSS	P8	GPIO[0]
B9	AD[18]	F9	VSS	K9	VSS	P9	CLKOUT[3]
B10	FRAME_L	F10	VSS	K10	VSS	P10	GPIO[4]
B11	STOP_L	F11	VD33	K11	VD33	P11	AD[62]
B12	AD[34]	F12	VD33	K12	VD33	P12	AD[58]
B13	AD[38]	F13	CBE[1]	K13	AD[1]	P13	CBE[7]
B14	AD[40]	F14	PAR	K14	AD[2]	P14	AD[53]
B15	AD[43]	F15	SERR_L	K15	AD[3]	P15	CBE[6]
B16	AD[44]	F16	PERR_L	K16	AD[4]	P16	TM2
C1	VSS	G1	VTT	L1	VDDAUX	R1	REQ_L[0]
C2	VDDP_PLL	G2	VDDP	L2	VSS	R2	REQ_L[2] / GPI[0]
C3	VSS	G3	TBN	L3	TDN	R3	HSEN
C4	CLKRUN_L	G4	TBP	L4	TDP	R4	GNT_L[0]
C5	PME_L	G5	VSS	L5	VTT	R5	GNT_L[4] / GPO[2]
C6	AD[28]	G6	VSS	L6	VSS	R6	INTB_L
C7	AD[24]	G7	VSS	L7	VSS	R7	GPIO[3]
C8	AD[21]	G8	VSS	L8	VSS	R8	CLKOUT[0]
C9	AD[17]	G9	VSS	L9	VSS	R9	CLKOUT[4]
C10	IRDY_L	G10	VSS	L10	VD33	R10	GPIO[5]
C11	CBE[4]	G11	VD33	L11	VD33	R11	AD[61]
C12	AD[35]	G12	VD33	L12	VD33	R12	AD[57]
C13	AD[39]	G13	AD[12]	L13	TCK	R13	AD[55]
C14	AD[41]	G14	AD[13]	L14	TRST_L	R14	AD[52]
C15	AD[46]	G15	AD[14]	L15	GPIO[6]	R15	AD[49]
C16	AD[45]	G16	AD[15]	L16	AD[0]	R16	AD[48]
D1	REFCLKN	H1	RBN	M1	RDN	T1	VD33
D2	REFCLKP	H2	RBP	M2	RDP	T2	REQ_L[3] / GPI[1]
D3	VDDA_PLL	H3	VDDA	M3	VDDP	T3	HSSW
D4	VSS	H4	RREF	M4	VSS	T4	GNT_L[1]
D5	AD[31]	H5	VDDCAUX	M5	VDDC	T5	GNT_L[5] / GPO[3]
D6	AD[27]	H6	VSS	M6	VDDC	T6	CLKIN / M66EN
D7	CBE[3]	H7	VSS	M7	VD33	T7	GPIO[2]
D8	AD[20]	H8	VSS	M8	VD33	T8	CLKOUT[1]
D9	AD[16]	H9	VSS	M9	VD33	T9	CLKOUT[5]
D10	TRDY_L	H10	VSS	M10	VD33	T10	INTC_L
D11	AD[32]	H11	VDDC	M11	VDDC	T11	AD[60]
D12	AD[36]	H12	VD33	M12	VDDC	T12	AD[56]
D13	VD33	H13	AD[8]	M13	IDSEL	T13	AD[54]
D14	REQ64_L	H14	AD[9]	M14	TDO	T14	AD[51]
D15	PAR64	H15	AD[10]	M15	TDI	T15	AD[50]
D16	AD[47]	H16	AD[11]	M16	TMS	T16	VD33

3 MODE SELECTION AND PIN STRAPPING

3.1 FUNCTIONAL MODE SELECTION

If TM2 is strapped to low, PI7C9X130 uses TM1, TM0, CFN_L, and REVRSB pins to select different modes of operations. These four input signals are required to be stable during normal operation. One of the sixteen combinations of normal operation can be selected by setting the logic values for the four mode select pins. For example, if the logic values are low for all four (TM1, TM0, CFN_L, and REVRSB) pins, the normal operation will have EEPROM (I2C) support in transparent mode with internal arbiter in forward bridge mode. The designated operation with respect to the values of the TM1, TM0, CFN_L, and REVRSB pins are defined on Table 3-1:

Table 3-1 Functional Mode Selection

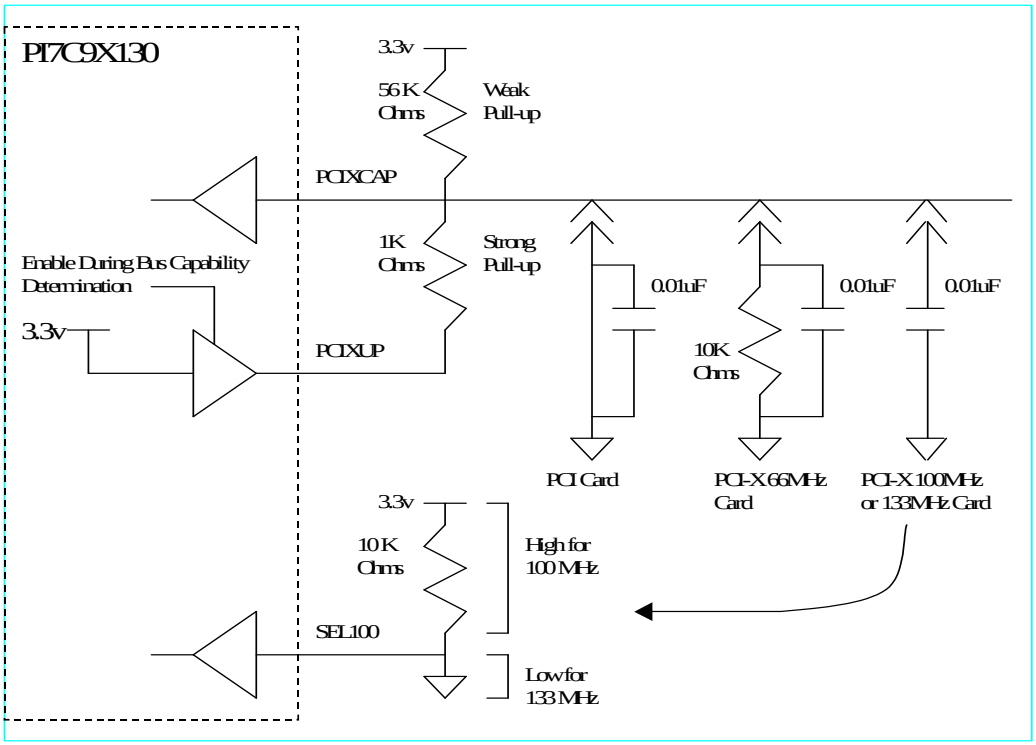
TM2 Strapped	TM1	TM0	CFN_L	REVRSB	Functional Mode
0	0	X	X	X	EEPROM (I2C) support
0	1	X	X	X	SM Bus support
0	X	0	X	X	Transparent mode
0	X	1	X	X	Non-Transparent mode
0	X	X	0	X	Internal arbiter
0	X	X	1	X	External arbiter
0	X	X	X	0	Forward bridge mode
0	X	X	X	1	Reverse bridge mode

3.2 PCI/PCI-X SELECTION

The secondary interface is capable of operating in either conventional PCI mode or in PCI-X mode. PI7C9X130 controls the mode and frequency for the secondary bus by utilizing a pull-up circuit connected to PCIXCAP. There are two pull-up resistors in the circuit as recommended by the PCI-X addendum. The first resistor is a weak pull-up (56K ohms) whose value is selected to set the voltage of PCIXCAP below its low threshold when a PCI-X 66MHz device is attached to the secondary bus. The second resistor is a strong pull-up, externally wired between PCIXCAP and PCIXUP. The value of the resistor (1K ohm) is selected to set the voltage of PCIXCAP above its high threshold when all devices on the secondary are PCI-X 66MHz capable. To detect the mode and frequency of the secondary bus, PCIXUP is initially disabled and PI7C9X130 samples the value on PCIXCAP.

If PI7C9X130 sees logic LOW on PCIXCAP, one or more devices on the secondary have either pulled the signal to ground (PCI-X 66MHz capable) or tied it to ground (only capable of conventional PCI mode). To differentiate between the two conditions, PI7C9X130 then enables PCIXUP to put the strong pull-up into the circuit node. If PCIXCAP remains at logic LOW, it must be tied to ground by one or more devices, and the bus is initialized to conventional PCI mode. If PCIXUP can be pulled up, one or more devices are capable of only PCI-X 66MHz operation so the bus is initialized to PCI-X 66MHz mode. If PI7C9X130 sees logic HIGH on PCIXCAP, then all devices on the secondary bus are capable of PCI-X 100MHz or 133MHz operation. PI7C9X130 then samples SEL100 to distinguish between the 100MHz and 133MHz clock frequencies. If PI7C9X130 sees logic HIGH on SEL100, the secondary bus is initialized to PCI-X 100MHz mode. If the value is LOW, PCI-X 133MHz is initialized. These two clock frequencies allow the flexibility to support different bus loading conditions.

Figure 3-1 PCI / PCI-X Selection



3.3 PIN STRAPPING

If TM2 is strapped to high, PI7C9X130 uses TM1, TM0, and MSK_IN as strapping pins. The strapping functions are listed in Table 3-2 to show the states of operations during the PCI Express PERST_L de-assertion transition in forward bridge mode or PCI RESET_L de-assertion transition in reverse bridge mode.

Table 3-2 Pin Strapping

TM2 Strapped	TM1 Strapped	TM0 Strapped	MSK_IN Strapped	Test Functions
1	0	0	1	PLL test
1	0	1	1	Shorten initialization test with Hot-Plug enabled
1	1	0	1	Functional loopback test
1	1	1	1	Bridge test (PRBS, IDDQ, etc.)
1	0	0	0	Reserved
1	0	1	0	Shorten initialization test with Hot-Plug disabled
1	1	0	0	Reserved
1	1	1	0	Reserved

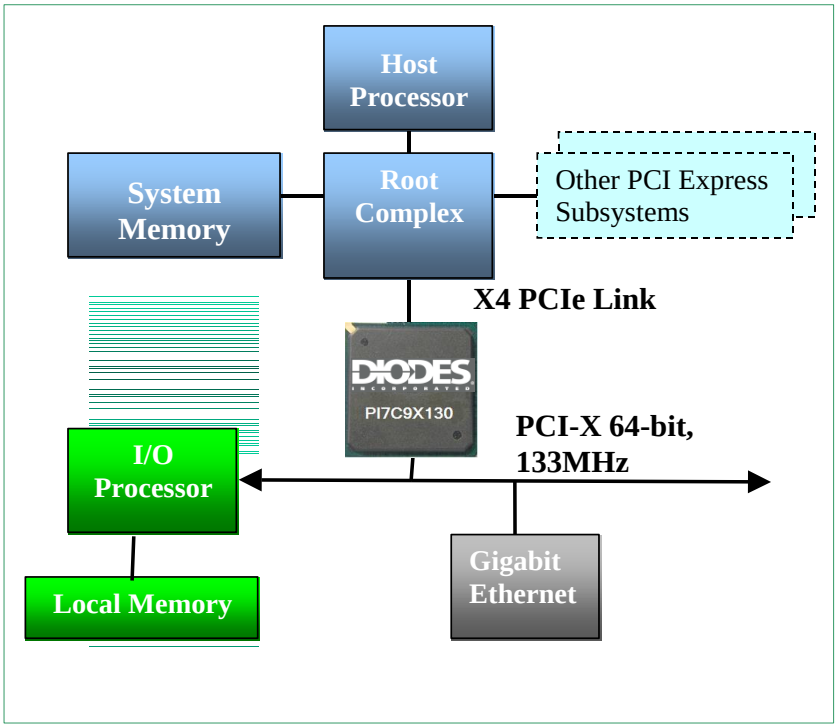
4 FORWARD AND REVERSE BRIDGING

PI7C9X130 supports forward or reverse and transparent or non-transparent combination modes of operation. For example, when PI7C9X130 is operating in forward (REVRSB=0) and non-transparent bridge mode (TM0=1) shown in Figure 4-1, its PCI Express interface is connected to a root complex and its PCI-X bus interface is connected to PCI-X devices. Another example, PI7C9X130 can be configured as a reverse (REVRSB=1) and transparent (TM0=0) bridge shown in Figure 4-2.

The non-transparent bridge feature of PI7C9X130 allows the I/O Processor to be isolated from the Host Processor and its memory map which avoiding memory address conflict when both host and I/O processors are needed side-by-side.

PCI/PCI-X based systems and peripherals are ubiquitous in the I/O interconnect technology market today. It will be a tremendous effort to convert existing PCI/PCI-X based products to be used in PCI Express systems. PI7C9X130 provides a solution to bridge existing PCI/PCI-X based products to the latest PCI Express technology.

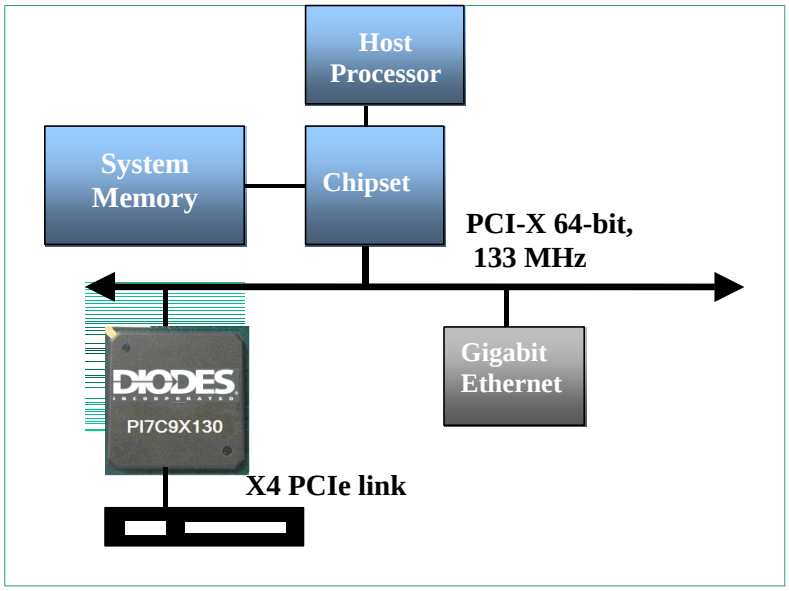
Figure 4-1 Forward and Non-transparent Mode



In reverse (REVRSB=1) and transparent (TM0=0) mode shown in Figure 3-2, PI7C9X130 becomes a PCI-to-PCI Express bridge that its PCI-X bus interface is connected to the host chipset between and the PCI Express x4 link. It enables the legacy PCI/PCI-X Host Systems to provide PCI Express capability.

PI7C9X130 provides a solution to convert existing PCI/PCI-X based designs to adapt quickly into PCI Express base platforms. Existing PIC/PCI-X based applications will not have to undergo a complete re-architecture in order to interface to PCI Express technology.

Figure 4-2 Reverse and Transparent Mode



5 TRANSPARENT AND NON-TRANSPARENT BRIDGING

5.1 TRANSPARENT MODE

In transparent bridge mode, base class code of PI7C9X130 is set to be 06h (bridge device). The sub-class code is set to be 04h (PCI-to-PCI bridge). Programming interface is 00h. Hence, PI7C9X130 is not a subtractive decoding bridge.

PI7C9X130 has type-1 configuration header if TM0 is set to 0 (transparent bridge mode). These configuration registers are the same as traditional transparent PCI-to-PCI Bridge. In fact, it is backward compatible to the software that supporting traditional transparent PCI-to-PCI bridges. Configuration registers can be accessed from several different ways. For PCI Express access, PCI Express configuration transaction is in forward bridge mode. For PCI access, PCI configuration cycle is mainly in reverse bridge mode. However, PI7C9X130 allows PCI configuration access in forward mode as secondary bus configuration access. For I2C access, I2C bus protocol is used with EEPROM selected (TM1=0). For SM bus access, SM bus protocol is used with SM bus selected (TM1=1).

5.2 NON-TRANSPARENT MODE

In non-transparent bridge mode, base class code of PI7C9X130 is set to be 06h (bridge device). The sub-class code is set to be 80h (other bridge). Programming interface is 00h. Hence, PI7C9X130 is not a subtractive decoding bridge.

PI7C9X130 has type-0 configuration header if TM0 is set to 1 (non-transparent mode). The configuration registers are similar to a traditional PCI device. However, there is one set of configuration registers for the primary interface and another set of configuration registers for the secondary interface. In addition, CSRs (Control and Status Registers) are implemented to support the memory or IO transfers between the primary and secondary buses. The CSRs are accessed through memory transaction access within the lowest memory range of 4K Space (bit [64:12] are zeros). The non-transparent configuration registers can be accessed through several different ways (PCI Express, PCI, I2C, and SM bus). For PCI Express and PCI access, the type-0 configuration transactions need to be used. For I2C access, I2C bus protocol needs to be used through I2C bus interface. For SM bus access, SM bus protocol needs to be used through SM bus interface. The hardware pins (B5 and A5) are shared for I2C and SM bus interface. If TM1=0, pins B5 and A5 will be SCL and SDA for I2C interface respectively. If TM1=1, pins B5 and A5 will be SMBCLK and SMBDAT for SM Bus interface respectively.

In non-transparent bridge mode, PI7C9X130 supports four or three memory BARs (Base Address Registers) and one or two IO BARs (Base Address Registers) depending on selection on the primary bus. Also, PI7C9X130 supports four or three memory BARs (Base Address Registers) and one or two IO BARs (Base Address Registers) depending on selection on the secondary bus.

Offset 10h is defined to be primary CSR and downstream memory 0 BAR. Offset 14h is defined to be primary CSR and downstream IO BAR. Offset 18h is defined to be downstream memory 1 or IO BAR (selectable by CSR setup register). Offset 1Ch is defined to be downstream memory 2 BAR. Offset 20h and 24h are defined to be downstream memory 3 lower BAR and memory 3 upper BAR respectively to support 64-bit decoding.

The direct offset translation of address from primary to secondary bus will be done by substituting the original Base Address at primary with the downstream Translation Base Address Register values and keeping the lower address bits the same to form a new address for forward the transaction to secondary bus.

For downstream memory 2, it uses direct address translation. There is no lookup table for downstream memory address translation.

Offset 50h is defined to be secondary CSR and upstream memory 0 BAR. Offset 54h is defined to be secondary CSR and upstream IO BAR. Offset 58h is defined to be upstream memory 1 or IO BAR (selectable by CSR setup register offset E4h). Offset 1Ch is defined to be upstream memory 2 BAR. Offset 60h and 64h are defined to be upstream memory 3 lower BAR and memory 3 upper BAR respectively to support 64-bit decoding.

The direct offset translation of address from secondary to primary bus will be done by substituting the original Base Address at secondary with the upstream Translation Base Address Register values and keeping the lower address bits the same to form a new address for forward the transaction to primary bus.

For upstream memory 2, it uses lookup table address translation method which using the original base address as index to select a new address on the upstream memory 2 lookup table based on the page and window size defined.

Table 5-1 Non-Transparent Registers

Non-transparent Registers	Typical Access
Primary CSR and Memory 0 BAR	Configuration access offset 10h
Downstream Memory 0 Translated Base	Configuration access offset 98h
Downstream Memory 0 Setup	Configuration access offset 9Ch
Primary CSR I/O BAR	Configuration access offset 14h
Downstream I/O or Memory 1 BAR	Configuration access offset 18h
Downstream I/O or Memroy 1 Translated Base	Configuration access offset A8h
Donwstream I/O or Memroy 1 Setup	Configuration access offset ACh
Downstream Memory 2 BAR	Configuration access offset 1Fh
Downstream Memory 2 Translated Base	Lower 4K I/O or Memory access offset 008h
Downstream Memory 2 Setup	Lower 4K I/O or Memory access offset 00Ch
Downstream Memory 3 BAR	Configuration access offset 23h
Downstream Memory 2 Setup	Lower 4K I/O or Memory access offset 00Ch
Downstream Memory 3 BAR	Configuration access offset 23h
Downstream Memory 2 Setup	Lower 4K I/O or Memory access offset 00Ch
Downstream Memory 3 BAR	Configuration access offset 23h
Secondary CSR Memory 0 BAR	Configuration access offset 50h
Upstream Memory 0 Translated Base	Configuration access offset E0h
Upstream Memory 0 Setup	Configuration access offset E4h
Secondary CSR I/O BAR	Configuration access offset 54h
Upstream I/O or Memory 1 BAR	Configuration access offset 58h
Upstream I/O or Memory 1 Translated Base	Configuration access offset E8h
Upstream I/O or Memory 1 Setup	Configuration access offset ECh
Upstream Memory 2 BAR	Configuration access offset 5Fh
Upstream Memory 2 Lookup Table Offset	Lower 4K I/O or Memory access offset 050h
Upstream Memory 2 Lookup Table Data	Lower 4K I/O or Memory access offset 054h
Upstream Memory 2 Lookup Table (64 32-bit entries)	Lower 4K I/O or Memory access offset 100h to 1FFh
Upstream Memory 3 BAR	Configuration access offset 63h
Upstream Memory 3 Upper 32-bit BAR	Configuration access offset 67h
Upstream Memory 3 Setup	Lower 4K I/O or Memory access offset 34h
Upstream Memory 3 Upper 32-bit Setup	Lower 4K I/O or Memory access offset 38h

6 PCI EXPRESS FUNCTIONAL OVERVIEW

6.1 TLP STRUCTURE

PCI Express TLP (Transaction Layer Packet) Structure is comprised of format, type, traffic class, attributes, TLP digest, TLP poison, and length of data payload.

There are four TLP formats defined in PI7C9X130 based on the states of FMT [1] and FMT [0] as shown on Table 6-1.

Table 6-1 TLP Format

FMT [1]	FMT [0]	TLP FORMAT
0	0	3 double word, without data
0	1	4 double word, without data
1	0	3 double word, with data
1	1	4 double word, with data

Data payload of PI7C9X130 can range from 4 (1DW) to 256 (64DW) bytes. PI7C9X130 supports three TLP routing mechanisms. They are comprised of Address, ID, and Implicit routings. Address routing is being used for Memory and IO requests. ID based (bus, device, function numbers) routing is being used for configuration requests. Implicit routing is being used for message routing. There are two message groups (baseline and advanced switching). The baseline message group contains INTx interrupt signaling, power management, error signaling, locked transaction support, slot power limit support, vendor defined messages, hot-plug signaling. The other is advanced switching support message group. The advanced switching support message contains data packet and signal packet messages. Advanced switching is beyond the scope of PI7C9X130 implementation.

The r [2:0] values of the "type" field will determine the destination of the message to be routed. All baseline messages must use the default traffic class zero (TC0).

6.2 VIRTUAL ISOCHRONOUS OPERATION

This section provides a summary of Virtual Isochronous Operation supported by PI7C9X130. Virtual Isochronous support is disabled by default. Virtual Isochronous feature can be turned on with setting bit [26] of offset 40h to one. Control bits are designated for selecting which traffic class (TC1-7) to be used for upstream (PCI Express-to-PCI). PI7C9X130 accepts only TC0 packets of configuration, IO, and message packets for downstream (PCI Express-to-PCI). If configuration, IO and message packets have traffic class other than TC0, PI7C9X130 will treat them as malformed packets. PI7C9X130 maps all downstream memory packets from PCI Express to PCI transactions regardless the virtual isochronous operation is enabled or not.

7 CONFIGURATION REGISTERS

PI7C9X130 supports Type-0 (non-transparent bridge mode) and Type-1 (transparent bridge mode) configuration space headers and Capability ID of 01h (PCI power management) to 10h (PCI Express capability structure).

With pin REVRSB = 0, device-port type (bit [7:4]) of capability register will be set to 7h (PCI Express-to-PCI/PIC-X bridge). When pin REVRSB = 1, device-port type (bit [7:4]) of capability register will be set to 8h (PCI/PCI-X-to-PCI Express bridge).

PI7C9X130 supports PCI Express capabilities register structure with capability version set to 1h (bit [3:0] of offset 02h).

When pin TM0=0, PI7C9X130 will be in transparent bridge mode and the configuration registers for transparent bridge should be used.

When pin TM0=1, PI7C9X130 will be in non-transparent bridge mode and the configuration registers for non-transparent bridge should be used.

7.1 CONFIGURATION REGISTER MAP

PI7C9X130 supports capability pointer with PCI-X (ID=07h), PCI power management (ID=01h), PCI bridge sub-system vendor ID (ID=0Dh), PCI Express (ID=10h), vital product data (ID=03h), and message signaled interrupt (ID=05h). Hot swap (ID=06h) can be enabled by setting HSEN=1. Slot identification (ID=04h) is off by default and can be turned on through configuration programming.

Table 7-1 Configuration Register Map (00h – FFh)

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
01h - 00h	01h – 00h	Vendor ID	Vendor ID	Yes[1]	Yes[5]
03h – 02h	03h – 02h	Device ID	Device ID	Yes[1]	Yes[5]
05h – 04h	45h – 44h	Command Register	Primary Command Register	No	Yes
07h – 06h	47h – 46h	Primary Status Register	Primary Status Register	No	Yes
0Bh – 08h	0Bh – 08h	Class Code and Revision ID	Class Code and Revision ID	Yes[1]	Yes[5]
0Ch	4Ch	Cacheline Size Register	Primary Cacheline Size Register	-	-
0Dh	4Dh	Primary Latency Timer	Primary Latency Timer	No	Yes
0Eh	4Eh	Header Type Register	Header Type Register	No	Yes
0Fh	4Fh	Reserved	Reserved	-	-
13h – 10h	53h – 50h	Reserved	Primary CSR	No	Yes

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
			and Memory 0 BAR		
17h – 14h	57h – 54h	Reserved	Primary CSR I/O BAR	No	Yes
18h	58h	Primary Bus Number Register	Downstream I/O or Memory 1 BAR	No	Yes
19h	59h	Secondary Bus Number Register	Downstream I/O or Memory 1 BAR	No	Yes
1Ah	5Ah	Subordinate Bus Number Register	Downstream I/O or Memory 1 BAR	No	Yes
1Bh	5Bh	Secondary Latency Timer	Downstream I/O or Memory 1 BAR	No	Yes
1Ch	5Ch	I/O Base Register	Downstream Memory 2 BAR	No	Yes
1Dh	5Dh	I/O Limit Register	Downstream Memory 2 BAR	No	Yes
1Fh – 1Eh	5Fh – 5Eh	Secondary Status Register	Downstream Memory 2 BAR	No	Yes
21h – 20h	61h – 60h	Memory Base Register	Downstream Memory 3 BAR	No	Yes
23h – 22h	63h – 62h	Memory Limit Register	Downstream Memory 3 BAR	No	Yes
25h – 24h	65h – 64h	Prefetchable Memory Base Register	Downstream Memory 3 Upper 32-bit BAR	No	Yes
27h – 26h	67h - 66h	Prefetchable Memory Limit Register	Downstream Memory 3 Upper 32-bit BAR	No	Yes
2Bh – 28h	2Bh – 28h	Prefetchable Memory Base Upper 32-bit Register	Reserved	No	Yes
2Dh – 2Ch	2Dh – 2Ch	Prefetchable Memory Limit Upper 32-bit Register	Subsystem Vendor ID	Yes[2]	Yes[5]
2Fh – 2Eh	2Fh – 2Eh	Prefetchable Memory Limit Upper 32-bit Register	Subsystem ID	Yes[2]	Yes[5]
31h – 30h	31h – 30h	I/O Base Upper 16-bit Register	Reserved	No	Yes
33h – 32h	33h – 32h	I/O Limit Upper 16-bit Register	Reserved	No	Yes
34h	34h	Capability Pointer	Capability Pointer	No	Yes
37h – 35h	37h – 35h	Reserved	Reserved	No	Yes
3Bh – 38h	3Bh – 38h	Reserved	Reserved	No	Yes
3Ch	7Ch	Interrupt Line	Primary	No	Yes

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
			Interrupt Line		
3Dh	7Dh	Interrupt Pin	Primary Interrupt Pin	No	Yes
3Eh	7Eh	Bridge Control	Primary Min_Gnt	Yes[3]	Yes[3]
3Fh	7Fh	Bridge Control	Primary Max_Lat	Yes[3]	Yes[3]
41h – 40h	41h – 40h	PCI Data Buffering Control	PCI Data Buffering Control	Yes	Yes
43h – 42h	43h – 42h	Chip Control 0	Chip Control 0	Yes	Yes
45h – 44h	05h – 04h	Reserved	Secondary Command Register	No	Yes
47h – 46h	07h – 06h	Reserved	Secondary Status Register	No	Yes
4Bh – 48h	4Bh – 48h	Arbiter Mode, Enable, Priority	Arbiter Mode, Enable, Priority	Yes	Yes
4Ch	0Ch	Reserved	Secondary Cacheline Size Register	No	Yes
4Dh	0Dh	Reserved	Secondary Status Register	No	Yes
4Eh	0Eh	Reserved	Header Type	No	Yes
4Fh	0Fh	Reserved	Reserved	-	-
53h – 50h	13h – 10h	Reserved	Secondary CSR and Memory 0 BAR	No	Yes
57h – 54h	17h – 14h	Reserved	Secondary CSR I/O BAR	No	Yes
5Bh – 58h	1Bh – 18h	Reserved	Upstream I/O or Memory 1 BAR	No	Yes
5Fh – 5Ch	1Fh – 1Ch	Reserved	Upstream Memory 2 BAR	No	Yes
63h – 60h	23h – 20h	Reserved	Upstream Memory 3 BAR	No	Yes
67h – 64h	27h – 24h	Reserved	Upstream Memory 3 Upper 32-bit BAR	No	Yes
69h – 68h	69h – 68h	PCI Express Tx and Rx Control	PCI Express Tx and Rx Control	Yes	Yes
6Ah	6Ah	Reserved	Memory Address Forwarding Control	Yes[3]	Yes[3]
6Bh	6Bh	Reserved	Reserved	No	Yes
6Dh – 6Ch	6Dh – 6Ch	Reserved	Subsystem Vendor ID	Yes[2]	Yes[5]
6Fh – 6Eh	6Fh – 6Eh	Reserved	Subsystem ID	Yes[2]	Yes[5]
73h – 70h	73h – 70h	EEPROM (I2C) Control and Status Register	EEPROM (I2C) Control and status Register	No	Yes
77h – 74h	77h – 74h	Hot Swap Capability	Hot Swap Capability	No	Yes

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
7Bh – 78h	7Bh – 78h	GPIO Data and Control (20 bits) Reserved (12 bits)	GPIO Data and Control (20 bits) Bridge Control and Status (10 bits) Reserved (2 bits)	No No No	Yes No No
7Ch	3Ch	Reserved	Secondary Interrupt Line	No	Yes
7Dh	3Dh	Reserved	Secondary Interrupt Pin	No	Yes
7Eh	3Eh	Reserved	Secondary Min_Gnt	Yes[3]	Yes[3]
7Fh	3Fh	Reserved	Secondary Max_Lat	Yes[3]	Yes[3]
83h – 80h	83h – 80h	PCI-X Capability	PCI-X Capability	No	Yes
87h – 84h	87h – 84h	PCI-X Bridge Status	PCI-X Bridge Status	No	Yes
8Bh – 88h	8Bh – 88h	Upstream Split Transaction	Upstream Split Transaction	No	Yes
8Fh – 8Ch	8Fh – 8Ch	Downstream Split Transaction	Downstream Split Transaction	No	Yes
93h – 90h	93h – 90h	Power Management Capability	Power Management Capability	Yes	Yes
97h – 94h	97h – 94h	Power Management Control and Status	Power Management Control and Status	No	Yes
9Bh – 98h	9Bh – 98h	Reserved	Downstream Memory 0 Translated Base	No	Yes
9Fh – 9Ch	9Fh – 9Ch	Reserved	Downstream Memory 0 Setup	Yes[3]	Yes[3]
A3h – A0h	A3h – A0h	Slot ID Capability	Slot ID Capability	No	Yes
A7h – A4h	A7h – A4h	PCI Clock and CLKRUN Control	PCI Clock and CLKRUN Control	Yes	Yes
ABh – A8h	ABh – A8h	SSID and SSVID Capability	Downstream I/O or Memory 1 Translated Base	No	Yes
Afh – ACh	Afh – ACh	Subsystem ID and Subsystem Vendor ID	Downstream I/O or Memory 1 Setup	Yes	Yes
B3h – B0h	B3h – B0h	PCI Express Capability	PCI Express Capability	No	Yes
B7h – B4h	B7h – B4h	Device Capability	Device Capability	Yes	Yes
BBh – B8h	BBh – B8h	Device Control	Device Control	No	Yes

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
		and Status	and Status		
BFh – BCh	BFh – BCh	Link Capability	Link Capability	Yes	Yes
C3h – C0h	C3h – C0h	Link Control and Status	Link Control and Status	No	Yes
C7h – C4h	C7h – C4h	Slot Capability	Slot Capability	No	Yes
CBh – C8h	CBh – C8h	Slot Control and Status	Slot Control and Status	No	Yes
CFh – CCh	CFh – CCh	XPIP Configuration Register 0	XPIP Configuration Register 0	Yes	Yes
D3h – D0h	D3h – D0h	XPIP Configuration Register 1	XPIP Configuration Register 1	Yes	Yes
D6h – D4h	D6h – D4h	XPIP Configuration Register 2	XPIP Configuration Register 2	Yes	Yes
D7h	D7h	Hot Swap Switch debounce counter	Hot Swap Switch debounce counter	Yes	Yes
DBh – D8h	DBh – D8h	VPD Capability Register	VPD Capability Register	No	Yes
DFh – DCh	DFh – DCh	VPD Data Register	VPD Data Register	Yes[4]	Yes
E3h – E0h	E3h – E0h	Extended Configuration Access Address Register	Upstream Memory 0 Translated Base	No	Yes
E7h – E4h	E7h – E4h	Extended Configuration Access Data Register	Upstream Memory 0 setup	Yes[3]	Yes[3]
EBh – E8h	EBh – E8h	Reserved	Upstream I/O or Memory 1 Translated Base	No	Yes
EFh – ECh	EFh – ECh	Reserved	Upstream I/O or Memory 1 Setup	Yes[3]	Yes[3]
F3h – F0h	F3h – F0h	MSI Capability Register	MSI Capability Register	No	Yes
F7h – F4h	F7h – F4h	Message Address	Message Address	No	Yes
FBh – F8h	FBh – F8h	Message Upper Address	Message Upper Address	No	Yes
FFh – FCh	FFh – FCh	Message Data	Message Data	No	Yes

Note [1]: When masquerade is enabled, it is pre-loadable.
Note [2]: When both masquerade and non-transparent mode are enabled, it is pre-loadable.
Note [3]: When non-transparent mode is enabled, it is pre-loadable.
Note [4]: The VPD data is read/write through I2C during VPD operation.
Note [5]: Read access only.

7.2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP

PI7C9X130 also supports PCI Express Extended Capabilities with from 257-byte to 4096-byte space. The offset range is from 100h to FFFh. The offset 100h is defined for Advance Error Reporting (ID=0001h). The offset 150h is defined for Virtual Channel (ID=0002h).

Table 7-2 PCI Express Extended Capability Register Map (100h – FFFh)

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
103h – 100h	103h – 100h	Advanced Error Reporting (AER) Capability	Advanced Error Reporting (AER) Capability	No	Yes[5]
107h – 104h	107h – 104h	Uncorrectable Error Status	Uncorrectable Error Status	No	Yes
10Bh – 108h	10Bh – 108h	Uncorrectable Error Mask	Uncorrectable Error Mask	No	Yes
10Fh – 10Ch	10Fh – 10Ch	Uncorrectable Severity	Uncorrectable Severity	No	Yes
113h – 110h	113h – 110h	Correctable Error Status	Correctable Error Status	No	Yes
117h – 114h	117h – 114h	Correctable Error Mask	Correctable Error Mask	No	Yes
11Bh – 118h	11Bh – 118h	AER Control	AER Control	No	Yes
12Bh – 11Ch	12Bh – 11Ch	Header Log Register	Header Log Register	No	Yes
12Fh – 12Ch	12Fh – 12Ch	Secondary Uncorrectable Error Status	Secondary Uncorrectable Error Status	No	Yes
133h – 130h	133h – 130h	Secondary Uncorrectable Error Mask	Secondary Uncorrectable Error Mask	No	Yes
137h – 134h	137h – 134h	Secondary Uncorrectable Severity	Secondary Uncorrectable Severity	No	Yes
13Bh – 138h	13Bh – 138h	Secondary AER Control	Secondary AER Control	No	Yes
14Bh – 13Ch	14Bh – 13Ch	Secondary Header Log Register	Secondary Header Log Register	No	Yes
14Fh – 14Ch	14Fh – 14Ch	Reserved	Reserved	No	Yes
153h – 150h	153h – 150h	VC Capability	VC Capability	No	Yes
157h – 154h	157h – 154h	Port VC Capability 1	Port VC Capability 1	No	Yes
15Bh – 158h	15Bh – 158h	Port VC Capability 2	Port VC Capability 2	No	Yes
15Fh – 15Ch	15Fh – 15Ch	Port VC Status and Control	Port VC Status and Control	No	Yes
163h – 160h	163h – 160h	VC0 Resource Capability	VC0 Resource Capability	No	Yes
167h – 164h	167h – 164h	VC0 Resource Control	VC0 Resource Control	No	Yes

Primary Bus Configuration Access for both Transparent and Non-transparent mode or Secondary Bus Configuration Access for Transparent Mode	Secondary Bus Configuration Access for Non-Transparent Mode only	Transparent Mode (type1)	Non-Transparent Mode (Type0)	EEPROM (I2C) Access	SM Bus Access
16Bh – 168h	16Bh – 168h	VC0 Resource Status	VC0 Resource Status	No	Yes
2FFh – 170h	2FFh – 170h	Reserved	Reserved	No	Yes
303h – 300h	503h – 500h	Extended GPIO Data and Control	Extended GPIO Data and Control	No	Yes
307h – 304h	507h – 504h	Extended GPI/GPO Data and Control	Extended GPI/GPO Data and Control	No	Yes
30Fh – 308h	50Fh – 508h	Reserved	Reserved	No	No
310h	510h	Replay and Acknowledge Latency Timer	Replay and Acknowledge Latency Timer	Yes	Yes
4FFh – 314h	4FFh – 314h	Reserved	Reserved	No	No
503h – 500h	303h – 300h	Reserved	Reserved	No	No
504h	304h	Reserved	Reserved	No	No
50Fh – 505h	30Fh – 305h	Reserved	Reserved	No	No
510h	310h	Reserved	Reserved	No	No
FFFh – 514h	FFFh – 514h	Reserved	Reserved	No	No

Note [5]: Read access only.

7.3 CONTROL AND STATUS REGISTER MAP

Table 7-3 Control and Status Register (CSR) Map (000h – FFFh)

PCI Express / PCI Memory Offset	SM Bus Offset	Register Name	Reset Value	EEPROM (I2C) Access	SM Bus Access
007h – 000h	207h – 200h	Reserved	0	No	Yes
00Bh – 008h	20Bh – 208h	Downstream Memory 2 Translated Base	XXXX_XXXXh	No	Yes
00Fh – 00Ch	20Fh – 20Ch	Downstream Memory 2 Setup	0000_0000h	Yes	Yes
013h – 010h	213h – 210h	Downstream Memory 3 Translated Base	XXXX_XXXXh	No	Yes
017h – 014h	217h – 214h	Downstream Memory 3 Setup	0000_0000h	Yes	Yes
01Bh – 018h	21Bh – 218h	Downstream Memory 3 Upper 32-bit Setup	0000_0000h	Yes	Yes
02Fh – 01Ch	22Fh – 21Ch	Reserved	0	No	Yes
033h – 030h	233h – 230h	Reserved	X	No	Yes
037h – 034h	237h – 234h	Upstream Memory 3 Setup	0000_0000h	Yes	Yes
03Bh – 038h	21Bh – 218h	Upstream	0000_0000h	Yes	Yes

PCI Express / PCI Memory Offset	SM Bus Offset	Register Name	Reset Value	EEPROM (I2C) Access	SM Bus Access
		Memory 3 Upper 32-bit Setup			
04Fh – 03Ch	24Fh – 23Ch	Reserved	0	No	Yes
050h	250h	Lookup Table Offset Register	XXh	No	Yes
053h – 051h	253h – 251h	Reserved	0	No	Yes
057h – 054h	257h – 254h	Lookup Table Data Register	XXXX_XXXXh	No	Yes
05Bh – 058h	25Bh – 258h	Upstream Page Boundary IRQ 0	0000_0000h	No	Yes
05Fh – 05Ch	25Fh – 25Ch	Upstream Page Boundary IRQ 1	0000_0000h	No	Yes
063h – 060h	263h – 260h	Upstream Page Boundary IRQ Mask 0	FFFF_FFFFh	No	Yes
067h – 064h	267h – 264h	Upstream Page Boundary IRQ Mask 1	FFFF_FFFFh	No	Yes
06Fh – 068h	26Fh – 268h	Reserved	0	No	Yes
071h – 070h	271h – 270h	Primary Clear IRQ Register	0000h	No	Yes
073h – 072h	273h – 272h	Secondary Clear IRQ Register	0000h	No	Yes
075h – 074h	275h – 274h	Primary Set IRQ Register	0000h	No	Yes
077h – 076h	277h – 276h	Secondary Set IRQ Register	0000h	No	Yes
079h – 078h	279h – 278h	Primary Clear IRQ Mask Register	FFFFh	No	Yes
07Bh – 07Ah	27Bh – 27Ah	Secondary Clear IRQ Mask Register	FFFFh	No	Yes
07Dh – 07Ch	27Dh – 27Ch	Primary Set IRQ Mask Register	FFFFh	No	Yes
07Fh – 07Eh	27Fh – 27Eh	Secondary Set IRQ Mask Register	FFFFh	No	Yes
09Fh – 080h	29Fh – 280h	Reserved	0	No	Yes
0A3h – 0A0h	2A3h – 2A0h	Scratch pad 0	XXXX_XXXXh	No	Yes
0A7h – 0A4h	2A7h – 2A4h	Scratch pad 1	XXXX_XXXXh	No	Yes
0ABh – 0A8h	2ABh – 2A8h	Scratch pad 2	XXXX_XXXXh	No	Yes
0AFh – 0ACh	2AFh – 2ACh	Scratch pad 3	XXXX_XXXXh	No	Yes
0B3h – 0B0h	2B3h – 2B0h	Scratch pad 4	XXXX_XXXXh	No	Yes
0B7h – 0B4h	2B7h – 2B4h	Scratch pad 5	XXXX_XXXXh	No	Yes
0BBh – 0B8h	2BBh – 2B8h	Scratch pad 6	XXXX_XXXXh	No	Yes
0BFh – 0BCh	2BCh – 2BFh	Scratch pad 7	XXXX_XXXXh	No	Yes
0FFh – 0C0h	2FFh – 2C0h	Reserved	0	No	Yes
1FFh – 100h	3FFh – 300h	Upstream Memory 2 Lookup Table	0	No	Yes
FFFh – 200h	11FFh – 400h	Reserved	0	No	Yes

7.4 PCI CONFIGURATION REGISTERS FOR TRANSPARENT BRIDGE MODE

The following section describes the configuration space when the device is in transparent mode. The descriptions for different register type are listed as follow:

Register Type	Descriptions
RO	Read Only
ROS	Read Only and Sticky
RW	Read/Write
RO(WS)	Read Only at primary interface and Read/Write at secondary interface
RWC	Read/Write "1" to clear
RWS	Read/Write and Sticky
RWCS	Read/Write "1" to clear and Sticky

7.4.1 VENDOR ID – OFFSET 00h

Bit	Function	Type	Description
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. Returns 12D8h when read.

7.4.2 DEVICE ID – OFFSET 00h

Bit	Function	Type	Description
31:16	Device ID	RO	Identifies this device as the PI7C9X130. Returns E130 when read.

7.4.3 COMMAND REGISTER – OFFSET 04h

Bit	Function	Type	Description
0	I/O Space Enable	RW	0: Ignore I/O transactions on the primary interface 1: Enable response to memory transactions on the primary interface Reset to 0
1	Memory Space Enable	RW	0: Ignore memory read transactions on the primary interface 1: Enable memory read transactions on the primary interface Reset to 0
2	Bus Master Enable	RW	0: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on the secondary interface 1: Enable the bridge to operate as a master on the primary interfaces for memory and I/O transactions forwarded from the secondary interface. If the primary of the reverse bridge is PCI-X mode, the bridge is allowed to initiate a split completion transaction regardless of the status bit. Reset to 0
3	Special Cycle Enable	RO	0: PI7C9X130 does not respond as a target to Special Cycle transactions, so this bit is defined as Read-Only and must return 0 when read Reset to 0
4	Memory Write and Invalidate Enable	RO	0: PI7C9X130 does not originate a Memory Write and Invalidate transaction. Implements this bit as Read-Only and returns 0 when read (unless forwarding a transaction for another master). This bit will be ignored in PCI-X mode. Reset to 0
5	VGA Palette Snoop Enable	RO / RW	**This bit applies to reverse bridge only.** 0: Ignore VGA palette access on the primary 1: Enable positive decoding response to VGA palette writes on the primary interface with I/O address bits AD [9:0] equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA alias; AD [15:0] are not decoded and may be any value)

Bit	Function	Type	Description
			Reset to 0
6	Parity Error Response Enable	RW	0: May ignore any parity error that is detected and take its normal action 1: This bit if set, enables the setting of Master Data Parity Error bit in the Status Register when poisoned TLP received or parity error is detected and takes its normal action Reset to 0
7	Wait Cycle Control	RO	Wait cycle control not supported Reset to 0
8	SERR_L Enable Bit	RW	0: Disable 1: Enable PI7C9X130 in forward bridge mode to report non-fatal or fatal error message to the Root Complex. Also, in reverse bridge mode to assert SERR_L on the primary interface Reset to 0
9	Fast Back-to-Back Enable	RO	Fast back-to-back enable not supported Reset to 0
10	Interrupt Disable	RO / RW	**This bit applies to reverse bridge only.** 0: INTA_L, INTB_L, INTC_L, and INTD_L can be asserted on PCI interface 1: Prevent INTA_L, INTB_L, INTC_L, and INTD_L from being asserted on PCI interface Reset to 0
15:11	Reserved	RO	Reset to 00000

7.4.4 PRIMARY STATUS REGISTER – OFFSET 04h

Bit	Function	Type	Description
19:16	Reserved	RO	Reset to 0000
20	Capability List Capable	RO	1: PI7C9X130 supports the capability list (offset 34h in the pointer to the data structure) Reset to 1
21	66MHz Capable	RO	**This bit is set only for forward bridge in 7.4.4** Forward bridge - reset to 1 Reverse bridge - reset to 0
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	**This bit applies to reverse bridge only.** 1: Enable fast back-to-back transactions Reset to 0 when forward bridge or 1 when reverse bridge in PCI mode.
24	Master Data Parity Error Detected	RWC	Bit set if its Parity Error Enable bit is set and either of the conditions occurs on the primary: FORWARD BRIDGE – • Receives a completion marked poisoned • Poisons a write request REVERSE BRIDGE – • Detected parity error when receiving data or Split Response for read • Observes P_PERR_L asserted when sending data or receiving Split Response for write • Receives a Split Completion Message indicating data parity error occurred for non-posted write Reset to 0

Bit	Function	Type	Description
26:25	DEVSEL_L Timing (medium decode)	RO	**These bits apply to reverse bridge only.** 00: fast DEVSEL_L decoding 01: medium DEVSEL_L decoding 10: slow DEVSEL_L decoding 11: reserved Reset to 00 when forward bridge or 01 when reverse bridge.
27	Signaled Target Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 completes a request using completer abort status on the primary REVERSE BRIDGE – This bit is set to indicate a target abort on the primary Reset to 0
28	Received Target Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 receives a completion with completer abort completion status on the primary REVERSE BRIDGE – This bit is set when PI7C9X130 detects a target abort on the primary Reset to 0
29	Received Master Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 receives a completion with unsupported request completion status on the primary REVERSE BRIDGE – This bit is set when PI7C9X130 detects a master abort on the primary
30	Signaled System Error	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 sends an ERR_FATAL or ERR_NON_FATAL message on the primary REVERSE BRIDGE – This bit is set when PI7C9X130 asserts SERR_L on the primary Reset to 0
31	Detected Parity Error	RWC	FORWARD BRIDGE – This bit is set when poisoned TLP is detected on the primary REVERSE BRIDGE – This bit is set when address or data parity error is detected on the primary Reset to 0

7.4.5 REVISION ID REGISTER – OFFSET 08h

Bit	Function	Type	Description
7:0	Revision	RO	Reset to 04h

7.4.6 CLASS CODE REGISTER – OFFSET 08h

Bit	Function	Type	Description
15:8	Programming Interface	RO	Subtractive decoding of PCI-PCI bridge not supported Reset to 00000000
23:16	Sub-Class Code	RO	Sub-Class Code 00000100: PCI-to-PCI bridge Reset to 00000100
31:24	Base Class Code	RO	Base class code 00000110: Bridge Device Reset to 00000110

7.4.7 CACHE LINE SIZE REGISTER – OFFSET 0Ch

Bit	Function	Type	Description
1:0	Reserved	RO	Bit [1:0] not supported Reset to 00
2	Cache Line Size	RW	1: Cache line size = 4 double words Reset to 0
3	Cache Line Size	RW	1: Cache line size = 8 double words Reset to 0
4	Cache Line Size	RW	1: Cache line size = 16 double words Reset to 0
5	Cache Line Size	RW	1: Cache line size = 32 double words Reset to 0
7:6	Reserved	RO	Bit [7:6] not supported Reset to 00

7.4.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

Bit	Function	Type	Description
15:8	Primary Latency Timer	RO / RW	8 bits of primary latency timer in PCI/PCI-X FORWARD BRIDGE – RO with reset to 00h REVERSE BRIDGE – RW with reset to 00h in PCI mode or 40h in PCI-X mode

7.4.9 HEADER TYPE REGISTER – OFFSET 0Ch

Bit	Function	Type	Description
22:16	PCI-to-PCI bridge configuration	RO	PCI-to-PCI bridge configuration (10 – 3Fh) Reset to 0000001
23	Single Function Device	RO	0: Indicates single function device Reset to 0
31:24	Reserved	RO	Reset to 00h

7.4.10 RESERVED REGISTERS – OFFSET 10h TO 17h

7.4.11 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

Bit	Function	Type	Description
7:0	Primary Bus Number	RW	Reset to 00h

7.4.12 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

Bit	Function	Type	Description
15:8	Secondary Bus Number	RW	Reset to 00h

7.4.13 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

Bit	Function	Type	Description
23:16	Subordinate Bus Number	RW	Reset to 00h

7.4.14 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

Bit	Function	Type	Description
31:24	Secondary Latency Timer	RW / RO	Secondary latency timer in PCI / PCI-X mode FORWARD BRIDGE – RW with reset to 00h in PCI mode or 40h in PCI-X mode REVERSE BRIDGE – RO with reset to 00h

7.4.15 I/O BASE REGISTER – OFFSET 1Ch

Bit	Function	Type	Description
1:0	32-bit I/O Addressing Support	RO	01: Indicates PI7C9X130 supports 32-bit I/O addressing Reset to 01
3:2	Reserved	RO	Reset to 00
7:4	I/O Base	RW	Indicates the I/O Base (0000_0000h) Reset to 0000

7.4.16 I/O LIMIT REGISTER – OFFSET 1Ch

Bit	Function	Type	Description
9:8	32-bit I/O Addressing Support	RO	01: Indicates PI7C9X130 supports 32-bit I/O addressing Reset to 01
11:10	Reserved	RO	Reset to 00
15:12	I/O Base	RW	Indicates the I/O Limit (0000_0FFFh) Reset to 0000

7.4.17 SECONDARY STATUS REGISTER – OFFSET 1Ch

Bit	Function	Type	Description
20:16	Reserved	RO	Reset to 00000
21	66MHz Capable	RO	**This bit is set only for forward bridge** Forward bridge - reset to 1 Reverse bridge - reset to 0
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	FORWARD BRIDGE: reset to 1 when secondary bus is in PCI mode (supports fast back-to-back transactions) or reset to 0 when secondary bus is in PCI-X mode (does not support fast back-to-back transactions) REVERSE BRIDGE: reset to 0 (does not support fast back-to-back transactions)

24	Master Data Parity Error Detected	RWC	This bit is set if its parity error enable bit is set and either of the conditions occur on the primary: FORWARD BRIDGE – • Detected parity error when receiving data or split response for read • Observes S_PERR_L asserted when sending data or receiving split response for write • Receives a split completion message indicating data parity error occurred for non-posted write REVERSE BRIDGE – • Receives a completion marked poisoned • Poisons a write request Reset to 0
26:25	DEVSEL_L Timing (medium decoding)	RO	**These bits apply to forward bridge only.** 01: medium DEVSEL_L decoding Reset to 01 when forward mode or 00 when reverse mode.
27	Signaled Target Abort	RWC	FORWARD BRIDGE – Bit is set when PI7C9X130 signals target abort REVERSE BRIDGE – Bit is set when PI7C9X130 completes a request using completer abort completion status Reset to 0
28	Received Target Abort	RWC	FORWARD BRIDGE – Bit is set when PI7C9X130 detects target abort on the secondary interface REVERSE BRIDGE – Bit is set when PI7C9X130 receives a completion with completer abort completion status on the secondary interface Reset to 0
29	Received Master Abort	RWC	FORWARD BRIDGE – Bit is set when PI7C9X130 detects master abort on the secondary interface REVERSE BRIDGE – Bit is set when PI7C9X130 receives a completion with unsupported request completion status on the primary interface Reset to 0
30	Received System Error	RWC	FORWARD BRIDGE – Bit is set when PI7C9X130 detects SERR_L assertion on the secondary interface REVERSE BRIDGE – Bit is set when PI7C9X130 receives an ERR_FATAL or ERR_NON_FATAL message on the secondary interface Reset to 0
31	Detected Parity Error	RWC	FORWARD BRIDGE – Bit is set when PI7C9X130 detects address or data parity error REVERSE BRIDGE – Bit is set when PI7C9X130 detects poisoned TLP on secondary interface Reset to 0

7.4.18 MEMORY BASE REGISTER – OFFSET 20h

Bit	Function	Type	Description
3:0	Reserved	RO	Reset to 0000
15:4	Memory Base	RW	Memory Base (80000000h) Reset to 800h

7.4.19 MEMORY LIMIT REGISTER – OFFSET 20h

Bit	Function	Type	Description
19:16	Reserved	RO	Reset to 0000
31:20	Memory Limit	RW	Memory Limit (000FFFFFh) Reset to 000h

7.4.20 PREFETCHABLE MEMORY BASE REGISTER – OFFSET 24h

Bit	Function	Type	Description
3:0	64-bit Addressing Support	RO	0001: Indicates PI7C9X130 supports 64-bit addressing Reset to 0001
15:4	Prefetchable Memory Base	RW	Prefetchable Memory Base (00000000_80000000h) Reset to 800h

7.4.21 PREFETCHABLE MEMORY LIMIT REGISTER – OFFSET 24h

Bit	Function	Type	Description
19:16	64-bit Addressing Support	RO	0001: Indicates PI7C9X130 supports 64-bit addressing Reset to 0001
31:20	Prefetchable Memory Limit	RW	Prefetchable Memory Limit (00000000_000FFFFFh) Reset to 000h

7.4.22 PREFETCHABLE BASE UPPER 32-BIT REGISTER – OFFSET 28h

Bit	Function	Type	Description
31:0	Prefetchable Base Upper 32-bit	RW	Bit [63:32] of prefetchable base Reset to 00000000h

7.4.23 PREFETCHABLE LIMIT UPPER 32-BIT REGISTER – OFFSET 2Ch

Bit	Function	Type	Description
31:0	Prefetchable Limit Upper 32-bit	RW	Bit [63:32] of prefetchable limit Reset to 00000000h

7.4.24 I/O BASE UPPER 16-BIT REGISTER – OFFSET 30h

Bit	Function	Type	Description
15:0	I/O Base Upper 16-bit	RW	Bit [31:16] of I/O Base Reset to 0000h

7.4.25 I/O BASE UPPER 16-BIT REGISTER – OFFSET 30h

Bit	Function	Type	Description
31:16	I/O Limit Upper 16-bit	RW	Bit [31:16] of I/O Limit Reset to 0000h

7.4.26 CAPABILITY POINTER – OFFSET 34h

Bit	Function	Type	Description
31:8	Reserved	RO	Reset to 0
7:0	Capability Pointer	RO	Capability pointer to 80h Reset to 80h

7.4.27 EXPANSION ROM BASE ADDRESS REGISTER – OFFSET 38h

Bit	Function	Type	Description
31:0	Expansion ROM Base Address	RO	Expansion ROM not supported. Reset to 00000000h

7.4.28 INTERRUPT LINE REGISTER – OFFSET 3Ch

Bit	Function	Type	Description
7:0	Interrupt Line	RW	**These bits apply to reverse bridge only.** For initialization code to program to tell which input of the interrupt controller the PI7C9X130's INTA_L in connected to. Reset to 00000000

7.4.29 INTERRUPT PIN REGISTER – OFFSET 3Ch

Bit	Function	Type	Description
15:8	Interrupt Pin	RO	**These bits apply to reverse bridge only.** Interrupt Pin INTA# is used. Reset to 01h when forward mode and reverse mode.

7.4.30 BRIDGE CONTROL REGISTER – OFFSET 3Ch

Bit	Function	Type	Description
16	Parity Error Response Enable	RW	0: Ignore parity errors on the secondary 1: Enable parity error detection on secondary FORWARD BRIDGE – Controls the response to uncorrectable address attribute and data errors on the secondary REVERSE BRIDGE – Controls the setting of the master data parity error bit in response to a received poisoned TLP from the secondary (PCIe link) Reset to 0
17	SERR_L Enable	RW	0: Disable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL 1: Enable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL Reset to 0 (FORWARD BRIDGE) RO bit for REVERSE BRIDGE
18	ISA Enable	RW	0: Forward downstream all I/O addresses in the address range defined by the I/O Base and Limit registers 1: Forward upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0

Bit	Function	Type	Description
19	VGA Enable	RW	0: Do not forward VGA compatible memory and I/O addresses from the primary to secondary, unless they are enabled for forwarding by the defined I/O and memory address ranges 1: Forward VGA compatible memory and I/O addresses from the primary and secondary (if the I/O enable and memory enable bits are set), independent of the ISA enable bit
20	VGA 16-bit Decode	RW	0: Execute 10-bit address decodes on VGA I/O accesses 1: Execute 16-bit address decode on VGA I/O accesses Reset to 0
21	Master Abort Mode	RW	0: Do not report master aborts (return FFFFFFFFh on reads and discards data on write) 1: Report master abort by signaling target abort if possible or by the assertion of SERR_L (if enabled). Reset to 0
22	Secondary Interface Reset	RW	0: Do not force the assertion of RESET_L on secondary PCI bus for forward bridge, or do not generate a hot reset on the PCIe link for reverse bridge 1: Force the assertion of RESET_L on secondary PCI bus for forward bridge, or generate a hot reset on the PCIe link for reverse bridge Reset to 0
23	Fast Back-to-Back Enable	RO	Fast back-to-back not supported Reset to 0
24	Primary Master Timeout	RW	0: Primary discard timer counts 2^{15} PCI clock cycles 1: Primary discard timer counts 2^{10} PCI clock cycles FORWARD BRIDGE – Bit is RO and ignored by the PI7C9X130 Reset to 0
25	Secondary Master Timeout	RW	0: Secondary discard timer counts 2^{15} PCI clock cycles 1: Secondary discard timer counts 2^{10} PCI clock cycles REVERSE BRIDGE – Bit is RO and ignored by PI7C9X130 Reset to 0
26	Master Timeout Status	RWC	Bit is set when the discard timer expires and a delayed completion is discarded at the PCI interface for the forward or reverse bridge Reset to 0
27	Discard Timer SERR_L Enable	RW	Bit is set to enable to generate ERR_NONFATAL or ERR_FATAL for forward bridge, or assert P_SERR_L for reverse bridge as a result of the expiration of the discard timer on the PCI interface. Reset to 0
31:28	Reserved	RO	Reset to 0000

7.4.31 PCI DATA BUFFERING CONTROL REGISTER – OFFSET 40h

Bit	Function	Type	Description
0	Secondary Internal Arbiter's PARK Function	RW	0: Park to the last master 1: Park to PI7C9X130 secondary port Reset to 0
1	Memory Read Prefetching Dynamic Control Disable	RW	0: Enable memory read prefetching dynamic control for PCI to PCIe read 1: Disable memory read prefetching dynamic control for PCI to PCIe read Reset to 0
2	Completion Data Prediction Control	RW	0: Enable completion data prediction for PCI to PCIe read. 1: Disable completion data prediction

Bit	Function	Type	Description
			Reset to 0
3	Reserved	RO	Reset to 0
5:4	PCI Read Multiple Prefetch Mode	RW	00: One cache line prefetch if memory read multiple address is in prefetchable range at PCI interface 10: Full prefetch if address is in prefetchable range at PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after it disconnected external master during burst read with Read Multiple command, until discard timer expired. 11: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after the Read Multiple is terminated either by ex-master or by bridge, until discard timer expired. These bits are ignored if PCI/X interface is in PCIX mode. Reset to 10
7:6	PCI Read Line Prefetch Mode	RW	00: One cache line prefetch if memory read line address is in prefetchable range at PCI interface 10: Full prefetch if memory read line address is in prefetchable range at PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after it disconnected external master during burst read with Read Line command, until discard timer expired. 11: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after the Read Line is terminated either by ex-master or by bridge, until discard timer expired. These bits are ignored if PCI/X interface is in PCIX mode. Reset to 00
9:8	PCI Read Prefetch Mode	RW	**00**: One cache line prefetch if memory read address is in prefetchable range at PCI interface **01**: Reserved **10**: Full prefetch if memory read address is in prefetchable range at PCI interface **11**: Disconnect on the first DWORD Reset to 00
10	PCI Special Delayed Read Mode Enable	RW	0: Retry any master at PCI bus that repeats its transaction with command code changes. 1: Allows any master at PCI bus to change memory command code (MR, MRL, MRM) after it has received a retry. The PI7C9X130 will complete the memory read transaction and return data back to the master if the address and byte enables are the same. Reset to 0
11	Reserved	RO	Reset to 0
14:12	Maximum Memory Read Byte Count	RW	Maximum byte count is used by the PI7C9X130 when generating memory read requests on the PCIe link in response to a memory read initiated on the PCI bus and bit [9:8], bit [7:6], and bit [5:4] are set to "full prefetch". 000: 512 bytes (default) 001: 128 bytes 010: 256 bytes 011: 512 bytes 100: 1024 bytes 101: 2048 bytes 110: 4096 bytes 111: 512 bytes Reset to 000

7.4.32 CHIP CONTROL 0 REGISTER – OFFSET 40h

Bit	Function	Type	Description
15	Flow Control Update Control	RW	0: Flow control is updated for every two credits available 1: Flow control is updated for every on credit available Reset to 0

Bit	Function	Type	Description
16	PCI Retry Counter Status	RWC	0: The PCI retry counter has not expired since the last reset 1: The PCI retry counter has expired since the last reset Reset to 0
18:17	PCI Retry Counter Control	RW	00: No expiration limit 01: Allow 256 retries before expiration 10: Allow 64K retries before expiration 11: Allow 2G retries before expiration Reset to 00
19	PCI Discard Timer Disable	RW	0: Enable the PCI discard timer in conjunction with bit [27] offset 3Ch (bridge control register) 1: Disable the PCI discard timer in conjunction with bit [27] offset 3Ch (bridge control register) Reset to 0
20	PCI Discard Timer Short Duration	RW	0: Use bit [24] offset 3Ch for forward bridge or bit [25] offset 3Ch for reverse bridge to indicate how many PCI clocks should be allowed before the PCI discard timer expires 1: 64 PCI clocks allowed before the PCI discard timer expires Reset to 0
22:21	Configuration Request Retry Timer Counter Value Control	RW	00: Timer expires at 25us 01: Timer expires at 0.5ms 10: Timer expires at 5ms 11: Timer expires at 25ms Reset to 01
23	Delayed Transaction Order Control	RW	0: Enable out-of-order capability between delayed transactions 1: Disable out-of-order capability between delayed transactions Reset to 0
25:24	Completion Timer Counter Value Control	RW	00: Timer expires at 50us 01: Timer expires at 10ms 10: Timer expires at 50ms 11: Timer disabled Reset to 01
26	Isochronous Traffic Support Enable	RW	0: All memory transactions from PCI-X to PCIe will be mapped to TC0 1: All memory transactions from PCI-X to PCIe will be mapped to Traffic Class defined in bit [29:27] of offset 40h. Reset to 0
29:27	Traffic Class Used For Isochronous Traffic	RW	Reset to 001
30	Serial Link Interface Loopback Enable	RW / RO	0: Normal mode 1: Enable serial link interface loopback mode (TX to RX) if TM0=LOW, TM1=HIGH, TM2=HIGH, MSK_IN=HIGH, REVRSB=HIGH. PCI transaction from PCI bus will loop back to PCI bus RO for forward bridge Reset to 0
31	Primary Configuration Access Lockout	RO / RW	0: PI7C9X130 configuration space can be accessed from both interfaces 1: PI7C9X130 configuration space can only be accessed from the secondary interface. Primary bus accessed receives completion with CRS status for forward bridge, or target retry for reverse bridge Reset to 0 if TM0 is LOW

7.4.33 RESERVED REGISTER – OFFSET 44h

Bit	Function	Type	Description
31:0	Reserved	RO	Reset to 00000000h

7.4.34 ARBITER ENABLE REGISTER – OFFSET 48h

Bit	Function	Type	Description
0	Enable Arbiter 0	RW	0: Disable arbitration for internal PI7C9X130 request 1: Enable arbitration for internal PI7C9X130 request Reset to 1
1	Enable Arbiter 1	RW	0: Disable arbitration for master 1 1: Enable arbitration for master 1 Reset to 1
2	Enable Arbiter 2	RW	0: Disable arbitration for master 2 1: Enable arbitration for master 2 Reset to 1
3	Enable Arbiter 3	RW	0: Disable arbitration for master 3 1: Enable arbitration for master 3 Reset to 1
4	Enable Arbiter 4	RW	0: Disable arbitration for master 4 1: Enable arbitration for master 4 Reset to 1
5	Enable Arbiter 5	RW	0: Disable arbitration for master 5 1: Enable arbitration for master 5 Reset to 1
6	Enable Arbiter 6	RW	0: Disable arbitration for master 6 1: Enable arbitration for master 6 Reset to 1
7	Enable Arbiter 7	RW	0: Disable arbitration for master 7 1: Enable arbitration for master 7 Reset to 1
8	Enable Arbiter 8	RW	0: Disable arbitration for master 8 1: Enable arbitration for master 8 Reset to 1

7.4.35 ARBITER MODE REGISTER – OFFSET 48h

Bit	Function	Type	Description
9	External Arbiter Bit	RO	**0**: Enable internal arbiter (if CFN_L is tied LOW) **1**: Use external arbiter (if CFN_L is tied HIGH) Reset to 0/1 according to what CFN_L is tied to
10	Broken Master Timeout Enable	RW	**0**: Broken master timeout disable **1**: This bit enables the internal arbiter to count 16 PCI bus cycles while waiting for FRAME_L to become active when a device's PCI bus GNT is active and the PCI bus is idle. If the broken master timeout expires, the PCI bus GNT for the device is de-asserted. Reset to 0
11	Broken Master Refresh Enable	RW	0: A broken master will be ignored forever after de-asserting its REQ_L for at least 1 clock 1: Refresh broken master state after all the other masters have been served once Reset to 0

Bit	Function	Type	Description
19:12	Arbiter Fairness Counter	RW	08h: These bits are the initialization value of a counter used by the internal arbiter. It controls the number of PCI bus cycles that the arbiter holds a device's PCI bus GNT active after detecting a PCI bus REQ_L from another device. The counter is reloaded whenever a new PCI bus GNT is asserted. For every new PCI bus GNT, the counter is armed to decrement when it detects the new fall of FRAME_L. If the arbiter fairness counter is set to 00h, the arbiter will not remove a device's PCI bus GNT until the device has de-asserted its PCI bus REQ. Reset to 08h
20	GNT_L Output Toggling Enable	RW	0: GNT_L not de-asserted after granted master assert FRAME_L 1: GNT_L de-asserts for 1 clock after 2 clocks of the granted master asserting FRAME_L Reset to 0
21	Reserved	RO	Reset to 0

7.4.36 ARBITER PRIORITY REGISTER – OFFSET 48h

Bit	Function	Type	Description
22	Arbiter Priority 0	RW	0: Low priority request to internal PI7C9X130 1: High priority request to internal PI7C9X130 Reset to 1
23	Arbiter Priority 1	RW	0: Low priority request to master 1 1: High priority request to master 1 Reset to 0
24	Arbiter Priority 2	RW	0: Low priority request to master 2 1: High priority request to master 2 Reset to 0
25	Arbiter Priority 3	RW	0: Low priority request to master 3 1: High priority request to master 3 Reset to 0
26	Arbiter Priority 4	RW	0: Low priority request to master 4 1: High priority request to master 4 Reset to 0
27	Arbiter Priority 5	RW	0: Low priority request to master 5 1: High priority request to master 5 Reset to 0
28	Arbiter Priority 6	RW	0: Low priority request to master 6 1: High priority request to master 6 Reset to 0
29	Arbiter Priority 7	RW	0: Low priority request to master 7 1: High priority request to master 7 Reset to 0
30	Arbiter Priority 8	RW	0: Low priority request to master 8 1: High priority request to master 8 Reset to 0
31	Reserved	RO	Reset to 0

7.4.37 RESERVED REGISTERS – OFFSET 4Ch TO 64h

7.4.38 EXPRESS TRANSMITTER/RECEIVER CONTROL REGISTER – OFFSET 68h

Bit	Function	Type	Description
1:0	Nominal Driver Current Control	RW	00: 20mA 01: 10mA 10: 28mA 11: Reserved Reset to 00
5:2	Driver Current Scale Multiple Control	RW	0000: 1.00 x nominal driver current 0001: 1.05 x nominal driver current 0010: 1.10 x nominal driver current 0011: 1.15 x nominal driver current 0100: 1.20 x nominal driver current 0101: 1.25 x nominal driver current 0110: 1.30 x nominal driver current 0111: 1.35 x nominal driver current 1000: 1.60 x nominal driver current 1001: 1.65 x nominal driver current 1010: 1.70 x nominal driver current 1011: 1.75 x nominal driver current 1100: 1.80 x nominal driver current 1101: 1.85 x nominal driver current 1110: 1.90 x nominal driver current 1111: 1.95 x nominal driver current Reset to 0000
11:8	Driver De-emphasis Level Control	RW	0000: 0.00 db 0001: -0.35 db 0010: -0.72 db 0011: -1.11 db 0100: -1.51 db 0101: -1.94 db 0110: -2.38 db 0111: -2.85 db 1000: -3.35 db 1001: -3.88 db 1010: -4.44 db 1011: -5.04 db 1100: -5.68 db 1101: -6.38 db 1110: -7.13 db 1111: -7.96 db Reset to 1000
13:12	Transmitter Termination Control	RW	00: 52 ohms 01: 57 ohms 10: 43 ohms 11: 46 ohms Reset to 00
15:14	Receiver Termination Control	RW	00: 52 ohms 01: 57 ohms 10: 43 ohms 11: 46 ohms Reset to 00
26:16	Reserved	RO	Reset to 0
29:27	Upstream memory read request transmitting control	RW	Reset to 111

7.4.39 UPSTREAM MEMORY WRITE FRAGMENT CONTROL REGISTER – OFFSET 68h

Bit	Function	Type	Description
31:30	Memory Write Fragment Control	RW	Upstream Memory Write Fragment Control

Bit	Function	Type	Description
			00: Fragment at 32-byte boundary 01: Fragment at 64-byte boundary 1x: Fragement at 128-byte boundary Reset to 10

7.4.40 RESERVED REGISTER – OFFSET 6Ch

7.4.41 EEPROM AUTOLOAD CONTROL/STATUS REGISTER – OFFSET 70h (default=00000080h)

Bit	Function	Type	Description
0	Initiate EEPROM Read or Write Cycle	RW	This bit will be reset to 0 after the EEPROM operation is finished. 0: EEPROM AUTOLOAD disabled 0 -> 1: Starts the EEPROM Read or Write cycle Reset to 0
1	Control Command for EEPROM	RW	0: Read 1: Write Reset to 0
2	EEPROM Error	RO	0: EEPROM acknowledge is always received during the EEPROM cycle 1: EEPROM acknowledge is not received during EEPROM cycle Reset to 0
3	EPROM Autoload Complete Status	RO	0: EEPROM autoload is not successfully completed 1: EEPROM autoload is successfully completed Reset to 0
5:4	EEPROM Clock Frequency Control	RW	Where PCLK is 125MHz 00: PCLK / 4096 01: PCLK / 2048 10: PCLK / 1024 11: PCLK / 128 Reset to 00
6	EEPROM Autoload Control	RW	0: Enable EEPROM autoload 1: Disable EEPROM autoload Reset to 0
7	Fast EEPROM Autoload Control	RW	0: Normal speed of EEPROM autoload 1: Increase EEPROM autoload by 32x Reset to 1
8	EEPROM Autoload Status	RO	0: EEPROM autoload is not on going 1: EEPROM autoload is on going Reset to 0
15:9	EEPROM Word Address	RW	EEPROM word address for EEPROM cycle Reset to 0000000
31:16	EEPROM Data	RW	EEPROM data to be written into the EEPROM Reset to 0000h

7.4.42 HOT SWAP CONTROL AND STATUS REGISTER – OFFSET 74h

Bit	Function	Type	Description
7:0	Capability ID for Hot Swap	RO	Reset to 06h when Hot Sawp is enable (HS_EN=1) or 00h when Hot Swap is disabled (HS_EN=0)

Bit	Function	Type	Description
15:8	Next Capability Pointer	RO	Reset to 00h to inidicate the end of the capability chain
16	Device Hiding Arm	RW	Device Hiding Armed when this bit is set to 1 Reset to 0
17	ENUM_L signal Mask	RW	ENUM_L signal is masked when this bit is set to 1 Reset to 0
18	Pending Insertion or Extraction	RW	When this bit is 1, INS is armed, or either INS or EXT has a value of logic 1 When this bit is 0, INS is not armed or both INS and EXT have a value of logic 0 Reset to 0h
19	LED On Off	RW	When this bit is 1, LED is on When this bit is 0, LED is off Reset to 0
21:20	Programming Interface	RO	PI=01 supports PI=00 plus device hiding and pending insertion or extraction bits Reset to 01
22	EXT for Extraction	RWC	EXT bit indicates ENUM_L status of extraction. When EXT is 1, ENUM_L is asserted Reset to 0
23	INS for Insertion	RWC	INS bit indicates ENUM_L status of insertion. When INS is 1, ENUM_L is asserted Reset to 1
31:24	Reserved	RO	Reset to 00h

7.4.43 GPIO DATA AND CONTROL REGISTER – OFFSET 78h

Bit	Function	Type	Description
11:0	Reserved	RO	Reset to 000h
15:12	GPIO Output Write-1-to-Clear	RW	Reset to 0h
19:16	GPIO Output Write-1-to-Set	RW	Reset to 0h
23:20	GPIO Output Enable Write-1-to-Clear	RW	Reset to 0h
27:24	GPIO Output Enable Write-1-to-Set	RW	Reset to 0h
31:28	GPIO Input Data Register	RO	Reset to 0h

7.4.44 RESERVED REGISTER – OFFSET 7Ch

7.4.45 PCI-X CAPABILITY ID REGISTER – OFFSET 80h

Bit	Function	Type	Description
7:0	PCI-X Capability ID	RO	PCI-X Capability ID Reset to 07h

7.4.46 NEXT CAPABILITY POINTER REGISTER – OFFSET 80h

Bit	Function	Type	Description
15:8	Next Capability Pointer	RO	Point to power management Reset to 90h

7.4.47 PCI-X SECONDARY STATUS REGISTER – OFFSET 80h

Bit	Function	Type	Description
16	64-bit Device on Secondary Bus Interface	RO	64-bit supported when DEV64 is set to high Reset to 1in forward bridge mode and DEV64 is set to high or reset to 0 in reverse bridge mode
17	133MHz Capable	RO	When this bit is 1, PI7C9X130 is 133MHz capable on its secondary bus interface Reset to 1 in forward bridge mode or 0 in reverse bridge mode
18	Split Completion Discarded	RO / RWC	This bit is a read-only and set to 0 in reverse bridge mode or is read-write in forward bridge mode When this is set to 1, a split completion has been discarded by PI7C9X130 at secondary bus because the requester did not accept the split completion transaction Reset to 0
19	Unexpected Split Completion	RWC	This bit is set to 0 in forward bridge mode or is read-write in reverse bridge mode When this bit is set to 1, an unexpected split completion has been received with the requester ID equaled to the secondary bus number, device number, and function number at the PI7X9X130 secondary bus interface Reset to 0
20	Split Completion Overrun	RWC	When this bit is set to 1, a split completion has been terminated by PI7C9X130 with either a retry or disconnect at the next ADB due to the buffer full condition Reset to 0
21	Split Request Delayed	RWC	When this bit is set to 1, a split request is delayed because PI7C9X130 is not able to forward the split request transaction to its secondary bus due to insufficient room within the limit specified in the split transaction commitment limit field of the downstream split transaction control register Reset to 0
24:22	Secondary Clock Frequency	RO	These bits are only meaningful in forward bridge mode. In reverse bridge mode, all three bits are set to zero. 000: Conventional PCI mode (minimum clock period not applicable) 001: 66MHz (minimum clock period is 15ns) 010: 100 to 133MHz (minimum clock period is 7.5ns) 011: Reserved 1xx: Reserved Reset to 000
31:25	Reserved	RO	0000000

7.4.48 PCI-X BRIDGE STATUS REGISTER – OFFSET 84h

Bit	Function	Type	Description
2:0	Function Number	RO	Function number (AD [10:8] of a type 0 configuration transaction) Reset to 000

Bit	Function	Type	Description
7:3	Device Number	RO	Device number (AD [15:11] of a type 0 configuration transaction) is assigned to the PI7C9X130 by the connection of system hardware. Each time the PI7C9X130 is addressed by a configuration write transaction, the bridge updates this register with the contents of AD [15:11] of the address phase of the configuration transaction, regardless of which register in the PI7C9X130 is addressed by the transaction. The PI7C9X130 is addressed by a configuration write transaction if all of the following are true: • The transaction uses a configuration write command • IDSEL is asserted during the address phase • AD [1:0] are 00 (type o configuration transaction) • AD [10:8] of the configuration address contain the appropriate function number Reset to 11111
15:8	Bus Number	RO	Additional address from which the contents of the primary bus number register on type 1 configuration space header is read. The PI7C9X130 uses the bus number, device number, and function number fields to create a completer ID when responding with a split completion to a read of an internal PI7C9X130 register. These fields are also used for cases when one interface is in conventional PCI mode and the other is in PCI-X mode. Reset to 11111111
16	64-bit Device on Primary Bus Interface	RO	64-bit supported when DEV64 is set to high Reset to 0 in forward bridge mode or in reverse bridge mode with REQ64_L is high at the de-assertion of RESET_L or reset to 1 in reverse bridge mode with REQ64_L is low at the de-assertion of RESET_L
17	133MHz Capable	RO	When this bit is 1, PI7C9X130 is 133MHz capable on its primary bus interface Reset to 0 in forward bridge mode or 1 in reverse bridge mode
18	Split Completion Discarded	RO / RWC	This bit is a read-only and set to 0 in reverse bridge mode or is read-write in forward bridge mode When this is set to 1, a split completion has been discarded by PI7C9X130 at primary bus because the requester did not accept the split completion transaction Reset to 0
19	Unexpected Split Completion	RWC	This bit is set to 0 in forward bridge mode or is read-write in reverse bridge mode When this is set to 1, an unexpected split completion has been received with the requester ID equaled to the primary bus number, device number, and function number at the PI7X9X130 primary bus interface Reset to 0
20	Split Completion Overrun	RWC	When this bit is set to 1, a split completion has been terminated by PI7C9X130 with either a retry or disconnect at the next ADB due to the buffer full condition Reset to 0
21	Split Request Delayed	RWC	When this bit is set to 1, a split request is delayed because PI7C9X130 is not able to forward the split request transaction to its primary bus due to insufficient room within the limit specified in the split transaction commitment limit field of the downstream split transaction control register Reset to 0
31:22	Reserved	RO	0000000000

7.4.49 UPSTREAM SPLIT TRANSACTION REGISTER – OFFSET 88h

Bit	Function	Type	Description
15:0	Upstream Split Transaction Capability	RO	Upstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the secondary bus in addressing the completers on the primary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h
31:16	Split Transaction Commitment Limit	RW	Upstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X130 is allowed to forward all split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

7.4.50 DOWNSTREAM SPLIT TRANSACTION REGISTER – OFFSET 8Ch

Bit	Function	Type	Description
15:0	Downstream Split Transaction Capability	RO	Downstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the primary bus in addressing the completers on the secondary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h
31:16	Downstream Split Transaction Commitment Limit	RW	Downstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X130 is allowed to forward all split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

7.4.51 POWER MANAGEMENT ID REGISTER – OFFSET 90h

Bit	Function	Type	Description
7:0	Power Management ID	RO	Power Management ID Register Reset to 01h

7.4.52 NEXT CAPABILITY POINTER REGISTER – OFFSET 90h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer (point to Subsystem ID and Subsystem Vendor ID) Reset to A8h

7.4.53 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 90h

Bit	Function	Type	Description
18:16	Version Number	RO	Version number that complies with revision 1.2 of the PCI Power Management Interface Specification. Reset to 011
19	PME Clock	RO	PME clock is not required for PME_L generation Reset to 0

Bit	Function	Type	Description
20	Reserved	RO	Reset to 0
21	Device Specific Initialization (DSI)	RO	DSI – no special initialization of this function beyond the standard PCI configuration header is required following transition to the D0 un-initialized state Reset to 0
24:22	AUX Current	RO	000: 0mA 001: 55mA 010: 100mA 011: 160mA 100: 220mA 101: 270mA 110: 320mA 111: 375mA Reset to 001
25	D1 Power Management	RO	D1 power management is not supported Reset to 0
26	D2 Power Management	RO	D2 power management is not supported Reset to 0
31:27	PME_L Support	RO	PME_L is supported in D3 cold, D3 hot, and D0 states. Reset to 11001

7.4.54 POWER MANAGEMENT CONTROL AND STATUS REGISTER – OFFSET 94h

Bit	Function	Type	Description
1:0	Power State	RW	Power State is used to determine the current power state of PI7C9X130. If a non-implemented state is written to this register, PI7C9X130 will ignore the write data. When present state is D3 and changing to D0 state by programming this register, the power state change causes a device reset without activating the RESET_L of PCI/PCI-X bus interface 00: D0 state 01: D1 state not implemented 10: D2 state not implemented 11: D3 state Reset to 00
7:2	Reserved	RO	Reset to 000000
8	PME Enable	RWS	0: PME_L assertion is disabled 1: PME_L assertion is enabled Reset to 0
12:9	Data Select	RO	Data register is not implemented Reset to 0000
14:13	Data Scale	RO	Data register is not implemented Reset to 00
15	PME Status	RWCS	PME_L is supported Reset to 0

7.4.55 PCI-TO-PCI BRIDGE SUPPORT EXTENSION REGISTER – OFFSET 94h

Bit	Function	Type	Description
21:16	Reserved	RO	Reset to 000000
22	B2/B3 Support	RO	0: B2 / B3 not support for D3hot Reset to 0

Bit	Function	Type	Description
23	PCI Bus Power/Clock Control Enable	RO	0: PCI Bus Power/Clock Disabled Reset to 0
31:24	Data Register	RO	Data register is not implemented Reset to 00h

7.4.56 RESERVED REGISTERS – OFFSET 98h TO 9Ch

7.4.57 CAPABILITY ID REGISTER – OFFSET A0h

Bit	Function	Type	Description
7:0	Capability ID	RO	Capability ID for Slot Identification. SI is off by default but can be turned on through EEPROM interface Reset to 04h

7.4.58 NEXT POINTER REGISTER – OFFSET A0h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer – points to PCI Express capabilities register Reset to B0h

7.4.59 SLOT NUMBER REGISTER – OFFSET A0h

Bit	Function	Type	Description
20:16	Expansion Slot Number	RW	Expansion slot number Reset to 00000
21	First In Chassis	RW	First in chassis Reset to 0
23:22	Reserved	RO	Reset to 00

7.4.60 CHASSIS NUMBER REGISTER – OFFSET A0h

Bit	Function	Type	Description
31:24	Chassis Number	RW	Chassis number Reset to 00h

7.4.61 SECONDARY CLOCK AND CLKRUN CONTROL REGISTER – OFFSET A4h

Bit	Function	Type	Description
1:0	CLKOUT0 Enable	RW	CLKOUT (Slot 0) Enable for forward bridge mode only 00: enable CLKOUT0 01: enable CLKOUT0 10: enable CLKOUT0 11: disable CLKOUT0 and driven LOW Reset to 00

Bit	Function	Type	Description
3:2	CLKOUT1 Enable	RW	CLKOUT (Slot 1) Enable for forward bridge mode only 00: enable CLKOUT1 01: enable CLKOUT1 10: enable CLKOUT1 11: disable CLKOUT1 and driven LOW Reset to 00
5:4	CLKOUT2 Enable	RW	CLKOUT (Slot 2) Enable for forward bridge mode only 00: enable CLKOUT2 01: enable CLKOUT2 10: enable CLKOUT2 11: disable CLKOUT2 and driven LOW Reset to 00
7:6	CLKOUT3 Enable	RW	CLKOUT (Slot 3) Enable for forward bridge mode only 00: enable CLKOUT3 01: enable CLKOUT3 10: enable CLKOUT3 11: disable CLKOUT3 and driven LOW Reset to 00
8	CLKOUT4 Enable	RW	CLKOUT (Device 1) Enable for forward bridge mode only 0: enable CLKOUT4 1: disable CLKOUT4 and driven LOW Reset to 0
9	CLKOUT5 Enable	RW	CLKOUT (Device 2) Enable for forward bridge mode only 0: enable CLKOUT5 1: disable CLKOUT5 and driven LOW Reset to 0
10	CLKOUT6 Enable	RW	CLKOUT (the bridge) Enable for forward bridge mode only 0: enable CLKOUT6 1: disable CLKOUT6 and driven LOW Reset to 0
11	Reserved	RO	Reset to 0
12	Reserved	RO	Reset to 0
13	Secondary Clock Stop Status	RO	Secondary clock stop status 0: secondary clock not stopped 1: secondary clock stopped Reset to 0
14	Secondary Clkrun Protocol Enable	RW	0: disable protocol 1: enable protocol Reset to 0
15	Clkrun Mode	RW	0: Stop the secondary clock only when bridge is at D3hot state 1: Stop the secondary clock whenever the secondary bus is idle and there are no requests from the primary bus Reset to 0
31:16	Reserved	RO	Reset to 0000h

7.4.62 CAPABILITY ID REGISTER – OFFSET A8h

Bit	Function	Type	Description
7:0	Capability ID	RO	Capability ID for subsystem ID and subsystem vendor ID Reset to 0Dh

7.4.63 NEXT POINTER REGISTER – OFFSET A8h

Bit	Function	Type	Description
15:8	Next Item Pointer	RO	Next item pointer (point to PCI Express Capability by default but can be programmed to A0h if Slot Identification Capability is enabled) Reset to B0h

7.4.64 RESERVED REGISTER – OFFSET A8h

Bit	Function	Type	Description
31:16	Reserved	RO	Reset to 0000h

7.4.65 SUBSYSTEM VENDOR ID REGISTER – OFFSET ACh

Bit	Function	Type	Description
15:0	Subsystem Vendor ID	RO	Subsystem vendor ID identifies the particular add-in card or subsystem Reset to 00h

7.4.66 SUBSYSTEM ID REGISTER – OFFSET ACh

Bit	Function	Type	Description
31:16	Subsystem ID	RO	Subsystem ID identifies the particular add-in card or subsystem Reset to 00h

7.4.67 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET B0h

Bit	Function	Type	Description
7:0	PCI Express Capability ID	RO	PCI Express capability ID Reset to 10h

7.4.68 NEXT CAPABILITY POINTER REGISTER – OFFSET B0h (default=0071F010h for forward bridge or =0181F010h for reverse bridge)

Bit	Function	Type	Description
15:8	Next Item Pointer	RO	Next item pointer (points to VPD register) Reset to F0h

7.4.69 PCI EXPRESS CAPABILITY REGISTER – OFFSET B0h

Bit	Function	Type	Description
19:16	Capability Version	RO	Reset to 1h

Bit	Function	Type	Description
23:20	Device / Port Type	RO	0000: PCI Express endpoint device 0001: Legacy PCI Express endpoint device 0100: Root port of PCI Express root complex 0101: Upstream port of PCI Express switch 0110: Downstream port of PCI Express switch 0111: PCI Express to PCI bridge 1000: PCI to PCI Express bridge Others: Reserved Reset to 7h for Forward Bridge or 8h for Reverse Bridge
24	Slot Implemented	RO	Reset to 0 for Forward Bridge or 1 for Reverse Bridge
29:25	Interrupt Message Number	RO	Reset to 0h
31:30	Reserved	RO	Reset to 0

7.4.70 DEVICE CAPABILITY REGISTER – OFFSET B4h

Bit	Function	Type	Description
2:0	Maximum Payload Size	RO	000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 010
4:3	Phantom Functions	RO	No phantom functions supported Reset to 0
5	8-bit Tag Field	RO	8-bit tag field supported Reset to 1h
8:6	Endpoint L0's Latency	RO	Endpoint L0's acceptable latency 000: less than 64 ns 001: 64 – 128 ns 010: 128 – 256 ns 011: 256 – 512 ns 100: 512 ns – 1 us 101: 1 – 2 us 110: 2 – 4 us 111: more than 4 us Reset to 000
11:9	Endpoint L1's Latency	RO	Endpoint L1's acceptable latency 000: less than 1 us 001: 1 – 2 us 010: 2 – 4 us 011: 4 – 8 us 100: 8 – 16 us 101: 16 – 32 us 110: 32 – 64 us 111: more than 64 us Reset to 000
12	Attention Button Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.

Bit	Function	Type	Description
13	Attention Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enable at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
14	Power Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enable at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
17:15	Reserved	RO	Reset to 000
25:18	Captured Slot Power Limit Value	RO	These bits are set by the Set_Slot_Power_Limit message Reset to 00h
27:26	Captured Slot Power Limit Scale	RO	This value is set by the Set_Slot_Power_Limit message Reset to 00
31:28	Reserved	RO	Reset to 0h

7.4.71 DEVICE CONTROL REGISTER – OFFSET B8h

Bit	Function	Type	Description
0	Correctable Error Reporting Enable	RW	Reset to 0h
1	Non-Fatal Error Reporting Enable	RW	Reset to 0h
2	Fatal Error Reporting Enable	RW	Reset to 0h
3	Unsupported Request Reporting Enable	RW	Reset to 0h
4	Relaxed Ordering Enable	RO	Relaxed Ordering disabled Reset to 0h
7:5	Max Payload Size	RW	This field sets the maximum TLP payload size for the PI7C9X130 000: 128 bytes 001: 256 bytes 010: 512 bytes 011:1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 000
8	Extended Tag Field Enable	RW	Reset to 0
9	Phantom Functions Enable	RO	Phantom functions not supported Reset to 0
10	Auxiliary Power PM Enable	RO	Auxiliary power PM not supported Reset to 0
11	No Snoop Enable	RO	Bridge never sets the No Snoop attribute in the transaction it initiates Reset to 0

Bit	Function	Type	Description
14:12	Maximum Read Request Size	RW	This field sets the maximum Read Request Size for the device as a requester 000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 2h
15	Configuration Retry Enable	RW	Reset to 0

7.4.72 DEVICE STATUS REGISTER – OFFSET B8h

Bit	Function	Type	Description
16	Correctable Error Detected	RWC	Reset to 0
17	Non-Fatal Error Detected	RWC	Reset to 0
18	Fatal Error Detected	RWC	Reset to 0
19	Unsupported Request Detected	RWC	Reset to 0
20	AUX Power Detected	RO	Reset to 1
21	Transaction Pending	RO	0: No transaction is pending on transaction layer interface 1: Transaction is pending on transaction layer interface Reset to 0
31:22	Reserved	RO	Reset to 0000000000

7.4.73 LINK CAPABILITY REGISTER – OFFSET BCh

Bit	Function	Type	Description
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link 0001: 2.5Gb/s link Reset to 1h
9:4	Maximum Link Width	RO	Indicates the maximum width of the Express link (x4 at reset) 000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000100
11:10	ASPM Support	RO	This field indicates the level of Active State Power Management Support 00: reserved 01: L0's entry supported 10: reserved 11: L0's and L1's supported Reset to 11
14:12	L0's Exit Latency	RO	Reset to 3h
17:15	L1's Exit Latency	RO	Reset to 0h
23:18	Reserved	RO	Reset to 0h

Bit	Function	Type	Description
31:24	Port Number	RO	Reset to 00h

7.4.74 LINK CONTROL REGISTER – OFFSET C0h

Bit	Function	Type	Description
1:0	ASPM Control	RW	This field controls the level of ASPM supported on the Express link 00: disabled 01: L0's entry enabled 10: L1's entry enabled 11: L0's and L1's entry enabled Reset to 00
2	Reserved	RO	Reset to 0
3	Read Completion Boundary (RCB)	RO	Read completion boundary not supported Reset to 0
4	Link Disable	RO / RW	RO for Forward Bridge Reset to 0
5	Retrain Link	RO / RW	RO for Forward Bridge Reset to 0
6	Common Clock Configuration	RW	Reset to 0
7	Extended Sync	RW	Reset to 0
15:8	Reserved	RO	Reset to 00h

7.4.75 LINK STATUS REGISTER – OFFSET C0h

Bit	Function	Type	Description
19:16	Link Speed	RO	This field indicates the negotiated speed of the Express link 001: 2.5Gb/s link Reset to 1h
25:20	Negotiated Link Width	RO	000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000100
26	Link Train Error	RO	Reset to 0
27	Link Training	RO	Reset to 0
28	Slot Clock Configuration	RO	Reset to 1
31:29	Reserved	RO	Reset to 0

7.4.76 SLOT CAPABILITY REGISTER – OFFSET C4h

Bit	Function	Type	Description
0	Attention Button Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
1	Power Controller Present	RO	Reset to 0

Bit	Function	Type	Description
2	MRL Sensor Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
3	Attention Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
4	Power Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
5	Hot Plug Surprise	RO	Reset to 0
6	Hot Plug Capable	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
14:7	Slot Power Limit Value	RO	Reset to 00h
16:15	Slot Power Limit Scale	RO	Reset to 00
18:17	Reserved	RO	Reset to 00
31:19	Physical Slot Number	RO	Reset to 0

7.4.77 SLOT CONTROL REGISTER – OFFSET C8h

Bit	Function	Type	Description
0	Attention Button Present Enable	RW	Reset to 0
1	Power Fault Detected Enable	RW	Reset to 0
2	MRL Sensor Changed Enable	RW	Reset to 0
3	Presence Detect Changed Enable	RW	Reset to 0
4	Command Completed Interrupt Enable	RW	Reset to 0
5	Hot Plug Interrupt Enable	RW	Reset to 0
7:6	Attention Indicator Control	RW	Reset to 0
9:8	Power Indicator Control	RW	Reset to 0
10	Power Controller Control	RW	Reset to 0
15:11	Reserved	RO	Reset to 0

7.4.78 SLOT STATUS REGISTER – OFFSET C8h

Bit	Function	Type	Description
16	Attention Button Pressed	RO	Reset to 0
17	Power Fault Detected	RO	Reset to 0
18	MRL Sensor Changed	RO	Reset to 0

Bit	Function	Type	Description
19	Presence Detect Changed	RO	Reset to 0
20	Command Completed	RO	Reset to 0
21	MRL Sensor State	RO	Reset to 0
22	Presence Detect State	RO	Reset to 0
31:23	Reserved	RO	Reset to 0

7.4.79 XPIP CONFIGURATION REGISTER 0 – OFFSET CCh

Bit	Function	Type	Description
0	Hot Reset Enable	RW	Reset to 0
1	Loopback Function Enable	RW	Reset to 0
2	Cross Link Function Enable	RW	Reset to 0
3	Software Direct to Configuration State when in LTSSM state	RW	Reset to 0
4	Internal Selection for Debug Mode	RW	Reset to 0
7:5	Negotiate Lane Number of Times	RW	Reset to 3h
12:8	TS1 Number Counter	RW	Reset to 10h
15:13	Reserved	RO	Reset to 0
31:16	LTSSM Enter L1 Timer Default Value	RW	Reset to 0400h

7.4.80 XPIP CONFIGURATION REGISTER 1 – OFFSET D0h (default=04000271h)

Bit	Function	Type	Description
9:0	L0's Lifetime Timer	RW	Reset to 271h
15:10	Reserved	RO	Reset to 0
31:16	L1 Lifetime Timer	RW	Reset to 0400h

7.4.81 XPIP CONFIGURATION REGISTER 2 – OFFSET D4h

Bit	Function	Type	Description
7:0	CDR Recovery Time (in the number of FTS order sets)	RW	Reset to 54h A Fast Training Sequence order set composes of one K28.5 (COM) Symbol and three K28.1 Symbols.
14:8	L0's Exit to L0 Latency	RW	Reset to 2h
15	Reserved	RO	Reset to 0
22:16	L1 Exit to L0 Latency	RW	Reset to 19h
23	Reserved	RO	Reset to 0

7.4.82 HOT SWAP SWITCH DEBOUNCE COUNTER – OFFSET D4h

Bit	Function	Type	Description
31:24	Hot Swap Debounce Counter	RO / RW	If Hot Swap is enabled, this counter is read-writeable (RW). This counter is read only (RO) if Hot Swap is disabled 00h: 1ms 01h: 2ms 02h: 3ms 03h: 4ms … FFh: 256ms Reset to 0

7.4.83 CAPABILITY ID REGISTER – OFFSET D8h

Bit	Function	Type	Description
7:0	Capability ID for VPD Register	RO	Reset to 03h

7.4.84 NEXT POINTER REGISTER – OFFSET D8h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer (F0h, points to MSI capabilities) Reset to F0h

7.4.85 VPD REGISTER – OFFSET D8h

Bit	Function	Type	Description
17:16	Reserved	RO	Reset to 0
23:18	VPD Address for Read/Write Cycle	RW	Reset to 0
30:24	Reserved	RO	Reset to 0
31	VPD Operation	RW	0: Generate a read cycle from the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '0' until EEPROM cycle is finished, after which the bit is then set to '1'. Data for reads is available at register ECh. 1: Generate a write cycle to the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '1' until EEPROM cycle is finished, after which it is then cleared to '0'. Reset to 0

7.4.86 VPD DATA REGISTER – OFFSET DCh

Bit	Function	Type	Description
31:0	VPD Data	RW	VPD Data (EEPROM data [address + 0x40]) The least significant byte of this register corresponds to the byte of VPD at the address specified by the VPD address register. The data read form or written to this register uses the normal PCI byte transfer capabilities. Reset to 0

7.4.87 EXTENDED CONFIGURATION ACCESS ADDRESS REGISTER – OFFSET E0h

Bit	Function	Type	Description
7:0	Register number	RW	Reset to 00h

Bit	Function	Type	Description
11:8	Extended Register number	RW	Reset to 0000
14:12	Function number	RW	Reset to 000
19:15	Device number	RW	Reset to 00000
27:20	BUS number	RW	Reset to 00h
30:28	Reserved	RO	Reset to 000
31	Enable bit for extended cfg access from PCI/X bus	RW	When set to '1', Extended Configuration Access function is enabled. Reset to 0

7.4.88 EXTENDED CONFIGURATION ACCESS DATA REGISTER – OFFSET E4h

Bit	Function	Type	Description
31:0	Extended Configuration Access Data	RW	Extended Cfg Access Data Register Reset to 0

7.4.89 RESERVED REGISTER - OFFSET E8h TO ECh

7.4.90 MESSAGE SIGNALED INTERRUPTS ID REGISTER – OFFSET F0h

Bit	Function	Type	Description
7:0	Capability ID for MSI Registers	RO	Reset to 05h

7.4.91 NEXT CAPABILITIES POINTER REGISTER – OFFSET F0h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer (00h indicates the end of capabilities) Reset to 00h

7.4.92 MESSAGE CONTROL REGISTER – OFFSET F0h

Bit	Function	Type	Description
16	MSI Enable	RW	0: Disable MSI and default to INTx for interrupt 1: Enable MSI for interrupt service and ignore INTx interrupt pins
19:17	Multiple Message Capable	RO	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
22:20	Multiple Message Enable	RW	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
23	64-bit Address Capable	RW	Reset to 1
31:24	Reserved	RO	Reset to 00h

7.4.93 MESSAGE ADDRESS REGISTER – OFFSET F4h

Bit	Function	Type	Description
1:0	Reserved	RO	Reset to 00
31:2	System Specified Message Address	RW	Reset to 0

7.4.94 MESSAGE UPPER ADDRESS REGISTER – OFFSET F8h

Bit	Function	Type	Description
31:0	System Specified Message Upper Address	RW	Reset to 0

7.4.95 MESSAGE DATA REGISTER – OFFSET FCh

Bit	Function	Type	Description
15:0	System Specified Message Data	RW	Reset to 0
31:16	Reserved	RO	Reset to 0

7.4.96 ADVANCE ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

Bit	Function	Type	Description
15:0	Advance Error Reporting Capability ID	RO	Reset to 0001h

7.4.97 ADVANCE ERROR REPORTING CAPABILITY VERSION REGISTER – OFFSET 100h

Bit	Function	Type	Description
19:16	Advance Error Reporting Capability Version	RO	Reset to 1h

7.4.98 NEXT CAPABILITY OFFSET REGISTER – OFFSET 100h

Bit	Function	Type	Description
31:20	Next Capability Offset	RO	Next capability offset (150h points to VC capability) Reset to 150h

7.4.99 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

Bit	Function	Type	Description
0	Training Error Status	RWCS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Status	RWCS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Status	RWCS	Reset to 0
13	Flow Control Protocol Error Status	RWCS	Reset to 0

Bit	Function	Type	Description
14	Completion Timeout Status	RWCS	Reset to 0
15	Completer Abort Status	RWCS	Reset to 0
16	Unexpected Completion Status	RWCS	Reset to 0
17	Receiver Overflow Status	RWCS	Reset to 0
18	Malformed TLP Status	RWCS	Reset to 0
19	ECRC Error Status	RWCS	Reset to 0
20	Unsupported Request Error Status	RWCS	Reset to 0
31:21	Reserved	RO	Reset to 0

7.4.100UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

Bit	Function	Type	Description
0	Training Error Mast	RWS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Mask	RWS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Mask	RWS	Reset to 0
13	Flow Control Protocol Error Mask	RWS	Reset to 0
14	Completion Timeout Mask	RWS	Reset to 0
15	Completion Abort Mask	RWS	Reset to 0
16	Unexpected Completion Mask	RWS	Reset to 0
17	Receiver Overflow Mask	RWS	Reset to 0
18	Malformed TLP Mask	RWS	Reset to 0
19	ECRC Error Mask	RWS	Reset to 0
20	Unsupported Request Error Mask	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

7.4.101UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

Bit	Function	Type	Description
0	Training Error Severity	RWS	Reset to 1
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Severity	RWS	Reset to 1
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Severity	RWS	Reset to 0
13	Flow Control Protocol Error Severity	RWS	Reset to 1
14	Completion Timeout Severity	RWS	Reset to 0
15	Completer Abort Severity	RWS	Reset to 0
16	Unexpected Completion Severity	RWS	Reset to 0
17	Receiver Overflow Severity	RWS	Reset to 1

Bit	Function	Type	Description
18	Malformed TLP Severity	RWS	Reset to 1
19	ECRC Error Severity	RWS	Reset to 0
20	Unsupported Request Error Severity	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

7.4.102CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h

Bit	Function	Type	Description
0	Receiver Error Status	RWCS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Status	RWCS	Reset to 0
7	Bad DLLP Status	RWCS	Reset to 0
8	REPLAY_NUM Rollover Status	RWCS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Status	RWCS	Reset to 0
13	Advisory Non-Fatal Error Status	RWCS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.4.103CORRECTABLE ERROR MASK REGISTER – OFFSET 114h

Bit	Function	Type	Description
0	Receiver Error Mask	RWS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Mask	RWS	Reset to 0
7	Bad DLLP Mask	RWS	Reset to 0
8	REPLAY_NUM Rollover Mask	RWS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Mask	RWS	Reset to 0
13	Advisory Non-Fatal Error Mask	RWS	This bit is set by default to enable compatiblity with software that does not comprehend Role-Based Error Reporting Reset to 1
31:14	Reserved	RO	Reset to 0

7.4.104ADVANCED ERROR CAPABILITIES & CONTROL REGISTER – OFFSET 118h

Bit	Function	Type	Description
4:0	First Error Pointer	ROS	Reset to 0h
5	ECRC Generation Capable	RO	Reset to 1
6	ECRC Generation Enable	RWS	Reset to 0
7	ECRC Check Capable	RO	Reset to 1
8	ECRC Check Enable	RWS	Reset to 0
31:9	Reserved	RO	Reset to 0

7.4.105HEADER LOG REGISTER 1 – OFFSET 11Ch

Bit	Function	Type	Description
7:0	Header Byte 3	ROS	Reset to 0
15:8	Header Byte 2	ROS	Reset to 0
23:16	Header Byte 1	ROS	Reset to 0
31:24	Header Byte 0	ROS	Reset to 0

7.4.106HEADER LOG REGISTER 2 – OFFSET 120h

Bit	Function	Type	Description
7:0	Header Byte 7	ROS	Reset to 0
15:8	Header Byte 6	ROS	Reset to 0
23:16	Header Byte 5	ROS	Reset to 0
31:24	Header Byte 4	ROS	Reset to 0

7.4.107HEADER LOG REGISTER 3 – OFFSET 124h

Bit	Function	Type	Description
7:0	Header Byte 11	ROS	Reset to 0
15:8	Header Byte 10	ROS	Reset to 0
23:16	Header Byte 9	ROS	Reset to 0
31:24	Header Byte 8	ROS	Reset to 0

7.4.108HEADER LOG REGISTER 4 – OFFSET 128h

Bit	Function	Type	Description
7:0	Header Byte 15	ROS	Reset to 0
15:8	Header Byte 14	ROS	Reset to 0
23:16	Header Byte 13	ROS	Reset to 0
31:24	Header Byte 12	ROS	Reset to 0

7.4.109SECONDARY UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 12Ch

Bit	Function	Type	Description
0	Target Abort on Split Completion Status	RWCS	Reset to 0
1	Master Abort on Split Completion Status	RWCS	Reset to 0
2	Received Target Abort Status	RWCS	Reset to 0
3	Received Master Abort Status	RWCS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Status	RWCS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Status	RWCS	Reset to 0
7	Uncorrectable Data Error Status	RWCS	Reset to 0
8	Uncorrectable Attribute Error Status	RWCS	Reset to 0
9	Uncorrectable Address Error Status	RWCS	Reset to 0

Bit	Function	Type	Description
10	Delayed Transaction Discard Timer Expired Status	RWCS	Reset to 0
11	PERR_L Assertion Detected Status	RWCS	Reset to 0
12	SERR_L Assertion Detected Status	RWCS	Reset to 0
13	Internal Bridge Error Status	RWCS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.4.110SECONDARY UNCORRECTABLE ERROR MASK REGISTER – OFFSET 130h

Bit	Function	Type	Description
0	Target Abort on Split Completion Mask	RWS	Reset to 0
1	Master Abort on Split Completion Mask	RWS	Reset to 0
2	Received Target Abort Mask	RWS	Reset to 0
3	Received Master Abort Mask	RWS	Reset to 1
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Mask	RWS	Reset to 1
6	Uncorrectable Split Completion Message Data Error Mask	RWS	Reset to 0
7	Uncorrectable Data Error Mask	RWS	Reset to 1
8	Uncorrectable Attribute Error Mask	RWS	Reset to 1
9	Uncorrectable Address Error Mask	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Mask	RWS	Reset to 1
11	PERR_L Assertion Detected Mask	RWS	Reset to 0
12	SERR_L Assertion Detected Mask	RWS	Reset to 1
13	Internal Bridge Error Mask	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.4.111SECONDARY UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 134h

Bit	Function	Type	Description
0	Target Abort on Split Completion Severity	RWS	Reset to 0
1	Master Abort on Split Completion Severity	RWS	Reset to 0
2	Received Target Abort Severity	RWS	Reset to 0
3	Received Master Abort Severity	RWS	Reset to 0
4	Reserved	RO	Reset to 0

Bit	Function	Type	Description
5	Unexpected Split Completion Error Severity	RWS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Severity	RWS	Reset to 1
7	Uncorrectable Data Error Severity	RWS	Reset to 0
8	Uncorrectable Attribute Error Severity	RWS	Reset to 1
9	Uncorrectable Address Error Severity	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Severity	RWS	Reset to 0
11	PERR_L Assertion Detected Severity	RWS	Reset to 0
12	SERR_L Assertion Detected Severity	RWS	Reset to 1
13	Internal Bridge Error Severity	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.4.112SECONDARY ERROR CAPABILITY AND CONTROL REGISTER – OFFSET 138h

Bit	Function	Type	Description
4:0	Secondary First Error Pointer	ROW	Reset to 0
31:5	Reserved	RO	Reset to 0

7.4.113SECONDARY HEADER LOG REGISTER – OFFSET 13Ch – 148h

Bit	Function	Type	Description
35:0	Transaction Attribute	ROS	Transaction attribute, CBE [3:0] and AD [31:0] during attribute phase Reset to 0
39:36	Transaction Command Lower	ROS	Transaction command lower, CBE [3:0] during first address phase Reset to 0
43:40	Transaction Command Upper	ROS	Transaction command upper, CBE [3:0] during second address phase of DAC transaction Reset to 0
63:44	Reserved	ROS	Reset to 0
95:64	Transaction Address	ROS	Transaction address, AD [31:0] during first address phase Reset to 0
127:96	Transaction Address	ROS	Transaction address, AD [31:0] during second address phase of DAC transaction Reset to 0

7.4.114RESERVED REGISTER – OFFSET 14Ch

7.4.115VC CAPABILITY ID REGISTER – OFFSET 150h

Bit	Function	Type	Description
15:0	VC Capability ID	RO	Reset to 0002h

7.4.116VC CAPABILITY VERSION REGISTER – OFFSET 150h

Bit	Function	Type	Description
19:16	VC Capability Version	RO	Reset to 1h

7.4.117NEXT CAPABILITY OFFSET REGISTER – OFFSET 150h

Bit	Function	Type	Description
31:20	Next Capability Offset	RO	Next capability offset – the end of capabilities Reset to 0

7.4.118PORT VC CAPABILITY REGISTER 1 – OFFSET 154h

Bit	Function	Type	Description
2:0	Extended VC Count	RO	Reset to 0
3	Reserved	RO	Reset to 0
6:4	Low Priority Extended VC Count	RO	Reset to 0
7	Reserved	RO	Reset to 0
9:8	Reference Clock	RO	Reset to 0
11:10	Port Arbitration Table Entry Size	RO	Reset to 0
31:12	Reserved	RO	Reset to 0

7.4.119PORT VC CAPABILITY REGISTER 2 – OFFSET 158h

Bit	Function	Type	Description
7:0	VC Arbitration Capability	RO	Reset to 0
23:8	Reserved	RO	Reset to 0
31:24	VC Arbitration Table Offset	RO	Reset to 0

7.4.120PORT VC CONTROL REGISTER – OFFSET 15Ch

Bit	Function	Type	Description
0	Load VC Arbitration Table	RO	Reset to 0
3:1	VC Arbitration Select	RO	Reset to 0
15:4	Reserved	RO	Reset to 0

7.4.121PORT VC STATUS REGISTER – OFFSET 15Ch

Bit	Function	Type	Description
16	VC Arbitration Table Status	RO	Reset to 0
31:17	Reserved	RO	Reset to 0

7.4.122VC0 RESOURCE CAPBILITY REGISTER – OFFSET 160h

Bit	Function	Type	Description
7:0	Port Arbitration Capability	RO	Reset to 0
13:8	Reserved	RO	Reset to 0
14	Advanced Packet Switching	RO	Reset to 0
15	Reject Snoop Transactions	RO	Reset to0
22:16	Maximum Time Slots	RO	Reset to 0
23	Reserved	RO	Reset to 0
31:24	Port Arbitration Table Offset	RO	Reset to 0

7.4.123VC0 RESOURCE CONTROL REGISTER – OFFSET 164h

Bit	Function	Type	Description
0	TC/VC Map(for TC0)	RO	Reset to 1
7:1	TC/VC Map(for TC7~1)	RW	Reset to 7Fh
15:8	Reserved	RO	Reset to 0
16	Load Port Arbitration Table	RO	Reset to 0
19:17	Port Arbitration Select	RO	Reset to 0
23:20	Reserved	RO	Reset to 0
26:24	VC ID	RO	Reset to 0
30:27	Reserved	RO	Reset to 0
31	VC Enable	RO	Reset to 1

7.4.124VC0 RESOURCE STATUS REGISTER – OFFSET 168h

Bit	Function	Type	Description
0	Port Arbitration Table 1	RO	Reset to 0
1	VC0 Negotiation Pending	RO	Reset to 0
31:2	Reserved	RO	Reset to 0

7.4.125RESERVED REGISTERS – OFFSET 16Ch TO 2FCh

7.4.126EXTENDED GPIO DATA AND CONTROL REGISTER – OFFSET 300h

Bit	Function	Type	Description
2:0	Extended GPIO output	RWC	GPIO [6:4] as output, write 1 to clear Reset to 0
5:3	Extended GPIO output	RWS	GPIO [6:4] as output, write 1 to set Reset to 0
8:6	Extended GPIO output enable	RWC	GPIO [6:4] enable, write 1 to clear Reset to 0
11:9	Extended GPIO output enable	RWS	GPIO [6:4] enable, write 1 to set Reset to 0
14:12	Extended GPIO input	RO	GPIO [6:4] as input Reset to 0
31:16	Reserved	RO	Reset to 0

7.4.127EXTRA GPI/GPO DATA AND CONTROL REGISTER – OFFSET 304h

Bit	Function	Type	Description
3:0	Extra GPO	RWC	GPO [3:0], write 1 to clear Reset to 0
7:4	Extra GPO	RWS	GPO [3:0], write 1 to set Reset to 0
11:8	Extra GPO enable	RWC	GPO [3:0] enable, write 1 to clear Reset to 0
15:12	Extra GPO enable	RWS	GPO [3:0] enable, write 1 to set Reset to 0
19:16	Extra GPI	RO	Extra GPI [3:0] Data Register Reset to 0
31:20	Reserved	RO	Reset to 0

7.4.128RESERVED REGISTERS – OFFSET 308h TO 30Ch

7.4.129REPLAY AND ACKNOWLEDGE LATENCY TIMERS – OFFSET 310h

Bit	Function	Type	Description
11:0	Replay Timer	RW	Replay Timer Reset to 115h
12	Replay Timer Enable	RW	Replay Timer Enable Reset to 0
15:13	Reserved	RO	Reset to 0
26:16	Reserved	RO	Reset to 0
29:27	Upstream memory read request transmitting control	RW	Reset to 111
30	Acknowledge Latency Timer Enable	RW	Acknowledge Latency Timer Enable Reset to 0
31	Reserved	RO	Reset to 0

7.4.130RESERVED REGISTERS – OFFSET 314h TO FFCh

7.5 PCI CONFIGURATION REGISTERS FOR NON-TRANSPARENT BRIDGE MODE

The following section describes the configuration space when the device is in non-transparent bridge mode. The descriptions for different register type are listed as follow:

Register Type	Descriptions
RO	Read Only
ROS	Read Only and Sticky
RW	Read/Write
RO(WS)	Read Only at primary interface and Read/Write at secondary interface
RWC	Read/Write "1" to clear
RWS	Read/Write and Sticky
RWCS	Read/Write "1" to clear and Sticky

7.5.1 VENDOR ID – OFFSET 00h

Bit	Function	Type	Description
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. Returns 12D8h when read.

7.5.2 DEVICE ID – OFFSET 00h

Bit	Function	Type	Description
31:16	Device ID	RO	Identifies this device as the PI7C9X130. Returns E130 when read.

7.5.3 PRIMARY COMMAND REGISTER – OFFSET 04h

Bit	Function	Type	Description
0	I/O Space Enable	RW	0: Ignore I/O transactions on the primary interface 1: Enable response to memory transactions on the primary interface Reset to 0
1	Memory Space Enable	RW	0: Ignore memory read transactions on the primary interface 1: Enable memory read transactions on the primary interface Reset to 0
2	Bus Master Enable	RW	0: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on the secondary interface 1: Enable the PI7C9X130 to operate as a master on the primary interfaces for memory and I/O transactions forwarded from the secondary interface. If the primary of the reverse bridge is PCI-X mode, the PI7C9X130 is allowed to initiate a split completion transaction regardless of the status bit. Reset to 0
3	Special Cycle Enable	RO	0: Bridge does not respond as a target to Special Cycle transactions, so this bit is defined as Read-Only and must return 0 when read Reset to 0
4	Memory Write and Invalidate Enable	RO	0: PI7C9X130 does not originate a Memory Write and Invalidate transaction. Implements this bit as Read-Only and returns 0 when read (unless forwarding a transaction for another master). This bit will be ignored in PCI-X mode. Reset to 0
5	VGA Palette Snoop Enable	RO	0: Ignore VGA palette snoop access on the primary Reset to 0

Bit	Function	Type	Description
6	Parity Error Response Enable	RW	0: May ignore any parity error that is detected and take its normal action 1: This bit if set, enables the setting of Master Data Parity Error bit in the Status Register when poisoned TLP received or parity error is detected and takes its normal action Reset to 0
7	Wait Cycle Control	RO	Wait cycle control not supported Reset to 0
8	Primary SERR_L Enable Bit	RW	0: Disable 1: Enable PI7C9X130 in forward bridge mode to report non-fatal or fatal error message to the Root Complex. Also, in reverse bridge mode to assert SERR_L on the primary interface Reset to 0
9	Fast Back-to-Back Enable	RO	Fast back-to-back enable not supported Reset to 0
10	Primary Interrupt Disable	RO / RW	0: INTx interrupt messages can be generated 1: Prevent INTx messages to be generated and any asserted INTx interrupts will be released. Reset to 0
15:11	Reserved	RO	Reset to 00000

7.5.4 PRIMARY STATUS REGISTER – OFFSET 04h

Bit	Function	Type	Description
18:16	Reserved	RO	Reset to 000
19	Primary Interrupt Status	RO	0: No INTx interrupt message request pending in PI7C9X130 primary 1: INTx interrupt message request pending in PI7C9X130 primary Reset to 0
20	Capability List Capable	RO	1: PI7C9X130 supports the capability list (offset 34h in the pointer to the data structure) Reset to 1
21	66MHz Capable	RO	**This bit applies to reverse bridge only.** 1: 66MHz capable Reset to 0 when forward bridge or 1 when reverse bridge.
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	**This bit applies to reverse bridge only.** 1: Enable fast back-to-back transactions Reset to 0 when forward bridge or 1 when reverse bridge with primary bus in PCI mode
24	Master Data Parity Error Detected	RWC	Bit set if its Parity Error Enable bit is set and either of the conditions occurs on the primary: FORWARD BRIDGE – • Receives a completion marked poisoned • Poisons a write request REVERSE BRIDGE – • Detected parity error when receiving data or Split Response for read • Observes P_PERR_L asserted when sending data or receiving Split Response for write • Receives a Split Completion Message indicating data parity error occurred for non-posted write Reset to 0

Bit	Function	Type	Description
26:25	DEVSEL_L Timing (medium decode)	RO	**These bits apply to reverse bridge only.** 00: fast DEVSEL_L decoding 01: medium DEVSEL_L decoding 10: slow DEVSEL_L decoding 11: reserved Reset to 00 when forward bridge or 01 when reverse bridge.
27	Signaled Target Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 completes a request using completer abort status on the primary REVERSE BRIDGE – This bit is set to indicate a target abort on the primary Reset to 0
28	Received Target Abort	RWC	FORWARD BRIDGE – This bit is set when bridge receives a completion with completer abort completion status on the primary REVERSE BRIDGE – This bit is set when PI7C9X130 detects a target abort on the primary Reset to 0
29	Received Master Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 receives a completion with unsupported request completion status on the primary REVERSE BRIDGE – This bit is set when PI7C9X130 detects a master abort on the primary
30	Signaled System Error	RWC	FORWARD BRIDGE – This bit is set when PI7C9X130 sends an ERR_FATAL or ERR_NON_FATAL message on the primary REVERSE BRIDGE – This bit is set when PI7C9X130 asserts SERR_L on the primary Reset to 0
31	Detected Parity Error	RWC	FORWARD BRIDGE – This bit is set when poisoned TLP is detected on the primary REVERSE BRIDGE – This bit is set when address or data parity error is detected on the primary Reset to 0

7.5.5 REVISION ID REGISTER – OFFSET 08h

Bit	Function	Type	Description
7:0	Revision	RO	Reset to 04h

7.5.6 CLASS CODE REGISTER – OFFSET 08h

Bit	Function	Type	Description
15:8	Programming Interface	RO	Subtractive decoding of non-transparent PCI bridge not supported Reset to 00000000
23:16	Sub-Class Code	RO	Sub-Class Code 10000000: Other bridge Reset to 10000000
31:24	Base Class Code	RO	Base class code 00000110: Bridge Device Reset to 00000110

7.5.7 PRIMARY CACHE LINE SIZE REGISTER – OFFSET 0C

Bit	Function	Type	Description
1:0	Reserved	RO	00: Cache line size of 1 DW and 2 DW are not supported Reset to 00
2	Cache Line Size	RW	1: Cache line size = 4 double words Reset to 0
3	Cache Line Size	RW	1: Cache line size = 8 double words Reset to 0
4	Cache Line Size	RW	1: Cache line size = 16 double words Reset to 0
5	Cache Line Size	RW	1: Cache line size = 32 double words
7:6	Reserved	RO	Bit [7:6] not supported Reset to 00

7.5.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

Bit	Function	Type	Description
15:8	Primary Latency Timer	RO / RW	8 bits of primary latency timer in PCI/PCI-X FORWARD BRIDGE – RO with reset to 00h REVERSE BRIDGE – RW with reset to 00h in PCI mode or 40h in PCI-X mode

7.5.9 PRIMARY HEADER TYPE REGISTER – OFFSET 0Ch

Bit	Function	Type	Description
22:16	Other Bridge Configuration	RO	Type-0 header format configuration (10 – 3Fh) Reset to 0000000
23	Single Function Device	RO	0: Indicates single function device Reset to 0
31:24	Reserved	RO	Reset to 00h

7.5.10 PRIMARY CSR AND MEMORY 0 BASE ADDRESS REGISTER – OFFSET 10h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01: 64-bit address decode range 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
11:4	Reserved	RO	Reset to 0

Bit	Function	Type	Description
31:12	Base Address	RW/RO	The size and type of this Base Address Register are defined from Downstream Memory 0 Setup Register (Offset 9Ch), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. The range of this register is from 4KB to 2GB. The lower 4KB if this address reange map to the PI7C9X130 CSRs into memory space. The remaining space is this range above 4KB, if any, specifies a range for forwarding downstream memory transactions. PI7X9X110A uses downstream Memory 0 Translated Base Register (Offset 98h) to formulate direct address translation. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.11 PRIMARY CSR IO BASE ADDRESS REGISTER – OFFSET 14h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 1
7:1	Reserved	RO	Reset to 0
31:8	Base Address	RO/RW	This Base Address Register maps to PI7C9X130 primary IO space. The maximum size is 256 bytes. Reset to 00000000h

7.5.12 DOWNSTREAM IO OR MEMORY 1 BASE ADDRESS REGISTER – OFFSET 18h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01: 64-bit address decode range 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
11:4	Reserved	RO	Reset to 0
31:12	Base Address	RW/RO	The size and type of this Base Address Register are defined from Downstream IO or Memory 1 Setup Register (Offset ACh), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup register to disable this register. The range of this register is from 4KB to 2GB for memory space or from 64B to 256B for IO space. PI7X9X110A uses downstream IO or Memory 1 Translated Base Register (Offset A8h) to formulate direct address translation. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.13 DOWNSTREAM MEMORY 2 BASE ADDRESS REGISTER – OFFSET 1Ch

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01, 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
11:4	Reserved	RO	Reset to 0
31:12	Base Address	RW/RO	The size and type of this Base Address Register are defined from Downstream Memory 2 Setup Register (CSR Offset 00Ch), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup register to disable this register. The range of this register is from 4KB to 2GB for memory space. PI7X9X110A uses downstream Memory 2 Translated Base Register (CSR Offset 008h) to formulate direct address translation. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.14 DOWNSTREAM MEMORY 3 BASE ADDRESS REGISTER – OFFSET 20h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01: 64-bit address decode range 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
11:4	Reserved	RO	Reset to 0
31:12	Base Address	RW/RO	The size and type of this Base Address Register are defined from Downstream Memory 3 Setup Register (CSR Offset 014h), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup registers (CSR Offset 014h and 018h) to disable this register. The range of this register is from 4KB to 9EB for memory space. PI7C9X130 uses Memory 3 Translated Base Register (CSR Offset 010h) to formulate direct address translation when 32-bit addressing programmed. When 64-bit addressing programmed, no address translation is performed. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.15 DOWNSTREAM MEMORY 3 UPPER BASE ADDRESS REGISTER – OFFSET 24h

Bit	Function	Type	Description
31:0	Base address	RO/RW	The size of this Base Address Register is defined from Downstream Memory 3 Upper 32-bit Setup Register (CSR Offset 018h), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup registers (CSR Offset 018h) to disable this register. This register defines the upper 32 bits of a memory range for downstream forwarding memory. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000000h

7.5.16 RESERVED REGISTER – OFFSET 28h

7.5.17 SUBSYSTEM ID AND SUBSYSTEM VENDOR ID REGISTER – OFFSET 2Ch

Bit	Function	Type	Description
15:0	Subsystem Vendor ID	RO	Identify the vendor ID for add-in card or subsystem Reset to 0000h
31:16	Subsystem ID	RO	Identify the vendor specific device ID for add-in card or subsystem Reset to 0000h

7.5.18 RESERVED REGISTER – OFFSET 30h

7.5.19 CAPABILITY POINTER – OFFSET 34h

Bit	Function	Type	Description
7:0	Capability Pointer	RO	Capability pointer to 80h Reset to 80h
31:8	Reserved	RO	Reset to 0

7.5.20 EXPANSION ROM BASE ADDRESS REGISTER – OFFSET 38h

Bit	Function	Type	Description
31:0	Expansion ROM Base Address	RO	Expansion ROM not supported. Reset to 00000000h

7.5.21 PRIMARY INTERRUPT LINE REGISTER – OFFSET 3Ch

Bit	Function	Type	Description
7:0	Primary Interrupt Line	RW	**These bits apply to reverse bridge only.** For initialization code to program to tell which input of the interrupt controller the bridge's INTA_L in connected to. Reset to 00000000

7.5.22 PRIMARY INTERRUPT PIN REGISTER – OFFSET 3Ch

Bit	Function	Type	Description
15:8	Primary Interrupt Pin	RO	**These bits apply to reverse bridge only.** 00000001: Designates interrupt pin INTA_L is used Reset to 00h when forward mode or 01h when reverse mode.

7.5.23 PRIMARY MINIMUM GRANT REGISTER – OFFSET 3Ch

Bit	Function	Type	Description
23:16	Primary Minimum Grant	RO	This register is valid only in reverse bridge mode. It specifies how long of a burst period that PI7C9X130 needs on the primary bus in the units of ¼ microseconds. Reset to 0

7.5.24 PRIMARY MAXIMUM LATNECY TIMER – OFFSET 3Ch

Bit	Function	Type	Description
31:24	Primary Maximum Latency Timer	RO	This register is valid only in reverse bridge mode. It specifies how often that PI7C9X130 needs to gain access to the primary bus in units of ¼ microseconds. Reset to 0

7.5.25 PCI DATA BUFFERING CONTROL REGISTER – OFFSET 40h

Bit	Function	Type	Description
0	Secondary Internal Arbiter's PARK Function	RW	0: Park to the last master 1: Park to PI7C9X130 secondary port Reset to 0
1	Memory Read Prefetching Dynamic Control Disable	RW	0: Enable memory read prefetching dynamic control for PCI to PCIe read 1: Disable memory read prefetching dynamic control for PCI to PCIe read Reset to 0
2	Completion Data Prediction Control	RW	0: Enable completion data prediction for PCI to PCIe read. 1: Disable completion data prediction Reset to 0
3	Reserved	RO	Reset to 0
5:4	PCI Read Multiple Prefetch Mode	RW	00: One cache line prefetch if memory read multiple address is in prefetchable range at PCI interface 10: Full prefetch if address is in prefetchable range at PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after it disconnected external master during burst read with Read Multiple command, until discard timer expired. 11: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after the Read Multiple is terminated either by ex-master or by bridge, until discard timer expired. These bits are ignored if PCI/X interface is in PCIX mode. Reset to 10

Bit	Function	Type	Description
7:6	PCI Read Line Prefetch Mode	RW	00: One cache line prefetch if memory read line address is in prefetchable range at PCI interface 10: Full prefetch if memory read line address is in prefetchable range at PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after it disconnected external master during burst read with Read Line command, until discard timer expired. 11: Full prefetch if address is in prefetchable range at PCI interface and the bridge will keep remaining data after the Read Line is terminated either by ex-master or by bridge, until discard timer expired. These bits are ignored if PCI/X interface is in PCIX mode. Reset to 00
9:8	PCI Read Prefetch Mode	RW	**00**: One cache line prefetch if memory read address is in prefetchable range at PCI interface **01**: Reserved **10**: Full prefetch if memory read address is in prefetchable range at PCI interface **11**: Disconnect on the first DWORD Reset to 00
10	PCI Special Delayed Read Mode Enable	RW	0: Retry any master at PCI bus that repeats its transaction with command code changes. 1: Allows any master at PCI bus to change memory command code (MR, MRL, MRM) after it has received a retry. The PI7C9X130 will complete the memory read transaction and return data back to the master if the address and byte enables are the same. Reset to 0
11	Reserved	RO	Reset to 0
14:12	Maximum Memory Read Byte Count	RW	Maximum byte count is used by the PI7C9X130 when generating memory read requests on the PCIe link in response to a memory read initiated on the PCI bus and bit [9:8], bit [7:6], and bit [5:4] are set to “full prefetch”. 000: 512 bytes 001: 128 bytes 010: 256 bytes 011: 512 bytes 100: 1024 bytes 101: 2048 bytes 110: 4096 bytes 111: 512 bytes Reset to 000

7.5.26 CHIP CONTROL 0 REGISTER – OFFSET 40h

Bit	Function	Type	Description
15	Flow Control Update Control	RW	0: Flow control is updated for every two credits available 1: Flow control is updated for every on credit available Reset to 0
16	PCI Retry Counter Status	RWC	0: The PCI retry counter has not expired since the last reset 1: The PCI retry counter has expired since the last reset Reset to 0
18:17	PCI Retry Counter Control	RW	00: No expiration limit 01: Allow 256 retries before expiration 10: Allow 64K retries before expiration 11: Allow 2G retries before expiration Reset to 00

Bit	Function	Type	Description
19	PCI Discard Timer Disable	RW	0: Enable the PCI discard timer in conjunction with bit [27] offset 3Ch (bridge control register) 1: Disable the PCI discard timer in conjunction with bit [27] offset 3Ch (bridge control register) Reset to 0
20	PCI Discard Timer Short Duration	RW	0: Use bit [24] offset 3Ch for forward bridge or bit [25] offset 3Ch for reverse bridge to indicate how many PCI clocks should be allowed before the PCI discard timer expires 1: 64 PCI clocks allowed before the PCI discard timer expires Reset to 0
22:21	Configuration Request Retry Timer Counter Value Control	RW	00: Timer expires at 25us 01: Timer expires at 0.5ms 10: Timer expires at 5ms 11: Timer expires at 25ms Reset to 01
23	Delayed Transaction Order Control	RW	0: Enable out-of-order capability between delayed transactions 1: Disable out-of-order capability between delayed transactions Reset to 0
25:24	Completion Timer Counter Value Control	RW	00: Timer expires at 50us 01: Timer expires at 1ms 10: Timer expires at 10ms 11: Timer expires at 50ms Reset to 01
26	Isochronous Traffic Support Enable	RW	0: All memory transactions from PCI-X to PCIe will be mapped to TC0 1: All memory transactions from PCI-X to PCIe will be mapped to Traffic Class defined in bit [29:27] of offset 40h. Reset to 0
29:27	Traffic Class Used For Isochronous Traffic	RW	This register can be programmed for virtual isochronous traffic mapping. By default, PI7C9X130 maps to traffic class 1. Reset to 001
30	Serial Link Interface Loopback Enable	RW / RO	0: Normal mode 1: Enable serial link interface loopback mode (TX to RX) if TM0=LOW, TM1=HIGH, TM2=HIGH, MSK_IN=HIGH, REVRSB=HIGH. PCI transaction from PCI bus will loop back to PCI bus RO for forward bridge Reset to 0
31	Primary Configuration Access Lockout	RO / RW	0: PI7C9X130 configuration space can be accessed from both interfaces 1: PI7C9X130 configuration space can only be accessed from the secondary interface. Primary bus accessed receives completion with CRS status for forward bridge, or target retry for reverse bridge Reset to 1 if TM0 is HIGH (the local host on secondary bus needs to program this bit to 0 after the secondary configuration programming is completed in non-transparent mode, otherwise there will be no configuration access from primary interface)

7.5.27 SECONDARY COMMAND REGISTER – OFFSET 44h

Bit	Function	Type	Description
0	I/O Space Enable	RW	0: Ignore I/O transactions on the secondary interface 1: Enable response to memory transactions on the secondary interface Reset to 0

Bit	Function	Type	Description
1	Memory Space Enable	RW	0: Ignore memory read transactions on the secondary interface 1: Enable memory read transactions on the secondary interface Reset to 0
2	Bus Master Enable	RW	0: Do not initiate memory or I/O transactions on the secondary interface and disable response to memory and I/O transactions on the secondary interface 1: Enable the PI7C9X130 to operate as a master on the secondary interfaces for memory and I/O transactions forwarded from the secondary interface. If the secondary of the reverse bridge is PCI-X mode, the PI7C9X130 is allowed to initiate a split completion transaction regardless of the status bit. Reset to 0
3	Special Cycle Enable	RO	0: Bridge does not respond as a target to Special Cycle transactions, so this bit is defined as Read-Only and must return 0 when read Reset to 0
4	Memory Write and Invalidate Enable	RO	0: PI7C9X130 does not originate a Memory Write and Invalidate transaction. Implements this bit as Read-Only and returns 0 when read (unless forwarding a transaction for another master). This bit will be ignored in PCI-X mode. Reset to 0
5	VGA Palette Snoop Enable	RO	0: Ignore VGA palette snoop access on the secondary Reset to 0
6	Parity Error Response Enable	RW	0: May ignore any parity error that is detected and take its normal action 1: This bit if set, enables the setting of Master Data Parity Error bit in the Status Register when poisoned TLP received or parity error is detected and takes its normal action Reset to 0
7	Wait Cycle Control	RO	Wait cycle control not supported Reset to 0
8	Secondary SERR_L Enable Bit	RW	0: Disable 1: Enable PI7C9X130 in forward bridge mode to report non-fatal or fatal error message to the Root Complex. Also, in reverse bridge mode to assert SERR_L on the secondary interface Reset to 0
9	Fast Back-to-Back Enable	RO	Fast back-to-back enable not supported Reset to 0
10	Secondary Interrupt Disable	RO / RW	0: INTx interrupt messages can be generated 1: Prevent INTx messages to be generated and any asserted INTx interrupts will be released. Reset to 0
15:11	Reserved	RO	Reset to 00000

7.5.28 SECONDARY STATUS REGISTER – OFFSET 44h

Bit	Function	Type	Description
18:16	Reserved	RO	Reset to 000
19	Secondary Interrupt Status	RO	0: No INTx interrupt message request pending in PI7C9X130 secondary 1: INTx interrupt message request pending in PI7C9X130 secondary Reset to 0
20	Capability List Capable	RO	1: PI7C9X130 supports the capability list (offset 34h in the pointer to the data structure) Reset to 1
21	66MHz Capable	RO	**This bit applies to forward bridge only.** 1: 66MHz capable Reset to 0 when reverse bridge or 1 when forward bridge.

Bit	Function	Type	Description
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	**This bit applies to forward bridge only.** 1: Enable fast back-to-back transactions Reset to 0 when reverse bridge or 1 when forward bridge with secondary bus in PCI mode
24	Master Data Parity Error Detected	RWC	Bit set if its Parity Error Enable bit is set and either of the conditions occurs on the secondary: REVERSE BRIDGE – • Receives a completion marked poisoned • Poisons a write request FORWARD BRIDGE – • Detected parity error when receiving data or Split Response for read • Observes P_PERR_L asserted when sending data or receiving Split Response for write • Receives a Split Completion Message indicating data parity error occurred for non-posted write Reset to 0
26:25	DEVSEL_L Timing (medium decode)	RO	**These bits apply to forward bridge only.** 00: fast DEVSEL_L decoding 01: medium DEVSEL_L decoding 10: slow DEVSEL_L decoding 11: reserved Reset to 00 when reverse bridge or 01 when forward bridge.
27	Signaled Target Abort	RWC	**REVERSE BRIDGE –** This bit is set when PI7C9X130 completes a request using completer abort status on the secondary **FORWARD BRIDGE –** This bit is set to indicate a target abort on the secondary Reset to 0
28	Received Target Abort	RWC	**REVERSE BRIDGE –** This bit is set when bridge receives a completion with completer abort completion status on the secondary **FORWARD BRIDGE –** This bit is set when PI7C9X130 detects a target abort on the secondary Reset to 0
29	Received Master Abort	RWC	**REVERSE BRIDGE –** This bit is set when PI7C9X130 receives a completion with unsupported request completion status on the secondary **FORWARD BRIDGE –** This bit is set when PI7C9X130 detects a master abort on the secondary
30	Signaled System Error	RWC	**REVERSE BRIDGE –** This bit is set when PI7C9X130 sends an ERR_FATAL or ERR_NON_FATAL message on the secondary **FORWARD BRIDGE –** This bit is set when PI7C9X130 asserts SERR_L on the secondary Reset to 0
31	Detected Parity Error	RWC	**REVERSE BRIDGE –** This bit is set when poisoned TLP is detected on the secondary **FORWARD BRIDGE –** This bit is set when address or data parity error is detected on the secondary Reset to 0

7.5.29 ARBITER ENABLE REGISTER – OFFSET 48h

Bit	Function	Type	Description
0	Enable Arbiter 0	RW	0: Disable arbitration for internal PI7C9X130 request 1: Enable arbitration for internal PI7C9X130 request Reset to 1
1	Enable Arbiter 1	RW	0: Disable arbitration for master 1 1: Enable arbitration for master 1 Reset to 1
2	Enable Arbiter 2	RW	0: Disable arbitration for master 2 1: Enable arbitration for master 2 Reset to 1
3	Enable Arbiter 3	RW	0: Disable arbitration for master 3 1: Enable arbitration for master 3 Reset to 1
4	Enable Arbiter 4	RW	0: Disable arbitration for master 4 1: Enable arbitration for master 4 Reset to 1
5	Enable Arbiter 5	RW	0: Disable arbitration for master 5 1: Enable arbitration for master 5 Reset to 1
6	Enable Arbiter 6	RW	0: Disable arbitration for master 6 1: Enable arbitration for master 6 Reset to 1
7	Enable Arbiter 7	RW	0: Disable arbitration for master 7 1: Enable arbitration for master 7 Reset to 1
8	Enable Arbiter 8	RW	0: Disable arbitration for master 8 1: Enable arbitration for master 8 Reset to 1

7.5.30 ARBITER MODE REGISTER – OFFSET 48h

Bit	Function	Type	Description
9	External Arbiter Bit	RO	0: Enable internal arbiter (if CFN_L is tied LOW) 1: Use external arbiter (if CFN_L is tied HIGH) Reset to 0/1 according to what CFN_L is tied to
10	Broken Master Timeout Enable	RW	**0**: Broken master timeout disable **1**: This bit enables the internal arbiter to count 16 PCI bus cycles while waiting for FRAME_L to become active when a device's PCI bus GNT_L is active and the PCI bus is idle. If the broken master timeout expires, the PCI bus GNT for the device is de-asserted. Reset to 0
11	Broken Master Refresh Enable	RW	**0**: A broken master will be ignored forever after de-asserting its REQ_L for at least 1 clock **1**: Refresh broken master state after all the other masters have been served once Reset to 0

Bit	Function	Type	Description
19:12	Arbiter Fairness Counter	RW	08h: These bits are the initialization value of a counter used by the internal arbiter. It controls the number of PCI bus cycles that the arbiter holds a device's PCI bus GNT active after detecting a PCI bus REQ_L from another device. The counter is reloaded whenever a new PCI bus GNT is asserted. For every new PCI bus GNT, the counter is armed to decrement when it detects the new fall of FRAME_L. If the arbiter fairness counter is set to 00h, the arbiter will not remove a device's PCI bus GNT until the device has de-asserted its PCI bus REQ. Reset to 08h
20	GNT_L Output Toggling Enable	RW	**0**: GNT_L not de-asserted after granted master assert FRAME_L **1**: GNT_L de-asserts for 1 clock after 2 clocks of the granted master asserting FRAME_L Reset to 0
21	Reserved	RO	Reset to 0

7.5.31 ARBITER PRIORITY REGISTER – OFFSET 48h

Bit	Function	Type	Description
22	Arbiter Priority 0	RW	0: Low priority request to internal bridge 1: High priority request to internal bridge Reset to 1
23	Arbiter Priority 1	RW	0: Low priority request to master 1 1: High priority request to master 1 Reset to 0
24	Arbiter Priority 2	RW	0: Low priority request to master 2 1: High priority request to master 2 Reset to 0
25	Arbiter Priority 3	RW	0: Low priority request to master 3 1: High priority request to master 3 Reset to 0
26	Arbiter Priority 4	RW	0: Low priority request to master 4 1: High priority request to master 4 Reset to 0
27	Arbiter Priority 5	RW	0: Low priority request to master 5 1: High priority request to master 5 Reset to 0
28	Arbiter Priority 6	RW	0: Low priority request to master 6 1: High priority request to master 6 Reset to 0
29	Arbiter Priority 7	RW	0: Low priority request to master 7 1: High priority request to master 7 Reset to 0
30	Arbiter Priority 8	RW	0: Low priority request to master 8 1: High priority request to master 8 Reset to 0
31	Reserved	RO	Reset to 0

7.5.32 SECONDARY CACHE LINE SIZE REGISTER – OFFSET 4Ch

Bit	Function	Type	Description
1:0	Reserved	RO	00: Cache line size of 1 DW and 2 DW are not supported Reset to 00

Bit	Function	Type	Description
2	Cache Line Size	RW	1: Cache line size = 4 double words Reset to 0
3	Cache Line Size	RW	1: Cache line size = 8 double words Reset to 0
4	Cache Line Size	RW	1: Cache line size = 16 double words Reset to 0
5	Cache Line Size	RW	1: Cache line size = 32 double words Reset to 0
7:6	Reserved	RO	Bit [7:6] not supported Reset to 00

7.5.33 SECONDARY LATENCY TIMER REGISTER – OFFSET 4Ch

Bit	Function	Type	Description
15:8	Secondary Latency Timer	RO / RW	8 bits of secondary latency timer in PCI/PCI-X REVERSE BRIDGE – RO with reset to 00h FORWARD BRIDGE – RW with reset to 00h in PCI mode or 40h in PCI-X mode

7.5.34 SECONDARY HEADER TYPE REGISTER – OFFSET 4C

Bit	Function	Type	Description
22:16	Other Bridge Configuration	RO	Type-0 header format configuration (10 – 3Fh) Reset to 0000000
23	Single Function Device	RO	0: Indicates single function device Reset to 0
31:24	Reserved	RO	Reset to 00h

7.5.35 SECONDARY CSR AND MEMORY 0 BASE ADDRESS REGISTER – OFFSET 50h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01: 64-bit address decode range 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
11:4	Reserved	RO	Reset to 0

Bit	Function	Type	Description
31:12	Base Address	RW/RO	The size and type of this Base Address Register are defined from Upstream Memory 0 Setup Register (Offset E4h), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. The range of this register is from 4KB to 2GB. The lower 4KB if this address reange map to the PI7C9X130 CSRs into memory space. The remaining space is this range above 4KB, if any, specifies a range for forwarding upstream memory transactions. PI7X9X110A uses upstream Memory 0 Translated Base Register (Offset E0h) to formulate direct address translation. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.36 SECONDARY CSR IO BASE ADDRESS REGISTER – OFFSET 54h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 1
7:1	Reserved	RO	Reset to 0
31:8	Base Address	RO/RW	This Base Address Register maps to PI7C9X130 secondary IO space. The maximum size is 256 bytes. Reset to 00000000h

7.5.37 UPSTREAM IO OR MEMORY 1 BASE ADDRESS REGISTER – OFFSET 58h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01: 64-bit address decode range 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
5:4	Reserved	RO	Reset to 0
31:6	Base Address	RW/RO	The size and type of this Base Address Register are defined from Upstream IO or Memory 1 Setup Register (Offset ECh), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup register to disable this register. The range of this register is from 4KB to 2GB for memory space or from 64B to 256B for IO space. PI7X9X110A uses upstream IO or Memory 1 Translated Base Register (Offset E8h) to formulate direct address translation. If a bit in the setup register is set to one, then the correspondent bit of this register will be changed to RW. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.38 UPSTREAM MEMORY 2 BASE ADDRESS REGISTER – OFFSET 5Ch

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01, 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
13:4	Reserved	RO	Reset to 0
31:14	Base Address	RW/RO	This Base Address register defines the address range for upstream memory transactions. PI7C9X130 uses a lookup table to do the address translation. The address range of this register is from 16KB to 2GB in memory space. The address range is divided into 64 pages. The size of each page is defined by Memory Address Forwarding Control register (Offset 6Ah), which is initialized by EEPROM (I2C) or SM Bus or local processor. Writing a zero to the bit [0] of the look up table entry can disable the corresponding page of this register (CSR Offset 1FFh: 100h). The number of writeable bit may change depending on the page size setup. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.39 UPSTREAM MEMORY 3 BASE ADDRESS REGISTER – OFFSET 60h

Bit	Function	Type	Description
0	Space Indicator	RO	0: Memory space 1: IO space Reset to 0
2:1	Address Type	RO	00: 32-bit address decode range 01: 64-bit address decode range 10 and 11: reserved Reset to 00
3	Prefetchable control	RO	0: Memory space is non-prefetchable 1: Memory space is prefetchable Reset to 0
11:4	Reserved	RO	Reset to 0
31:12	Base Address	RW/RO	The size and type of this Base Address Register are defined from Upstream Memory 3 Setup Register (CSR Offset 034h), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup registers (CSR Offset 034h and 038h) to disable this register. The range of this register is from 4KB to 9EB for memory space. PI7C9X130 uses this register and the Upstream Memory 3 Upper Base Address Register when 64-bit addressing programmed (bit [21] of Offset 68h). When 64-bit addressing is disabled, no address translation is performed. All 64-bit address transactions on the secondary interface falling outside of the Downstream Memory 3 address range are forwarded upstream. Reset to 00000h This BAR is disabled if this filed is set to 0h.

7.5.40 UPSTREAM MEMORY 3 UPPER BASE ADDRESS REGISTER – OFFSET 64h

Bit	Function	Type	Description
31:0	Base address	RO/RW	The size of this Base Address Register is defined from Upstream Memory 3 Upper 32-bit Setup Register (CSR Offset 038h), which can be initialized by EEPROM (I2C) or SM Bus or Local Processor. Writing a zero to bit [31] of the setup registers (CSR Offset 038h) to disable this register. This register defines the upper 32 bits of a memory range for upstream forwarding memory. PI7C9X130 uses this register and the Upstream Memory 3 Base Address Register when 64-bit addressing programmed (bit [21] of Offset 68h). When 64-bit addressing is disabled, no address translation is performed. All 64-bit address transactions on the secondary interface falling outside of the Downstream Memory 3 address range are forwarded upstream. Reset to 00000000h

7.5.41 EXPRESS TRANSMITTER/RECEIVER CONTROL REGISTER – OFFSET 68h

Bit	Function	Type	Description
1:0	Nominal Driver Current Control	RW	00: 20mA 01: 10mA 10: 28mA 11: Reserved Reset to 00
5:2	Driver Current Scale Multiple Control	RW	0000: 1.00 x nominal driver current 0001: 1.05 x nominal driver current 0010: 1.10 x nominal driver current 0011: 1.15 x nominal driver current 0100: 1.20 x nominal driver current 0101: 1.25 x nominal driver current 0110: 1.30 x nominal driver current 0111: 1.35 x nominal driver current 1000: 1.60 x nominal driver current 1001: 1.65 x nominal driver current 1010: 1.70 x nominal driver current 1011: 1.75 x nominal driver current 1100: 1.80 x nominal driver current 1101: 1.85 x nominal driver current 1110: 1.90 x nominal driver current 1111: 1.95 x nominal driver current Reset to 0000
11:8	Driver De-emphasis Level Control	RW	0000: 0.00 db 0001: -0.35 db 0010: -0.72 db 0011: -1.11 db 0100: -1.51 db 0101: -1.94 db 0110: -2.38 db 0111: -2.85 db 1000: -3.35 db 1001: -3.88 db 1010: -4.44 db 1011: -5.04 db 1100: -5.68 db 1101: -6.38 db 1110: -7.13 db 1111: -7.96 db Reset to 1000
13:12	Transmitter Termination Control	RW	00: 52 ohms 01: 57 ohms 10: 43 ohms 11: 46 ohms Reset to 00

Bit	Function	Type	Description
15:14	Receiver Termination Control	RW	00: 52 ohms 01: 57 ohms 10: 43 ohms 11: 46 ohms Reset to 00

7.5.42 MEMORY ADDRESS FORWARDING CONTROL REGISTER – OFFSET 68h

Bit	Function	Type	Description

19:16	Lookup Table Page Size	RW	If bit [20] of Offset 68h is low, then
			0000: Disable Upstream Memory 2 Base Address Register
			0001: 256 bytes
			0010: 512 bytes
			0011: 1K bytes
			0100: 2K bytes
			0101: 4K bytes
			0110: 8K bytes
			0111: 16K bytes
			1000: 32K bytes
			1001: 64K bytes
			1010: 128K bytes
			1011: 256K bytes
			1100: 512K bytes
			1101: 1M bytes
			1110: 2M bytes
			1111: 4M bytes
			
			If bit [20] of Offset 68h is high, then
			0000: Disable Upstream Memory 2 Base Address Register
			0001: 8M bytes
			0010: 16M bytes
			0011: 32M bytes
			01XX: Disable Upstream Memory 2 Base Address Register
			1XXX: Disable Upstream Memory 2 Base Address Register
			
			Reset to 0h

20	Lookup Table Page Size Extension	RW	0: Normal Lookup Table Page Size 1: Coarse Lookup Table Page Size Reset to 0
21	Upstream 64-bit Address Range Enable	RW	0: Any 64-bit address transactions on secondary interface falling outside of Downstream Memory 3 address range are forwarded upstream 1: Enable 64-bit address transaction forwarding upstream based on Upstream Memory 3 address range without address translation Reset to 0
26:22	Reserved	RO	Reset to 0
29:27	Upstream memory read request transmitting control	RW	Reset to 111

7.5.43 UPSTREAM MEMORY WRITE FRAGMENT CONTROL REGISTER – OFFSET 68h

Bit	Function	Type	Description
31:30	Memory Write Fragment Control	RW	Upstream Memory Write Fragment Control 00: Fragment at 32-byte boundary 01: Fragment at 64-byte boundary 1x: Fragement at 128-byte boundary Reset to 10

7.5.44 SUBSYSTEM VENDOR ID REGISTER – OFFSET 6Ch

Bit	Function	Type	Description
15:0	Subsystem Vendor ID	RO	Subsystem vendor ID identifies the particular add-in card or subsystem Reset to 00h

7.5.45 SUBSYSTEM ID REGISTER – OFFSET 6Ch

Bit	Function	Type	Description
31:16	Subsystem ID	RO	Subsystem ID identifies the particular add-in card or subsystem Reset to 00h

7.5.46 EEPROM AUTOLOAD CONTROL/STATUS REGISTER – OFFSET 70h (default=00000080h)

Bit	Function	Type	Description
0	Initiate EEPROM Read or Write Cycle	RW	This bit will be reset to 0 after the EEPROM operation is finished 0:EEPROM AUTOLOAD disabled 0 -> 1: Starts the EEPROM Read or Write cycle Reset to 0
1	Control Command for EEPROM	RW	0: Read 1: Write Reset to 0
2	EEPROM Error	RO	0: EEPROM acknowledge is always received during the EEPROM cycle 1: EEPROM acknowledge is not received during EEPROM cycle Reset to 0
3	EPROM Autoload Complete Status	RO	0: EEPROM autoload is not successfully completed 1: EEPROM autoload is successfully completed Reset to 0
5:4	EEPROM Clock Frequency Control	RW	Where PCLK is 125MHz 00: PCLK / 4096 01: PCLK / 2048 10: PCLK / 1024 11: PCLK / 128 Reset to 00
6	EEPROM Autoload Control	RW	0: Enable EEPROM autoload 1: Disable EEPROM autoload Reset to 0
7	Fast EEPROM Autoload Control	RW	0: Normal speed of EEPROM autoload 1: Increase EEPROM autoload by 32x Reset to 1
8	EEPROM Autoload Status	RO	0: EEPROM autoload is not on going 1: EEPROM autoload is on going Reset to 0
15:9	EEPROM Word Address	RW	EEPROM word address for EEPROM cycle Reset to 0000000
31:16	EEPROM Data	RW	EEPROM data to be written into the EEPROM Reset to 0000h

7.5.47 HOT SWAP CONTROL AND STATUS REGISTER – OFFSET 74h

Bit	Function	Type	Description
7:0	Capability ID for Hot Swap	RO	Reset to 06h when Hot Sawp is enable (HS_EN=1) or 00h when Hot Swap is disabled (HS_EN=0)
15:8	Next Capability Pointer	RO	Reset to 00h to inidicate the end of the capability chain
16	Device Hiding Arm	RW	Device Hiding Armed when this bit is set to 1 Reset to 0
17	ENUM_L signal Mask	RW	ENUM_L signal is masked when this bit is set to 1 Reset to 0
18	Pending Insertion or Extraction	RW	When this bit is 1, INS is armed, or either INS or EXT has a value of logic 1 When this bit is 0, INS is not armed or both INS and EXT have a value of logic 0 Reset to 0h
19	LED On Off	RW	When this bit is 1, LED is on When this bit is 0, LED is off Reset to 0
21:20	Programming Interface	RO	PI=01 supports PI=00 plus device hiding and pending insertion or extraction bits Reset to 01
22	EXT for Extraction	RWC	EXT bit indicates ENUM_L status of extraction. When EXT is 1, ENUM_L is asserted Reset to 0
23	INS for Insertion	RWC	INS bit indicates ENUM_L status of insertion. When INS is 1, ENUM_L is asserted Reset to 1
31:24	Reserved	RO	Reset to 00h

7.5.48 BRIDGE CONTROL AND STATUS REGISTER – OFFSET 78h

Bit	Function	Type	Description
1:0	Reserved	RO	Reset to 00
2	SERR_L Forward Enable	RW/RO	**0**: Disable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL **1**: Enable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL Reset to 0 (FORWARD BRIDGE) RO bit for REVERSE BRIDGE
3	Secondary Interface Reset	RW	**0**: Do not force the assertion of RESET_L on secondary PCI/PCI-X bus in forward bridge mode, or do not generate a hot reset on the PCI Express link in reverse bridge mode **1**: Force the assertion of RESET_L on secondary PCI/PCI-X bus in forward bridge mode, or generate a hot reset on the PCI Express link in reverse bridge mode Reset to 0
5:4	VGA Enable	RW	**00**: VGA memory and I/O transactions on the primary and secondary interfaces are ignored, unless decoded by other mechanism **01**: VGA memory and I/O transactions on the primary interface are forwarded to secondary interface without address translation, but VGA transactions on secondary interface are ignored **10**: VGA memory and I/O transactions on the secondary interface are forwarded to primary interface without address translation, but VGA transactions on primary interface are ignored Reset to 00

Bit	Function	Type	Description
6	VGA 16-bit Decode	RW	0: Execute 10-bit address decodes on VGA I/O accesses 1: Execute 16-bit address decode on VGA I/O accesses Reset to 0
7	Master Abort Mode	RW	0: Do not report master aborts (return FFFFFFFFh on reads and discards data on write) 1: Report master abort by signaling target abort if possible or by the assertion of SERR_L (if enabled). Reset to 0
8	Primary Master Timeout	RW	0: Primary discard timer counts 2^{15} PCI clock cycles 1: Primary discard timer counts 2^{10} PCI clock cycles FORWARD BRIDGE – Bit is RO and ignored by PI7C9X130 Reset to 0
9	Secondary Master Timeout	RW	0: Secondary discard timer counts 2^{15} PCI clock cycles 1: Secondary discard timer counts 2^{10} PCI clock cycles REVERSE BRIDGE – Bit is RO and ignored by PI7C9X130 Reset to 0
10	Master Timeout Status	RWC	Bit is set when the discard timer expires and a delayed completion is discarded at the PCI interface for the forward or reverse bridge Reset to 0
11	Discard Timer SERR_L Enable	RW	Bit is set to enable to generate ERR_NONFATAL or ERR_FATAL for forward bridge, or assert SERR_L for reverse bridge as a result of the expiration of the discard timer. It has no meaning if PI7C9X130 is in PCI-X mode. Reset to 0

7.5.49 GPIO DATA AND CONTROL REGISTER – OFFSET 78h

Bit	Function	Type	Description
15:12	GPIO Output Write-1-to-Clear	RW	Reset to 0h
19:16	GPIO Output Write-1-to-Set	RW	Reset to 0h
23:20	GPIO Output Enable Write-1-to-Clear	RW	Reset to 0h
27:24	GPIO Output Enable Write-1-to-Set	RW	Reset to 0h
31:28	GPIO Input Data Register	RO	Reset to 0h

7.5.50 SECONDARY INTERRUPT LINE REGISTER – OFFSET 7Ch

Bit	Function	Type	Description
7:0	Secondary Interrupt Line	RW	**These bits apply to forward bridge only.** For initialization code to program to tell which input of the interrupt controller the bridge's INTA_L in connected to. Reset to 00000000

7.5.51 SECONDARY INTERRUPT PIN REGISTER – OFFSET 7Ch

Bit	Function	Type	Description
15:8	Secondary Interrupt Pin	RO	**These bits apply to forward bridge only.** 00000001: Designates interrupt pin INTA_L is used Reset to 00h when reverse mode or 01h when forward mode.

7.5.52 SECONDARY MINIMUM GRANT REGISTER – OFFSET 7Ch

Bit	Function	Type	Description
23:16	Secondary Minimum Grant	RO	This register is valid only in forward bridge mode. It specifies how long of a burst period that PI7C9X130 needs on the secondary bus in the units of ¼ microseconds. Reset to 0

7.5.53 SECONDARY MAXIMUM LATENCY TIMER – OFFSET 7Ch

Bit	Function	Type	Description
31:24	Secondary Maximum Latency Timer	RO	This register is valid only in forward bridge mode. It specifies how often that PI7C9X130 needs to gain access to the primary bus in units of ¼ microseconds. Reset to 0

7.5.54 PCI-X CAPABILITY ID REGISTER – OFFSET 80h

Bit	Function	Type	Description
7:0	PCI-X Capability ID	RO	PCI-X Capability ID Reset to 07h

7.5.55 NEXT CAPABILITY POINTER REGISTER – OFFSET 80h

Bit	Function	Type	Description
15:8	Next Capability Pointer	RO	Point to power management Reset to 90h

7.5.56 PCI-X SECONDARY STATUS REGISTER – OFFSET 80h

Bit	Function	Type	Description
16	64-bit Device on Secondary Bus Interface	RO	64-bit supported when DEV64 is set to high Reset to 1in forward bridge mode and DEV64 is set to high or reset to 0 in reverse bridge mode
17	133MHz Capable	RO	When this bit is 1, PI7C9X130 is 133MHz capable on its secondary bus interface Reset to 1 in forward bridge mode or 0 in reverse bridge mode
18	Split Completion Discarded	RO / RWC	This bit is a read-only and set to 0 in reverse bridge mode or is read-write in forward bridge mode When this is set to 1, a split completion has been discarded by PI7C9X130 at secondary bus because the requester did not accept the split completion transaction Reset to 0

Bit	Function	Type	Description
19	Unexpected Split Completion	RWC	This bit is set to 0 in forward bridge mode or is read-write in reverse bridge mode When this bit is set to 1, an unexpected split completion has been received with the requester ID equaled to the secondary bus number, device number, and function number at the PI7X9X130 secondary bus interface Reset to 0
20	Split Completion Overrun	RWC	When this bit is set to 1, a split completion has been terminated by PI7C9X130 with either a retry or disconnect at the next ADB due to the buffer full condition Reset to 0
21	Split Request Delayed	RWC	When this bit is set to 1, a split request is delayed because PI7C9X130 is not able to forward the split request transaction to its secondary bus due to insufficient room within the limit specified in the split transaction commitment limit field of the downstream split transaction control register Reset to 0
24:22	Secondary Clock Frequency	RO	These bits are only meaningful in forward bridge mode. In reverse bridge mode, all three bits are set to zero. 000: Conventional PCI mode (minimum clock period not applicable) 001: 66MHz (minimum clock period is 15ns) 010: 100 to 133MHz (minimum clock period is 7.5ns) 011: Reserved 1xx: Reserved Reset to 000
31:25	Reserved	RO	0000000

7.5.57 PCI-X BRIDGE STATUS REGISTER – OFFSET 84h

Bit	Function	Type	Description
2:0	Function Number	RO	Function number (AD [10:8] of a type 0 configuration transaction) Reset to 000
7:3	Device Number	RO	Device number (AD [15:11] of a type 0 configuration transaction) is assigned to the PI7C9X130 by the connection of system hardware. Each time the PI7C9X130 is addressed by a configuration write transaction, the bridge updates this register with the contents of AD [15:11] of the address phase of the configuration transaction, regardless of which register in the PI7C9X130 is addressed by the transaction. The PI7C9X130 is addressed by a configuration write transaction if all of the following are true: • The transaction uses a configuration write command • IDSEL is asserted during the address phase • AD [1:0] are 00 (type o configuration transaction) • AD [10:8] of the configuration address contain the appropriate function number Reset to 11111
15:8	Bus Number	RO	Additional address from which the contents of the primary bus number register on type 1 configuration space header is read. The PI7C9X130 uses the bus number, device number, and function number fields to create a completer ID when responding with a split completion to a read of an internal PI7C9X130 register. These fields are also used for cases when one interface is in conventional PCI mode and the other is in PCI-X mode. Reset to 11111111
16	64-bit Device on Primary Bus Interface	RO	64-bit supported when DEV64 is set to high Reset to 0 in forward bridge mode or in reverse bridge mode with REQ64_L is high at the de-assertion of RESET_L or reset to 1 in reverse bridge mode with REQ64_L is low at the de-assertion of RESET_L

Bit	Function	Type	Description
17	133MHz Capable	RO	When this bit is 1, PI7C9X130 is 133MHz capable on its primary bus interface Reset to 0 in forward bridge mode or 1 in reverse bridge mode
18	Split Completion Discarded	RO / RWC	This bit is a read-only and set to 0 in reverse bridge mode or is read-write in forward bridge mode When this is set to 1, a split completion has been discarded by PI7C9X130 at primary bus because the requester did not accept the split completion transaction Reset to 0
19	Unexpected Split Completion	RWC	This bit is set to 0 in forward bridge mode or is read-write in reverse bridge mode When this is set to 1, an unexpected split completion has been received with the requester ID equaled to the primary bus number, device number, and function number at the PI7X9X130 primary bus interface Reset to 0
20	Split Completion Overrun	RWC	When this bit is set to 1, a split completion has been terminated by PI7C9X130 with either a retry or disconnect at the next ADB due to the buffer full condition Reset to 0
21	Split Request Delayed	RWC	When this bit is set to 1, a split request is delayed because PI7C9X130 is not able to forward the split request transaction to its primary bus due to insufficient room within the limit specified in the split transaction commitment limit field of the downstream split transaction control register Reset to 0
31:22	Reserved	RO	0000000000

7.5.58 UPSTREAM SPLIT TRANSACTION REGISTER – OFFSET 88h

Bit	Function	Type	Description
15:0	Upstream Split Transaction Capability	RO	Upstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the secondary bus in addressing the completers on the primary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h
31:16	Split Transaction Commitment Limit	RW	Upstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X130 is allowed to forward all split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

7.5.59 DOWNSTREAM SPLIT TRANSACTION REGISTER – OFFSET 8Ch

Bit	Function	Type	Description
15:0	Downstream Split Transaction Capability	RO	Downstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the primary bus in addressing the completers on the secondary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h

Bit	Function	Type	Description
31:16	Downstream Split Transaction Commitment Limit	RW	Downstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X130 is allowed to forward all split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

7.5.60 POWER MANAGEMENT ID REGISTER – OFFSET 90h

Bit	Function	Type	Description
7:0	Power Management ID	RO	Power management ID = 01h Reset to 01h

7.5.61 NEXT CAPABILITY POINTER REGISTER – OFFSET 90h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer (point to Subsystem ID and Subsystem Vendor ID) Reset to A8h

7.5.62 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 90h

Bit	Function	Type	Description
18:16	Version Number	RO	Version number that complies with revision 1.2 of the PCI Power Management Interface Specification. Reset to 011
19	PME Clock	RO	PME clock is not required for PME_L generation Reset to 0
20	Reserved	RO	Reset to 0
21	Device Specific Initialization (DSI)	RO	DSI – no special initialization of this function beyond the standard PCI configuration header is required following transition to the D0 un-initialized state Reset to 0
24:22	AUX Current	RO	000: 0mA 001: 55mA 010: 100mA 011: 160mA 100: 220mA 101: 270mA 110: 320mA 111: 375mA Reset to 001
25	D1 Power Management	RO	D1 power management is not supported Reset to 0
26	D2 Power Management	RO	D2 power management is not supported Reset to 0
31:27	PME_L Support	RO	PME_L is supported in D3 cold, D3 hot, and D0 states. Reset to 11001

7.5.63 POWER MANAGEMENT CONTROL AND STATUS REGISTER – OFFSET 94h

Bit	Function	Type	Description
1:0	Power State	RW	Power State is used to determine the current power state of PI7C9X130. If a non-implemented state is written to this register, PI7C9X130 will ignore the write data. When present state is D3 and changing to D0 state by programming this register, the power state change causes a device reset without activating the RESET_L of PCI/PCI-X bus interface 00: D0 state 01: D1 state not implemented 10: D2 state not implemented 11: D3 state Reset to 00
7:2	Reserved	RO	Reset to 000000
8	PME Enable	RWS	0: PME_L assertion is disabled 1: PME_L assertion is enabled Reset to 0
12:9	Data Select	RO	Data register is not implemented Reset to 0000
14:13	Data Scale	RO	Data register is not implemented Reset to 00
15	PME Status	RWCS	PME_L is supported Reset to 0

7.5.64 PCI-TO-PCI BRIDGE SUPPORT EXTENSION REGISTER – OFFSET 94h

Bit	Function	Type	Description
21:16	Reserved	RO	Reset to 000000
22	B2/B3 Support	RO	B2 / B3 not support for D3hot Reset to 0
23	PCI Bus Power/Clock Control	RO	PCI Bus Power/Clock Disabled Reset to 0
31:24	Data Register	RO	Data register is not implemented Reset to 00h

7.5.65 DOWNSTREAM MEMORY 0 TRANSLATED BASE REGISTER – OFFSET 98h

Bit	Function	Type	Description
11:0	Reserved	RO	Reset to 000h
31:12	Downstream Memory 0 Translated Base	RW	Define the translated base address for downstream memory transactions whose initiator addresses fall into Downstream Memory 0 (above lower 4K boundary) address range. The number of bits that are used for translated base is determined by its setup register (offset 9Ch) Reset to 00000h

7.5.66 DOWNSTREAM MEMORY 0 SETUP REGISTER – OFFSET 9Ch

Bit	Function	Type	Description
0	Type Selector	RO	0: Memory space is requested Reset to 0

Bit	Function	Type	Description
2:1	Address Type	RO (WS)	00: 32-bit address space 01: 64-bit address space Reset to 00
3	Prefetchable Control	RO (WS)	0: Non-prefetchable 1: Prefetchable Reset to 0
11:4	Reserved	RO	Reset to 00h
30:12	Base Address Register Size	RO (WS)	0: Set the corresponding bit in the Base Address Register to read only. 1: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range. Reset to 7FFFFh
31	Base Address Register Enable	RO (WS)	Always set to 1 when a bus master attempts to write a zero to this bit. PI7C9X130 returns bit [31:12] as FFFFFh (for 4KB size). Reset to 1

7.5.67 CAPABILITY ID REGISTER – OFFSET A0h

Bit	Function	Type	Description
7:0	Capability ID	RO	Capability ID for SI Reset to 04h

7.5.68 NEXT POINTER REGISTER – OFFSET A0h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer – points to PCI Express capabilities register Reset to B0h

7.5.69 SLOT NUMBER REGISTER – OFFSET A0h

Bit	Function	Type	Description
20:16	Expansion Slot Number	RW	Expansion slot number Reset to 00000
21	First In Chassis	RW	First in chassis Reset to 0
23:22	Reserved	RO	Reset to 00

7.5.70 CHASSIS NUMBER REGISTER – OFFSET A0h

Bit	Function	Type	Description
31:24	Chassis Number	RW	Chassis number Reset to 00h

7.5.71 SECONDARY CLOCK AND CLKRUN CONTROL REGISTER – OFFSET A4h

Bit	Function	Type	Description
1:0	CLKOUT0 Enable	RW	CLKOUT (Slot 0) Enable 00: enable CLKOUT0 01: enable CLKOUT0 10: enable CLKOUT0 11: disable CLKOUT0 and driven LOW Reset to 00
3:2	CLKOUT1 Enable	RW	CLKOUT (Slot 1) Enable 00: enable CLKOUT1 01: enable CLKOUT1 10: enable CLKOUT1 11: disable CLKOUT1 and driven LOW Reset to 00
5:4	CLKOUT2 Enable	RW	CLKOUT (Slot 2) Enable 00: enable CLKOUT2 01: enable CLKOUT2 10: enable CLKOUT2 11: disable CLKOUT2 and driven LOW Reset to 00
7:6	CLKOUT3 Enable	RW	CLKOUT (Slot 3) Enable 00: enable CLKOUT3 01: enable CLKOUT3 10: enable CLKOUT3 11: disable CLKOUT3 and driven LOW Reset to 00
8	CLKOUT4 Enable	RW	CLKOUT (Device 1) Enable 0: enable CLKOUT4 1: disable CLKOUT4 and driven LOW Reset to 0
9	CLKOUT5 Enable	RW	CLKOUT (Device 2) Enable 0: enable CLKOUT5 1: disable CLKOUT5 and driven LOW Reset to 0
10	CLKOUT6 Enable	RW	CLKOUT (the bridge) Enable for forward bridge mode only 0: enable CLKOUT6 1: disable CLKOUT6 and driven LOW Reset to 0
11	Reserved	RO	Reset to 0
12	Reserved	RO	Reset to 0
13	Secondary Clock Stop Status	RO	Secondary clock stop status 0: secondary clock not stopped 1: secondary clock stopped Reset to 0
14	Secondary Clkrun Protocol Enable	RW	0: disable protocol 1: enable protocol Reset to 0

Bit	Function	Type	Description
15	Clkrun Mode	RW	0: Stop the secondary clock only when PI7C9X130 is at D3hot state 1: Stop the secondary clock whenever the secondary bus is idle and there are no requests from the primary bus Reset to 0
31:16	Reserved	RO	Reset 0000h

7.5.72 DOWNSTREAM I/O OR MEMORY 1 TRANSLATED BASE REGISTER – OFFSET A8h

Bit	Function	Type	Description
5:0	Reserved	RO	Reset to 000000
31:6	Downstream I/O or Memory 1 Translated Base	RW	Define the translated base address for downstream I/O or memory transactions whose initiator addresses fall into Downstream I/O or Memory 1 address range. The number of bits that are used for translated base is determined by its setup register (offset ACh) Reset to 00000h

7.5.73 DOWNSTREAM I/O OR MEMORY 1 SETUP REGISTER – OFFSET ACh

Bit	Function	Type	Description
0	Type Selector	RO	0: Memory space is requested Reset to 0
2:1	Address Type	RO (WS)	00: 32-bit address space 01: 64-bit address space Reset to 00
3	Prefetchable Control	RO (WS)	0: Non-prefetchable 1: Prefetchable Reset to 0
5:4	Reserved	RO	Reset to 00
30:6	Base Address Register Size	RO (WS)	0: Set the corresponding bit in the Base Address Register to read only. 1: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range. If memory space is selected, bit [11:6] should be set to zeros. Reset to 00000000h
31	Base Address Register Enable	RO (WS)	0: Disable this Base Address Register 1: Enable this Base Address Register Reset to 0

7.5.74 CAPABILITY ID REGISTER – OFFSET B0h

Bit	Function	Type	Description
7:0	PCI Express Capability ID	RO	PCI Express capability ID Reset to 10h

7.5.75 NEXT CAPABILITY POINTER REGISTER – OFFSET B0h (default=0071F010h for forward bridge or =0181F010h for reverse bridge)

Bit	Function	Type	Description
15:8	Next Item Pointer	RO	Next item pointer (points to VPD register) Reset to F0h

7.5.76 PCI EXPRESS CAPABILITY REGISTER – OFFSET B0h

Bit	Function	Type	Description
19:16	Capability Version	RO	Reset to 1h
23:20	Device / Port Type	RO	0000: PCI Express endpoint device 0001: Legacy PCI Express endpoint device 0100: Root port of PCI Express root complex 0101: Upstream port of PCI Express switch 0110: Downstream port of PCI Express switch 0111: PCI Express to PCI bridge 1000: PCI to PCI Express bridge Others: Reserved Reset to 7h for Forward Bridge or 8h for Reverse Bridge
24	Slot Implemented	RO	Reset to 0h for Forward Bridge or 1h for Reverse Bridge
29:25	Interrupt Message Number	RO	Reset to 0h
31:30	Reserved	RO	Reset to 0

7.5.77 DEVICE CAPABILITY REGISTER – OFFSET B4h

Bit	Function	Type	Description
2:0	Maximum Payload Size	RO	000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 010
4:3	Phantom Functions	RO	No phantom functions supported Reset to 0
5	8-bit Tag Field	RO	8-bit tag field supported Reset to 1h
8:6	Endpoint L0's Latency	RO	Endpoint L0's acceptable latency 000: less than 64 ns 001: 64 – 128 ns 010: 128 – 256 ns 011: 256 – 512 ns 100: 512 ns – 1 us 101: 1 – 2 us 110: 2 – 4 us 111: more than 4 us Reset to 000

Bit	Function	Type	Description
11:9	Endpoint L1's Latency	RO	Endpoint L1's acceptable latency 000: less than 1 us 001: 1 – 2 us 010: 2 – 4 us 011: 4 – 8 us 100: 8 – 16 us 101: 16 – 32 us 110: 32 – 64 us 111: more than 64 us Reset to 000
12	Attention Button Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
13	Attention Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enable at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
14	Power Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enable at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
17:15	Reserved	RO	Reset to 000
25:18	Captured Slot Power Limit Value	RO	These bits are set by the Set_Slot_Power_Limit message Reset to 00h
27:26	Captured Slot Power Limit Scale	RO	This value is set by the Set_Slot_Power_Limit message Reset to 00
31:28	Reserved	RO	Reset to 0h

7.5.78 DEVICE CONTROL REGISTER – OFFSET B8h

Bit	Function	Type	Description
0	Correctable Error Reporting Enable	RW	Reset to 0h
1	Non-Fatal Error Reporting Enable	RW	Reset to 0h
2	Fatal Error Reporting Enable	RW	Reset to 0h
3	Unsupported Request Reporting Enable	RW	Reset to 0h
4	Relaxed Ordering Enable	RO	Reset to 0h
7:5	Max Payload Size	RW	This field sets the maximum TLP payload size for the bridge 000: 128 bytes 001: 256 bytes 010: 512 bytes 011:1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 000
8	Extended Tag Field Enable	RW	Reset to 0

Bit	Function	Type	Description
9	Phantom Functions Enable	RO	Phantom functions not supported Reset to 0
10	Auxiliary Power PM Enable	RO	Auxiliary power PM not supported Reset to 0
11	No Snoop Enable	RO	PI7C9X130 never sets the No Snoop attribute in the transaction it initiates Reset to 0
14:12	Maximum Read Request Size	RW	This field sets the maximum Read Request Size for the device as a requester 000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 2h
15	Configuration Retry Enable	RW	Reset to 0

7.5.79 DEVICE STATUS REGISTER – OFFSET B8h

Bit	Function	Type	Description
16	Correctable Error Detected	RWC	Reset to 0
17	Non-Fatal Error Detected	RWC	Reset to 0
18	Fatal Error Detected	RWC	Reset to 0
19	Unsupported Request Detected	RWC	Reset to 0
20	AUX Power Detected	RO	Reset to 1
21	Transaction Pending	RO	0: No transaction is pending on transaction layer interface 1: Transaction is pending on transaction layer interface Reset to 0
31:22	Reserved	RO	Reset to 0000000000

7.5.80 LINK CAPABILITY REGISTER – OFFSET BCh

Bit	Function	Type	Description
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link 0001: 2.5Gb/s link Reset to 1
9:4	Maximum Link Width	RO	Indicates the maximum width of the Express link 000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000001

Bit	Function	Type	Description
11:10	ASPM Support	RO	This field indicates the level of Active State Power Management Support 00: reserved 01: L0's entry supported 10: reserved 11: L0's and L1's supported Reset to 0
14:12	L0's Exit Latency	RO	Reset to 3h
17:15	L1's Exit Latency	RO	Reset to 0h
23:18	Reserved	RO	Reset to 0h
31:24	Port Number	RO	Reset to 00h

7.5.81 LINK CONTROL REGISTER – OFFSET C0h

Bit	Function	Type	Description
1:0	ASPM Control	RW	This field controls the level of ASPM supported on the Express link 00: disabled 01: L0's entry enabled 10: L1's entry enabled 11: L0's and L1's entry enabled Reset to 00
2	Reserved	RO	Reset to 0
3	Read Completion Boundary (RCB)	RO	Read completion boundary not supported Reset to 0
4	Link Disable	RO / RW	RO for Forward Bridge Reset to 0
5	Retrain Link	RO / RW	RO for Forward Bridge Reset to 0
6	Common Clock Configuration	RW	Reset to 0
7	Extended Sync	RW	Reset to 0
15:8	Reserved	RO	Reset to 00h

7.5.82 LINK STATUS REGISTER – OFFSET C0h

Bit	Function	Type	Description
19:16	Link Speed	RO	This field indicates the negotiated speed of the Express link 001: 2.5Gb/s link Reset to 1h
25:20	Negotiated Link Width	RO	000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000001
26	Link Train Error	RO	Reset to 0
27	Link Training	RO	Reset to 0
28	Slot Clock Configuration	RO	Reset to 1
31:29	Reserved	RO	Reset to 0

7.5.83 SLOT CAPABILITY REGISTER – OFFSET C4h

Bit	Function	Type	Description
0	Attention Button Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
1	Power Controller Present	RO	Reset to 0
2	MRL Sensor Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
3	Attention Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
4	Power Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
5	Hot Plug Surprise	RO	Reset to 0
6	Hot Plug Capable	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
14:7	Slot Power Limit Value	RO	Reset to 00h
16:15	Slot Power Limit Scale	RO	Reset to 00
18:17	Reserved	RO	Reset to 00
31:19	Physical Slot Number	RO	Reset to 0

7.5.84 SLOT CONTROL REGISTER – OFFSET C8h

Bit	Function	Type	Description
0	Attention Button Present Enable	RW	Reset to 0
1	Power Fault Detected Enable	RW	Reset to 0
2	MRL Sensor Changed Enable	RW	Reset to 0
3	Presence Detect Changed Enable	RW	Reset to 0
4	Command Completed Interrupt Enable	RW	Reset to 0
5	Hot Plug Interrupt Enable	RW	Reset to 0
7:6	Attention Indicator Control	RW	Reset to 0
9:8	Power Indicator Control	RW	Reset to 0
10	Power Controller Control	RW	Reset to 0
15:11	Reserved	RO	Reset to 0

7.5.85 SLOT STATUS REGISTER – OFFSET C8h

Bit	Function	Type	Description
16	Attention Button Pressed	RO	Reset to 0
17	Power Fault Detected	RO	Reset to 0
18	MRL Sensor Changed	RO	Reset to 0
19	Presence Detect Changed	RO	Reset to 0
20	Command Completed	RO	Reset to 0
21	MRL Sensor State	RO	Reset to 0
22	Presence Detect State	RO	Reset to 0
31:23	Reserved	RO	Reset to 0

7.5.86 XPIP CONFIGURATION REGISTER 0 – OFFSET CCh

Bit	Function	Type	Description
0	Hot Reset Enable	RW	Reset to 0
1	Loopback Function Enable	RW	Reset to 0
2	Cross Link Function Enable	RW	Reset to 0
3	Software Direct to Configuration State when in LTSSM state	RW	Reset to 0
4	Internal Selection for Debug Mode	RW	Reset to 0
7:5	Negotiate Lane Number of Times	RW	Reset to 3h
12:8	TS1 Number Counter	RW	Reset to 10h
15:13	Reserved	RO	Reset to 0
31:16	LTSSM Enter L1 Timer Default Value	RW	Reset to 0400h

7.5.87 XPIP CONFIGURATION REGISTER 1 – OFFSET D0h (default=04000271h)

Bit	Function	Type	Description
9:0	L0's Lifetime Timer	RW	Reset to 271h
15:10	Reserved	RO	Reset to 0
31:16	L1 Lifetime Timer	RW	Reset to 0400h

7.5.88 XPIP CONFIGURATION REGISTER 2 – OFFSET D4h

Bit	Function	Type	Description
7:0	CDR Recovery Time (in FTS units)	RW	Reset to 54h
14:8	L0's Exit to L0 Latency	RW	Reset to 2h
15	Reserved	RO	Reset to 0
22:16	L1 Exit to L0 Latency	RW	Reset to 19h
31:23	Reserved	RO	Reset to 0

7.5.89 CAPABILITY ID REGISTER – OFFSET D8h

Bit	Function	Type	Description
7:0	Capability ID for VPD Register	RO	Reset to 03h

7.5.90 NEXT POINTER REGISTER – OFFSET D8h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer (F0h, points to MSI capabilities) Reset to F0h

7.5.91 VPD REGISTER – OFFSET D8h

Bit	Function	Type	Description
17:16	Reserved	RO	Reset to 0
23:18	VPD Address for Read/Write Cycle	RW	Reset to 0
30:24	Reserved	RO	Reset to 0
31	VPD Operation	RW	0: Generate a read cycle from the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '0' until EEPROM cycle is finished, after which the bit is then set to '1'. Data for reads is available at register ECh. 1: Generate a write cycle to the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '1' until EEPROM cycle is finished, after which it is then cleared to '0'. Reset to 0

7.5.92 VPD DATA REGISTER – OFFSET DCh

Bit	Function	Type	Description
31:0	VPD Data	RW	VPD Data (EEPROM data [address + 0x40]) The least significant byte of this register corresponds to the byte of VPD at the address specified by the VPD address register. The data read form or written to this register uses the normal PCI byte transfer capabilities. Reset to 0

7.5.93 UPSTREAM MEMORY 0 TRANSLATED BASE - OFFSET E0h

Bit	Function	Type	Description
11:0	Reserved	RO	Reset to 000h
31:12	Downstream Memory 0 Translated Base	RW	Define the translated base address for upstream memory transactions whose initiator addresses fall into Upstream Memory 0 (above lower 4K boundary) address range. The number of bits that are used for translated base is determined by its setup register (offset E4h) Reset to 00000h

7.5.94 UPSTREAM MEMORY 0 SETUP REGISTER – OFFSET E4h

Bit	Function	Type	Description
0	Type Selector	RO	0: Memory space is requested Reset to 0

Bit	Function	Type	Description
2:1	Address Type	RO (WS)	00: 32-bit address space 01: 64-bit address space Reset to 00
3	Prefetchable Control	RO (WS)	0: Non-prefetchable 1: Prefetchable Reset to 0
11:4	Reserved	RO	Reset to 00h
30:12	Base Address Register Size	RO (WS)	0: Set the corresponding bit in the Base Address Register to read only. 1: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range. Reset to 00000h
31	Base Address Register Enable	RO (WS)	Always set to 1 when a bus master attempts to write a zero to this bit. PI7C9X130 returns bit [31:12] as FFFFFh (for 4KB size). Reset to 1

7.5.95 UPSTREAM I/O OR MEMORY 1 TRANSLATED BASE REGISTER – OFFSET E8h

Bit	Function	Type	Description
5:0	Reserved	RO	Reset to 000000
31:6	Upstream I/O or Memory 1 Translated Base	RW	Define the translated base address for upstream I/O or memory transactions whose initiator addresses fall into Upstream I/O or Memory 1 address range. The number of bits that are used for translated base is determined by its setup register (offset ECh) Reset to 00000h

7.5.96 UPSTREAM I/O OR MEMORY 1 SETUP REGISTER – OFFSET ECh

Bit	Function	Type	Description
0	Type Selector	RO	0: Memory space is requested Reset to 0
2:1	Address Type	RO (WS)	00: 32-bit address space 01: 64-bit address space Reset to 00
3	Prefetchable Control	RO (WS)	0: Non-prefetchable 1: Prefetchable Reset to 0
5:4	Reserved	RO	Reset to 00
30:6	Base Address Register Size	RO (WS)	0: Set the corresponding bit in the Base Address Register to read only. 1: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range. If memory space is selected, bit [11:6] should be set to zeros. Reset to 00000000h
31	Base Address Register Enable	RO (WS)	0: Disable this Base Address Register 1: Enable this Base Address Register Reset to 0

7.5.97 MESSAGE SIGNALED INTERRUPTS ID REGISTER – OFFSET F0h

Bit	Function	Type	Description
7:0	Capability ID for MSI Registers	RO	Reset to 05h

7.5.98 NEXT CAPABILITY POINTER REGISTER – OFFSET F0h

Bit	Function	Type	Description
15:8	Next Pointer	RO	Next pointer (00h indicates the end of capabilities) Reset to 00h

7.5.99 MESSAGE CONTROL REGISTER – OFFSET F0h

Bit	Function	Type	Description
16	MSI Enable	RW	0: Disable MSI and default to INTx for interrupt 1: Enable MSI for interrupt service and ignore INTx interrupt pins
19:17	Multiple Message Capable	RO	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
22:20	Multiple Message Enable	RW	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
23	64-bit Address Capable	RW	Reset to 1
31:24	Reserved	RO	Reset to 00h

7.5.100MESSAGE ADDRESS REGISTER – OFFSET F4h

Bit	Function	Type	Description
1:0	Reserved	RO	Reset to 00
31:2	System Specified Message Address	RW	Reset to 0

7.5.101MESSAGE UPPER ADDRESS REGISTER – OFFSET F8h

Bit	Function	Type	Description
31:0	System Specified Message Upper Address	RW	Reset to 0

7.5.102MESSAGE DATA REGISTER – OFFSET FCh

Bit	Function	Type	Description
15:0	System Specified Message Data	RW	Reset to 0
31:16	Reserved	RO	Reset to 0

7.5.103ADVANCE ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

Bit	Function	Type	Description
15:0	Advance Error Reporting Capability ID	RO	Reset to 0001h

7.5.104ADVANCE ERROR REPORTING CAPABILITY VERSION REGISTER – OFFSET 100h

Bit	Function	Type	Description
19:16	Advance Error Reporting Capability Version	RO	Reset to 1h

7.5.105NEXT CAPABILITY OFFSET REGISTER – OFFSET 100h

Bit	Function	Type	Description
31:20	Next Capability Offset	RO	Next capability offset (150h points to VC capability) Reset to 150h

7.5.106UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

Bit	Function	Type	Description
0	Training Error Status	RWCS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Status	RWCS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Status	RWCS	Reset to 0
13	Flow Control Protocol Error Status	RWCS	Reset to 0
14	Completion Timeout Status	RWCS	Reset to 0
15	Completer Abort Status	RWCS	Reset to 0
16	Unexpected Completion Status	RWCS	Reset to 0
17	Receiver Overflow Status	RWCS	Reset to 0
18	Malformed TLP Status	RWCS	Reset to 0
19	ECRC Error Status	RWCS	Reset to 0
20	Unsupported Request Error Status	RWCS	Reset to 0
31:21	Reserved	RO	Reset to 0

7.5.107UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

Bit	Function	Type	Description
0	Training Error Mast	RWS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Mask	RWS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Mask	RWS	Reset to 0
13	Flow Control Protocol Error Mask	RWS	Reset to 0

Bit	Function	Type	Description
14	Completion Timeout Mask	RWS	Reset to 0
15	Completion Abort Mask	RWS	Reset to 0
16	Unexpected Completion Mask	RWS	Reset to 0
17	Receiver Overflow Mask	RWS	Reset to 0
18	Malformed TLP Mask	RWS	Reset to 0
19	ECRC Error Mask	RWS	Reset to 0
20	Unsupported Request Error Mask	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

7.5.108UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

Bit	Function	Type	Description
0	Training Error Severity	RWS	Reset to 1
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Severity	RWS	Reset to 1
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Severity	RWS	Reset to 0
13	Flow Control Protocol Error Severity	RWS	Reset to 1
14	Completion Timeout Severity	RWS	Reset to 0
15	Completer Abort Severity	RWS	Reset to 0
16	Unexpected Completion Severity	RWS	Reset to 0
17	Receiver Overflow Severity	RWS	Reset to 1
18	Malformed TLP Severity	RWS	Reset to 1
19	ECRC Error Severity	RWS	Reset to 0
20	Unsupported Request Error Severity	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

7.5.109CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h

Bit	Function	Type	Description
0	Receiver Error Status	RWCS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Status	RWCS	Reset to 0
7	Bad DLLP Status	RWCS	Reset to 0
8	REPLAY_NUM Rollover Status	RWCS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Status	RWCS	Reset to 0
31:13	Reserved	RO	Reset to 0

7.5.110CORRECTABLE ERROR MASK REGISTER – OFFSET 114h

Bit	Function	Type	Description
0	Receiver Error Mask	RWS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Mask	RWS	Reset to 0
7	Bad DLLP Mask	RWS	Reset to 0
8	REPLAY_NUM Rollover Mask	RWS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Mask	RWS	Reset to 0
13	Advisory Non-Fatal Error Mask	RWS	This bit is set by default to enable compatiblity with software that does not comprehend Role-Based Error Reporting Reset to 1
31:14	Reserved	RO	Reset to 0

7.5.111ADVANCED ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

Bit	Function	Type	Description
4:0	First Error Pointer	ROS	Reset to 0h
5	ECRC Generation Capable	RO	Reset to 1
6	ECRC Generation Enable	RWS	Reset to 0
7	ECRC Check Capable	RO	Reset to 1
8	ECRC Check Enable	RWS	Reset to 0
31:9	Reserved	RO	Reset to 0

7.5.112HEADER LOG REGISTER 1 – OFFSET 11Ch

Bit	Function	Type	Description
7:0	Header Byte 3	ROS	Reset to 0
15:8	Header Byte 2	ROS	Reset to 0
23:16	Header Byte 1	ROS	Reset to 0
31:24	Header Byte 0	ROS	Reset to 0

7.5.113HEADER LOG REGISTER 2 – OFFSET 120h

Bit	Function	Type	Description
7:0	Header Byte 7	ROS	Reset to 0
15:8	Header Byte 6	ROS	Reset to 0
23:16	Header Byte 5	ROS	Reset to 0
31:24	Header Byte 4	ROS	Reset to 0

7.5.114HEADER LOG REGISTER 3 – OFFSET 124h

Bit	Function	Type	Description
7:0	Header Byte 11	ROS	Reset to 0
15:8	Header Byte 10	ROS	Reset to 0
23:16	Header Byte 9	ROS	Reset to 0
31:24	Header Byte 8	ROS	Reset to 0

7.5.115HEADER LOG REGISTER 4 – OFFSET 128h

Bit	Function	Type	Description
7:0	Header Byte 15	ROS	Reset to 0

Bit	Function	Type	Description
15:8	Header Byte 14	ROS	Reset to 0
23:16	Header Byte 13	ROS	Reset to 0
31:24	Header Byte 12	ROS	Reset to 0

7.5.116SECONDARY UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 12Ch

Bit	Function	Type	Description
0	Target Abort on Split Completion Status	RWCS	Reset to 0
1	Master Abort on Split Completion Status	RWCS	Reset to 0
2	Received Target Abort Status	RWCS	Reset to 0
3	Received Master Abort Status	RWCS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Status	RWCS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Status	RWCS	Reset to 0
7	Uncorrectable Data Error Status	RWCS	Reset to 0
8	Uncorrectable Attribute Error Status	RWCS	Reset to 0
9	Uncorrectable Address Error Status	RWCS	Reset to 0
10	Delayed Transaction Discard Timer Expired Status	RWCS	Reset to 0
11	PERR_L Assertion Detected Status	RWCS	Reset to 0
12	SERR_L Assertion Detected Status	RWCS	Reset to 0
13	Internal Bridge Error Status	RWCS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.5.117SECONDARY UNCORRECTABLE ERROR MASK REGISTER – OFFSET 130h

Bit	Function	Type	Description
0	Target Abort on Split Completion Mask	RWS	Reset to 0
1	Master Abort on Split Completion Mask	RWS	Reset to 0
2	Received Target Abort Mask	RWS	Reset to 0
3	Received Master Abort Mask	RWS	Reset to 1
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Mask	RWS	Reset to 1
6	Uncorrectable Split Completion Message Data Error Mask	RWS	Reset to 0

Bit	Function	Type	Description
7	Uncorrectable Data Error Mask	RWS	Reset to 1
8	Uncorrectable Attribute Error Mask	RWS	Reset to 1
9	Uncorrectable Address Error Mask	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Mask	RWS	Reset to 1
11	PERR_L Assertion Detected Mask	RWS	Reset to 0
12	SERR_L Assertion Detected Mask	RWS	Reset to 1
13	Internal Bridge Error Mask	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.5.118SECONDARY UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 134h

Bit	Function	Type	Description
0	Target Abort on Split Completion Severity	RWS	Reset to 0
1	Master Abort on Split Completion Severity	RWS	Reset to 0
2	Received Target Abort Severity	RWS	Reset to 0
3	Received Master Abort Severity	RWS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Severity	RWS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Severity	RWS	Reset to 1
7	Uncorrectable Data Error Severity	RWS	Reset to 0
8	Uncorrectable Attribute Error Severity	RWS	Reset to 1
9	Uncorrectable Address Error Severity	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Severity	RWS	Reset to 0
11	PERR_L Assertion Detected Severity	RWS	Reset to 0
12	SERR_L Assertion Detected Severity	RWS	Reset to 1
13	Internal Bridge Error Severity	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

7.5.119SECONDARY ERROR CAPABILITY AND CONTROL REGISTER – OFFSET 138h

Bit	Function	Type	Description
4:0	Secondary First Error Pointer	ROW	Reset to 0
31:5	Reserved	RO	Reset to 0

7.5.120SECONDARY HEADER LOG REGISTER – OFFSET 13Ch – 148h

Bit	Function	Type	Description
35:0	Transaction Attribute	ROS	Transaction attribute, CBE [3:0] and AD [31:0] during attribute phase Reset to 0
39:36	Transaction Command Lower	ROS	Transaction command lower, CBE [3:0] during first address phase Reset to 0
43:40	Transaction Command Upper	ROS	Transaction command upper, CBE [3:0] during second address phase of DAC transaction Reset to 0
63:44	Reserved	ROS	Reset to 0
95:64	Transaction Address	ROS	Transaction address, AD [31:0] during first address phase Reset to 0
127:96	Transaction Address	ROS	Transaction address, AD [31:0] during second address phase of DAC transaction Reset to 0

7.5.121RESERVED REGISTER – OFFSET 14Ch

7.5.122VC CAPABILITY ID REGISTER – OFFSET 150h

Bit	Function	Type	Description
15:0	VC Capability ID	RO	Reset to 0002h

7.5.123VC CAPABILITY VERSION REGISTER – OFFSET 150h

Bit	Function	Type	Description
19:16	VC Capability Version	RO	Reset to 1h

7.5.124NEXT CAPABILITY OFFSET REGISTER – OFFSET 150h

Bit	Function	Type	Description
31:20	Next Capability Offset	RO	Next capability offset – the end of capabilities Reset to 0

7.5.125PORT VC CAPABILITY REGISTER 1 – OFFSET 154h

Bit	Function	Type	Description
2:0	Extended VC Count	RO	Reset to 0
3	Reserved	RO	Reset to 0
6:4	Low Priority Extended VC Count	RO	Reset to 0
7	Reserved	RO	Reset to 0
9:8	Reference Clock	RO	Reset to 0
11:10	Port Arbitration Table Entry Size	RO	Reset to 0
31:12	Reserved	RO	Reset to 0

7.5.126PORT VC CAPABILITY REGISTER 2 – OFFSET 158h

Bit	Function	Type	Description
7:0	VC Arbitration Capability	RO	Reset to 0
23:8	Reserved	RO	Reset to 0
31:24	VC Arbitration Table Offset	RO	Reset to 0

7.5.127PORT VC CONTROL REGISTER – OFFSET 15Ch

Bit	Function	Type	Description
0	Load VC Arbitration Table	RO	Reset to 0
3:1	VC Arbitration Select	RO	Reset to 0
15:4	Reserved	RO	Reset to 0

7.5.128PORT VC STATUS REGISTER – OFFSET 15Ch

Bit	Function	Type	Description
16	VC Arbitration Table Status	RO	Reset to 0
31:17	Reserved	RO	Reset to 0

7.5.129VC0 RESOURCE CAPBILITY REGISTER – OFFSET 160h

Bit	Function	Type	Description
7:0	Port Arbitration Capability	RO	Reset to 0
13:8	Reserved	RO	Reset to 0
14	Advanced Packet Switching	RO	Reset to 0
15	Reject Snoop Transactions	RO	Reset to0
22:16	Maximum Time Slots	RO	Reset to 0
23	Reserved	RO	Reset to 0
31:24	Port Arbitration Table Offset	RO	Reset to 0

7.5.130VC0 RESOURCE CONTROL REGISTER – OFFSET 164h

Bit	Function	Type	Description
0	TC/VC Map(for TC0)		Reset to 1
	TC/VC Map(for TC7~1)		Reset to 7Fh
15:8	Reserved	RO	Reset to 0
16	Load Port Arbitration Table	RO	Reset to 0
19:17	Port Arbitration Select	RO	Reset to 0
23:20	Reserved	RO	Reset to 0
26:24	VC ID	RO	Reset to 0
30:27	Reserved	RO	Reset to 0
31	VC Enable	RO	Reset to 1

7.5.131VC0 RESOURCE STATUS REGISTER – OFFSET 168h

Bit	Function	Type	Description
0	Port Arbitration Table 1	RO	Reset to 0
1	VC0 Negotiation Pending	RO	Reset to 0
31:2	Reserved	RO	Reset to 0

7.5.132RESERVED REGISTERS – OFFSET 16Ch TO 2FCh

7.5.133EXTENDED GPIO DATA AND CONTROL REGISTER – OFFSET 300h

Bit	Function	Type	Description
2:0	Extended GPIO output	RWC	GPIO [6:4] as output, write 1 to clear Reset to 0
5:3	Extended GPIO output	RWS	GPIO [6:4] as output, write 1 to set Reset to 0
8:6	Extended GPIO output enable	RWC	GPIO [6:4] enable, write 1 to clear Reset to 0
11:9	Extended GPIO output enable	RWS	GPIO [6:4] enable, write 1 to set Reset to 0
14:12	Extended GPIO input	RO	GPIO [6:4] as input Reset to 0
31:16	Reserved	RO	Reset to 0

7.5.134EXTRA GPI/GPO DATA AND CONTROL REGISTER – OFFSET 304h

Bit	Function	Type	Description
3:0	Extra GPO	RWC	GPO [3:0], write 1 to clear Reset to 0
7:4	Extra GPO	RWS	GPO [3:0], write 1 to set Reset to 0
11:8	Extra GPO enable	RWC	GPO [3:0] enable, write 1 to clear Reset to 0
15:12	Extra GPO enable	RWS	GPO [3:0] enable, write 1 to set Reset to 0
19:16	Extra GPI	RO	Extra GPI [3:0] Data Register Reset to 0
31:20	Reserved	RO	Reset to 0

7.5.135RESERVED REGISTERS – OFFSET 308h TO 30Ch

7.5.136REPLAY AND ACKNOWLEDGE LATENCY TIMERS – OFFSET 310h

Bit	Function	Type	Description
11:0	Replay Timer	RW	Replay Timer Reset to 115h
12	Replay Timer Enable	RW	Replay Timer Enable Reset to 0
15:13	Reserved	RO	Reset to 0
29:16	Acknowledge Latency Timer	RW	Acknowledge Latency Timer Reset to CDh
30	Acknowledge Latency Timer Enable	RW	Acknowledge Latency Timer Enable Reset to 0
31	Reserved	RO	Reset to 0

7.5.137RESERVED REGISTERS – OFFSET 314h TO FFCh

7.6 CONTROL AND STATUS REGISTERS FOR NON-TRANSPARENT BRIDGE MODE

Control and Status Registers (CSRs) can be accessed by Memory or I/O transactions from both primary and secondary ports. The CSRs are defined and to be used along with configuration registers (see previous section 7.5 for details) for non-transparent bridge operations.

Register Type	Descriptions
RO	Read Only
ROS	Read Only and Sticky
RW	Read/Write
RO(WS)	Read Only at primary interface and Read/Write at secondary interface
RWC	Read/Write "1" to clear
RWS	Read/Write and Sticky
RWCS	Read/Write "1" to clear and Sticky

7.6.1 RESERVED REGISTERS – OFFSET 000h TO 004h

7.6.2 DOWNSTREAM MEMORY 2 TRANSLATED BASE REGISTER – OFFSET 008h

Bit	Function	Type	Description
11:0	Reserved	RO	Reset to 000h
31:12	Downstream Memory 2 Translated Base	RW	Define the translated base address for downstream memory transactions whose initiator addresses fall into Downstream Memory 2 address range. The number of bits that are used for translated base is determined by its setup register (offset 00Ch) Reset to 00000h

7.6.3 DOWNSTREAM MEMORY 2 SETUP REGISTER – OFFSET 00Ch

Bit	Function	Type	Description
0	Type Selector	RO	0: Memory space is requested Reset to 0
2:1	Address Type	RO (WS)	00: 32-bit address space 01: 64-bit address space Reset to 00
3	Prefetchable Control	RO (WS)	0: Non-prefetchable 1: Prefetchable Reset to 0
11:4	Reserved	RO	Reset to 00
30:12	Base Address Register Size	RO (WS)	0: Set the corresponding bit in the Base Address Register to read only 1: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range Reset to 00000h
31	Base Address Register Enable	RO (WS)	0: Disable this Base Address Register 1: Enable this Base Address Register Reset to 0

7.6.4 DOWNSTREAM MEMORY 3 TRANSLATED BASE REGISTER – OFFSET 010h

Bit	Function	Type	Description
11:0	Reserved	RO	Reset to 000000
31:12	Downstream Memory 3 Translated Base	RW	Define the translated base address for downstream memory transactions whose initiator addresses fall into Downstream Memory 3 address range. The number of bits that are used for translated base is determined by its setup register (offset 014h) Reset to 00000h

7.6.5 DOWNSTREAM MEMORY 3 SETUP REGISTER – OFFSET 014h

Bit	Function	Type	Description
0	Type Selector	RO	0: Memory space is requested Reset to 0
2:1	Address Type	RO (WS)	00: 32-bit address space 01: 64-bit address space Reset to 00
3	Prefetchable Control	RO (WS)	0: Non-prefetchable 1: Prefetchable Reset to 0
11:4	Reserved	RO	Reset to 00
30:12	Base Address Register Size	RO (WS)	0: Set the corresponding bit in the Base Address Register to read only 1: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range Reset to 00000h
31	Base Address Register Enable	RO (WS)	0: Disable this Base Address Register 1: Enable this Base Address Register Reset to 0

7.6.6 DOWNSTREAM MEMORY 3 UPPER 32-BIT SETUP REGISTER – OFFSET 018h

Bit	Function	Type	Description
30:0	Base Address Register Size	RW	0: Set the corresponding bit in the Upper 32-bit Base Address Register to read only 1: Set the corresponding bit in the Upper 32-bit Base Address Register to read/write in order to control the size of the address range Reset to 00000000h
31	Base Address Register Enable	RW)	0: Disable 64-bit Base Address Register 1: Enable 64-bit Base Address Register Reset to 0

7.6.7 RESERVED REGISTERS – OFFSET 01Ch TO 030h

7.6.8 UPSTREAM MEMORY 3 SETUP REGISTER – OFFSET 034h

Bit	Function	Type	Description
0	Type Selector	RO	**0**: Memory space is requested Reset to 0
2:1	Address Type	RO	**00**: 32-bit address space **01**: 64-bit address space Reset to 01

Bit	Function	Type	Description
3	Prefetchable Control	RW	**0**: Non-prefetchable **1**: Prefetchable Reset to 0
11:4	Reserved	RO	Reset to 00
31:12	Base Address Register Size	RW	**0**: Set the corresponding bit in the Base Address Register to read only **1**: Set the corresponding bit in the Base Address Register to read/write in order to control the size of the address range Reset to 00000h

7.6.9 UPSTREAM MEMORY 3 UPPER 32-BIT SETUP REGISTER – OFFSET 038h

Bit	Function	Type	Description
30:0	Base Address Register Size	RW	0: Set the corresponding bit in the Upper 32-bit Base Address Register to read only 1: Set the corresponding bit in the Upper 32-bit Base Address Register to read/write in order to control the size of the address range Reset to 00000000h
31	Base Address Register Enable	RW	0: Disable 64-bit Base Address Register 1: Enable 64-bit Base Address Register Reset to 0

7.6.10 RESERVED REGISTERS – OFFSET 3Ch TO 4Ch

7.6.11 LOOKUP TABLE OFFSET – OFFSET 50h

Bit	Function	Type	Description
7:0	Lookup Table Offset	RW	This register contains the byte offset of the Lookup Table Entry to be accessed for upstream memory 2. The access is initiated when the lookup Table Data Register is accessed. This register should be written first before any Lookup Table Data access. Reset to 00h
31:8	Reserved	RO	Reset to 0

7.6.12 LOOKUP TABLE DATA – OFFSET 054h

Bit	Function	Type	Description
0	Valid	RW	0: Invalid lookup 1: Valid lookup Reset to 0
2:1	Reserved	RO	Reset to 00
3	Prefetchable	RW	0: Memory address is non-prefetchable 1: Memory address is Reset to 0
7:4	Reserved	RO	Reset to 0h
24:8	Translated base or Reserved	RW/RO	Data written or read from the Lookup Table at the offset specified in the Lookup Table Offset Register. When writing to this register, the data value is written to the specified Lookup Table entry. When reading from this register, the data reflects the data value from the specified Lookup Table entry. The bit [24:8] is Translated Base Register bit when the lookup table size is set to 256B range. The bit [24:8] is reserved when the lookup table size is set to 32MB range (see PCI configuration offset 68h for non-transparent mode). Reset to 0

Bit	Function	Type	Description
31:25	Translated Base	RW	Data written or read from the Lookup Table at the offset specified in the Lookup Table Offset Register. When writing to this register, the data value is written to a specific Lookup Table entry (CSR offset 100h – 1FFh). When reading from this register, the data reflects the data value from the specific Lookup Table entry. Reset to 0

7.6.13 UPSTREAM PAGE BOUNDARY IRQ 0 REQUEST REGISTER - OFFSET 058h

Bit	Function	Type	Description
31:0	Upstream Page Boundary IRQ 0	RWC	Each interrupt request bit is correspondent to a page entry in the lower half of the Upstream Memory 2 range. Bit [0] is for the first page, and bit [31] is for the 32nd page. PI7C9X130 sets the appropriate bit when it successfully transfers data to or from the imitator that addresses the last Double Word in a page. PI7C9X130 initiates an interrupt request on secondary interface when the interrupt request bit is set and the corresponding Upstream Page Boundary IRQ 0 Mask bit is reset. When forward bridge, PI7C9X130 asserts INTA_L or generates MSI on secondary bus (PCI interface). When reverse bridge, PI7C9X130 sends INTA_L assertion message or generates MSI on secondary interface (PCI Express). When writing a "1" to this register, it clears the corresponding interrupt request bit. Reset to 0

7.6.14 UPSTREAM PAGE BOUNDARY IRQ 1 REQUEST REGISTER - OFFSET 05Ch

Bit	Function	Type	Description
31:0	Upstream Page Boundary IRQ 1	RWC	Each interrupt request bit is correspondent to a page entry in the lower half of the Upstream Memory 2 range. Bit [0] is for the 33rd page, and bit [31] is for the 64th page. PI7C9X130 sets the appropriate bit when it successfully transfers data to or from the initiator that addresses the last Double Word in a page. PI7C9X130 initiates an interrupt request on secondary interface when the interrupt request bit is set and the corresponding Upstream Page Boundary IRQ 1 Mask bit is reset. When forward bridge, PI7C9X130 asserts INTA_L or generates MSI on secondary bus (PCI interface). When reverse bridge, PI7C9X130 sends INTA_L assertion message or generates MSI on secondary interface (PCI Express). When wrting a "1" to this register, it clears the corresponding interrupt request bit. Reset to 0

7.6.15 UPSTREAM PAGE BOUNDARY IRQ 0 MASK REGISTER - OFFSET 060h

Bit	Function	Type	Description
31:0	Upstream Page Boundary IRQ 0 Mask	RWC	**0**: PI7C9X130 can initiate an interrupt request when the correspondent request bit is set **1**: PI7C9X130 cannot initiate any interrupt request even though the correspondent request bit is set Reset to FFFFFFFFh

7.6.16 UPSTREAM PAGE BOUNDARY IRQ 1 MASK REGISTER - OFFSET 064h

Bit	Function	Type	Description
31:0	Upstream Page Boundary IRQ 1 Mask	RWC	**0**: PI7C9X130 can initiate an interrupt request when the correspondent request bit is set **1**: PI7C9X130 cannot initiate any interrupt request even though the correspondent request bit is set Reset to FFFFFFFFh

7.6.17 RESERVED REGISTER – OFFSET 068C

7.6.18 PRIMARY CLEAR IRQ REGISTER - OFFSET 070h

Bit	Function	Type	Description
15:0	Primary Clear IRQ	RWC	When writing "1" to this register bit, it clears the correspondent interrupt request bit. When reading this register, it returns the interrupt request bit status: 0: It is not the bit that causes the interrupt request on primary interface 1: It is the bit that causes the interrupt request on primary interface Reset to 0000h

7.6.19 SECONDARY CLEAR IRQ REGISTER - OFFSET 070h

Bit	Function	Type	Description
31:16	Secondary Clear IRQ	RWC	When writing "1" to this register bit, it clears the correspondent interrupt request bit. When reading this register, it returns the interrupt request bit status: 0: It is not the bit that causes the interrupt request on secondary interface 1: It is the bit that causes the interrupt request on secondary interface Reset to 0000h

7.6.20 PRIMARY SET IRQ REGISTER - OFFSET 074h

Bit	Function	Type	Description
15:0	Primary Set IRQ	RWS	When writing "1" to this register bit, it set the correspondent interrupt request bit. When reading this register, it returns the interrupt request bit status: 0: It is not the bit that causes the interrupt request on primary interface 1: It is the bit that causes the interrupt request on primary interface Reset to 0000h

7.6.21 SECONDARY SET IRQ REGISTER - OFFSET 074h

Bit	Function	Type	Description
31:16	Secondary Set IRQ	RWS	When writing "1" to this register bit, it set the correspondent interrupt request bit. When reading this register, it returns the interrupt request bit status: 0: It is not the bit that causes the interrupt request on secondary interface 1: It is the bit that causes the interrupt request on secondary interface Reset to 0000h

7.6.22 PRIMARY CLEAR IRQ MASK REGISTER - OFFSET 078h

Bit	Function	Type	Description
15:0	Primary Clear IRQ Mask	RWS	When writing "1" to this register bit, it clears the correspondent interrupt request mask bit. When reading this register, it returns the primary Clear IRQ Mask bit status: 0: It allows to clear an interrupt request on primary interface 1: It does not allow to clear any interrupt request on primary interface Reset to FFFFh

7.6.23 SECONDARY CLEAR IRQ MASK REGISTER - OFFSET 078h

Bit	Function	Type	Description
31:16	Secondary Clear IRQ Mask	RWS	When writing "1" to this register bit, it clears the correspondent interrupt request mask bit. When reading this register, it returns the Secondary Clear IRQ Mask bit status: 0: It allows to clear an interrupt request on secondary interface 1: It does not allow to clear any interrupt request on secondary interface Reset to FFFFh

7.6.24 PRIMARY SET IRQ MASK REGISTER - OFFSET 07Ch

Bit	Function	Type	Description
15:0	Primary Set IRQ Mask	RWS	When writing "1" to this register bit, it set the correspondent interrupt request mask bit. When reading this register, it returns the Primary Set IRQ Mask bit status: 0: It allows to set an interrupt request on primary interface 1: It does not allow to set any interrupt request on primary interface Reset to FFFFh

7.6.25 SECONDARY SET IRQ MASK REGISTER - OFFSET 07Ch

Bit	Function	Type	Description
31:16	Secondary Set IRQ Mask	RWC	When writing "1" to this register bit, it set the correspondent interrupt request mask bit. When reading this register, it returns the Secondary Set IRQ Mask bit status: 0: It allows to set an interrupt request on secondary interface 1: It does not allow to set any interrupt request on secondary interface Reset to FFFFh

7.6.26 RESERVED REGISTERS – OFFSET 080h TO 09Ch

7.6.27 SCRATCHPAD 0 REGISTER - OFFSET 0A0h

Bit	Function	Type	Description
31:0	Scratchpad 0	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.28 SCRATCHPAD 1 REGISTER - OFFSET 0A4h

Bit	Function	Type	Description
31:0	Scratchpad 1	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.29 SCRATCHPAD 2 REGISTER - OFFSET 0A8h

Bit	Function	Type	Description
31:0	Scratchpad 2	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.30 SCRATCHPAD 3 REGISTER - OFFSET 0ACh

Bit	Function	Type	Description
31:0	Scratchpad 3	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.31 SCRATCHPAD 4 REGISTER - OFFSET 0B0h

Bit	Function	Type	Description
31:0	Scratchpad 4	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.32 SCRATCHPAD 5 REGISTER - OFFSET 0B4h

Bit	Function	Type	Description
31:0	Scratchpad 5	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.33 SCRATCHPAD 6 REGISTER - OFFSET 0B8h

Bit	Function	Type	Description
31:0	Scratchpad 6	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.34 SCRATCHPAD 7 REGISTER - OFFSET 0BCh

Bit	Function	Type	Description
31:0	Scratchpad 7	RW	The scratchpad is a 32-bit internal register that can be accessed from both primary and secondary interfaces. The external devices can use the scratchpad as a temporary storage. Primary and secondary bus devices can communicate through the scratchpad. However, writing and reading the scratchpad does not generate any interrupt request. Reset to 00000000h

7.6.35 RESERVED REGISTERS – OFFSET 0C0h TO 0FCh

7.6.36 LOOKUP TABLE REGISTERS – OFFSET 100h TO 1FCh

Bit	Function	Type	Description
2047:0	Lookup Table	RW	The lookup table has 64 entries. Each entry has 32-bit mapped to each page of the Upstream Memory 2 base address range

64th page: bit [2047:2016]	63rd page: bit [2015:1984]
62nd page: bit [1983:1952]	61st page: bit [1951:1920]
60th page: bit [1919:1888]	59th page: bit [1887:1856]
58th page: bit [1855:1824]	57th page: bit [1823:1792]
56th page: bit [1791:1760]	55th page: bit [1759:1728]
54th page: bit [1727:1696]	53rd page: bit [1695:1664]
52nd page: bit [1663:1632]	51st page: bit [1631:1600]
50th page: bit [1599:1568]	49th page: bit [1567:1536]
48th page: bit [1535:1504]	47th page: bit [1503:1472]
46th page: bit [1471:1440]	45th page: bit [1439:1408]
44th page: bit [1407:1376]	43rd page: bit [1375:1344]
42nd page: bit [1343:1312]	41st page: bit [1311:1280]
40th page: bit [1279:1248]	39th page: bit [1247:1216]
38th page: bit [1215:1184]	37th page: bit [1183:1152]
36th page: bit [1151:1120]	35th page: bit [1119:1088]
34th page: bit [1087:1056]	33rd page: bit [1055:1024]
32nd page: bit [1023:992]	31st page: bit [991:960]
30th page: bit [959:928]	29th page: bit [927:896]
28th page: bit [895:864]	27th page: bit [863:832]
26th page: bit [831:800]	25th page: bit [799:768]
24th page: bit [767:736]	23rd page: bit [735:704]
22nd page: bit [703:672]	21st page: bit [671:640]
20th page: bit [639:608]	19th page: bit [607:576]
18th page: bit [575:544]	17th page: bit [543:512]
16th page: bit [511:480]	15th page: bit [479:448]
14th page: bit [447:416]	13th page: bit [415:383]
12th page: bit [382:352]	11th page: bit [351:320]
10th page: bit [319:288]	9th page: bit [287:256]
8th page: bit [255:224]	7th page: bit [223:192]
6th page: bit [191:160]	5th page: bit [159:128]
4th page: bit [127:96]	3rd page: bit [95:64]
2nd page: bit [63:32]	1st page: bit [31:0]

Reset to unknown

7.6.37 RESERVED REGISTERS – OFFSET 200h TO FFCh

8 GPIO PINS AND SM BUS ADDRESS

GPIO [3:1] of PI7C9X130 are defined for hot-plug usage if MSK_IN=1 during Reset. Please see configuration register definition (offset 78h – 7Bh).

GPIO [3:0] are also defined the address bits of SMBUS device ID if SM Bus is selected (TM1=1).
The address-strapping table of SMBUS with GPIO [3:0] pins is defined in the following table:

Table 8-1 SM Bus Device ID Strapping

SM Bus Address Bit	SM Bus device ID
Address bit [7]	= 1
Address bit [6]	= 1
Address bit [5]	= 0
Address bit [4]	= GPIO [3]
Address bit [3]	= GPIO [2]
Address bit [2]	= GPIO [1]
Address bit [1]	= GPIO [0]

GPIO [3:0] pins can be further defined to serve other functions in the next generation Device.

Four GPI [3:0] and four GPO [3:0] have been added to PI7C9X130 when external arbiter is selected (CFN_L=1).
If external arbiter is selected, REQ_L [5:2] and GNT [5:2] will become the GPI [3:0] and GPO [3:0] respectively.

9 CLOCK SCHEME

PCI Express interface:

PI7C9X130 requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins.

PCI-X / PCI interface:

To use external clock source, PI7C9X130 requires PCI-X clock (up to 133MHz) to be connected to the Pin T6, CLKIN / M66EN. PI7C9X130 uses the CLKIN and generates seven clock outputs, CLKOUT [6:0]. Also, PI7C9X130 requires one of the CLKOUT [6:0] (preferably CLKOUT [6]) to be connected to FBCLKIN for the PCI-X interface logic of PI7C9X130.

To enable internal clock generator and auto frequency detection, CLKIN / M66EN needs to connect to M66EN of a PCIX / PCI compliant device. The CLK / M66EN input pin is driven high or low to enable the internal clock generator and auto frequency detection. Please note that PI7C9X130 samples CLKIN/M66EN pin continuously throughout the entire operation. If PI7C9X130 detectes 15 or more rising edges on CLKIN/M66EN pin due to signal glitches or other reasons any time in the operation, PI7C9X130 will switch to external clock mode immediately and stay in the mode until the chip is reset. Therefore, it is important that CLKIN/M66EN signal be maintained in a stable state when internal clock is used. The frequency output of CLKOUT[0:6] is determined by the state of CLKIN (M66EN), PCIXCAP, PCIXUP and SEL100 listed as below:

CLKIN (M66EN)	PCIXCAP	SEL100	Frequency
low	gnd	high	PCI 25 Mhz
low	gnd	low	PCI 33 Mhz
high	gnd	high	PCI 50 Mhz
high	gnd	low	PCI 66 Mhz
dont care	10K to gnd	high	PCIX 50 Mhz
dont care	10K to gnd	low	PCIX 66 Mhz
dont care	high	High	PCIX 100 Mhz
dont care	high	low	PCIX 133 Mhz

The actual number of masters supported will vary depending on the loading of the PCI-X bus. Typically, PI7C9X130 can support up to one 133MHz PCI-X slot or two 66MHz PCI-X slots.

The PI7C9X130 PCI Clock Outputs, CLKOUT [6:0], can be enabled or disabled through the configuration register.

10 INTERRUPTS

PI7C9X130 supports interrupt message packets on PCIe side. PI7C9X130 supports PCI interrupt (INTA, B, C, D) pins or MSI (Message Signaled Interrupts) on PCI side. PCI interrupts and MSI are mutually exclusive. In order words, if MSI is enabled, PCI interrupts will be disabled. PI7C9X130 support 64-bit addressing MSI.

In reverse bridge mode, PI7C9X130 maps the interrupt message packets to PCI interrupt pins or MSI if MSI is enable (see configuration register bit [16] of Offset F0h).

In forward bridge mode, PI7C9X130 maps the PCI interrupts pins or MSI if enable on PCI side to interrupt message packets on PCIe side.

There are eight interrupt message packets. They are Assert_INTA, Assert_INTB, Assert_INTC, Assert_INTD, Deassert_INTA, Deassert_INTB, Deassert_INTC, and Deassert_INTD. These eight interrupt messages are mapped to the four PCI interrupts (INTA, INTB, INTC, and INTD). See table 10-1 for interrupt mapping information in reverse bridge mode. PI7C9X130 tracks the PCI interrupt (INTA, INTB, INTC, and INTD) pins and maps them to the eight interrupt messages. See table 10-2 for interrupt mapping information in forward bridge mode.

Table 10-1 PCIe Interrupt Messages to PCI Interrupts Mapping in Reverse Bridge Mode

PCIe Interrupt messages (from sources of interrupt)	PCI Interrupts (to host controller)
INTA message	INTA
INTB message	INTB
INTC message	INTC
INTD message	INTD

Table 10-2 PCI Interrupts to PCIe Interrupt Messages Mapping in Forward Bridge Mode

PCI Interrupts (from sources of interrupts)	PCIe Interrupt message packets (to host controller)
INTA	INTA message
INTB	INTB message
INTC	INTC message
INTD	INTD message

11 EEPROM (I2C) INTERFACE AND SYSTEM MANAGEMENT BUS

11.1 EEPROM (I2C) INTERFACE

PI7C9X130 supports EEPROM interface through I2C bus. In EEPROM interface, pin A2 is the EEPROM clock (SCL) and pin A1 is the EEPROM data (SDL). When TM2 is strapped to low, TM1 selects EEPROM interface or System Management Bus. To select EEPROM (I2C) interface, TM1 needs to be set to low. When EEPROM interface is selected, SCL is an output. SCL is the I2C bus clock to the I2C device. In addition, SDL is a bi-directional signal for sending and receiving data.

11.2 SYSTEM MANAGEMENT BUS

PI7C9X130 supports SM bus protocol if TM1=1 when TM2 is strapped to low. In addition, SMBCLK (pin A2) and SMBDAT (pin A1) are utilized as the clock and data pins respectively for the SM bus.

When SM bus interface is selected, SMBCLK pin is an input for the clock of SM bus and SMBDAT pin is an open drain buffer that requires external pull-up resistor for proper operation.

12 HOT PLUG OPERATION

PI7C9X130 is not equipped with standard hot-plug controller (SHPC) integrated. However, PI7C9X130 supports hot-plug signaling messages and registers to simplify the implementation of hot-plug system.

Using PI7C9X130 on motherboard:

PI7C9X130 supports hot-plug on PCI bus if forward bridging is selected (REVRSB=0).

PI7C9X130 supports hot-plug function on PCI Express bus when reverse bridge mode is selected (REVRSB=1).

Using PI7C9X130 on add-in card:

PI7C9X130 supports hot-plug on PCI Express bus in forward bridge mode. Hot-plug messages will be generated by PI7C9X130 based on the add-in card conditions.

PI7C9X130 supports hot-plug function on PCI bus when reverse bridge mode is selected. PI7C9X130 will tri-state the PCI bus when RESET is asserted. Also, PI7C9X130 will de-assert INTA_L if RESET is asserted. The state machine of PI7C9X130 PCI bus interface will remain idle if the RESET is asserted. After RESET is de-asserted, PI7C9X130 will remain in idle state until an address phase containing a valid address for PI7C9X130 or its downstream devices.

PI7C9X130 expects the REFCLK signal will be provided to its upstream PCI Express Port prior to the de-assertion of RESET. The Downstream PCI Port of PI7C9X130 supports a range of frequency up to 66MHz.

PI7C9X130 also supports subsystem vendor and subsystem ID. PI7C9X130 will ignore target response while the bus is idle.

PRSNT1# and PRSNT2# are not implemented on both PI7C9X130. The use of these two signals is mandatory on an add-in card in order to support hot-plug.

13 RESET SCHEME

PI7C9X130 requires the fundamental reset (PERST_L) input for internal logic when it is set as forward bridge mode. PI7C9X130 requires the PCI/PCI-X reset (RESET_L) input when it is set as reverse bridge mode. Also, PI7C9X130 has a power-on-reset (POR) circuit to detect VDDCAUX power supply for auxiliary logic control.

Cold Reset:
A cold reset is a fundamental or power-on reset that occurs right after the power is applied to PI7C9X130 (during initial power up). See section 7.1.1 of PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 for details.

Warm Reset:
A warm reset is a reset that triggered by the hardware without removing and re-applying the power sources to PI7C9X130.

Hot Reset:
A hot reset is a reset that used an in-band mechanism for propagating reset across a PCIe link to PI7C9X130. PI7C9X130 will enter to training control reset when it receives two consecutive TS1 or TS2 order-sets with reset bit set.

DL_DOWN Reset:
If the PCIe link goes down, the Transaction and Data Link Layer will enter DL_DOWN status. PI7C9X130 discards all transactions and returns all logic and registers to initial state except the sticky registers.

Upon receiving reset (cold, warm, hot, or DL_DOWN) on PCIe interface, PI7C9X130 will generate PCI/PCI-X reset (RESET_L) to the downstream devices on the PCI/PCI-X bus in forward bridge mode. The PCI/PCI-X reset de-assertion follows the de-assertion of the reset received from PCIe interface. The reset bit of Bridge Control Register may be set depending on the application. PI7C9X130 will tolerant to receive and process SKIP order-sets at an average interval between 1180 to 1538 Symbol Times. PI7C9X130 does not keep PCI/PCI-X reset active when VD33 power is off even though VAUX (3.3v) is supported. It is recommended to add a weak pull-down resistor on its application board to ensure PCI/PCI-X reset is low when VD33 power is off (see section 7.3.2 of PCI Bus Power management Specification Revision 1.1).

In reverse bridge mode, PI7C9X130 generates fundamental reset (PERST_L) and then 1024 TS1 order-sets with reset bit set when PCI/PCI-X reset (RESET_L) is asserted to PI7C9X130. PI7C9X130 has scheduling skip order-set for insertion at an interval between 1180 and 1538 Symbol Times.

PI7C9X130 transmits one Electrical Idle order-set and enters to Electrical Idle.

14 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X130 for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up. The JTAG signal lines are not active when the PCI resource is operating PCI bus cycles.

14.1 INSTRUCTION REGISTER

PI7C9X130 implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in Table 14-1. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction:

Table 14-1 Instruction Register Codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
MEM_BIST	01010	Memory BIST	Memory BIST test

14.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X130.

14.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 14-2 JTAG Device ID Register

Bit	Type	Value	Description
31:28	RO	00h	Version number
27:12	RO	E130h	Last 4 digits (hex) of the die part number
11:1	RO	23Fh	Pericom identifier assigned by JEDEC
0	RO	1b	Fixed bit equal to 1'b1

14.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X130 package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

14.5 JTAG BOUNDARY SCAN REGISTER ORDER

Table 14-3 JTAG Boundary Scan Register Definition

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
0	GPIO [6]	L15	BIDIR	1
1	-	-	CONTROL	-
2	AD [0]	L16	BIDIR	3
3	-	-	CONTROL	-
4	AD [1]	K13	BIDIR	5
5	-	-	CONTROL	-
6	AD [2]	K14	BIDIR	7
7	-	-	CONTROL	-
8	AD [3]	K15	BIDIR	9
9	-	-	CONTROL	-
10	AD [4]	K16	BIDIR	11
11	-	-	CONTROL	-
12	AD [5]	J13	BIDIR	13
13	-	-	CONTROL	-
14	AD [6]	J14	BIDIR	15
15	-	-	CONTROL	-
16	AD [7]	J15	BIDIR	17
17	-	-	CONTROL	-
18	CBE [0]	J16	BIDIR	19
19	-	-	CONTROL	-
20	AD [8]	H13	BIDIR	21
21	-	-	CONTROL	-
22	AD [9]	H14	BIDIR	23
23	-	-	CONTROL	-
24	AD [10]	H15	BIDIR	25

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
25	-	-	CONTROL	-
26	AD [11]	H16	BIDIR	27
27	-	-	CONTROL	-
28	AD [12]	G13	BIDIR	29
29	-	-	CONTROL	-
30	AD [13]	G14	BIDIR	31
31	-	-	CONTROL	-
32	AD [14]	G15	BIDIR	33
33	-	-	CONTROL	-
34	AD [15]	G16	BIDIR	35
35	-	-	CONTROL	-
36	CBE [1]	F13	BIDIR	37
37	-	-	CONTROL	-
38	PAR	F14	BIDIR	39
39	-	-	CONTROL	-
40	SERR_L	F15	BIDIR	41
41	-	-	CONTROL	-
42	PERR_L	F16	BIDIR	43
43	-	-	CONTROL	-
44	LOCK_L	E13	BIDIR	45
45	-	-	CONTROL	-
46	SEL100	E14	INPUT	-
47	DEV64	E15	INPUT	-
48	ACK64_L	E16	BIDIR	49
49	-	-	CONTROL	-
50	REQ64_L	D14	BIDIR	51
51	-	-	CONTROL	-
52	PAR64	D15	BIDIR	53
53	-	-	CONTROL	-
54	AD [47]	D16	BIDIR	55
55	-	-	CONTROL	-
56	AD [46]	C15	BIDIR	57
57	-	-	CONTROL	-
58	AD [45]	C16	BIDIR	59
59	-	-	CONTROL	-
60	AD [44]	B16	BIDIR	61
61	-	-	CONTROL	-
62	AD [43]	B15	BIDIR	63
63	-	-	CONTROL	-
64	AD [42]	A15	BIDIR	65
65	-	-	CONTROL	-
66	AD [41]	C14	BIDIR	67
67	-	-	CONTROL	-
68	AD [40]	B14	BIDIR	69
69	-	-	CONTROL	-
70	CBE [5]	A14	BIDIR	71
71	-	-	CONTROL	-
72	AD [39]	C13	BIDIR	73
73	-	-	CONTROL	-
74	AD [38]	B13	BIDIR	75

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
75	-	-	CONTROL	-
76	AD [37]	A13	BIDIR	77
77	-	-	CONTROL	-
78	AD [36]	D12	BIDIR	79
79	-	-	CONTROL	-
80	AD [35]	C12	BIDIR	81
81	-	-	CONTROL	-
82	AD [34]	B12	BIDIR	83
83	-	-	CONTRL	-
84	AD [33]	A12	BIDIR	85
85	-	-	CONTROL	-
86	AD [32]	D11	BIDIR	87
87	-	-	CONTROL	-
88	CBE [4]	C11	BIDIR	89
89	-	-	CONTROL	-
90	STOP_L	B11	BIDIR	91
91	-	-	CONTROL	-
92	DEVSEL_L	A11	BIDIR	93
93	-	-	CONTROL	-
94	TRDY_L	D10	BIDIR	93
95	IRDY_L	C10	BIDIR	96
96	-	-	CONTROL	-
97	FRAME_L	B10	BIDIR	98
98	-	-	CONTROL	-
99	CBE [2]	A10	BIDIR	100
100	-	-	CONTROL	-
101	AD [16]	D9	BIDIR	102
102	-	-	CONTROL	-
103	AD [17]	C9	BIDIR	104
104	-	-	CONTROL	-
105	AD [18]	B9	BIDIR	106
106	-	-	CONTROL	-
107	AD [19]	A9	BIDIR	108
108	-	-	CONTROL	-
109	AD [20]	D8	BIDIR	110
110	-	-	CONTROL	-
111	AD [21]	C8	BIDIR	112
112	-	-	CONTROL	-
113	AD [22]	B8	BIDIR	114
114	-	-	CONTROL	-
115	AD [23]	A8	BIDIR	116
116	-	-	CONTROL	-
117	CBE [3]	D7	BIDIR	118
118	-	-	CONTROL	-
119	AD [24]	C7	BIDIR	120
120	-	-	CONTROL	-
121	AD [25]	B7	BIDIR	122
122	-	-	CONTROL	-
123	AD [26]	A7	BIDIR	124
124	-	-	CONTROL	-
125	AD [27]	D6	BIDIR	126

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
126	-	-	CONTROL	-
127	AD [28]	C6	BIDIR	128
128	-	-	CONTROL	-
129	AD [29]	B6	BIDIR	130
130	-	-	CONTROL	-
131	AD [30]	A6	BIDIR	132
132	-	-	CONTROL	-
133	AD [31]	D5	BIDIR	134
134	-	-	CONTROL	-
135	PME_L	C5	BIDIR	136
136	-	-	CONTROL	-
137	SMBCLK	B5	BIDIR	138
138	-	-	CONTROL	-
139	SMBDAT	A5	BIDIR	140
140	-	-	CONTROL	-
141	CLKRUN_L	C4	BIDIR	142
142	-	-	CONTROL	-
143	FBCLKIN	B4	INPUT	-
144	PCIXCAP	A4	INPUT	-
145	PCIXUP	B3	OUTPUT3	146
146	-	-	CONTROL	-
147	PERST_L	P1	BIDIR	148
148	-	-	CONTROL	-
149	REQ_L [0]	R1	INPUT	-
150	REQ_L [1]	P2	INPUT	-
151	REQ_L [2]	R2	INPUT	-
152	REQ_L [3]	T2	INPUT	-
153	REQ_L [4]	N3	INPUT	-
154	REQ_L [5]	P3	INPUT	-
155	HSEN	R3	INPUT	-
156	HSSW	T3	INPUT	-
157	INTA_L	P4	BIDIR	158
158	-	-	CONTROL	-
159	GNT_L [0]	R4	OUTPUT3	160
160	-	-	CONTROL	-
161	GNT_L [1]	T4	OUTPUT3	166
162	GNT_L [2]	N5	OUTPUT3	166
163	GNT_L [3]	P5	OUTPUT3	166
164	GNT_L [4]	R5	OUTPUT3	166
165	GNT_L [5]	T5	OUTPUT3	166
166	-	-	CONTROL	-
167	LOO	N6	OUTPUT3	168
168	-	-	CONTROL	-
169	ENUM_L	P6	OUTPUT3	170
170	-	-	CONTROL	-
171	INTB_L	R6	BIDIR	172
172	-	-	CONTROL	-
173	CLKIN / M66EN	T6	INPUT	-
174	RESET_L	N7	BIDIR	175
175	-	-	CONTROL	-

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
176	CFN_L	P7	INPUT	-
177	GPIO [3]	R7	BIDIR	178
178	-	-	CONTROL	-
179	GPIO [2]	T7	BIDIR	180
180	-	-	CONTROL	-
181	GPIO [1]	N8	BIDIR	182
182	-	-	CONTROL	-
183	GPIO [0]	P8	BIDIR	184
184	-	-	CONTROL	-
185	CLKOUT [0]	R8	OUTPUT3	192
186	CLKOUT [1]	T8	OUTPUT3	192
187	CLKOUT [2]	N9	OUTPUT3	192
188	CLKOUT [3]	P9	OUTPUT3	192
189	CLKOUT [4]	R9	OUTPUT3	192
190	CLKOUT [5]	T9	OUTPUT3	192
191	CLKOUT [6]	N10	OUTPUT3	192
192	-	-	CONTROL	-
193	GPIO [4]	P10	BIDIR	194
194	-	-	CONTROL	-
195	GPIO [5]	R10	BIDIR	196
196	-	-	CONTROL	-
197	INTC_L	T10	BIDIR	198
198	-	-	CONTROL	-
199	AD [63]	N11	BIDIR	200
200	-	-	CONTROL	-
201	AD [62]	P11	BIDIR	202
202	-	-	CONTROL	-
203	AD [61]	R11	BIDIR	204
204	-	-	CONTROL	-
205	AD [60]	T11	BIDIR	206
206	-	-	CONTROL	-
207	AD [59]	N12	BIDIR	208
208	-	-	CONTROL	-
209	AD [58]	P12	BIDIR	210
210	-	-	CONTROL	-
211	AD [57]	R12	BIDIR	212
212	-	-	CONTROL	-
213	AD [56]	T12	BIDIR	214
214	-	-	CONTROL	-
215	CBE [7]	P13	BIDIR	216
216	-	-	CONTROL	-
217	AD [55]	R13	BIDIR	218
218	-	-	CONTROL	-
219	AD [54]	T13	BIDIR	220
220	-	-	CONTROL	-
221	AD [53]	P14	BIDIR	222
222	-	-	CONTROL	-
223	AD [52]	R14	BIDIR	224
224	-	-	CONTROL	-
225	AD [51]	T14	BIDIR	226

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
226	-	-	CONTROL	-
227	AD [50]	T15	BIDIR	228
228	-	-	CONTROL	-
229	AD [49]	R15	BIDIR	230
230	-	-	CONTROL	-
231	AD [48]	R16	BIDIR	232
232	-	-	CONTROL	-
233	CBE [6]	P15	BIDIR	234
234	-	-	CONTROL	-
235	REVRSB	N14	INPUT	-
236	INTD_L	N15	BIDIR	237
237	-	-	CONTROL	-
238	MSK_IN	N16	INPUT	-
239	IDSEL	M13	INPUT	-

15 POWER MANAGEMENT

PI7C9X130 supports D0, D3-hot, D3-cold Power States. D1 and D2 states are not supported. The PCI Express Physical Link Layer of the PI7C9X130 device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States. For the PCI Port of PI7C9X130, it supports the standard PCI Power Management States with B0, B1, B2 and B3.

During D3-hot state, the main power supplies of VDDP, VDDC, and VD33 can be turned off to save power while keeping the VDDAUX, VDDCAUX, and VAUX with the auxiliary power supplies to maintain all necessary information to be restored to the full power D0 state. PI7C9X130 has been designed to have sticky registers that are powered by auxiliary power supplies. PME_L pin allows PCI devices to request power management state changes. Along with the operating system and application software, PCI devices can achieve optimum power saving by using PME_L in forward bridge mode. PI7C9X130 converts PME_L signal information to power management messages to the upstream switches or root complex. In reverse bridge mode, PI7C9X130 converts the power management event messages from PCIe devices to the PME_L signal and continues to request power management state change to the host bridge.

PI7C9X130 also supports ASPM (Active State Power Management) to facilitate the link power saving.

PI7C9X130 supports beacon generation but does not support WAKE# signal.

16 POWER SEQUENCING

The PI7C9X130D require two voltages: 3.3V I/O voltage and 1.8V core voltage. The 1.8V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X130D, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.8V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X130D will not be damaged as long as 3.3V is applied either before or at the same time as 1.8V.

During power cycle, if there is a delay in applying 1.8V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states.

The typical time for PI7C9X130D to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Figure 16-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 16-2 shows the recommended power sequence timing.

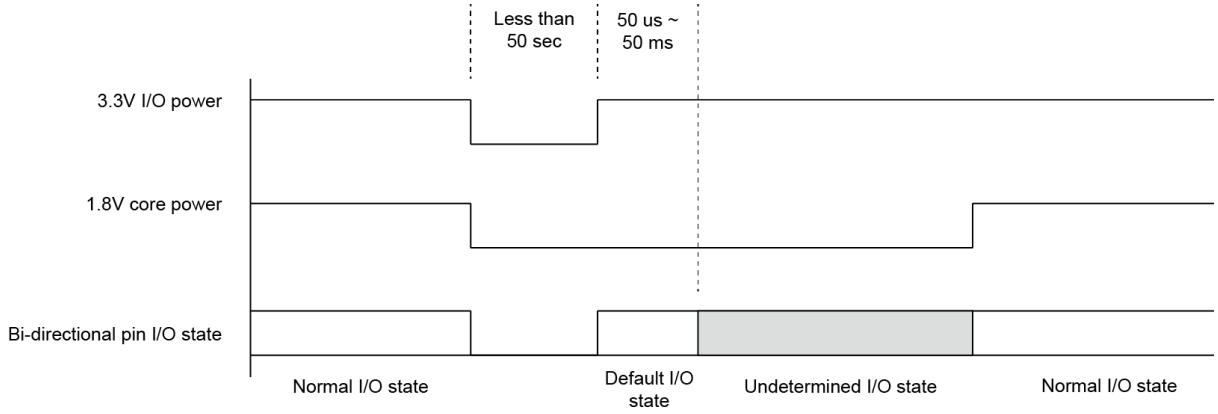


Figure 16-1 Timing Sequence with Undetermined I/O State

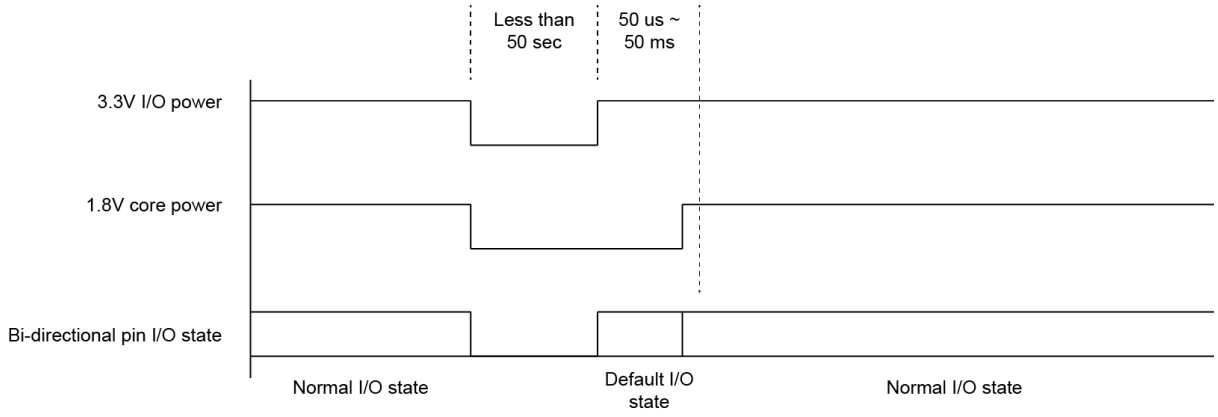


Figure 16-2 Recommended Power Sequence

If the gap between 3.3V IO power and 1.8V core power is too big, there might be glitch at pins PERST_L and RESET_L. The maximum gap is recommended to be 50us~50ms, customer needs to measure the waveform of PERST_L and RESET_L to make sure there is no glitch during the gap.

16.1 INITIAL POWER-UP (G3 TO L0)

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (3.3V and 12V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (T_{PVPERL}) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

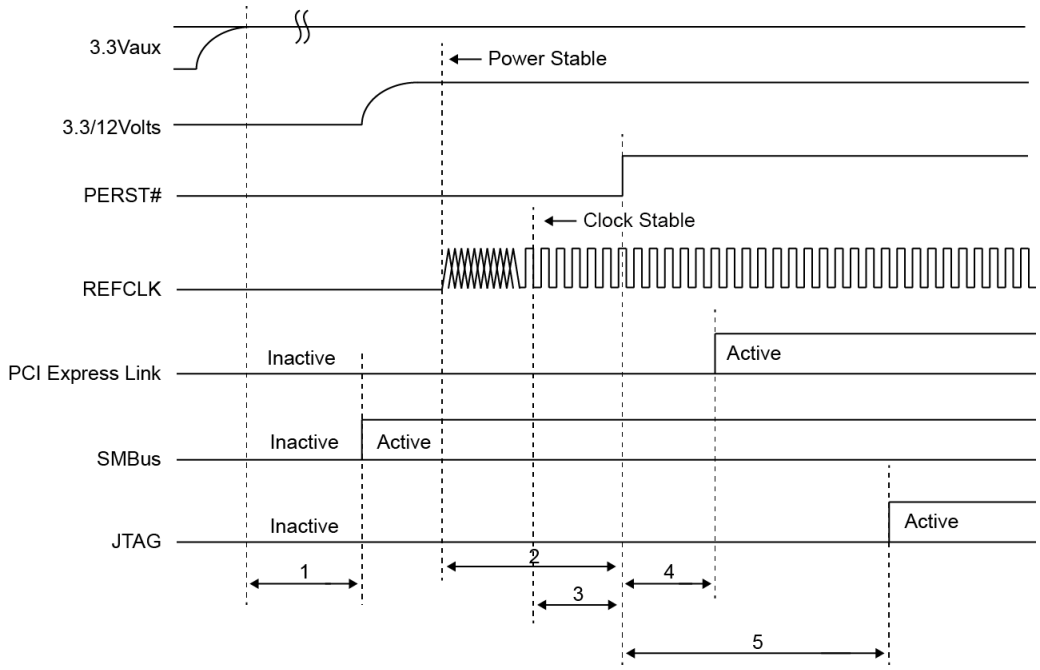


Figure 16-3 Initial Power-up

1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$)
4. Minimum PERST# inactive to PCI Express link out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

Table 16-1 Power Sequencing and Reset Signal Timings

Symbol	Parameter	Min	Max	Units
T_{PVPERL} (1)	Power stable to PERST# inactive	100		ms
$T_{PERST-CLK}$ (2)	REF CLK stable before PERST# inactive	100		µs
T_{PERST}	PERST# active time	100		µs
T_{FAIL} (3)	Power level invalid to PERST# active		500	ns
T_{WKRF} (4)	WAKE# rise – fall time		100	ns

Note:
1. Any supplied power is stable when it meets the requirements specified for that power supply.
2. A supplied reference clock is stable when it meets the requirements specified for the reference clock. The PEREST# signal is asserted and de-asserted asynchronously with respect to the supplied reference clock.
3. The PEREST# signal must be asserted within T_{FAIL} of any supplied power going out specification.
4. Measured from WAKE# assertion/de-assertion to valid input level at the system PM controller. Since WAKE# is an open-drain signal, the rise time is dependent on the total capacitance on the platform and the system board pull-up resistor. It is the responsibility of the system designer to meet the rise time specification.

16.2 POWER-OFF SQUENCE

The power off sequence is the reverse of the power on sequence, that is, asserts the PERST# first, then after T_{PERST_CLK} disable the REFCLK, and power off core power and I/O power, but I/O power off should be the same time or later than the core power off.

17 ELECTRICAL AND TIMING SPECIFICATIONS

17.1 ABSOLUTE MAXIMUM RATINGS

Table 17-1 Absolute Maximum Ratings

Item	Absolute Max. Rating
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature (Tj)	125°C
PCI Express supply voltage to ground potential (VDDA, VDDP, VDDC, VDDAUX, and VDDCAUX)	-0.3v to 2.1v
PCI Express Termination Supply Voltage to ground potential (VTT)	-0.3v to 2.1v
PCI supply voltage to ground potential (VD33 and VAUX)	-0.3v to 3.8v
DC input voltage for PCI Express signals	-0.3v to 2.1v
DC input voltage for PCI signals	-0.3v to 5.75v

17.2 DC SPECIFICATIONS

Table 17-2 provides DC Electrical Characteristics of PI7C9X130:

Table 17-2 DC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VDDA	Analog Power Supply for PCI Express Interface		1.6	1.8	2.0	V
VDDP	Digital Power Supply for PCI Express Interface		1.6	1.8	2.0	V
VDDC	Digital Power Supply for the Core		1.6	1.8	2.0	V
VDDAUX	Digital Auxiliary Power Supply for PCI Express Interface		1.6	1.8	2.0	V
VDDCAUX	Digital Auxiliary Power Supply for the Core		1.6	1.8	2.0	V
VDDA_PLL	Analog Power Supply for PLL of PCI-X Interface		1.6	1.8	2.0	V
VDDP_PLL	Digital Power Supply for PLL of PCI-X Interface		1.6	1.8	2.0	V
VTT	Termination Power Supply for PCI Express Interface		1.6	1.8	2.0	V
VD33	Digital Power Supply for PCI/PCI-X Interface		3.0	3.3	3.6	V
VAUX	Digital Auxiliary Power Supply for PCI/PCI-X Interface		3.0	3.3	3.6	V
V_{IH}	PCI Input High Voltage		1.55		5.5	V
V_{IL}	PCI Input Low Voltage		-0.3		1.08	V
I_{IL}	PCI Input Leakage Current	$0<V_{IN}<VD33$			±10	µA
V_{OH}	PCI Output High Voltage	I_{out} = -500µA	2.7			V
V_{OL}	PCI Output Low Voltage	I_{out} = 1500µA			0.36	V
C_{IN}	PCI Input Pin Capacitance				10	pF
C_{CLK}	PCI CLK Pin Capacitance		5		12	pF
C_{IDSEL}	PCI IDSEL Pin Capacitance				8	pF

In order to support auxiliary power management fully, it is recommended to have VDDP and VDDAUX separated. By the same token, VD33/VDDC and VAUX/VDDCAUX need to be separated for auxiliary power management support. However, if auxiliary power management is not required, VD33 and VDDC can be connected to VAUX and VDDCAUX respectively. The typical power consumption of PI7C9X130 is about 1.5 watt. PI7C9X130 is capable of sustaining 2000V human body model for the ESD protection without any damages.

17.3 AC SPECIFICATIONS

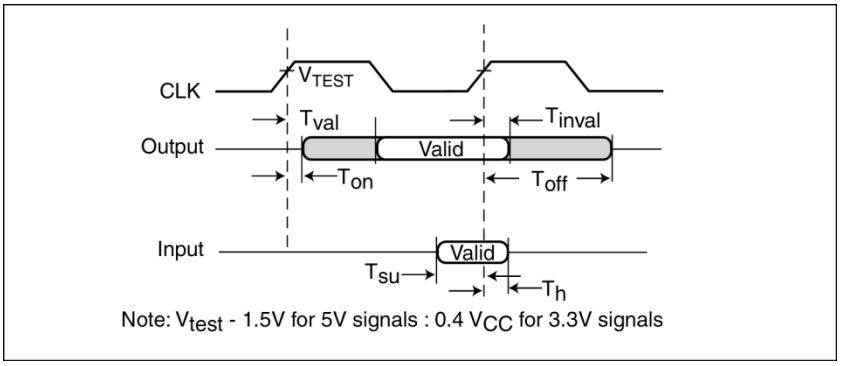
Provides PCI Bus Timing Parameters of PI7C9X130.

Table 17-3 PCI Bus Timing Parameters

Symbol	Parameter	PCI-X 133MHz		PCI 66 MHz		PCI 33 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Tsu	Input setup time to CLK – bused signals [1,2,3]	1.2	-	3	-	7	-	ns
Tsu (ptp)	Input setup time to CLK – point-to-point [1,2,3]	1.2	-	5	-	10, 12[4]	-	
Th	Input signal hold time from CLK [1,2]	0.5	-	0	-	0	-	
Tval	CLK to signal valid delay – bused signals [1,2,3]	0.7	3.8	2	6	2	11	
Tval (ptp)	CLK to signal valid delay – point-to-point [1,2,3]	0.7	3.8	2	6	2	12	
Ton	Float to active delay [1,2]	0	-	2	-	2	-	
Toff	Active to float delay [1,2]	-	7	-	14	-	28	

1. See Figure 16 –1 PCI Signal Timing Measurement Conditions.
2. All PCI interface signals are synchronized to FBCLKIN.
3. Point-to-point signals are REQ_L [7:0], GNT_L [7:0], LOO, and ENUM_L. Bused signals are AD, CBE, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, LOCK_L, STOP_L and IDSEL.
4. PCI Control Signals: FRAME_L, TRDY_L, IRDY_L, DEVSEL_L, STOP_L, SERR_L, PERR_L, LOCK_L, INTA_L, INTB_L, INTC_L, INTD_L, REQ64_L and ACT64_L of PI7C9X130 require pull-up resistors (~5K ohm) if PI7C9X130 is implemented as a PCIX host on the system motherboard.
5. If the system needs to support 32-bit PCI add-in card then AD[63::32] and C/BE[7::4]_L pins need pull-up resistor (~5K ohm)
6. REQ_L signals have a setup of 10ns and GNT_L signals have a setup of 12ns.

Figure 17-1 PCI Signal Timing Conditions



PI7C9X130 PBGA256 17x17 Thermal Data:

TA = 75oC

Air Flow	0 m/s	1 m/s	2 m/s
θ_{JC}	7.2		
θ_{JA}	24.2	21.3	20.1
Max Power (W)	2.07	2.35	2.49

Calculation formula:

1. Maximum Tj is 125oC. This is the junction temperature of the IC.
2. Since there is no way to measure actual Tj, we use the following formula to calculate this number:
   a. Tj = θ_{JA} * Power + Ta
   b. Tj = θ_{JC} * Power + Tc or
   c. Maximum Tc = Tj - θ_{JC} * Power

Where: Ta : Ambient temperature, and Tc : Case temperature.

Example:

1. Using typical power of 2W and 75oC ambient temperature in the calculation:
2. From first formula: Tj = 24.2 * 2 + 75 = 123.4oC. From second formula, the maximum Tc = 125oC – 7.2 * 2 = 110.6oC

Table 17-4 specifies the voltage and timing requirements for the input clock signals.

Table 17-4 PCIe Reference Clock Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Units
$ClkIn_{FREQ}$	Input clock frequency range		100		MHz
$ClkIn_{DC}$	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2	QCUI*
V_{SW}	Differential input voltage swing (peak-to-peak)	400	600	1200	mV
V_{CM}	Input common voltage	0.6	0.65	0.7	V

*RCUI(Reference Clock Unit Interval) refers to the reference clock period.

Table 17-5 PCI Express Interface - Differential Transmitter (TX) Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Lower power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0	-	-4.0	dB
Minimum TX eye width	T_{TX-EYE}	0.75	-	-	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125	-	-	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5	-	-	MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 2 UI	ps

Table 17-6 PCI Express Interface - Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175	-	1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4	-	-	UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80	-	120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200	-	-	kΩ
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV
Lane to Lane skew	$L_{RX-SKEW}$	-	-	20	ns

17.4 OPERATING AMBIENT TEMPERATURE

Table 17-7 Operating Ambient Temperature

(Above witch the useful life may be impaired.)

Item	Low	High	Unit
Ambient Temperature with power applied	-40	85	°C

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

18 PACKAGE INFORMATION

Figure 18-1 Top View Drawing

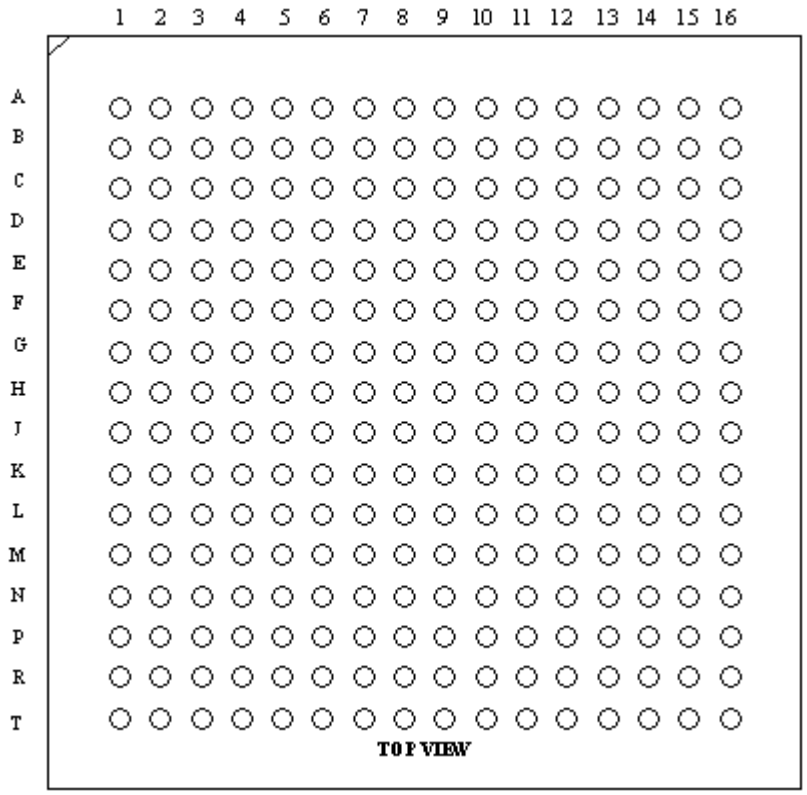
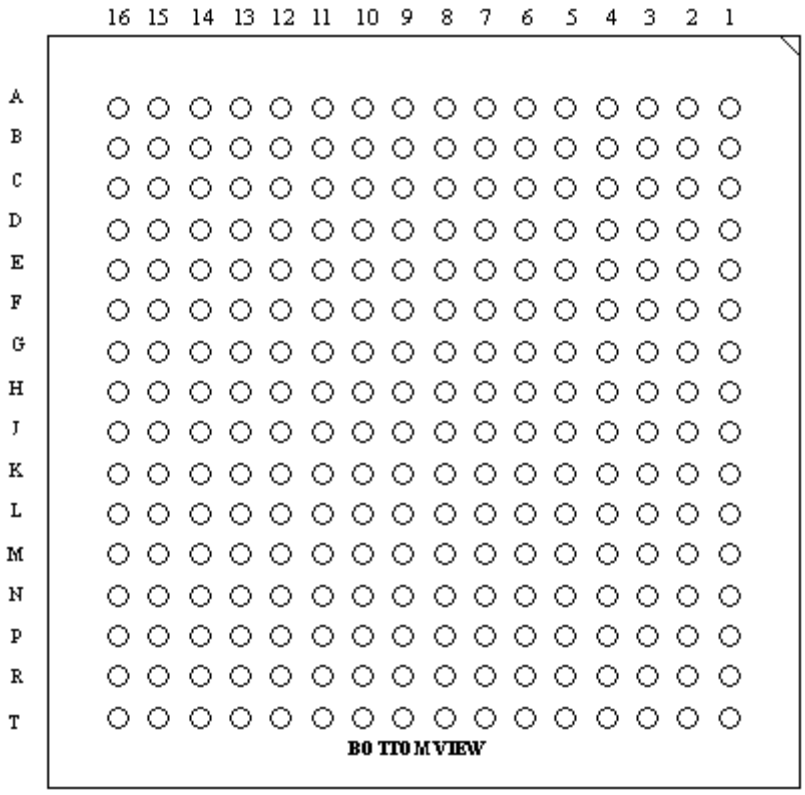


Figure 18-2 Bottom View Drawing



The package of PI7C9X130 is a 17mm x 17mm PBGA (256 Pin) package. The ball pitch is 1.0mm and the ball size is 0.5mm. The following are the package information and mechanical dimension:

Figure 18-3 Package Outline Drawing

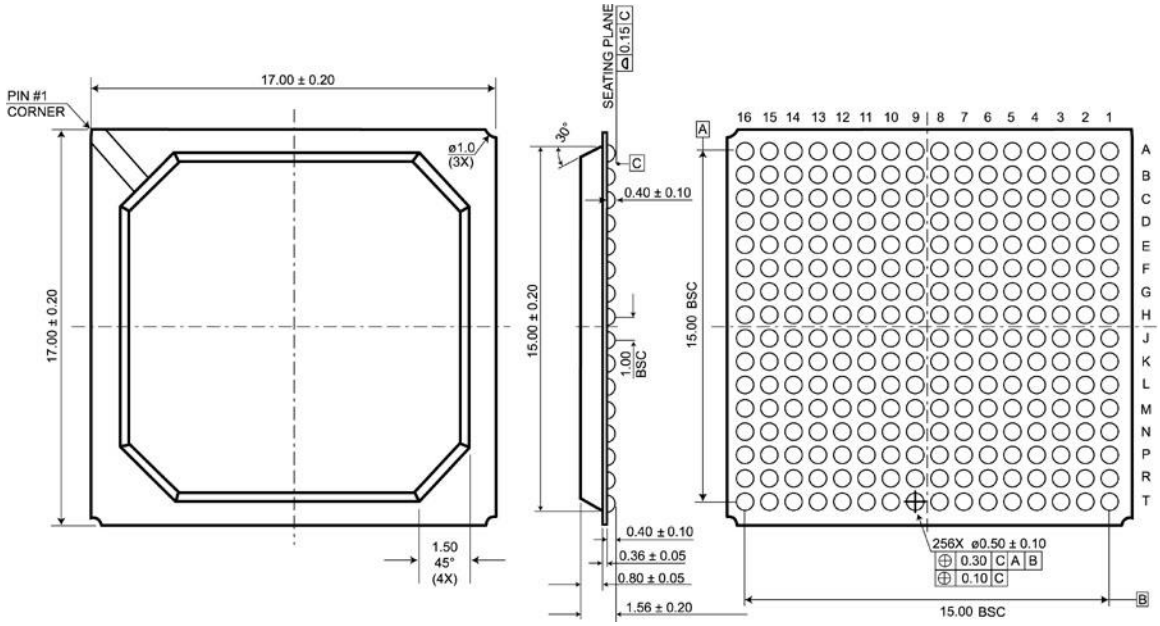


Figure 18-4 Part Marking

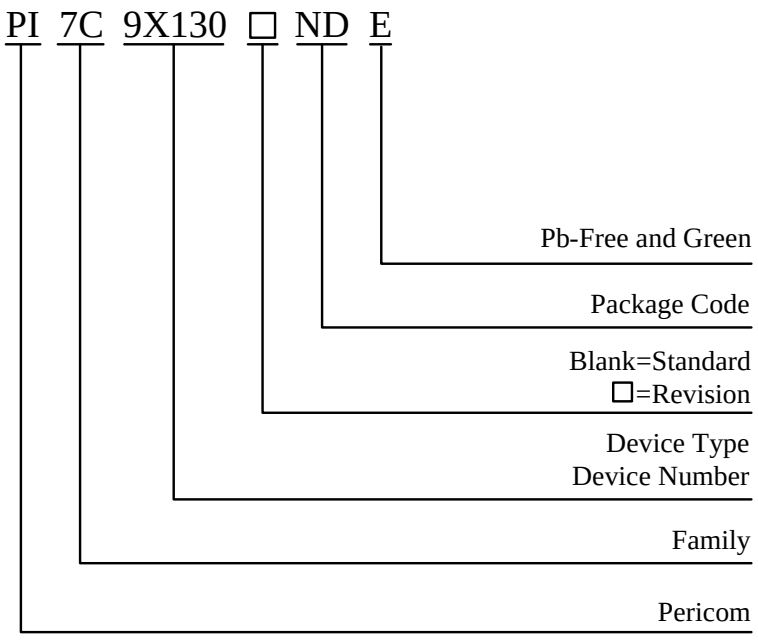
Z:Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code
Bar Above the 2nd X means Cu Wire
Without a bar means Au Wire

19 ORDERING INFORMATION

Device	Package	RoHS Compliant	Temperature Range
PI7C9X130□NDE	256-pin PBGA17 x 17mm	Yes	-40°C to 85°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel



20 ASYNCHRONOUS CLOCK

20.1 ASYNCHRONOUS CLOCK SUPPORT

PI7C9X130 supports PCI Express Asynchronous Clock Domain only in a x1 PCIe Link interface. To operate in a x4 PCIe Link, REFCLK pin of PI7C9X130 requires a synchronous clock source from the same clock domain of PCIe Root Complex or PCIe End Point that PI7C9X130 is connected to. The requirement of synchronous clock source applies to both Forward and Reverse Mode Operations.