PI74FCT151T
PI74FCT251T
(25Ω Series) PI74FCT2151T

Fast CMOS 8-Input Multiplexer

Product Features:

- PI74FCT151/251/2151T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2xxx Only)
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 16-pin 150-mil wide plastic QSOP (Q)
  – 16-pin 300-mil wide plastic SOIC (S)
  – 16-pin 150-mil wide plastic SOIC (W)

Product Description:

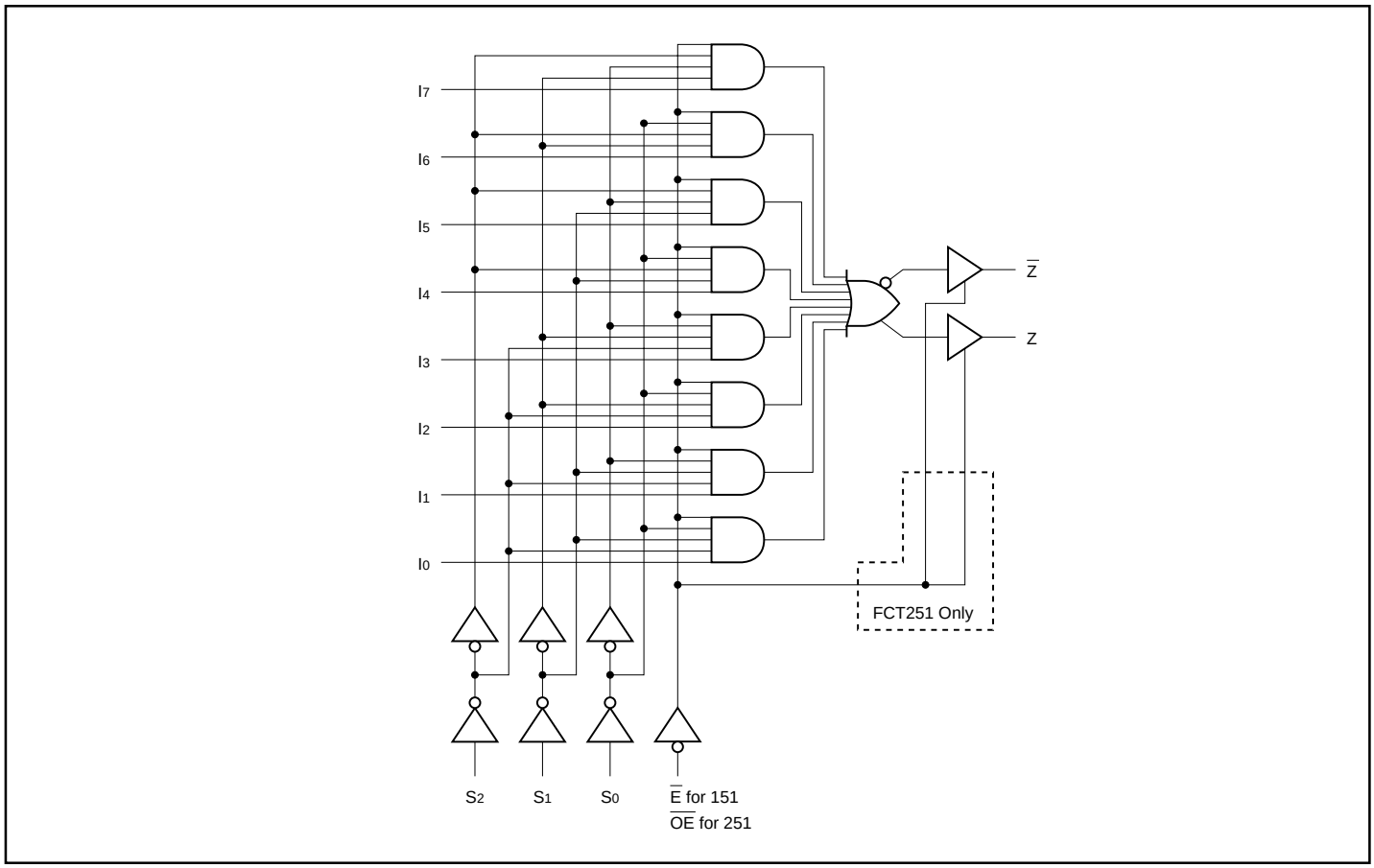
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT151T, PI74FCT251T, and PI74FCT2151T are high-speed 8-input multiplexers. They select one bit from a source of eight under the control of three select inputs. Both assertion and negation outputs are provided.

The PI74FCT151/2151T has a common, active-LOW, Enable input ($\overline{E}$). When $\overline{E}$ is LOW, data from one of eight inputs is directed to the complementary outputs based on the 3-bit code applied to the Select (S_0-S_2) inputs. The PI74FCT151/2151T can be used as a data routing device from one of eight sources.

The PI74FCT251T has a common Active-LOW Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, data from one of eight inputs is directed to the complementary outputs. When $\overline{OE}$ is HIGH, both outputs are switched to a high-impedance state allowing multiplexer expansion by tying several outputs together.

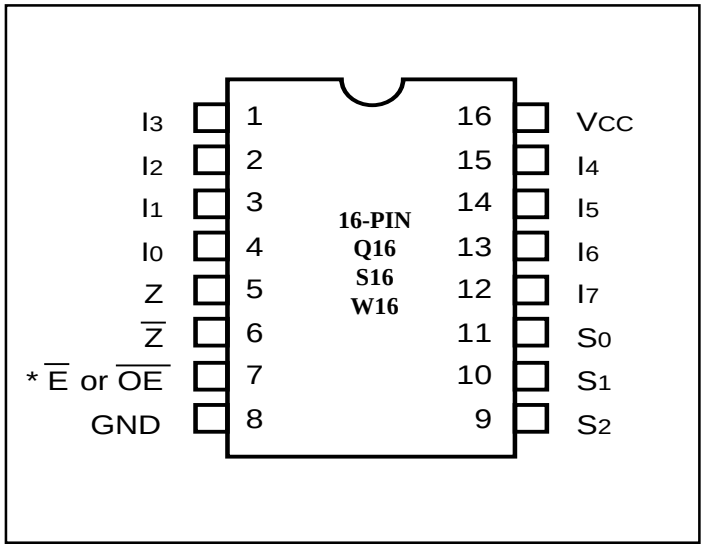
Logic Block Diagram



Product Pin Description

Pin Name	Description
I_0-I_7	Data Inputs
S_0-S_2	Select Inputs
$\overline{E}$	Enable Input (Active LOW) FCT151/2151T
$\overline{OE}$	Output Enable (Active LOW) FCT251T
Z	Data Output
$\overline{Z}$	Inverted Data Output
GND	Ground
V_{CC}	Power

PI74FCT151/2151T Product Pin Configuration



* $\overline{E}$ for 151/2151 only, $\overline{OE}$ for 251 only

Truth Table(1)

Inputs				Outputs	
S_2	S_1	S_0	$\overline{E}/\overline{OE}$(2)	Z	$\overline{Z}$
X	X	X	H	L(3)	H(3)
X	X	X	H	Z(4)	Z(4)
L	L	L	L	I_0	$\overline{I_0}$
L	L	H	L	I_1	$\overline{I_1}$
L	H	L	L	I_2	$\overline{I_2}$
L	H	H	L	I_3	$\overline{I_3}$
H	L	L	L	I_4	$\overline{I_4}$
H	L	H	L	I_5	$\overline{I_5}$
H	H	L	L	I_6	$\overline{I_6}$
H	H	H	L	I_7	$\overline{I_7}$

Notes:
1. $\overline{E}$ for 151/2151, $\overline{OE}$ for 251.
2. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
3. 151/2151 ONLY.
4. 251 ONLY.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.3	0.50	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA (25Ω series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_I = 10 MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		3.2	6.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		3.5	7.5[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT151/2151T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	151T/2151T Com. Min	151T/2151T Com. Max	151AT/2151AT Com. Min	151AT/2151AT Com. Max	151CT/2151CT Com. Min	151CT/2151CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$	C_L = 50 pF R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to Z		1.5	10.5	1.5	6.8	1.5	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		1.5	7.0	1.5	5.6	1.5	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		1.5	9.5	1.5	5.8	1.5	5.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		1.5	6.5	1.5	5.2	1.5	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		1.5	7.5	1.5	5.5	1.5	4.7	ns

PI74FCT251T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	251T Com. Min	251T Com. Max	251AT Com. Min	251AT Com. Max	251CT Com. Min	251CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$	C_L = 50 pF R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to Z		1.5	11.0	1.5	6.8	1.5	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		1.5	7.0	1.5	5.2	1.5	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		1.5	7.0	1.5	5.5	1.5	4.7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{Z}$		1.5	9.0	1.5	6.7	1.5	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to $\overline{Z}$		1.5	7.5	1.5	6.0	1.5	5.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z		1.5	9.0	1.5	6.7	1.5	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Z		1.5	7.0	1.5	6.0	1.5	5.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.