12-Bit To 24-Bit Registered Bus Exchanger with 3-State Outputs

Product Features

- PI74ALVCH16270 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce)
  < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
  < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-STATE, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)

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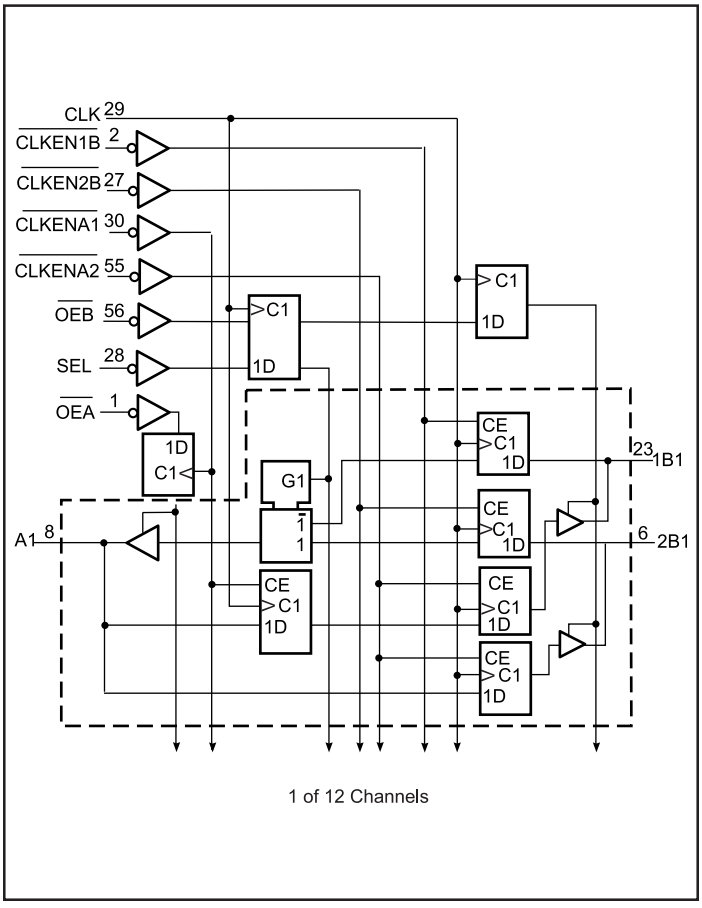
Logic Block Diagram



Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI7ALVCH16270 is used in applications where data must be transferred from a narrow high-speed bus to a wider lower frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate $\overline{\text{CLKEN}}$ inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two stage pipeline is provided in the A-to1B path,with a single storage register in the A-to-2B path. Proper control of the $\overline{\text{CLKENA}}$ inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit on the B port. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$). The control terminals are registered to synchronize the bus direction changes with the CLK.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to Vcc through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to $\overline{\text{OE}}$ being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock
$\overline{SEL}$	Select (Active Low)
$\overline{CLKEN}$	Clock Enable (Active Low)
A,1B,2B	3-State Outputs
GND	Ground
VCC	Power

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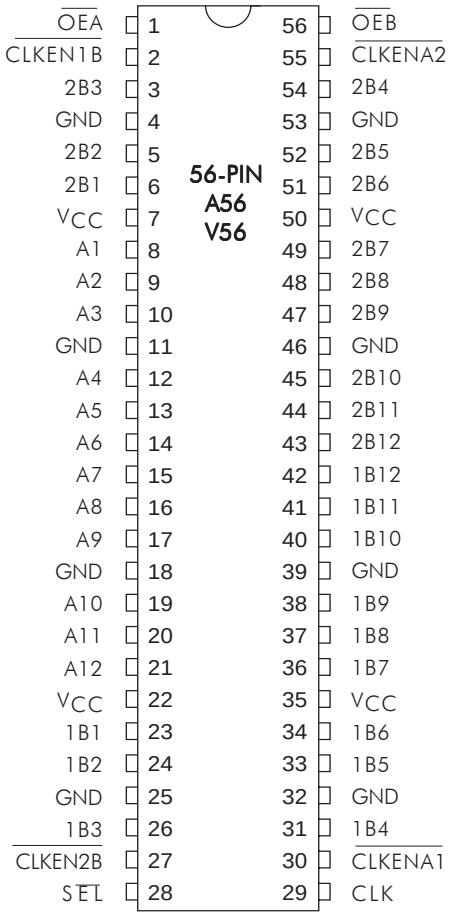
Product Pin Configuration



Truth Tables[1]

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A to B Storage ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	X	X	$1B0^{(3)}$	$2B0^{(3)}$
L	H	X	X	$1B0^{(3)}$	$2B0^{(3)}$
L	L	↑	L	$L^{(2)}$	L
L	L	↑	H	$H^{(2)}$	H
H	L	↑	L	$1B0^{(3)}$	L
H	L	↑	H	$1B0^{(3)}$	H
H	H	X	X	$1B0^{(3)}$	$2B0^{(3)}$

B to A Storage ($\overline{OEA}$ = L)

Inputs						Outputs A
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	SEL	1B	2B	
H	X	X	H	X	X	$A0^{(3)}$
X	H	X	L	X	X	$A0^{(3)}$
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

Notes:
1. H = High Signal Level
   L = Low Signal Level
   X = Irrelevant
   Z = High Impedance
   ↑ = Transition, Low to High
2. Two CLK edges are needed to propagate data.
3. Output level before the indicated steady state input conditions were established.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Input Voltage Range, V_{IN}	–0.5V to V_{CC} +0.5V
Output Voltage Range, V_{OUT}	–0.5V to V_{CC} +0.5V
DC Input Voltage	–0.5V to +5.0V
DC Output Current	100 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 10%)

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Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}(3)	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}(3)	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}(3)	Input Voltage		0		V_{CC}	
V_{OUT}(3)	Output Voltage		0		V_{CC}	
V_{OH}	Output HIGH Voltage	I_{OH} = -100µA, V_{CC} = Min. to Max.	V_{CC} -0.2			
		V_{IH} = 1.7V, I_{OH} = -6mA, V_{CC} = 2.3V	2.0			
		V_{IH} = 1.7V, I_{OH} = -12mA, V_{CC} = 2.3V	1.7			
		V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 2.7V	2.2			
		V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 3.0V	2.4			
		V_{IH} = 2.0V, I_{OH} = -24mA, V_{CC} = 3.0V	2.0			
V_{OL}	Output LOW Voltage	I_{OL} = 100µA, V_{IL} = Min. to Max.			0.2	
		V_{IL} = 0.7V, I_{OL} = 6mA, V_{CC} = 2.3V			0.4	
		V_{IL} = 0.7V, I_{OL} = 12mA, V_{CC} = 2.3V			0.7	
		V_{IL} = 0.8V, I_{OL} = 12mA, V_{CC} = 2.7V			0.4	
		V_{IL} = 0.8V, I_{OL} = 24mA, V_{CC} = 3.0V			0.55	
I_{OH}(3)	Output HIGH Current	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}(3)	Output LOW Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	

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DC Electrical Characteristics-Continued (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ±10%)

Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
I_{IN}	Input Current	V_{IN} = V_{CC} or GND, V_{CC} = 3.6V			±5	μA
I_{IN} (HOLD)	Input Hold Current	V_{IN} = 0.7V, V_{CC} = 2.3V	45			
		V_{IN} = 1.7V, V_{CC} = 2.3V	-45			
		V_{IN} = 0.8V, V_{CC} = 3.0V	75			
		V_{IN} = 2.0V, V_{CC} = 3.0V	-75			
		V_{IN} = 0 to 3.6V, V_{CC} = 3.6V			±500	
I_{OZ}	Output Current (3-STATE Outputs)	V_{OUT} = V_{CC} or GND, V_{CC} = 3.6V			±10	
I_{CC}	Supply Current	V_{CC} = 3.6V, I_{OUT} = 0μA, V_{IN} = GND or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = 3.0V to 3.6V One Input at V_{CC} - 0.6V Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	V_{IN} = V_{CC} or GND, V_{CC} = 3.3V		3.5		pF
C_O	Outputs	V_O = V_{CC} or GND, V_{CC} = 3.3V		9		

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Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

Timing Requirements over Operating Range

Parameters	Description		V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency		0	150	0	150	0	150	Mhz
t_W	Pulse duration, CLK HIGHor Low		3.3		3.3		3.3		ns
t_{SU}	Setup time	A data before CLK↑	4.1		3.8		3.1		
		B data before CLK↑	0.9		1.2		0.9		
		CLKENA1 or CLKENA2 before CLK↑	3.5		3.2		2.7		
		CLKEN1B or CLKEN2B before CLK↑	3.4		3		2.6		
		OE data before CLK↑	4.4		3.9		3.2		
t_H	Hold time	A data after CLK↑	0		0		0.2		
		B data after CLK↑	1.4		1		1.7		
		CLKENA1 or CLKENA2 before CLK↑	0		0.1		0.3		
		CLKEN1B or CLKEN2B before CLK↑	0		0		0.6		
		OE after CLK↑	0		0		0.1		
$\Delta t/\Delta V$(1)	Input Transition Rise or Fall		0	10	0	10	0	10	ns/V

Notes:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

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Switching Characteristics over Operating Range[1]

Parameters	From (INPUT)	To (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.[2]	
F_{MAX}			150		150		150		ns
	CLK	B	2	6.5		5.8	1.1	5.1	
	CLK	A	1.7	6		5.4	1	4.7	
t_{PD}	$\overline{SEL}$	A	1.9	6.8		6.4	1	5.5	
t_{EN}	CLK	A or B	1.6	7.5		6.8	1	6	
t_{DIS}	CLK	A or B	2.6	7.4		6.5	1.1	5.8	

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Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF, f = 10 MHz	87	120	pF
	Outputs Disabled		80.5	118	

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