

2.5V/3.3V, 500 MHz Twelve 2-to-1 Differential LVPECL Clock Multiplexer

Features

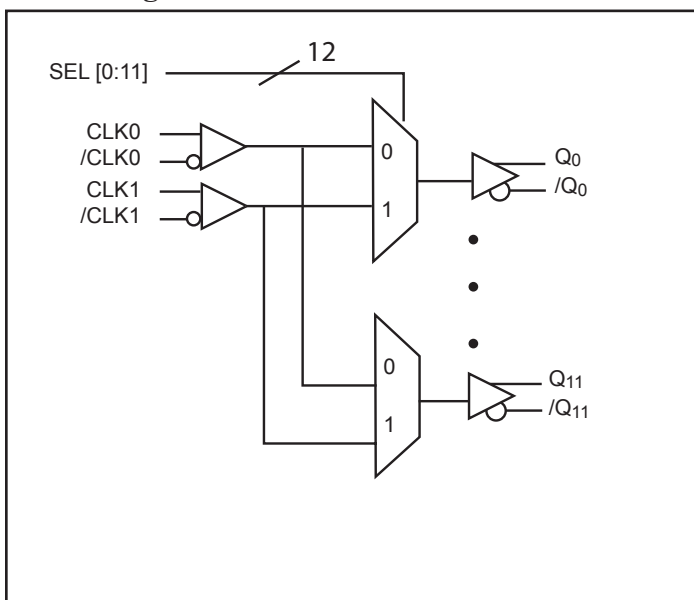
- Pin-to-pin compatible to ICS85352I
- $F_{MAX} \leq 500$ MHz
- Propagation Delay < 4 ns
- Output-to-output skew < 100 ps
- 12 pairs of differential LVPECL outputs
- Selectable differential CLK and /CLK inputs
- CLK, /CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- Select input accept CMOS/LVTTL levels
- 2.5V/3.3V power supply
- Operating Temperature: -40°C to $+85^{\circ}\text{C}$
- Packaging (Pb-free & Green):
— 48-pin TQFP (FA)

Description

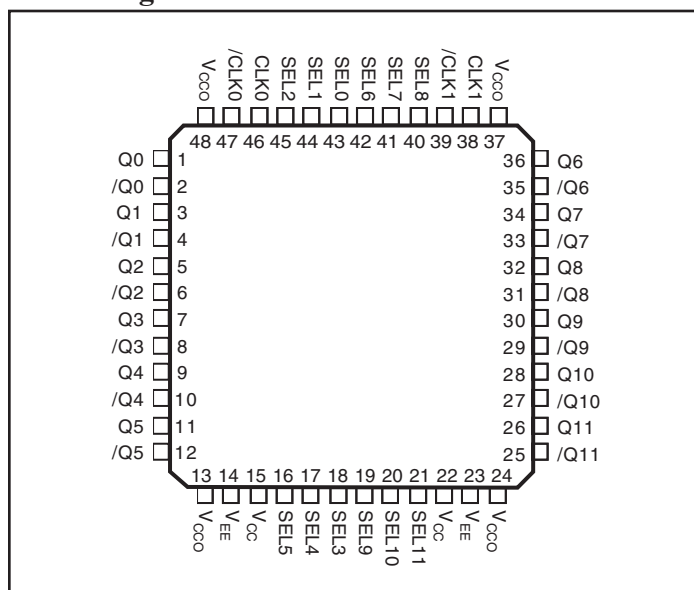
The PI6C485352 is a high-performance low-skew LVPECL fanout buffer. PI6C485352 features two selectable differential inputs and translates to twelve LVPECL output pairs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LVPECL, LVDS, LVHSTL, SSTL or HCSL signals. The PI6C485352 is ideal for differential to LVPECL translations and/or LVPECL clock distribution.

Typical clock translation and distribution applications are data-communications and telecommunications.

Block Diagram



Pin Configuration



Pin Description

Pin #	Name	Pullup/ Pulldown	Description
1, 2 3, 4 5, 6 7, 8 9, 10 11, 12 25, 26 27, 28 29, 30 31, 32 33, 34 35, 36	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 /Q11, Q11 /Q10, Q10 /Q9, Q9 /Q8, Q8 /Q7, Q7 /Q6, Q6		Differential LVPECL Output pairs. LVPECL interface levels
13, 24 37, 48	V _{CCO}		Output supply pins
14, 23	V _{EE}		Ground pins
15, 22	V _{CC}		Core supply pins
16, 17 18, 19 20, 21 40, 41 42, 43 44, 45	SEL5, SEL4, SEL3, SEL9, SEL10, SEL11, SEL8, SEL7, SEL6, SEL0, SEL1, SEL2	Pulldown	Clock select inputs. LVCMOS/LVTTL interface levels
38	CLK1	Pulldown	Non-inverting differential clock input
39	/CLK1	Pullup/ Pulldown	Inverting differential clock input.
46	CLK0	Pulldown	Non-inverting differential clock input
47	/CLK0	Pullup/ Pulldown	Inverting differential clock input.

Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{CC}	Supply voltage	Referenced to GND			4.6	V
V _{IN}	Input voltage	Referenced to GND	-0.5		V _{CC} +0.5V	
Outputs, I _O	Surge current				100	mA
T _{STG}	Storage temperature		-65		150	°C
θ _{JA}	Package thermal impedance				73	°C/W

Note:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C _{IN}	Input Capacitance				4	pF
R _{pullup}	Input Pullup Resistance			50		kΩ
R _{pulldown}	Input Pulldown Resistance			50		kΩ

Control Input Function Table

SELx	Selected Clock Inputs
0	CLK0, /CLK0
1	CLK1, /CLK1

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{CC}	Power Supply Voltage		3.0	3.3	3.6	V
V _{CCO}	Output Power Supply Voltage		2.375		3.6	V
T _A	Ambient Temperature		-40		85	°C
I _{EE}	Power Supply Current				200	mA

LVC MOS/LVTTL DC Characteristics (T_A = -40°C to +85°C, V_{CC} = 3.3V ±10%, V_{CCO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V _{IH}	Input High Voltage	SEL0:SEL11		2		V _{CC} +0.3	V
V _{IL}	Input Low Voltage	SEL0:SEL11		-0.3		0.8	
I _{IH}	Input High Current	SEL0:SEL11	V _{IN} = V _{CC} = 3.6V			150	μA
I _{IL}	Input Low Current	SEL0:SEL11	V _{IN} = 0V, V _{CC} = 3.6V	-5			μA

Differential DC Characteristics (T_A = -40°C to +85°C, V_{CC} = 3.3V ±10%, V_{CCO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I _{IH}	Input High Current	CLK0, CLK1	V _{IN} = V _{CC} = 3.6V			150	μA
		/CLK0, /CLK1	V _{IN} = V _{CC} = 3.6V			150	μA
I _{IL}	Input Low Current	CLK0, CLK1	V _{CC} = 3.6V, V _{IN} = 0V	-5			μA
		/CLK0, /CLK1	V _{CC} = 3.6V, V _{IN} = 0V	-150			μA
V _{PP}	Peak-to-peak Voltage			0.15		1.3	V
V _{CMR}	Common Mode Input Voltage ⁽¹⁾			V _{EE} +0.5		V _{CC} -0.85V	V

Note:

- For single ended applications, the maximum input voltage for CLK and /CLK is V_{CC}+0.3V

LVPECL DC Characteristics⁽¹⁾ ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$, $V_{CCO} = 2.5\text{V} \pm 5\%$ to $3.3\text{V} \pm 10\%$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{CC} = 3.6\text{V}$		150	μA
		/CLK0, /CLK1	$V_{IN} = V_{CC} = 3.6\text{V}$		150	μA
I_{IL}	Input Low Current	CLK0, CLK1	$V_{CC} = 3.6\text{V}$, $V_{IN} = 0\text{V}$	-5		μA
		/CLK0, /CLK1	$V_{CC} = 3.6\text{V}$, $V_{IN} = 0\text{V}$	-150		μA
V_{OH}	Output High Voltage ⁽²⁾	$V_{CCO} = 3.3\text{V}$ or 2.5V	$V_{CCO}-1.4$		$V_{CCO}-0.9$	V
V_{OL}	Output Low Voltage ⁽²⁾	$V_{CCO} = 3.3\text{V}$ or 2.5V	$V_{CCO}-2.0$		$V_{CCO}-1.7$	V

Notes:

- For single-ended applications, the maximum input voltage for CLK and /CLK is $V_{CC}+0.3\text{V}$.
- Outputs terminated with 50Ω to $V_{CCO}-2.0\text{V}$

AC Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$, $V_{CCO} = 2.5\text{V} \pm 5\%$ to $3.3\text{V} \pm 10\%$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{\max}$	Output Frequency				500	MHz
t_{pd}	Propagation Delay ⁽¹⁾				4	ns
T_{sk}	Output-to-output Skew ⁽²⁾				100	ps
T_{skpp}	Part-to-part Skew ⁽³⁾				500	ps
t_r/t_f	Output Rise/Fall time	20% - 80%	150		700	ps
odc	Output duty cycle		45		55	%

Notes:

- Measured from the differential input to the differential output crossing point
- Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point.
- Defined as skew between outputs on different parts operating at the same supply voltage and with equal loads. Measured at the outputs differential crossing point.

Applications Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be placed as close as possible to the input pin. The ratio of R1 and R2 should be adjusted to position the V_{REF} at the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R1/R2 = 0.609$.

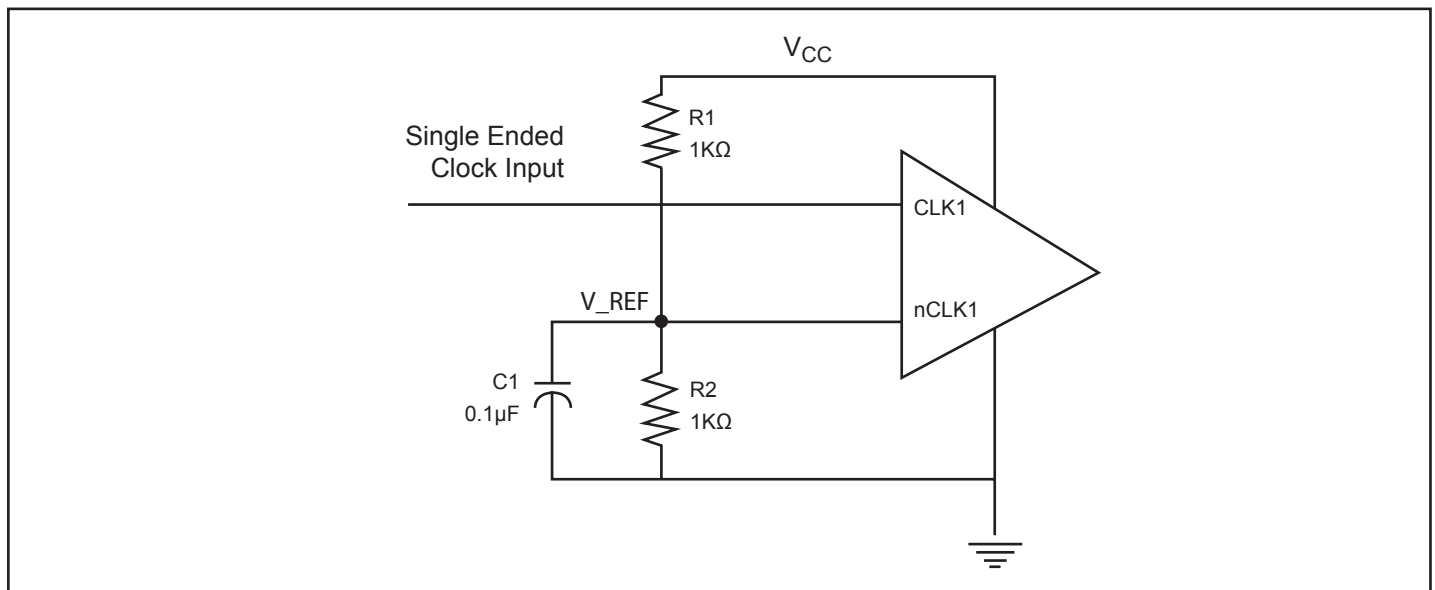
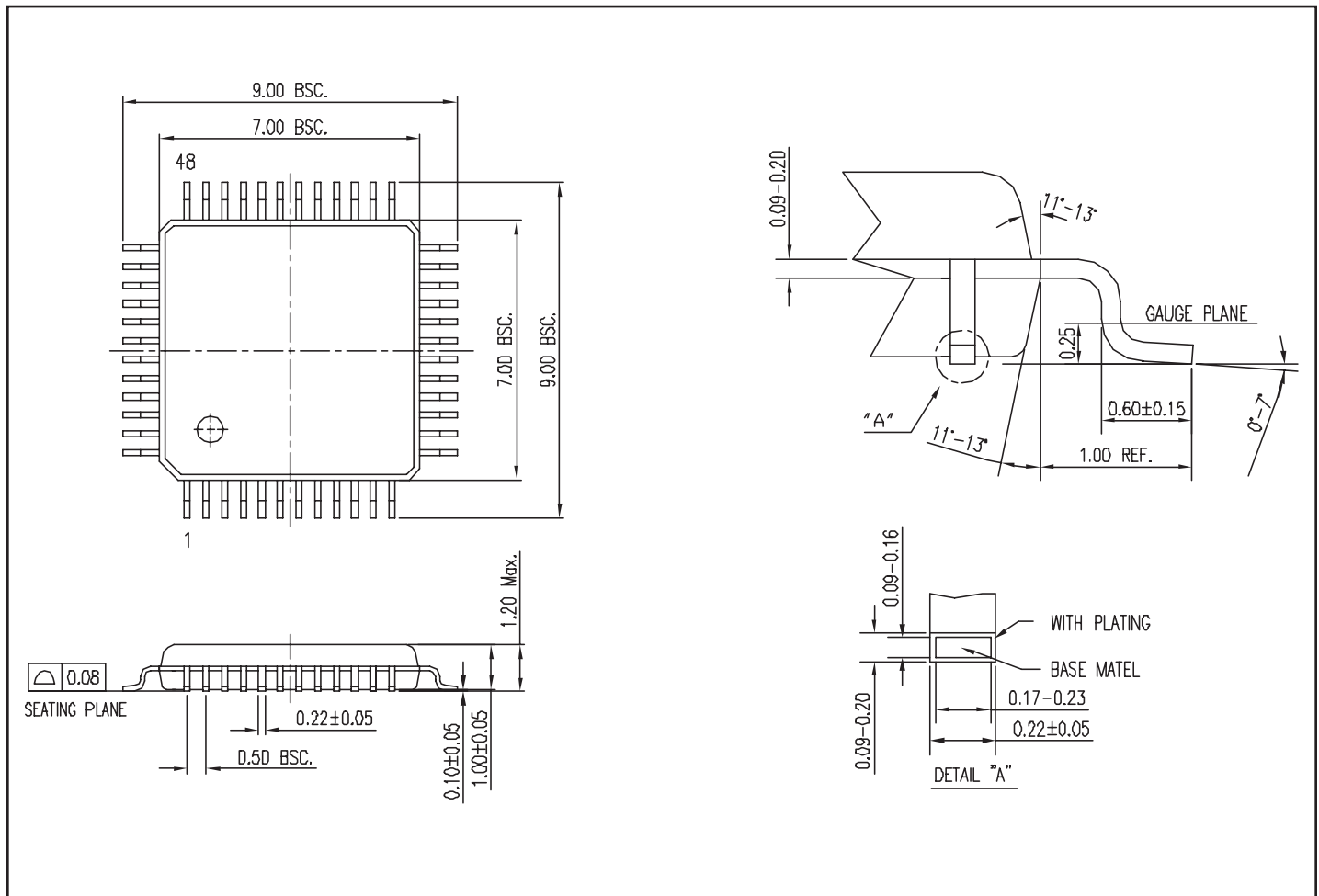


Figure 1: Single-ended Signal Driving Differential Input

Packaging Mechanical: 48-Pin TQFP (FA)



Ordering Information(1,2,3)

Ordering Code	Package Code	Package Description
PI6C485352FAE	FA	Pb-free & Green, 48-pin, 276-mil wide TQFP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X suffix = Tape/Reel