PERICOM®

PI3HDX412B

HDMI 1.4b Splitter/Demux 1:2 for 3.4Gbps Data Rate with Equalization & Pre-emphasis

Features

- **Support up to 3.4Gbps TMDS Serial Link**
- **HDMI 1-to-2 Splitter or 1-to-2 DeMux with Equalization & Pre-emphasis up to 340 MHz Clock**
- **AC or DC Coupled Differential Signaling Input**
- **Configurable TMDS Output Signal with Port Selection, Pre-emphasis, Voltage Swing, Slew Rate Control**
- **Support Squelch Mode with Built-in Clock detector for PI3HDX412BD and PI3HDX412BE**
- **Control Status Register controlled by Pin strap or I^2C mode programming**
- **ESD Protection on I/O pins to connector: 8KV contact per IEC6100-4-2 and 2KV HBM**
- **Supply Voltage: 3.3V±5%**
- **Industrial Temperature Range: -40°C to 85°C**
- **Packaging (Pb-free & Green): 56-contact TQFN (ZB56)**

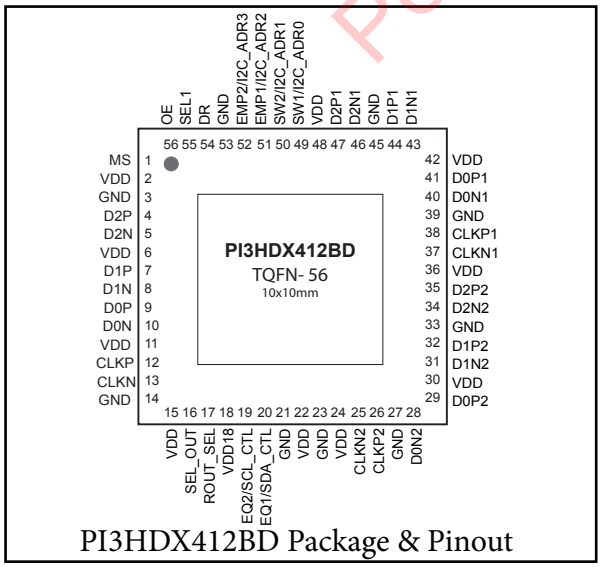
General Description

The device provides 1-to-2 HDMI 1.4b Active 3.4 Gbps splitter outputs and Demux features with programmable equalization, output voltage swing, pre-emphasis by setting either pin strapping option or I2C control, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

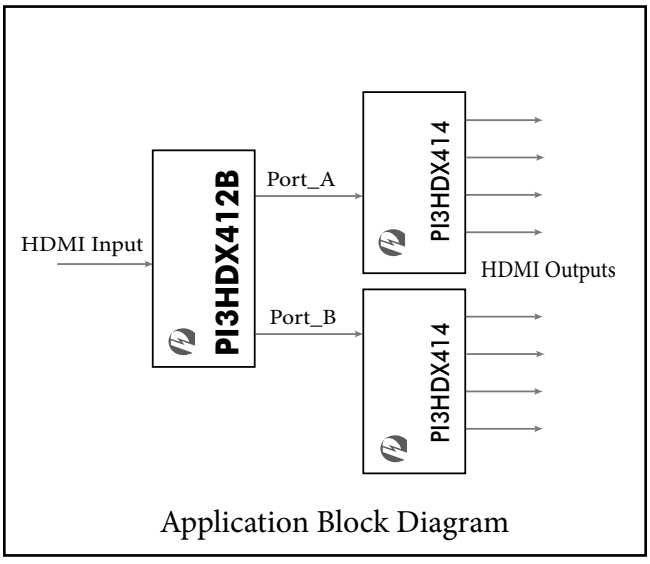
The integrated equalization circuitry provides flexibility with signal integrity of the signal before the high speed Demux, whereas the integrated pre-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

Applications

- HDMI Switches and Splitters
- Wall Screen Multi Display System
- Notebook Computer and Docking
- TV, Monitors and Set-top-Box

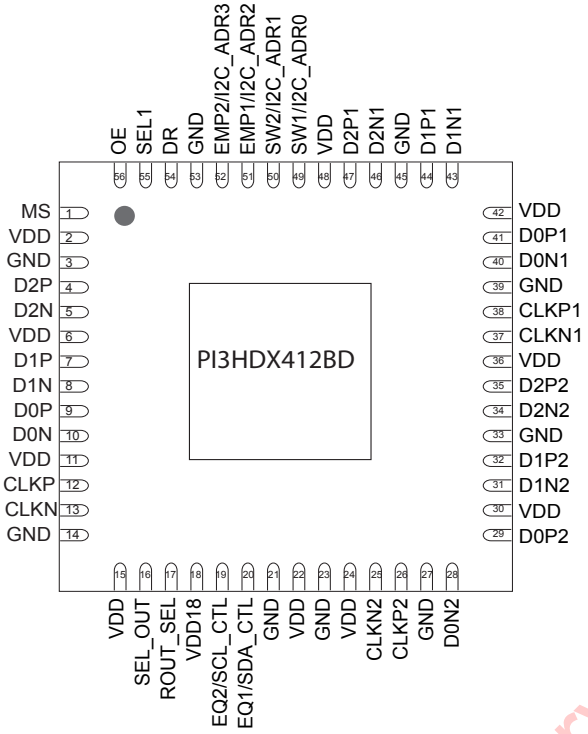


PI3HDX412BD Package & Pinout

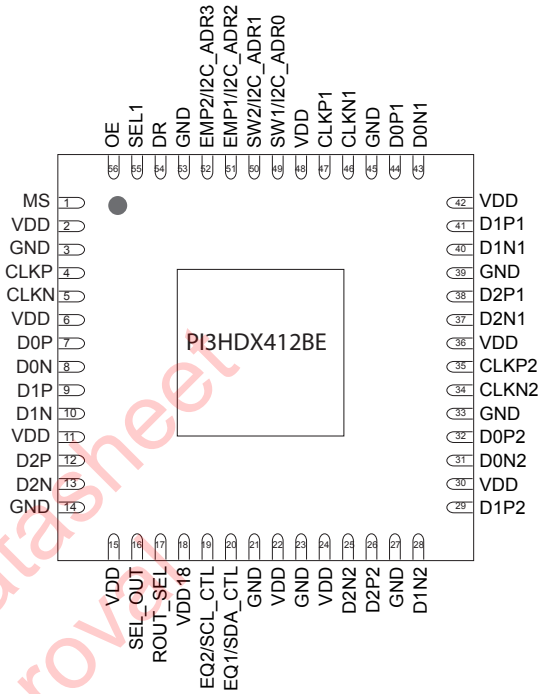


Application Block Diagram

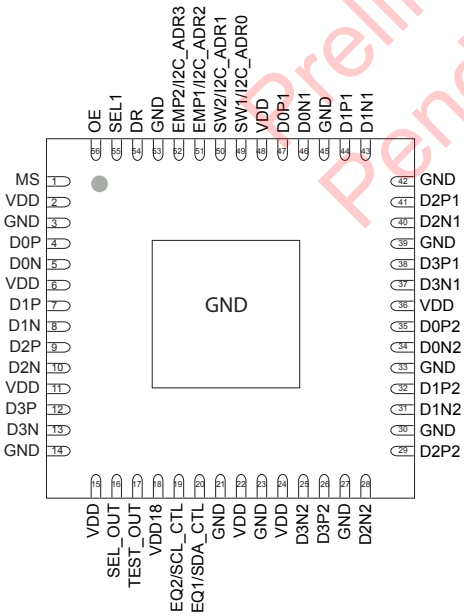
Pin Configuration Options



Note: PI3HDX412BD : Source(Double) Termination Type. TMDS CLK and Data order assignment for top-mount source side application



Note : PI3HDX412BE : Reversed TMDS CLK and Data Pin assignment of PI3HDX412BD for top mount sink-side system application



Note : PI3HDX412BO : Open Drain Output Type. No dedicated Clock and Data Pairs. Squelch Function does not support too.

PI3HDX412BD/ PI3HDX412BE/ PI3HDX412BO TMDS In/Out Pin Assignment

Pin #	PI3HDX-412BD	PI3HDX-412BE	PI3HDX-412BO	Type	Description
4	D2P	CLKP	D0P	I	TMDS CLK/Data inputs. When Input Termination Resistor (Rt = 50 Ohm) tied to VDD or GND; Rpd=200 kOhm shall be "OFF" state. I2C registers can control Rt and Rpd ON/OFF state.
5	D2N	CLKN	D0N	I	
7	D1P	D0P	D1P	I	
8	D1N	D0N	D1N	I	
9	D0P	D1P	D2P	I	
10	D0N	D1N	D2N	I	
12	CLKP	D2P	D3P	I	
13	CLKN	D2N	D3N	I	
25	CLKN2	D2N2	D3N2	O	Port 1 TMDS CLK/Data outputs. ROUT_SEL enables Output Termination Resistor (Rout=50 Ohm).
26	CLKP2	D2P2	D3P2	O	
28	D0N2	D1N2	D2N2	O	
29	D0P2	D1P2	D2P2	O	
31	D1N2	D0N2	D1N2	O	
32	D1P2	D0P2	D1P2	O	
34	D2N2	CLKN2	D0N2	O	
35	D2P2	CLKP2	D0P2	O	
37	CLKN1	D2N1	D3N1	O	Port 2 TMDS CLK/Data outputs. ROUT_SEL enables Output Termination Resistor (Rout=50 Ohm).
38	CLKP1	D2P1	D3P1	O	
40	D0N1	D1N1	D2N1	O	
41	D0P1	D1P1	D2P1	O	
43	D1N1	D0N1	D1N1	O	
44	D1P1	D0P1	D1P1	O	
46	D2N1	CLKN1	D0N1	O	
47	D2P1	CLKP1	D0P1	O	

Note: Pin Polarity P/N is always interchangeable in redriver. For example. Pins 4, 5, 47, 46, 35 and 34 of PI3HDX412BE can be assigned as CLKN, CLKP, CLKN1, CLKP1, CLKN2 and CLKP2, respectively.

Other Pin Assignment Difference

Pin	PI3HDX412BD & PI3HDX-412BE	PI3HDX412BO	PI3HDMI412AD (2.5Gbps 1:2 Splitter)
17	ROUT_SEL	TEST_OUT	TEST_OUT
18	VDD18	VDD18	NC
30	VDD	GND	GND
42	VDD	GND	GND

Control Pins

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>19</td><td>EQ2/SCL_CTL</td><td>IO</td><td>Shared Pin for EQ2 and I²C Clock, compatible with standard I²C-Bus Specification, up to 400 kb/s.
<table>
<tr><td>EQ2/SCL_CTL</td><td>Functional Description</td></tr>
<tr><td>MS="High"</td><td>Assign to SCL_CTL Pin</td></tr>
<tr><td>MS="Low"</td><td>Assign to EQ2 Pin</td></tr>
</table>
Internal Pull-Up at 100 kOhm and Pull-Down at 100 kOhm. Pin Control EQ ode setting is below. "M" is Tri-state.
<table>
<tr><th>MS
(Pin #1)</th><th>EQ2/SCL_CTL
(Pin# 19)</th><th>EQ1/SDA_CTL
(Pin# 20)</th><th>Equalization Setting
(dB)</th></tr>
<tr><td rowspan="9">"Low"</td><td>0</td><td>M</td><td>2.5</td></tr>
<tr><td>0</td><td>0</td><td>5</td></tr>
<tr><td>M</td><td>0</td><td>7.5</td></tr>
<tr><td>0</td><td>1</td><td>10</td></tr>
<tr><td>M</td><td>M</td><td>12.5</td></tr>
<tr><td>1</td><td>0</td><td>15</td></tr>
<tr><td>1</td><td>M</td><td>17.5</td></tr>
<tr><td>1</td><td>1</td><td>20</td></tr>
</table></td></tr>
<tr><td>20</td><td>EQ1/SDA_CTL</td><td>IO</td><td>Shared Pin for EQ1 and I²C Data, compatible with I²C-Bus Specification, up to 400 kb/s. Internal Pull-Up at 100 kOhm and pull-down at 100 kOhm. Please refer to Pin# 19 Equalization setting table.</td></tr>
<tr><td>49
50
51
52</td><td>SW1/I2C_ADR0
SW2/I2C_ADR1
EMP1/I2C_ADR2
EMP2/I2C_ADR3</td><td>I</td><td>Shared Pin for SW/EMP or I2C_ADR pins.
<table>
<tr><td>Pin #49,#50,#51,#52</td><td>Functional Description</td></tr>
<tr><td>When MS="High"</td><td>These Shared Pins assign to I2C_ADR[3:0]</td></tr>
<tr><td>When MS="Low"</td><td>These Shared Pins assign to SW1/2 and EMP1/2</td></tr>
</table>
These SW2 and SW1 do voltage swing control adjustment as following. These pins have internal Pull-Up at 100K Ohm.
<table>
<tr><td>SW2 (#50)</td><td>SW1 (#49)</td><td>Voltage Swing Setting</td></tr>
<tr><td>0</td><td>0</td><td>500 mV</td></tr>
<tr><td>0</td><td>1</td><td>-10 %</td></tr>
<tr><td>1</td><td>0</td><td>+10 %</td></tr>
<tr><td>1</td><td>1</td><td>+20 %</td></tr>
</table></td></tr>
</table>

Pin #	Pin Name	Type	Description
49 50 51 52	(Continued)	I	These EMP2 and EMP1 pin configuration do pre-emphasis control as following. These pins have internally Pull-Up at 100K Ohm. EMP2 (#52) / EMP1 (#51) / Pre-emphasis Setting (dB) 0 / 0 / 0 0 / 1 / 1.5 1 / 0 / 2.5 1 / 1 / 3.5
1	MS	I	Mode Selection Pin. Internal pull-up at 100K Ohm. MS (Pin#1) / Functional Description When "High" / I^2C Control Mode When "Low" / Pin Control Mode
56	OE	I	Output Enable Control Pin. Internal pull-up at 100K Ohm. OE / Functional Description When "High" / Output Port Enable When "Low" / Turn off Rout and Rt(termination resistor). TMDS Receiver and TMDS Output Drivers are "OFF" state.
54	DR	I	Direction Control Pin DR / Functional Description When "High" / All ports are Active at same time When "Low" / Output Ports are controlled by SEL1 (Pin#55) control. Please refer SEL1 pin definition
55	SEL1	I	Port 1 or 2 Output Enable pin. Internal pull-up at 100K Ohm. SEL1 / Functional Description When "High" / Enable Output Port 2 When "Low" / Enable Output Port 1
16	SEL_OUT	O	SEL_OUT is control by I^2C Register Offset 0x00 Bit[5] Offset 0x00 Bit[5] / Functional Description When b[5] = "1" / Enable Port 1 Output When b[5] = "0" / Disable Port 1 Output

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="2">17*</td><td>TEST_OUT
(with PI3HDX-412BO)</td><td>O</td><td>TEST_OUT is controlled by I²C Register Offset 0x00 Bit[4]
<table><tr><td>Offset 0x00 Bit<4></td><td>Functional Description</td></tr><tr><td>When b[4] = "1"</td><td>Enable Port 2 Output</td></tr><tr><td>When b[0] = "0"</td><td>Disable Port 2 Output</td></tr></table></td></tr>
<tr><td>ROUT_SEL
(with PI3H-DX412BD and PI3HDX412BE)</td><td>I</td><td>Source termination selection pin. Internal pull-up at 100K Ohm.
<table><tr><td>ROUT_SEL</td><td>Functional Description</td></tr><tr><td>When "High"</td><td>Source Termination Output (Rout) Resistor "ON", connect to VDD in Output Driver</td></tr><tr><td>When "Low"</td><td>Source Termination Output (Rout) Resistor "OFF". Output Driver works as Open Drain</td></tr></table></td></tr>
</table>

* Note: Shared Pin with Bonding Option.

Power/Ground Pins

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>18</td><td>VDD18</td><td>Power</td><td>LDO Output Pin for internal core supplier. Add external 4.7 uF capacitor to GND</td></tr>
<tr><td>3,14,21,23,27,33,39,45,53</td><td>GND</td><td>Ground</td><td>Ground Pins</td></tr>
<tr><td>30,42</td><td>GND/VDD</td><td>Ground/ Power</td><td>3.3V Power Supply or Ground. Please see below table.
<table><tr><td>Part Number</td><td>Pin #</td><td>Description</td></tr><tr><td>PI3HDX412BO</td><td>30,42</td><td>Ground</td></tr><tr><td>PI3HDX412BD/BE</td><td>30,42</td><td>3.3V Power Supply</td></tr></table></td></tr>
</table>

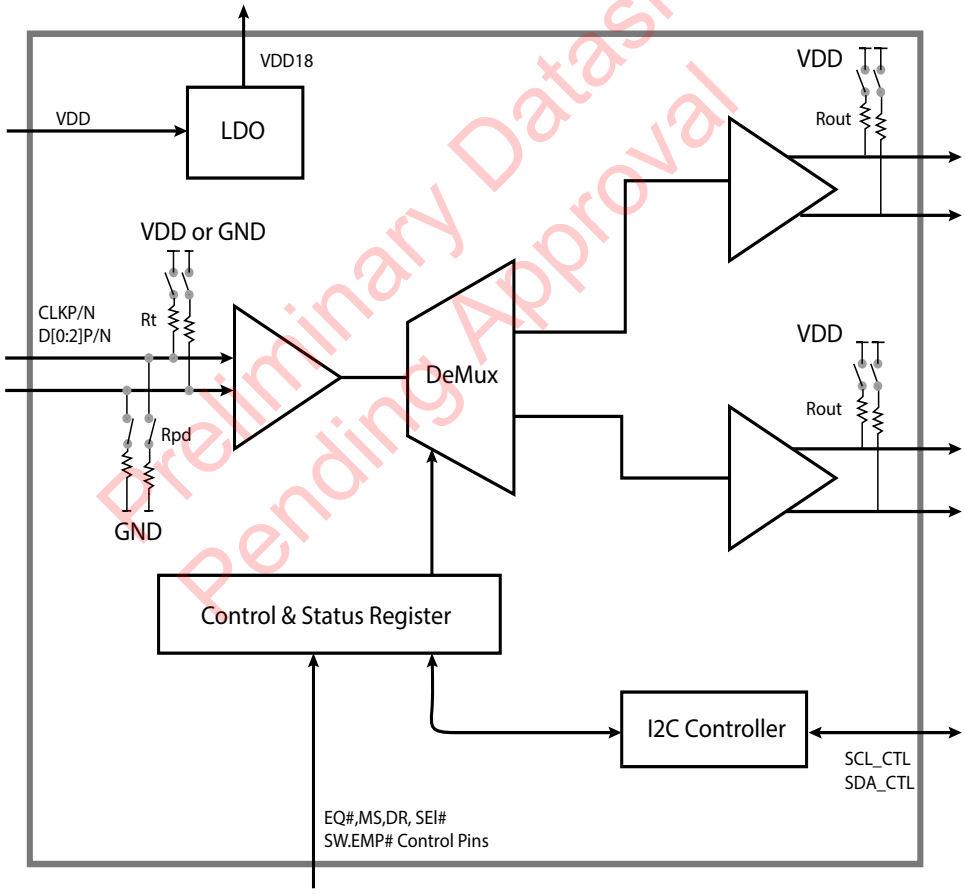
Functional Description

Output Disable(Squelch) Mode

Output Disable(Squelch) Mode uses CLK channel signal detection. When low-signal levels on the source TMDS(Main Link) input are sensed(a squelch event), a transition to this state occurs and TMDS D [0:2]P/N signals are disable; when the source TMDS(Main Link) input signal levels are above a pre-determined threshold, a transition back to the appropriate active mode occurs.

In squelch state, TMDS output is set to "high impedance at TMDS open drain output" or "pull-up to VDD by internal 50 Ohm resistor at TMDS double termination output".

Squelch is enabled as default setting. Enable squelch mode means input termination resistor is enabled. When squelch is disable in RX_SET[1]="1", TMDS D[0:2]P/N will be unknown during no TMDS input signals.



I²C Configuration Register

Pin Name	I/O	Description
SCL_CTL	I	I2C Clock, compatible with I2C-bus specification, up to 400 kb/s
SDA_CTL	IO	I2C Data, compatible with I2C-bus specification, up to 400 kb/s
I2C_ADR[3:0]	I	I2C Control Address Setting
Byte output : 0x00 - 0x07	O	I2C Control registers output (there are 10 Byte register in base)

I²C Address Byte

	b[7] MSB	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (R/W)
Address Byte	1	0	1	A3	A2	A1	A0	1/0*

Note: Read "1", Write "0"

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th><th>Power Up Condition</th><th>Type</th></tr>
<tr><td>0x00</td><td>CONFIG[7:0]</td><td>[7] Enable Standby. In standby mode, TMDS equalizer and output driver are powered down.
"0": Standby mode
"1": Normal mode
[6] Reserved
[5] Port 1 Select
"0": Disable
"1": Active
[4] Port 2 Selected
"0": Disable
"1": Active
[3] Reserved
[2:0] Reserved</td><td>0xFF</td><td>R/W</td></tr>
<tr><td>0x01</td><td>RX_SET[7:0]</td><td>Receiver Equalization setting
[7] Disable port termination resistors
"0" = Rpd connected
"1" = Rpd disconnected
[6] TMDS input termination V-bias selection
"0": Connect to GND (default)
"1": Connect to VDD
[5] V-bias register selection enable
"0": bit[6] control disable (as default)
"1": bit[6] control enable
[4:2] EQ programmable setting
<table><tr><th>b[4:2]</th><th>EQ Setting (dB)</th></tr><tr><td>000</td><td>2.5</td></tr><tr><td>001</td><td>5</td></tr><tr><td>010</td><td>7.5</td></tr><tr><td>011</td><td>10</td></tr><tr><td>100</td><td>12.5</td></tr><tr><td>101</td><td>15</td></tr><tr><td>110</td><td>17.5</td></tr><tr><td>111</td><td>20</td></tr></table>[1] Squelch disable
"0": Squelch enable (as default)
"1": Squelch disable
[0] Reserved</td><td>0x00</td><td>R/W</td></tr>
<tr><td>0x02</td><td>Reserved</td><td>[7:0] Reserved</td><td>0x00</td><td>R/W</td></tr>
</table>

Offset	Name	Description	Power Up Condition	Type
0x03	TX_SET[7:0] for port1	TMDS output setting for PI3HDX412BD,-BE [7] TMDS output control "0": Open drain "1": Double termination [6:4] TMDS output Pre-emphasis control "000": 0 dB "001": 1.5 dB "010": 2.5 dB "011": 3.5 dB "1xx": 6 dB (750 mVpp swing) [3:2] Reserved by test only TMDS output swing setting "00": 500 mV as default "01": -10% "10": +10% "11": +20% [1:0] Reserved by test adjust TMDS output slew rate setting "00": as default "01" / "10": + 5% "11": +10%	0x00	R/W
0x04	TX_SET[7:0] for port2	TMDS output setting for PI3HDX412BD, -BE [7] TMDS output control "0": Open drain "1": Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only TMDS output swing setting "00" : 500 mV as default setting "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust TMDS output slew rate setting "00" : Default setting "01" / "10" : + 5% "11" : +10%	0x00	R/W
0x05	Reserved	[7:0] Reserved	0x00	R/W
0x06	Reserved	[7:0] Reserved	0x0F	R/W
0x07	Reserved	[7:0] Reserved	0x00	R/W

Maximum Ratings

Supply Voltage to Ground Potential 3.6V
DC SIG Voltage . . . . . –0.5V to V_{DD}+0.5V
DC Output Current . . . . . TBD
Power Dissipation Continuous . . . . . TBD
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . -40 to +85°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Characteristics

Symbol	Parameter	Ratings	Units
T_{Jmax}	Junction Temperature	125	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	24	

Electrical Characteristics T_J=25 °C unless otherwise noted

DC Specifications VDD=3.3V +/- 10%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Operation Voltage		3.0	3.3	3.6	V
I_{DD}	VDD Supply Current			TBD		mA
I_{DDQ}	VDD Quiescent Current	OE = 1, No input signal		15		mA
I_{STB}	Standby mode	OE = 0		6		mA
TMDS Differential Pins						
VOH	Single-ended high level output voltage	VDD = 3.3 V, Rout=50 Ω	VDD-10		VDD+10	mV
VOL	Single-ended low level output voltage		VDD-600		VDD–400	mV
Vswing	Single-ended output swing voltage		400		600	mV
VOD(O)	Overshoot of output differential voltage				180	mV
VOD(U)	Undershoot of output differential voltage				200	mV
VOC(SS)	Change in steady-state common- mode output voltage between logic states				5	mV
IOS	Short Circuit output current		-12		12	mA
IOS	Short Circuit output current at double termination mode		-24		24	mA

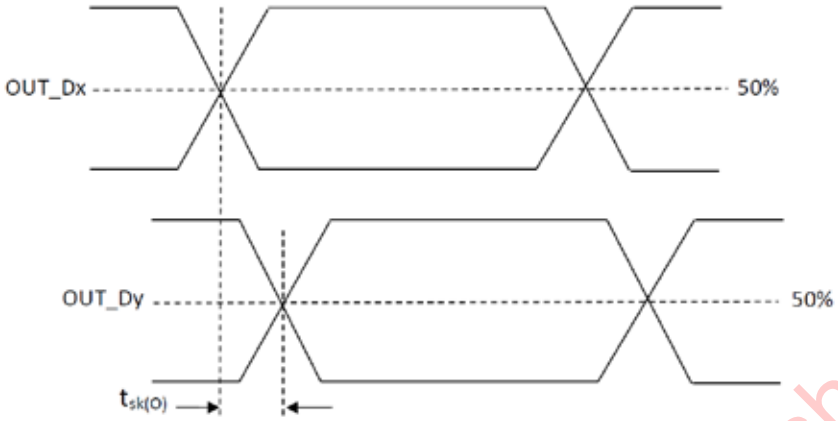
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VI(open)	Single-ended input voltage under high impedance input or open input	IL = 10 uA	VDD-10		VDD+10	mV
RT	Input termination resistance	VIN = 2.9 V	45	50	55	Ohm
IOZ	Leakage current with Hi-Z I/O	VDD = 3.6 V, OE = 0		30	100	µA
Control pins (OE, SEL1, EMP2, EMP1, SW2, SW1, MS)						
I_{IH}	High level digital input current	V_{IH} =V_{DD}	-10		10	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-50		10	µA
V_{IH}	High level digital input voltage		2.4			V
V_{IL}	Low level digital input voltage		0		0.8	V

AC Specifications

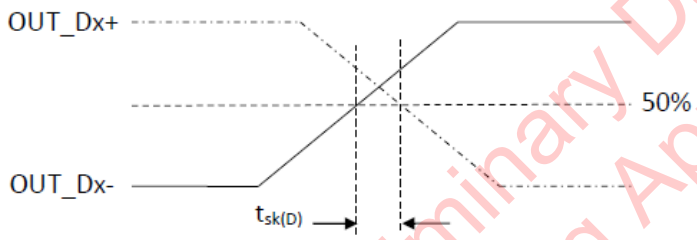
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
tpd	Propagation delay				2000	ps
tr	Differential output signal rise time (20% - 80%), 0 dB / Open drain	VDD=3.3V, ROUT=50 ohm		117		ps
tf	Differential output signal fall time (20% - 80%), 0 dB / Open drain			117		ps
tsk(p)	Pulse skew			15	50	ps
tsk(D)	Intra-pair differential skew			25	50	ps
tsk(O)	Inter-pair differential skew				100	ps
tSX	Select to switch output				50	ns
ten	Enable time				600	ns
tdis	Disable time				50	ns
tjit_clk(pp)	Peak-to-peak output jitter CLK residual jitter	Data: 3.4 Gbps data pattern Clock: 340 MHz		10		ps
tjit_data(pp)	Peak-to-peak output jitter Date residual jitter			28		ps

Note:
1. Overshoot of output differential voltage $V_{OD(O)}$ = ($V_{SWING(MAX)}$ *2) * 15%
2. Undershoot of output differential voltage $V_{OD(O)}$ = ($V_{SWING(MIN)}$ *2) * 25%

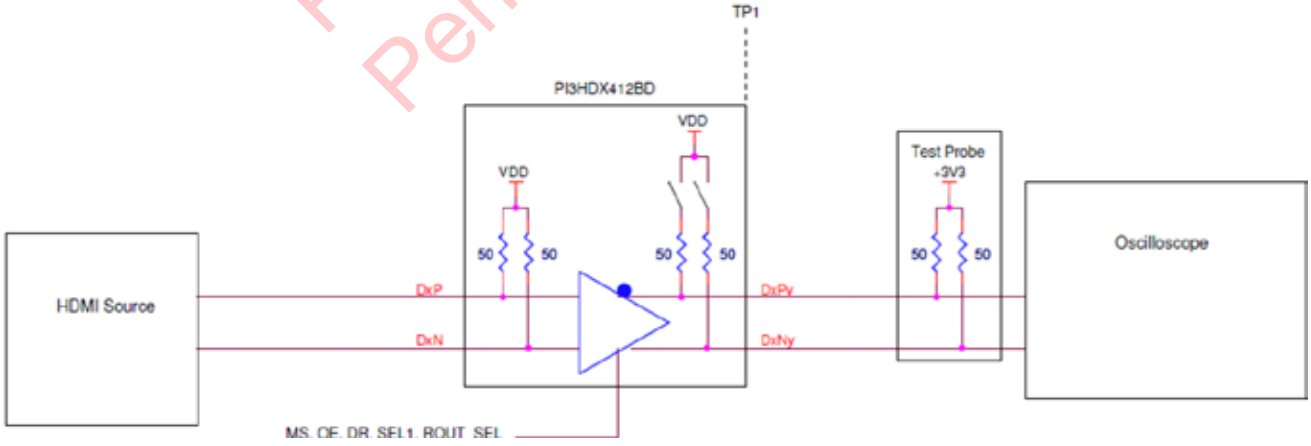
Inter-pair Skew Definition



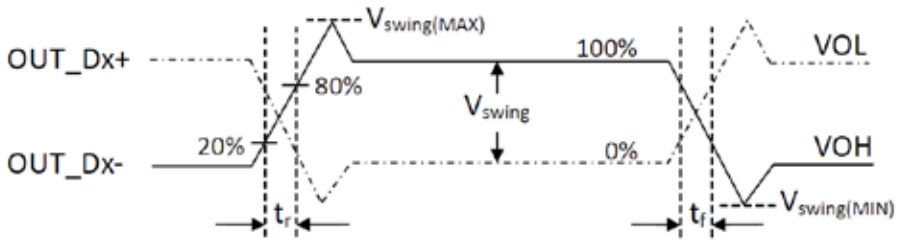
Intra-pair Skew Definition



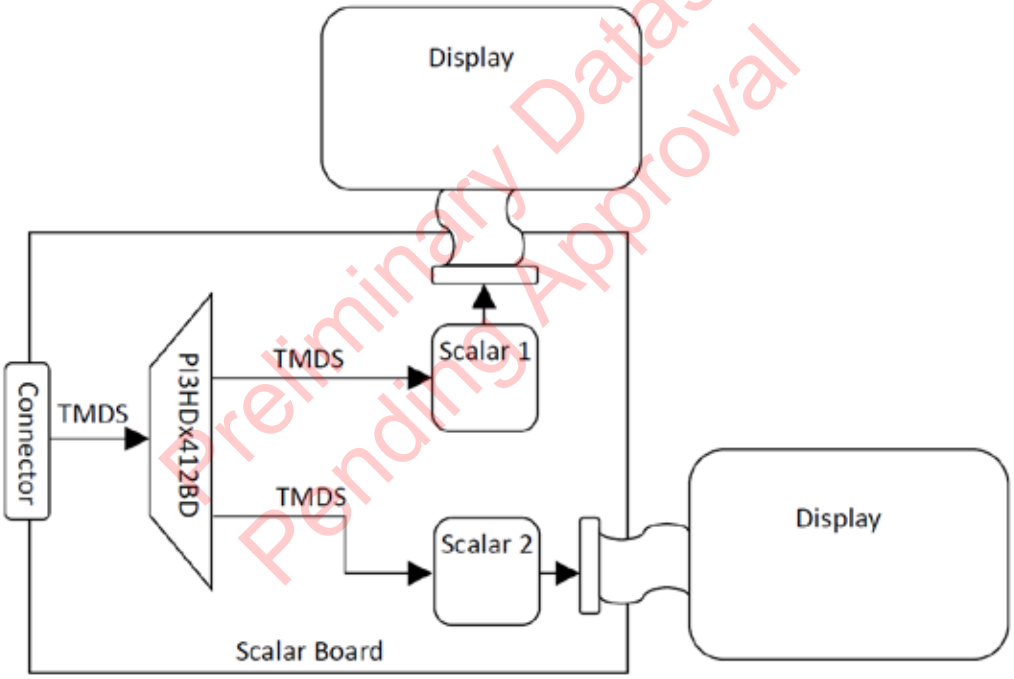
Test Setup of DC-coupled TMDS Input Measurement



Rise/Fall Time and Single-ended Swing Voltage

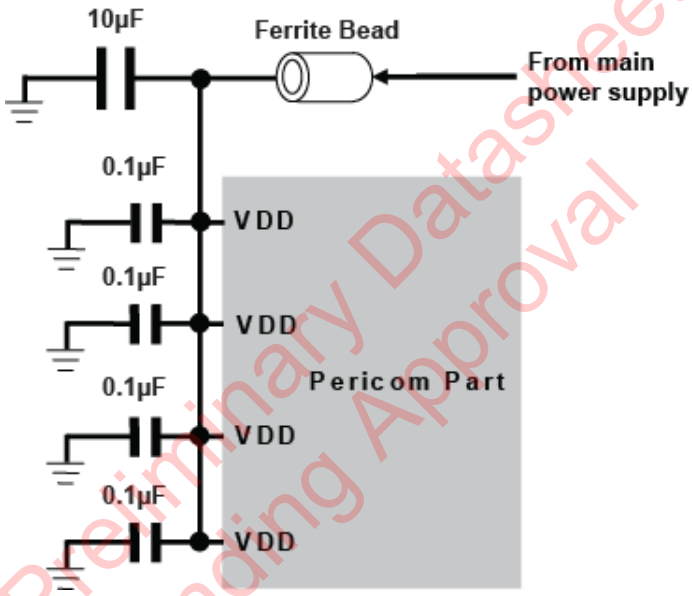


Typical Splitter Application



Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



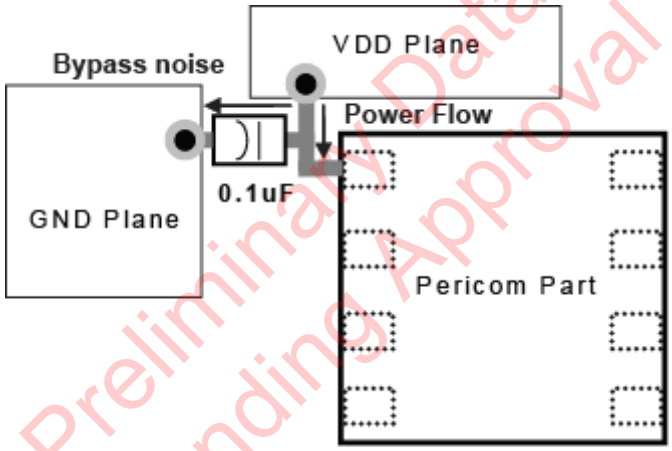
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the De-coupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

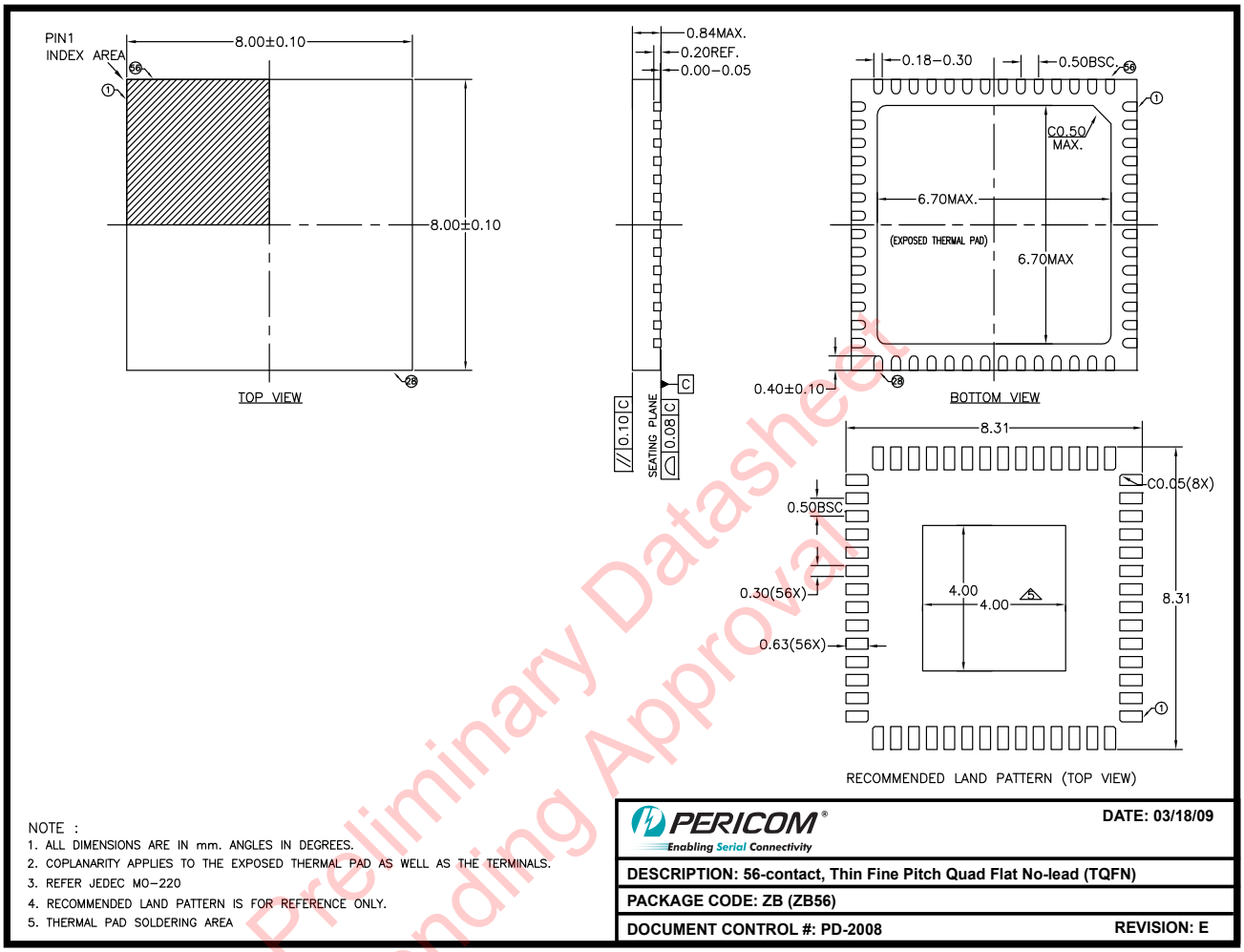
Layout and Decoupling Capacitor Placement Consideration

- Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- VDD and GND planes should be used to provide a low impedance path for power and ground.
- Via holes should be placed to connect to VDD and GND planes directly.
- Trace should be as wide as possible
- Trace should be as short as possible.
- The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



Decoupling Capacitor Placement Diagram

Package Mechanical: 56-pad, TQFN (ZB56)



Note:
For latest package info, please check: http://www.pericom.com/products/packaging

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDX412BDZBE	ZB	56-pin, Pb-free & Green TQFN, Source Termination Type
PI3HDX412BEZBE	ZB	56-pin, Pb-free & Green TQFN, Source Termination Type
PI3HDX412BOZBE	ZB	56-pin, Pb-free & Green TQFN, Open Drain Type

Notes:
Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
PI3HDX412B : Root Part Number
-D/E : D= Source Termination TMDS Top Mount Type, E = Source Termination TMDS Bottom Mount Type
-ZB = 56-pin TQFN Package Type
-E = Pb-free and Green
Adding an -X Suffix = Tape/Reel Type

Related Products Information

Part Number	Product Description
PI3HDX414	HDMI 1.4b 3.4Gbps Splitter 1:4 with Signal Conditioning
PI3HDX412BD	HDMI 1.4b 3.4Gbps Splitter 1:2 with Signal Conditioning
PI3WVR12412	Wide Voltage Range DisplayPort & HDMI 2.0 Video Switch
PI3HDX511A	HDMI 1.4b 3.4Gbps Redriver and DP++ Level Shifter
PI3EQXDP1201	DisplayPort 1.2 Re-driver with Built-in AUX Listener
PI3VDP1430	Dual Mode DisplayPort to HDMI Level Shifter and Re-driver
PI3VDP3212	2-Lane DisplayPort1.2 Compliant Passive Switch
PI3VDP12412	4-Lane DisplayPort1.2 Compliant Passive Switch
PI3HDMI521	HDMI 1.4b 3.4Gbps 2:1 Switch/Re-driver with built-in ARC and Fast Switching support
PI3HDMI336	Active HDMI 3:1 Switch/Re-driver with I^2C control and ARC Transmitter

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Pericom Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Pericom Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Pericom Semiconductor. The datasheet is for reference information only.