PERICOM®

PI3A412

0.4Ω, 3.3V, Quad SPDT Analog Switch

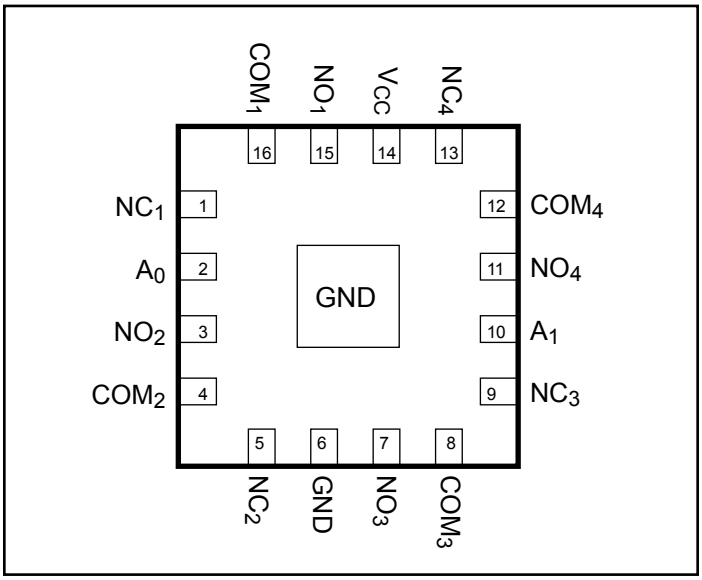
Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.4Ω (+2.7V Supply)
- Wide V_{CC} Range: +1.6V to +4.2V ±10%
- I_{CC} = 0.3µA @ T_A = +25˚C
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 20ns TYP. at 3.3V
- High Off Isolation: -65dB
- Crosstalk Rejection: -65dB
- Extended Industrial Temperature Range: –40°C to 85°C
- Packaging: (Pb-free & Green)
  – 16-contact TQFN (ZL), 2.5mm x 2.5mm
  – 16-contact TQFN (ZH), 3.0mm x 3.0mm

Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals
- Audio & Video Signal Routing
- PCMCIA Cards
- Modems
- Hard Drives
- JTAG Testing

Pin Configuration (top view)

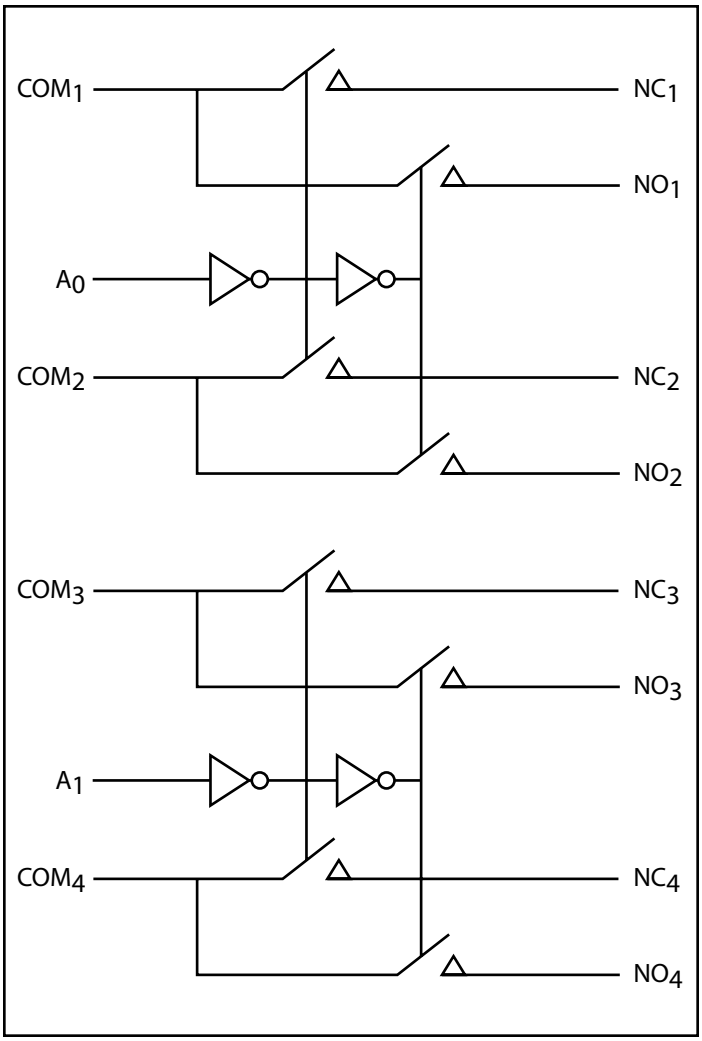


Description

The PI3A412 is a quad single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, +1.6V to +4.2V, the switch has an On-Resistance of 0.4Ω at 2.7V.

Control inputs, Ax, tolerates input drive signals up to 5V, independent of supply voltage.

Block Diagram



Pin Description

Pin #	Name	Description
4, 8, 12, 16	COM_X	Common Output / Data Port
1, 5, 9, 13	NC_X	Data Port (normally connect)
3, 7, 11, 15	NO_X	Data Port (normally open)
2, 10	A_0, A_1	Logic Input Control
6	GND	Ground
14	V_{CC}	Positive Power Supply

Notes :

1. X = 1, 2, 3, or 4

Function Tables

A_0	Function
0	NC_X Connected to COM_X
1	NO_X Connected to COM_X

A_1	Function
0	NC_Y Connected to COM_Y
1	NO_Y Connected to COM_Y

Notes :

1. X = 1 or 2
2. Y = 3 or 4

Absolute Maximum Ratings

Voltages Referenced to GND

V_{CC} ..... 1.5V to +4.6V

V_{NOx}, V_{NCx}, V_{COMx}, V_{Ax} (1) .....–0.5V to V_+ +0.3V or 30mA, whichever occurs first

Current (any terminal)..... ±200mA

Peak Current, $V_{NC} + V_{NO}$
(Pulsed at 1ms, 10% duty cycle)..... ±400mA

Thermal Information

Continuous Power Dissipation

16-pin Thin QFN (derate 7.1mW/ºC above +70ºC)..... 0.5W

Storage Temperature .....–65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Note 1: Signals on NC, NO, COM, or A exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +3.3V Supply

(V_{CC} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.3V, V_{IL} = 0.5V) (T_A = –40°C to +85°C)

Parameter	Symbol	Conditions	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Signal Range (3)	V_{ANALOG}		0		V_{CC}	V
On Resistance	R_{ON}	V_{CC} = 2.7V, I_{COM} = 100mA, V_{IN} = +1.5V		0.4	0.6	Ω
On-Resistance Match Between Channels(4)	ΔR_{ON}			0.08	0.09	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{CC} = 2.7V, I_{COMx} = 100mA, V_{IN} = 0.8V, 2.0V		0.1	0.15	
Off Leakage Current(6)	I_{NC} (off) or I_{NO} (off)	V_{CC} = 3.6V V_{NO} or V_{NC} = 0.3V, 3.3V	-400		400	nA
On Leakage Current(6)	$I_{COMx\ (on)}$	V_{CC} = 3.6V, V_{COMx}= 0.3V, 3.3V	-400		400	

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ match between channels
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.

Electrical Specifications - Single +4.2V Supply

(V_{CC} = +4.2V ± 10%, GND = 0V, V_{IH} = 1.6V, V_{IL} = 0.7V) (T_A = –40°C to +85°C)

Parameter	Symbol	Conditions	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Signal Range (3)	V_{ANALOG}		0		V_{CC}	V
On Resistance	R_{ON}	V_{CC} = 4.0V, I_{COMx} = 100mA, V_{IN} = +1.5V		0.4	0.6	Ω
On-Resistance Match Between Channels(4)	ΔR_{ON}			0.08	0.09	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{CC} = 4.0V, I_{COMx} = 100mA, V_{IN} = 0.8V, 2.0V		0.1	0.15	
Off Leakage Current(6)	I_{NC} (off) or I_{NO} (off)	V_{CC} = 4.4V, V_{NO} or V_{NC} = 0.3V, 3.3V	-400		400	nA
On Leakage Current(6)	I_{COMx} (on)	V_{CC} = 4.4V, V_{COMx} = 0.3V, 3.3V	-400		400	

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ match between channels
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.

Electrical Specifications - Single +4.2V Supply

(V_{CC} = +4.2V ± 10%, GND = 0V, V_{IH} = 1.6V, V_{IL} = 0.7V) (T_A = –40°C to +85°C)

Description	Parameter	Test Conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
Logic Input						
Input High Voltage	V_{IH}	Guaranteed logic High Level	1.6			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level			0.7	
Input Current with Voltage High	I_{AH}	V_A = 1.4V, all others = 0.5V	–1		1	µA
Input Current with Voltage Low	I_{AL}	V_A = 0.5V, all other = 1.4V	–1		1	
Dynamic						
Turn-On Time	t_{ON}	V_{CC} = 4.2V, V_{COM} = 2.0V, Figure 1 & 2		20	25	ns
Turn-Off Time	t_{OFF}			12	15	
Break-Before-Make	t_{BBM}	V_{IN} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 3	1	12	15	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4		100		pC
Off Isolation(4)	O_{IRR}	R_L = 50Ω, f = 100kHz, Figure 5		-65		dB
Cross Talk(5)	X_{TALK}	R_L = 50Ω, f = 100kHz, Figure 6		-65		
3dB Bandwidth	f_{3db}	See Test Circuit Figure 9		40		MHz
Off Capacitance	$C_{NC(OFF)}$	f = 1 MHz, Figure 7		50		pF
Off Capacitance	$C_{NO(OFF)}$			50		
On Capacitance	C_{ON}	f = 1 MHz, Figure 8		135		
Supply						
Power-Supply Range	V_{CC}		1.5		4.4	V
Positve Supply Current	I_{CC}	V_{CC} = 4.2V, V_A = 0V or V_{CC}		0.5		µA

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. Off Isolation = $20\log_{10}$ [(V_{NO} or V_{NC}) / V_{COM}]. See Figure 5.
5. Between any two switches. See Figure 6.

Electrical Specifications - Single +3.3V Supply

(V_{CC} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.3V, V_{IL} = 0.5V) (T_A = –40°C to +85°C)

Description	Parameters	Test Conditions	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input						
Input High Voltage	V_{IH}	Guaranteed logic High Level	1.3			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level			0.5	
Input Current with Voltage High	I_{AH}	V_A = 1.4V, all others = 0.5V	–1		1	µA
Input Current with Voltage Low	I_{AL}	V_A = 0.5V, all other = 1.4V	–1		1	
Dynamic						
Turn-On Time	t_{ON}	V_{CC} = 3.3V, V_{COM} = 2.0V, Figure 1 & 2		20	25	ns
Turn-Off Time	t_{OFF}			12	15	
Break-Before-Make	t_{BBM}	V_{IN} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 3	1	12	15	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4		100		pC
Off Isolation(4)	O_{IRR}	R_L = 50Ω, f = 100kHz, Figure 5		-65		dB
Cross Talk(5)	X_{TALK}	R_L = 50Ω, f = 100kHz, Figure 6		-65		
3dB Bandwidth	f_{3db}	See Test Circiut Figure 9		40		MHz
Off Capacitance	$C_{NC(OFF)}$	f = 1 MHz, Figure 7		50		pF
Off Capacitance	$C_{NO(OFF)}$			50		
On Capacitance	C_{ON}	f = 1 MHz, Figure 8		135		

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. Off Isolation = $20\log_{10}$ [(V_{NO} or V_{NC}) / V_{COM}]. See Figure 5.
5. Between any two switches. See Figure 6.

Test Circuits and Timing Diagrams

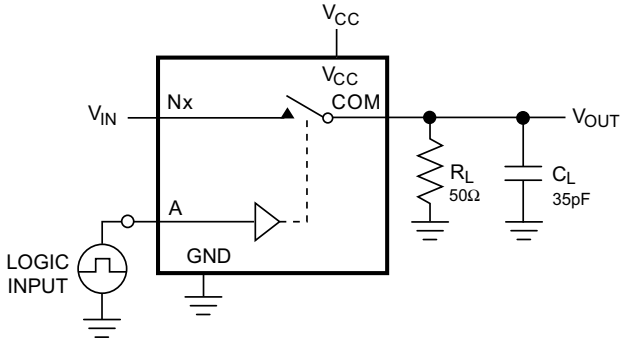


Figure 1. AC Test Circuit

Notes:

Unused N_X inputs must be grounded.

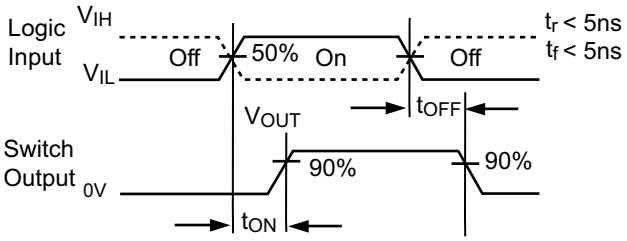


Figure 2. AC Waveforms

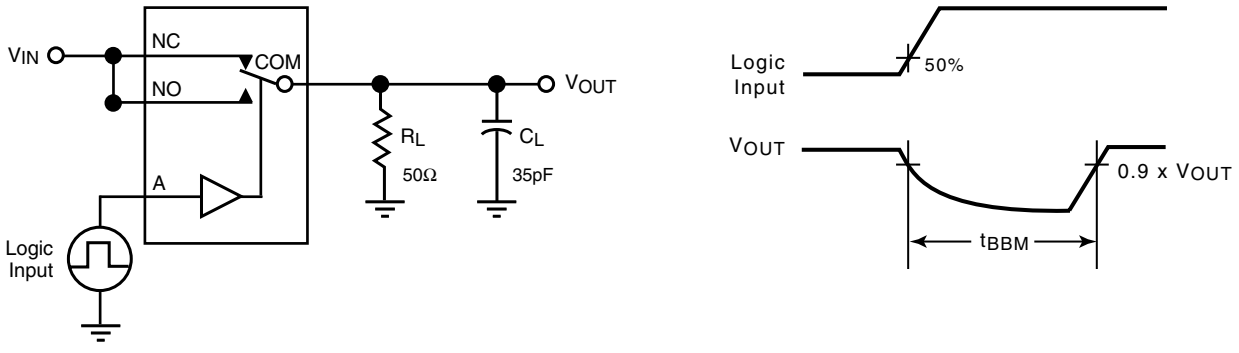


Figure 3. Break Before Make Interval Timing

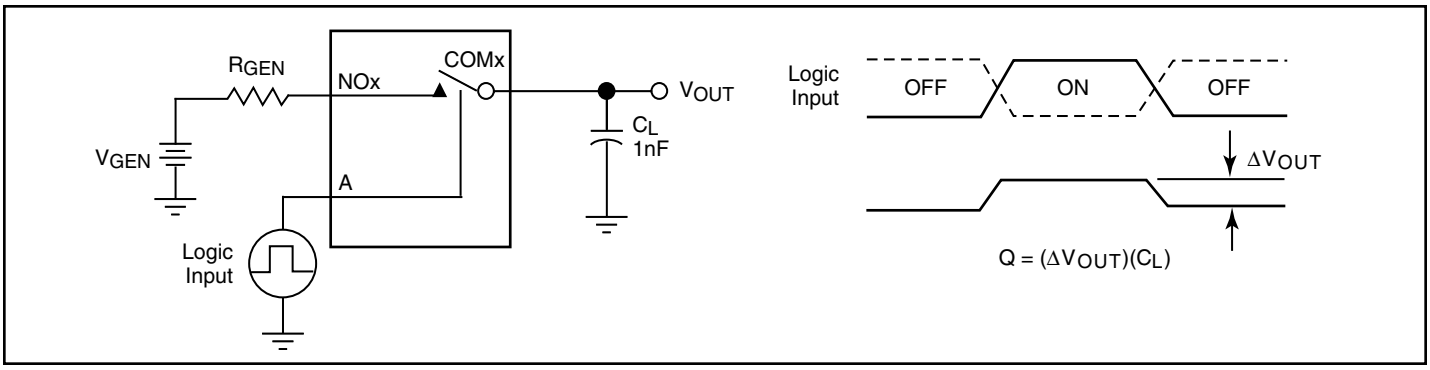


Figure 4. Charge Injection Test

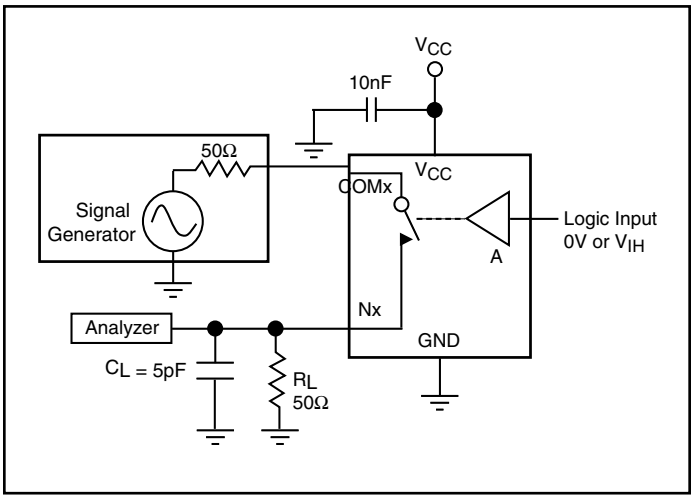


Figure 5. Off Isolation

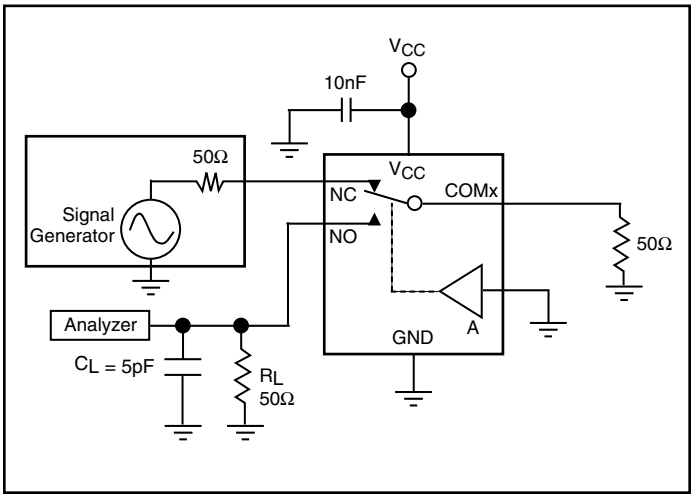


Figure 6. Crosstalk

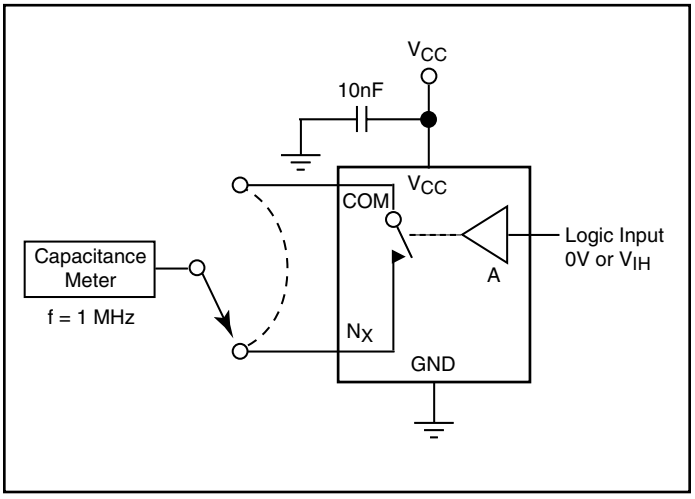


Figure 7. Channel Off Capacitance

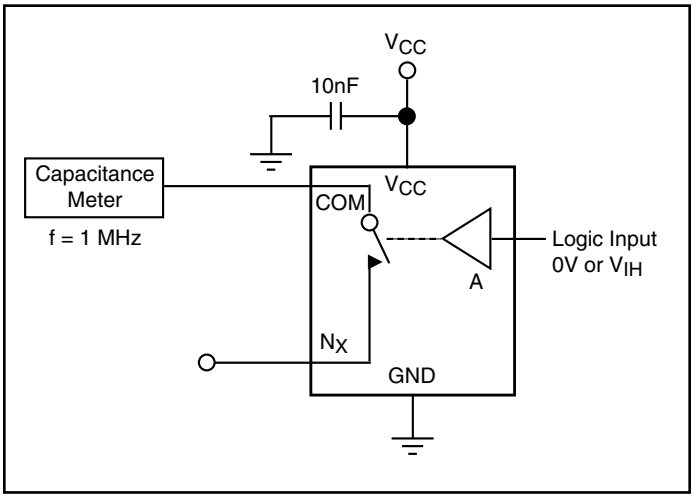


Figure 8. Channel On Capacitance

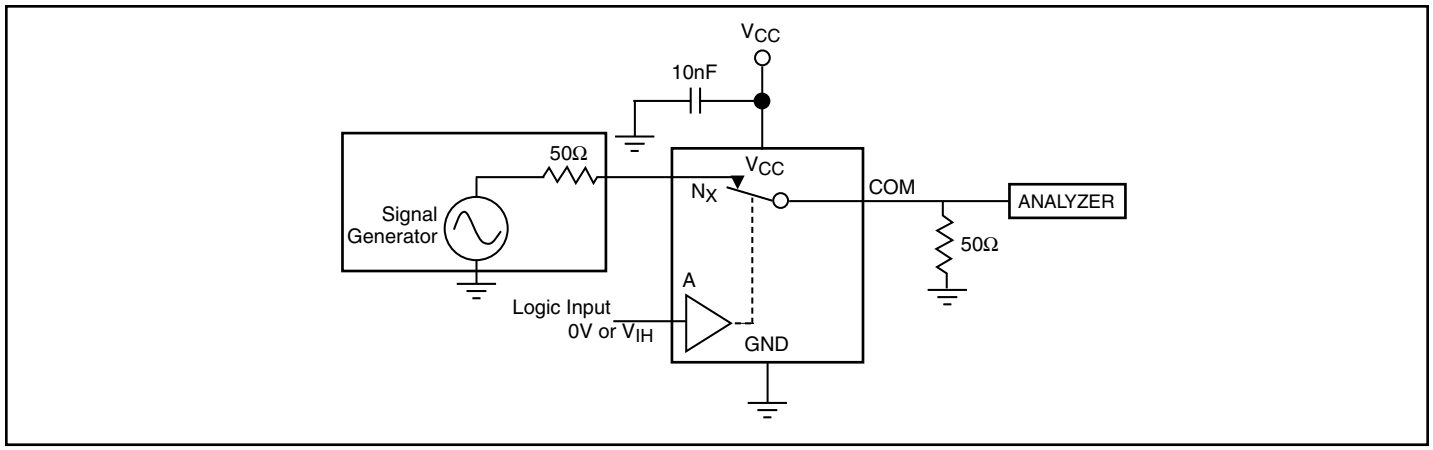
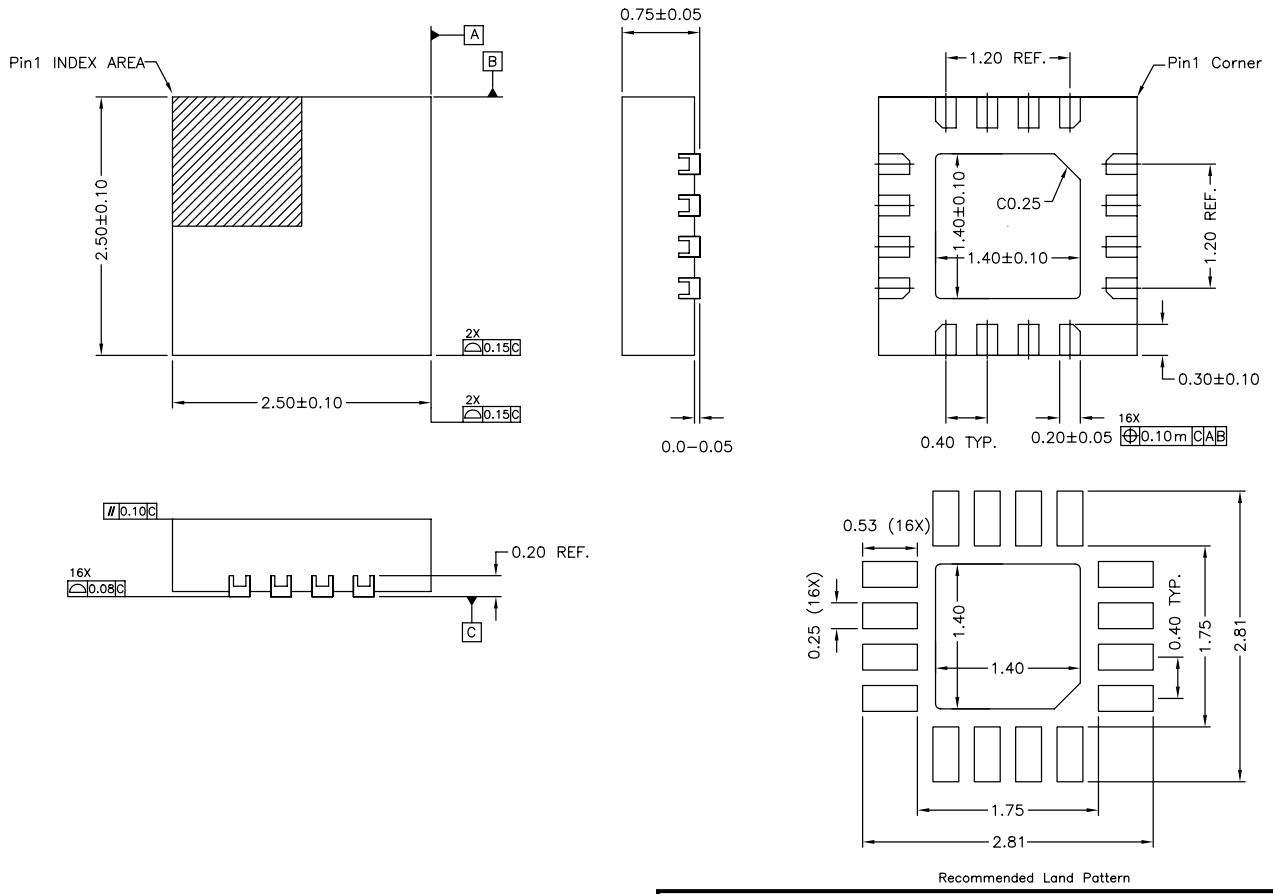


Figure 9. Bandwidth



Recommended Land Pattern

Notes:
1) All dimensions are in millimeters, angles in degrees
2) Coplanarity applies to the exposed pad as well as the terminals
3) Ref JEDEC: MO-220

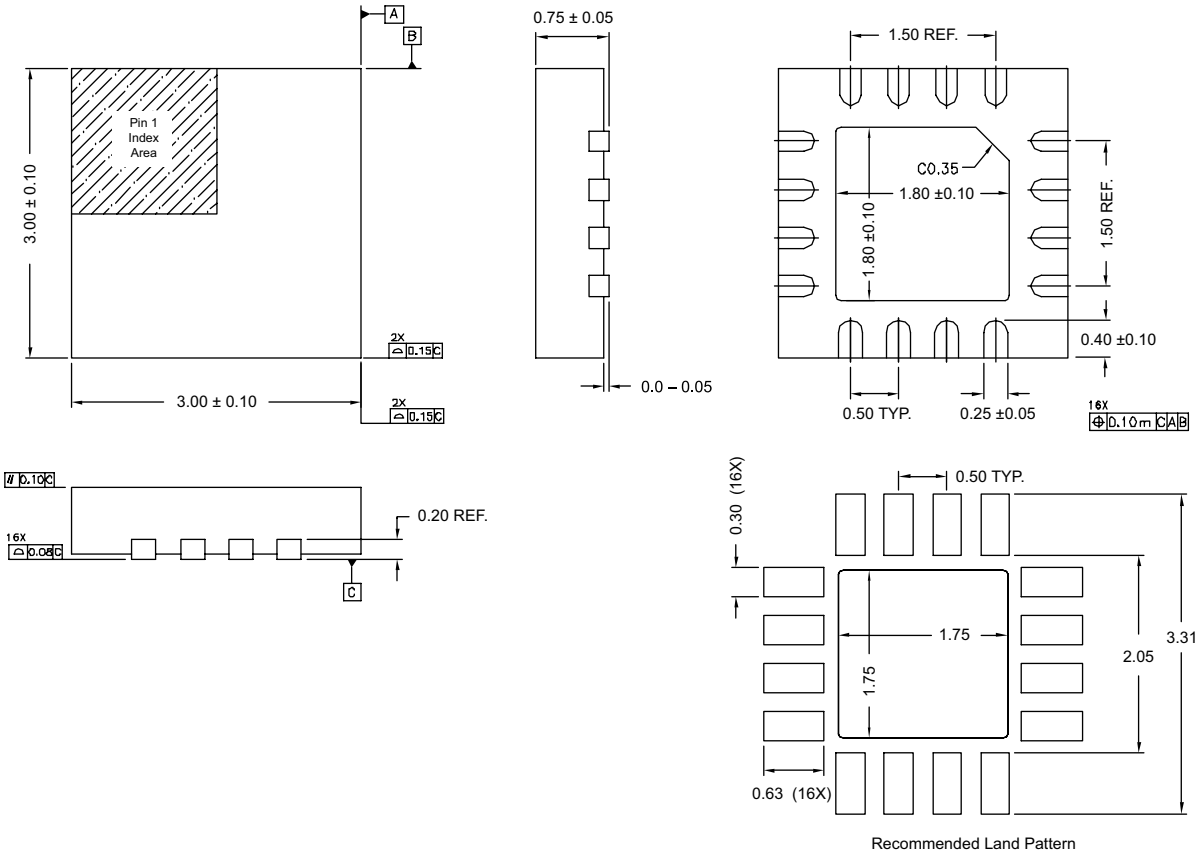
PERICOM Semiconductor Corporation

DATE: 4/28/06

DESCRIPTION: 16-contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL16

DOCUMENT CONTROL #: PD-2061 **REVISION: -**



Recommended Land Pattern

Notes:
1) All dimensions are in millimeters
2) Ref JEDEC: MO-220J (WEED)
3) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

PERICOM Semiconductor Corporation

DATE: 03/16/06

DESCRIPTION: 16-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH16)

DOCUMENT CONTROL #: PD-2047 **REVISION: A**

Ordering Information

Ordering Code	Package Code	Package Description
PI3A412ZLE	ZL	Pb-free & Green, 16-contact TQFN
PI3A412ZHE	ZH	Pb-free & Green, 16-contact TQFN

Notes:

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
• E = Lead-free and Green Packaging
• Adding X suffix = Tape/Reel