

PHK18NQ03LT

N-channel TrenchMOS logic level FET

Rev. 03 — 17 March 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies
- Notebook computers
- Voltage regulators

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 ; see Figure 3	-	-	20.3	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C};$ see Figure 2	-	-	6.25	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 10 ; see Figure 11	-	7.1	8.9	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 15\text{ A};$ $V_{DS} = 12\text{ V};$ see Figure 12 ; see Figure 13	-	2.5	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	<p>SOT96-1 (SO8)</p>	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

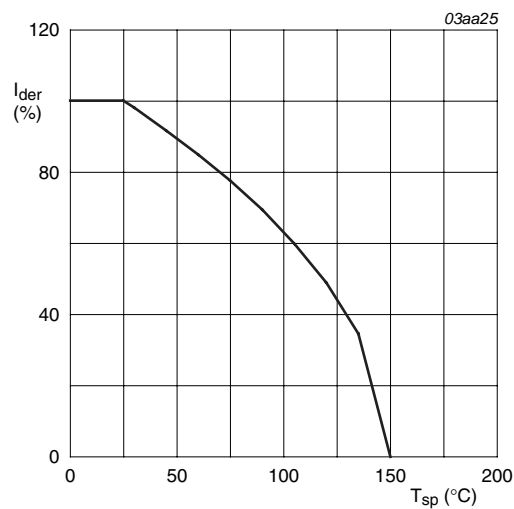
Type number	Package		Version
	Name	Description	
PHK18NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

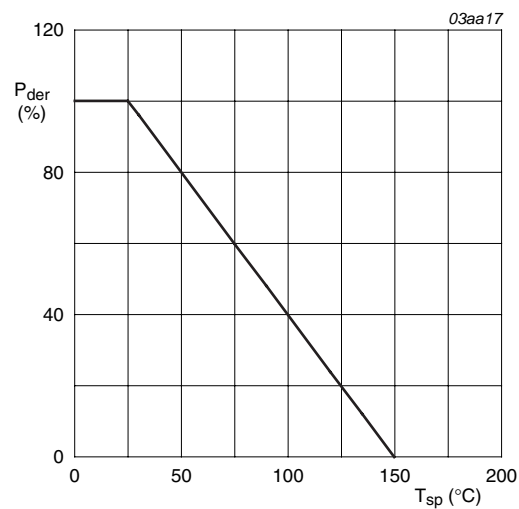
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	-	20.3	A
		$T_{sp} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	12.1	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	80	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	6.25	W
T_{stg}	storage temperature		-55	150	$^{\circ}\text{C}$
T_j	junction temperature		-55	150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	5.2	A
I_{SM}	peak source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	20.8	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $I_D = 31.5\text{ A}$; $V_{sup} \leq 25\text{ V}$; unclamped; $t_p = 0.07\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	50	mJ



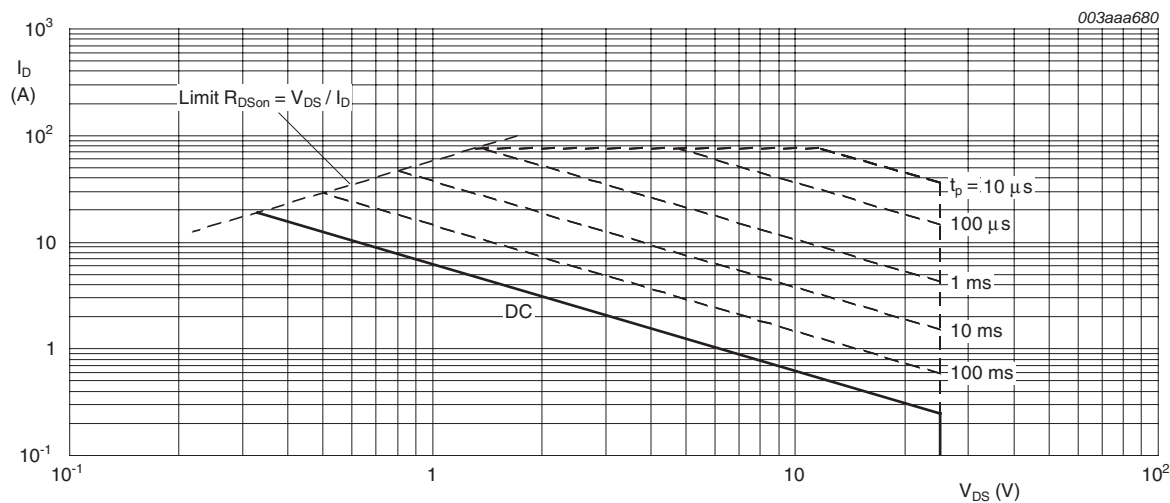
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



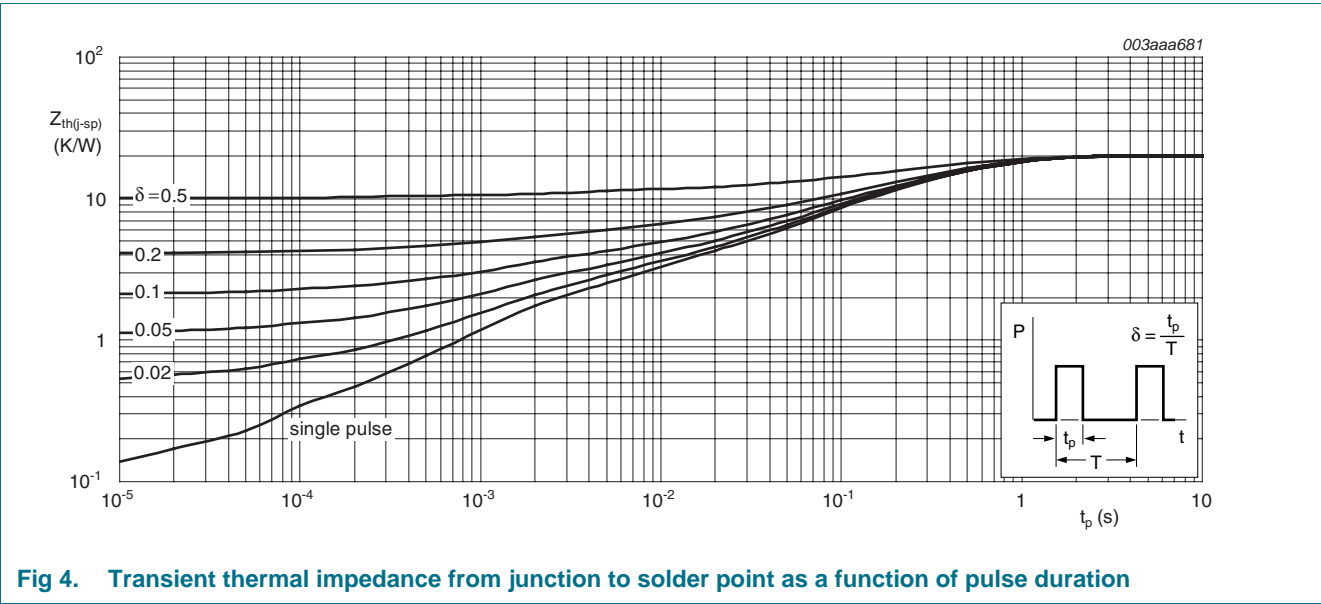
$T_{sp} = 25^{\circ}\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	20	K/W



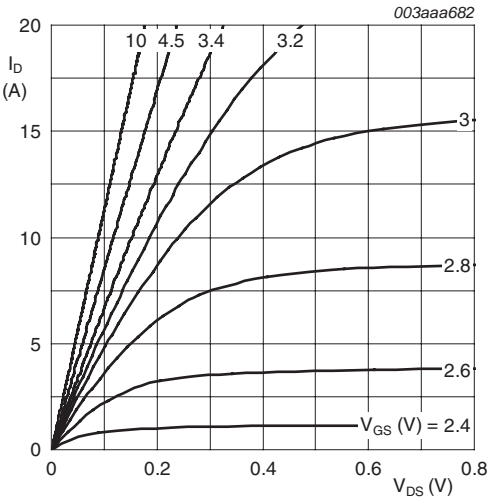
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	30	-	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = -55\ ^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$; see Figure 8 ; see Figure 9	1.3	1.7	2.15	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 150\ ^\circ\text{C}$; see Figure 8 ; see Figure 9	0.8	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ\text{C}$; see Figure 8 ; see Figure 9	-	-	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 10 ; see Figure 11	-	7.1	8.9	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 10	-	12.1	15.1	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 10 ; see Figure 11	-	10.1	12.5	m Ω
R_G	gate resistance	$f = 1\ \text{MHz}$	-	1.6	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 12 ; see Figure 13	-	10.6	-	nC
Q_{GS}	gate-source charge		-	4.85	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	2.4	-	nC
Q_{GS2}	post-threshold gate-source charge		-	2.45	-	nC
Q_{GD}	gate-drain charge		-	2.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15\ \text{A}$; $V_{DS} = 12\ \text{V}$; see Figure 12 ; see Figure 13	-	3	-	V
C_{iss}	input capacitance	$V_{DS} = 12\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_j = 25\ ^\circ\text{C}$; see Figure 14	-	1380	-	pF
		$V_{DS} = 0\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_j = 25\ ^\circ\text{C}$; see Figure 14	-	1590	-	pF
C_{oss}	output capacitance	$V_{DS} = 12\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_j = 25\ ^\circ\text{C}$; see Figure 14	-	290	-	pF
C_{rss}	reverse transfer capacitance		-	135	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ \text{V}$; $R_L = 0.8\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_{G(ext)} = 5.6\ \Omega$	-	19	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	11	-	ns

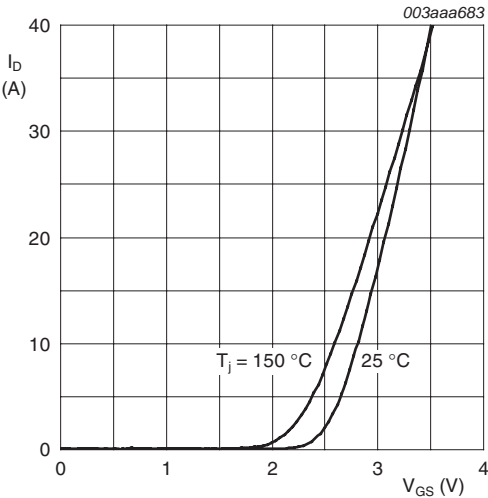
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 15	-	0.95	1.2	V
t_{rr}	reverse recovery time	$I_S = 15\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$	-	34	-	ns
Q_r	recovered charge	$I_S = 15\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	14	-	nC



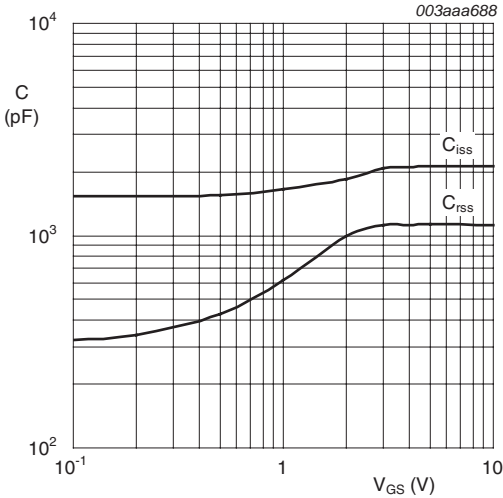
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



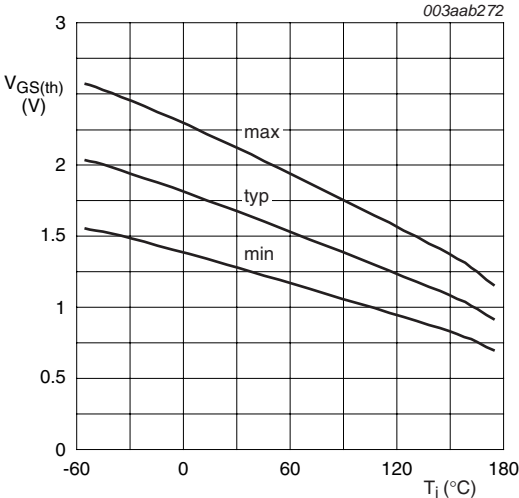
$T_j = 25\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



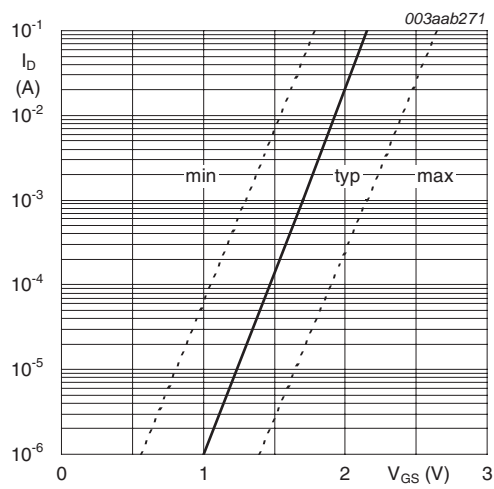
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



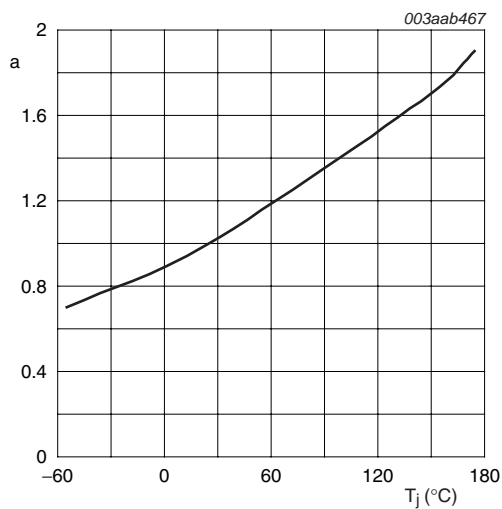
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



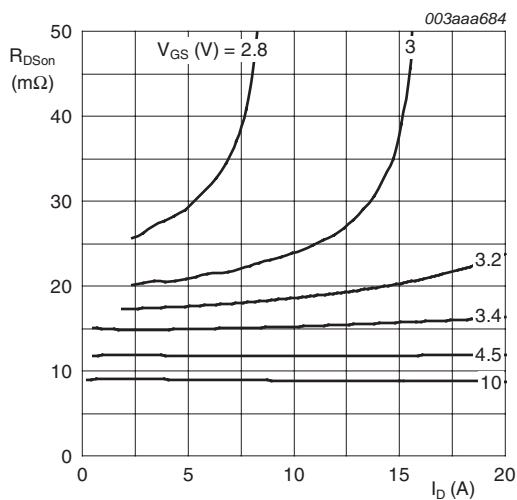
$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values

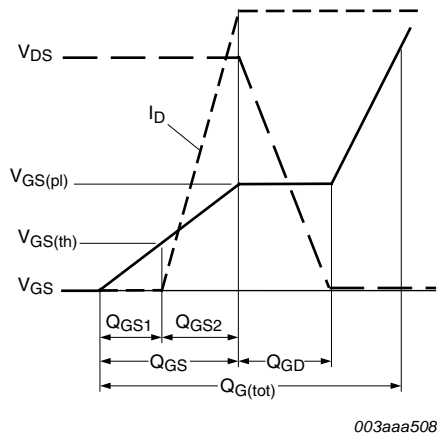
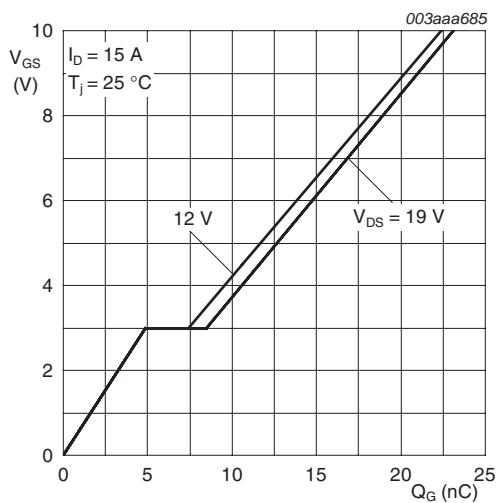
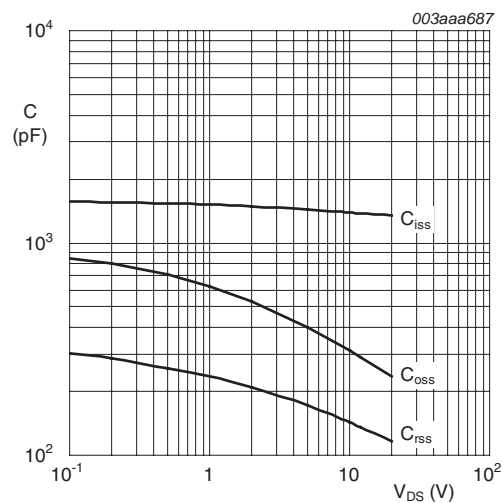


Fig 12. Gate charge waveform definitions



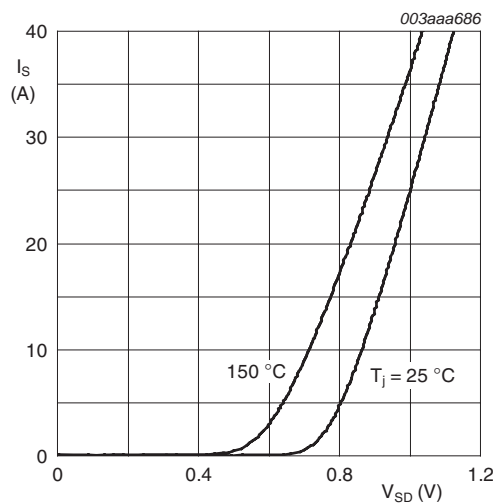
$I_D = 15\text{ A}$; $V_{DS} = 12\text{ V}$ and 19 V

Fig 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

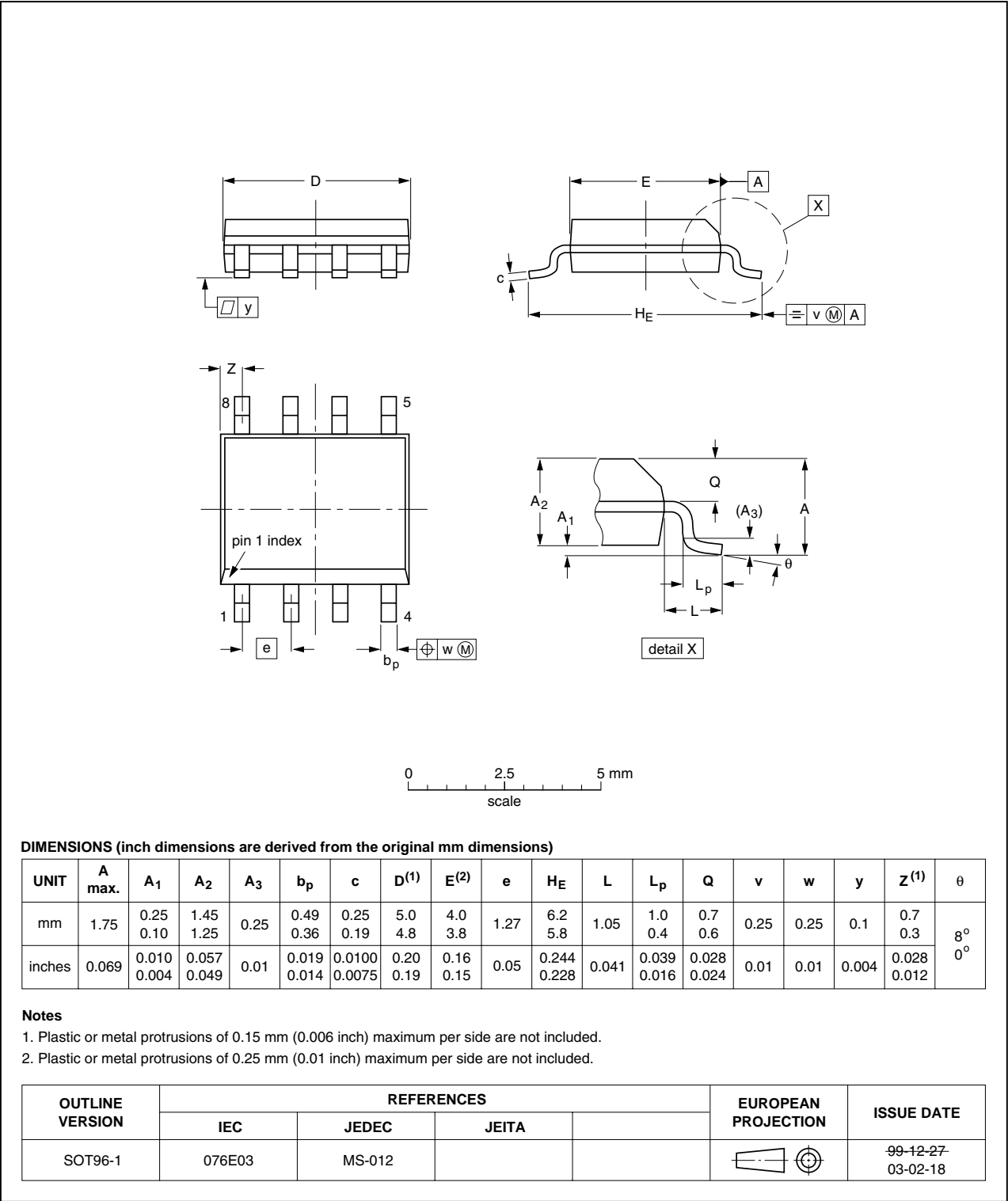


Fig 16. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK18NQ03LT v.3	20110317	Product data sheet	-	PHK18NQ03LT v.2
Modifications:	• Various changes to content.			
PHK18NQ03LT v.2	20101221	Product data sheet	-	PHK18NQ03LT v.1

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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