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PGA112, PGA113, PGA116, PGA117

SBOS424C - MARCH 2008 - REVISED NOVEMBER 2015

PGA11x Zerø-Drift Programmable Gain Amplifier With Mux

Features 1

Texas

INSTRUMENTS

- Rail-to-Rail Input and Output
- Offset: 25 µV (Typical), 100 µV (Maximum)
- Zerø Drift: 0.35 µV/°C (Typical), 1.2 µV/°C (Maximum)
- Low Noise: 12 nV/VHz
- Input Offset Current: ±5 nA Maximum (25°C)
- Gain Error: 0.1% Maximum ($G \leq 32$), 0.3% Maximum (G > 32)
- Binary Gains: 1, 2, 4, 8, 16, 32, 64, 128 (PGA112, PGA116)
- Scope Gains: 1, 2, 5, 10, 20, 50, 100, 200 (PGA113, PGA117)
- Gain Switching Time: 200 ns
- 2 Channel MUX: PGA112, PGA113 10 Channel MUX: PGA116, PGA117
- Four Internal Calibration Channels
- Amplifier Optimized for Driving CDAC ADCs
- Output Swing: 50 mV to Supply Rails
- AV_{DD} and DV_{DD} for Mixed Voltage Systems
- $I_{O} = 1.1 \text{ mA}$ (Typical)
- Software and Hardware Shutdown: $I_{O} \le 4 \mu A$ (Typical)
- Temperature Range: -40°C to 125°C
- SPI™ Interface (10 MHz) With Daisy-Chain Capability

2 Applications

- Remote e-Meter Reading
- Automatic Gain Control
- Portable Data Acquisition
- PC-Based Signal Acquisition Systems
- Test and Measurement
- Programmable Logic Controllers
- **Battery-Powered Instruments**
- Handheld Test Equipment

3 Description

The PGA112 and PGA113 devices (binary and scope gains) offer two analog inputs, a three-pin SPI interface, and software shutdown in a 10-pin, VSSOP package. The PGA116 and PGA117 (binary and scope gains) offer 10 analog inputs, a SPI interface with daisy-chain capability, and hardware and software shutdown in a 20-pin TSSOP package.

All versions provide internal calibration channels for system-level calibration. The channels are tied to GND, 0.9 V_{CAL} , 0.1 V_{CAL} , and V_{REF} , respectively. V_{CAL}, an external voltage connected to Channel 0, is used as the system calibration reference. Binary gains are: 1, 2, 4, 8, 16, 32, 64, and 128; scope gains are: 1, 2, 5, 10, 20, 50, 100, and 200.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA112, PGA113	VSSOP (10)	3.00 mm × 3.00 mm
PGA116, PGA117	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	nanges from Revision B (September 2008) to Revision C	Page
•	Added ESD Ratings table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Levout section, Device and	
	Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1



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5 Device Comparison

DEVICE	NO. OF MUX INPUTS	GAINS	SPI DAISY- CHAIN	SHUT	DACKACE	
DEVICE		(EIGHT EACH)		HARDWARE	SOFTWARE	PACKAGE
PGA112	2	Binary	No	No	\checkmark	VSSOP-10
PGA113	2	Scope	No	No	\checkmark	VSSOP-10
PGA116	10	Binary	\checkmark	1	\checkmark	TSSOP-20
PGA117	10	Scope	\checkmark	1	\checkmark	TSSOP-20

6 Pin Configuration and Functions



Pin Functions: PGA112, PGA113

PIN		1/0	DESCRIPTION			
NO.	NAME	1/0	DESCRIPTION			
1	AV _{DD}	I	Analog supply voltage (2.2 V to 5.5 V)			
2	CH1	I	Input MUX channel 1			
3	V _{CAL} /CH0	I	Input MUX channel 0 and V _{CAL} input. For system calibration purposes, connect this pin to a low- impedance external reference voltage to use internal calibration channels. The four internal calibration channels are connected to GND, 0.9 V _{CAL} , 0.1 V _{CAL} , and V _{REF} , respectively. V _{CAL} is loaded with 100 k Ω (typical) when internal calibration channels CAL2 or CAL3 are selected. Otherwise, V _{CAL} /CH0 appears as high impedance.			
4	V _{REF}	Ι	Reference input pin. Connect external reference for V_{OUT} offset shift or to midsupply for midsupply referenced systems. V_{REF} must be connected to a low-impedance reference capable of sourcing a sinking at least 2 mA or V_{REF} must be connected to GND.			
5	V _{OUT}	0	Analog voltage output. When $AV_{DD} < DV_{DD}$, V_{OUT} is clamped to AV_{DD} + 300 mV.			
6	GND	_	Ground pin			
7	SCLK	I	Clock input for SPI serial interface			
8	DIO	Ι	Data input/output for SPI serial interface. DIO contains a weak, 10-µA internal pulldown current source.			
9	CS	I	Chip select line for SPI serial interface			
10	DV _{DD}	I	Digital and op amp output stage supply voltage (2.2 V to 5.5 V). Useful in multi-supply systems to prevent overvoltage and lockup condition on an analog-to-digital (ADC) input (for example, a microcontroller with an ADC running on 3 V and the PGA powered from 5 V). Digital I/O levels to be relative to DV_{DD} . DV_{DD} should be bypassed with a 0.1-µF ceramic capacitor, and DV_{DD} must supply the current for the digital portion of the PGA as well as the load current for the op amp output stage.			

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Pin Functions: PGA116, PGA117

PIN		1/0	DESCRIPTION		
NO.	NAME	1/0	DESCRIPTION		
1	AV _{DD}	I	Analog supply voltage (2.2 V to 5.5 V)		
2	CH5	I	Input MUX channel 5		
3	CH4	I	Input MUX channel 4		
4	CH3	I	Input MUX channel 3		
5	CH2	I	Input MUX channel 2		
6	CH1	I	Input MUX channel 1		
7	V _{CAL} /CH0	I	Input MUX channel 0 and V _{CAL} input. For system calibration purposes, connect this pin to a low- impedance external reference voltage to use internal calibration channels. The four internal calibration channels are connected to GND, 0.9 V _{CAL} , 0.1 V _{CAL} , and V _{REF} , respectively. V _{CAL} is loaded with 100 k Ω (typical) when internal calibration channels CAL2 or CAL3 are selected. Otherwise, V _{CAL} /CH0 appears as high impedance.		
8	V _{REF}	I	Reference input pin. Connect external reference for V _{OUT} offset shift or to midsupply for midsupply referenced systems. V _{REF} must be connected to a low-impedance reference capable of sourcing and sinking at least 2 mA or to GND.		
9	V _{OUT}	0	Analog voltage output. When $AV_{DD} < DV_{DD}$, V_{OUT} is clamped to $AV_{DD} + 300$ mV.		
10	CH7	I	Input MUX channel 7		
11	CH8	I	Input MUX channel 8		
12	CH9	I	Input MUX channel 9		
13	ENABLE	I	Hardware enable pin. Logic low puts the part into Shutdown mode ($I_Q < 1 \mu A$).		
14	GND	_	Ground pin		
15	SCLK	I	Clock input for SPI serial interface		
16	DIN	I	Data input for SPI serial interface. DIN contains a weak, 10-µA internal pulldown current source to allow for ease of daisy-chain configurations.		
17	DOUT	0	Data output for SPI serial interface. DOUT goes to high-Z state when \overline{CS} goes high for standard SPI interface.		
18	CS	I	Chip select line for SPI serial interface		
19	DV _{DD}	I	Digital and op amp output stage supply voltage (2.2 V to 5.5 V). Useful in multi-supply systems to prevent overvoltage and lockup condition on an ADC input (for example, a microcontroller with an ADC running on 3 V and the PGA powered from 5 V). Digital I/O levels to be relative to DV_{DD} . DV_{DD} should be bypassed with a 0.1-µF ceramic capacitor, and DV_{DD} must supply the current for the digital portion of the PGA as well as the load current for the op amp output stage.		
20	CH6	I	Input MUX channel 6		

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.⁽¹⁾

	MIN	MAX	UNIT
Supply voltage		7	V
Signal input terminals, voltage ⁽²⁾	GND – 0.5	AV _{DD} + 0.5	V
Signal input terminals, current ⁽²⁾		±10	mA
Output short circuit	Continuous		
Operating temperature	-40	125	°C
Junction temperature		150	°C
Storage temperature	-65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrosta		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	
	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V
		Machine Model (MM)	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
AV _{DD}	2.2	5	5.5	V
DV _{DD}	2.2	5	5.5	V
Operating temperature	-40	25	125	°C

7.4 Thermal Information

		PGA112, PGA113	PGA116, PGA117	
		DGS (VSSOP)	PW (TSSOP)	UNIT
		10 PINS	20 PINS	
$R_{ extsf{ heta}JA}$	Junction-to-ambient thermal resistance	98.3	100.3	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	57	36.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	50.6	°C/W
ΨJT	Junction-to-top characterization parameter	1.3	2.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	36.9	50.2	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	4.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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STRUMENTS

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7.5 Electrical Characteristics: $V_s = AV_{DD} = DV_{DD} = 5 V$

at $T_A = 25^{\circ}C$, $R_L = 10k\Omega//C_L = 100 \text{ pF}$ connected to $DV_{DD}/2$, and $V_{REF} = GND$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
Input offset voltage	Vos	$AV_{DD} = DV_{DD} = 5 \text{ V}, \text{ V}_{REF} = \text{V}_{IN} = AV_{DD}/2, \text{ V}_{CM} = 2.5$	V		±25	±100	μV
	1	$AV_{DD} = DV_{DD} = 5 \text{ V}, \text{ V}_{REF} = \text{V}_{IN} = AV_{DD}/2, \text{ V}_{CM} = 4.5$	V		±75	±325	μV
vs temperature, -40°C to 125°C	dV _{OS} /dT	$AV_{DD} = DV_{DD} = 5 V, V_{CM} = 2.5 V$	$T_A = -40^{\circ}C$ to $125^{\circ}C$		0.35	1.2	μV/°C
vs temperature, -40°C to 85°C		$AV_{DD} = DV_{DD} = 5 \text{ V}, V_{CM} = 2.5 \text{ V}$			0.15	0.9	µV/°C
vs temperature, -40°C to 125°C		$AV_{DD} = DV_{DD} = 5 \text{ V}, V_{CM} = 4.5 \text{ V}$	$T_A = -40^{\circ}C$ to 125°C		0.6	1.8	µV/°C
vs temperature, -40°C to 85°C		$AV_{DD} = DV_{DD} = 5 \text{ V}, V_{CM} = 4.5 \text{ V}$			0.3	1.3	µV/°C
vs power supply	PSRR	$\begin{array}{l} AV_{DD} = DV_{DD} = 2.2 \ V \ \text{to} \ 5.5 \ V, \ V_{CM} = 0.5 \ V, \\ V_{REF} = V_{IN} = AV_{DD}/2 \end{array}$			5	20	μV/V
Over temperature, -40°C to 125	°C		$T_A = -40^{\circ}C$ to $125^{\circ}C$		5	40	μV/V
INPUT ON-CHANNEL CURRENT						4	
Input on-channel current (Ch0, Ch1)	I _{IN}	$V_{REF} = V_{IN} = AV_{DD}/2$			±1.5	±5	nA
Over temperature, -40°C to 125	°C	$V_{REF} = V_{IN} = AV_{DD}/2$		See Typical	Characteris	tics	nA
INPUT VOLTAGE RANGE							
Input voltage range ⁽¹⁾	I _{VR}			GND – 0.1		$AV_{DD} + 0.1$	V
Overvoltage input range	•	No output phase reversal ⁽²⁾		GND – 0.3		$AV_{DD} + 0.3$	V
INPUT IMPEDANCE (Channel On)	(3)						
Channel input capacitance	C _{CH}				2		pF
Channel switch resistance	R _{SW}				150		Ω
Amplifier input capacitance	C _{AMP}				3		pF
Amplifier input resistance	R _{AMP}	Input resistance to GND			10		GΩ
V _{CAL} /CH0	R _{IN}	CAL1 or CAL2 selected			100		kΩ
GAIN SELECTIONS							
Nominal gains		Binary gains: 1, 2, 4, 8, 16, 32, 64, 128		1		128	
		Scope gains: 1, 2, 5, 10, 20, 50, 100, 200		1		200	
DC gain error	G = 1	$\rm V_{OUT}$ = GND + 85 mV to $\rm DV_{DD}$ – 85 mV			0.006%	0.1%	
	1 < G ≤ 32	$\rm V_{OUT}$ = GND + 85 mV to $\rm DV_{DD}$ – 85 mV				0.1%	
	G ≥ 50	V_{OUT} = GND + 85 mV to DV_{DD} – 85 mV				0.3%	
DC gain drift	G = 1	V_{OUT} = GND + 85 mV to DV_{DD} – 85 mV	$T_A = -40^{\circ}C$ to $125^{\circ}C$		0.5		ppm/°C
	1 < G ≤ 32	V_{OUT} = GND + 85 mV to DV_{DD} – 85 mV	$T_A = -40^{\circ}C$ to $125^{\circ}C$		2		ppm/°C
	G ≥ 50	V_{OUT} = GND + 85 mV to DV_{DD} – 85 mV	$T_A = -40^{\circ}C$ to $125^{\circ}C$		6		ppm/°C
CAL2 DC gain error ⁽⁴⁾		$\begin{array}{l} Op \ Amp + Input = 0.9 \ V_{GAL}, \\ V_{REF} = V_{CAL} = AV_{Dp}/2, \ G = 1 \end{array}$			0.02%		
CAL2 DC gain drift ⁽⁴⁾		Op Amp + Input = 0.9 V _{CAL} , V _{REF} = V _{CAL} = AV _{DD} /2, G = 1	$T_A = -40^{\circ}C$ to 125°C		2		ppm/°C
CAL3 DC gain error ⁽⁴⁾		$\begin{array}{l} \text{Op Amp + Input = 0.1 } V_{\text{CAL}}, \\ \text{V}_{\text{REF}} = \text{V}_{\text{CAL}} = \text{AV}_{\text{DD}}/2, \text{ G} = 1 \end{array}$			0.02%		
CAL3 DC gain drift ⁽⁴⁾		$ \begin{array}{l} Op \ Amp + \overline{Input} = 0.1 \ V_{CAL}, \\ V_{REF} = V_{CAL} = AV_{DD}/2, \ G = 1 \end{array} $	$T_A = -40^{\circ}C$ to 125°C		2		ppm/°C
INPUT IMPEDANCE (CHANNEL O	FF) ⁽³⁾						
Input impedance	C _{CH}	See Figure 55			2		pF

Gain error is a function of the input voltage. Gain error outside of the range (GND + 85 mV ≤ V_{OUT} ≤ DV_{DD} - 85 mV) increases to 0.5% (typical).

(2) Input voltages beyond this range must be current-limited to < |10 mA| through the input protection diodes on each channel to prevent permanent destruction of the device.

(3) See Figure 55.

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(4) Total V_{OUT} error must be computed using input offset voltage error multiplied by gain. Includes op amp G = 1 error.

Electrical Characteristics: $V_s = AV_{DD} = DV_{DD} = 5 V$ (continued)

at $T_A = 25^{\circ}$ C, $R_L = 10 k\Omega / C_L = 100 \text{ pF}$ connected to $DV_{DD}/2$, and $V_{REF} = GND$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ST CONDITIONS MIN TYP MAX U					
INPUT OFF-CHANNEL CURRENT								
Input Off-Channel Current (Ch0, Ch1) ⁽⁵⁾	I _{LKG}				±0.05	±1	nA	
Over temperature, -40°C to 125	°C	$V_{REF} = GND, V_{OFF-CHANNEL} = AV_{DD}/2,$ $V_{ON-CHANNEL} = AV_{DD}/2 - 0.1 V$		See Typical C	haracteris	tics		
Channel-to-Channel Crosstalk				130		dB		
OUTPUT					1			
Voltage output swing from rail		$I_{OUT} = \pm 0.25 \text{ mA}, \text{AV}_{DD} \ge \text{DV}_{DD}^{(6)}$	GND + 0.05		DV _{DD} - 0.05	V		
		$I_{OUT} = \pm 5 \text{ mA}, \text{AV}_{DD} \ge \text{DV}_{DD}^{(6)}$	GND + 0.25		DV _{DD} - 0.25	V		
DC output nonlinearity		V_{OUT} = GND + 85 mV to DV_{DD} – 85 mV ⁽⁷⁾			0.0015		%FSR	
Short circuit current	I _{SC}			-	-30/+60		mA	
Capacitive load drive	CLOAD			See Typical C				
NOISE								
Input voltage noise density	en	$f > 10 \text{ kHz}, C_L = 100 \text{ pF}, V_S = 5 \text{ V}$			12		nV/√Hz	
		$f > 10 \text{ kHz}, C_L = 100 \text{ pF}, V_S = 2.2 \text{ V}$			22		nV/√Hz	
Input voltage noise	e _n	f = 0.1 Hz to 10 Hz, C_L = 100 pF, V_S = 5 V			0.362		μV_{PP}	
		f = 0.1 Hz to 10 Hz, C_L = 100 pF, V_S = 2.2 V		0.736				
Input current density	l _n	f = 10 kHz, C _L = 100 pF	pF 400					
SLEW RATE								
Slew rate	SR			See Ta	able 1		V/µs	
SETTLING TIME								
Settling time	ts			See Ta	able 1		μs	
FREQUENCY RESPONSE								
Frequency response				See Ta	able 1		MHz	
THD + NOISE								
		G = 1, f = 1 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100 pF			0.003%			
		G = 10, f = 1 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100 p	F		0.005%			
		G = 50, f = 1 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100 p	F		0.03%			
		G = 128, f = 1 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100	pF		0.08%			
		G = 200, f = 1 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100	pF		0.1%			
		G = 1, f = 20 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100 p	Γ		0.02%			
		G = 10, f = 20 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100	pF		0.01%			
		G = 50, f = 20 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 100	pF		0.03%			
		G = 128, f = 20 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 10	0 pF		0.08%			
		G = 200, f = 20 kHz, V_{OUT} = 4 V_{PP} at 2.5 V_{DC} , C_L = 10	0 pF		0.11%			
POWER SUPPLY								
Operating voltage range ⁽⁶⁾	AV _{DD}			2.2		5.5	V	
	DV_DD			2.2		5.5	V	
Quiescent current analog	I _{QA}	$I_0 = 0, G = 1, V_{OUT} = V_{REF}$			0.33	0.45	mA	
Over temperature, -40°C to 125	°C		$T_A = -40^{\circ}C$ to $125^{\circ}C$			0.45	mA	
Quiescent current digital ⁽⁸⁾⁽⁹⁾⁽¹⁰⁾	I _{QD}	$\frac{I_{O}}{CS} = 0, G = 1, V_{OUT} = V_{REF}, SCLK at 10 MHz, CS = Logic 0, DIO or DIN = Logic 0$			0.75	1.2	mA	
Over temperature, -40°C to 125	°C ⁽⁸⁾⁽⁹⁾⁽¹⁰⁾	$I_{0} = 0, G = 1, V_{OUT} = V_{REF}, SCLK at 10 MHz, \overline{CS} = Logic 0, DIO or DIN = Logic 0 TABLE T$					mA	
Shutdown current analog + digital ⁽⁸⁾⁽⁹⁾	I _{SDA} + I _{SDD}	$I_{O} = 0, \ V_{OUT} = V_{REF}, \ G = 1, \ SCLK \ Idle$			4		μA	
		$I_0 = 0$, $V_{OUT} = 0$, $G = 1$, SCLK at 10MHz, $\overline{CS} = Logic 0$, DIO or DIN = Logic 0			245		μA	
POWER-ON RESET (POR)								
POR trip voltage		Digital interface disabled and Command Register set DV_{DD} < POR Trip Voltage	to POR values for		1.6		V	

Maximum specification limitation limited by final test time and capability. (5)

(6) When AV_{DD} is less than DV_{DD} , the output is clamped to AV_{DD} + 300 mV.

(7) Measurement limited by noise in test equipment and test time.
 (8) Does not include current into or out of the V_{REF} pin. Internal R_F and R_I are always connected between V_{OUT} and V_{REF}.
 (9) Digital logic levels: DIO or DIN = logic 0. 10-μA internal pulldown current source.

(10) Includes current from op amp output structure.

Electrical Characteristics: $V_s = AV_{DD} = DV_{DD} = 5 V$ (continued)

at $T_A = 25^{\circ}C$, $R_L = 10k\Omega//C_L = 100 \text{ pF}$ connected to $DV_{DD}/2$, and $V_{REF} = GND$ (unless otherwise noted)

PARAMETER	_	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE						
Specified range			-40		125	°C
Operating range			-40		125	°C
Thermal resistance	θ _{JA}					
VSSOP-10				164		°C/W
DIGITAL INPUTS (SCLK, CS, DIO, D	DIN)					
Logic low			0		$0.3 DV_{DD}$	V
Input leakage current (SCLK and CS	only)		-1		1	μA
Weak pulldown current (DIO, DIN only	y)			10		μA
Logic high			$0.7 DV_{DD}$		DV_DD	V
Hysteresis				700		mV
DIGITAL OUTPUT (DIO, DOUT)						
Logic high		$I_{OH} = -3 \text{ mA} \text{ (sourcing)}$	$DV_{DD} - 0.4$		DV_DD	V
Logic low		I _{OL} = 3 mA (sinking)	GND		GND + 0.4	V
CHANNEL AND GAIN TIMING						
Channel select time				0.2		μs
Gain select time				0.2		μs
SHUTDOWN MODE TIMING						
Enable time				4		μs
Disable time		V_{OUT} goes high-impedance, R_{F} and R_{I} remain connected between V_{OUT} and V_{REF}		2		μs
POWER-ON-RESET (POR) TIMING						
POR power-up time		$DV_{DD} \ge 2 V$		40		μs
POR power-down time		DV _{DD} ≤ 1.5 V		5		μs

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7.6 SPI Timing: $V_s = AV_{DD} = DV_{DD} = 2.2 V$ to 5 V

At $T_A = +25^{\circ}C$, $R_L = 10k\Omega//C_L = 100pF$ connected to $DV_{DD}/2$, and $V_{REF} = GND$, unless otherwise noted.

		MIN	NOM MAX	UNIT
	Input capacitance (SCLK, CS, and DIO pins)		1	pF
t _{RFI}	I <u>npu</u> t rise and fall time ⁽¹⁾ (CS, SCLK, and DIO pins)		2	μs
t _{RFO}	Output rise and fall time (DIO pin) ⁽¹⁾ $C_{LOAD} = 60 \text{ pF}$		10	ns
t _{CSH}	$\overline{\text{CS}}$ high time ($\overline{\text{CS}}$ pin) ⁽¹⁾	40		ns
t _{CSO}	SCLK edge to \overline{CS} fall setup time ⁽¹⁾	10		ns
t _{CSSC}	CS fall to first SCLK edge setup time	10		ns
f _{SCLK}	SCLK Frequency ⁽²⁾		10	MHz
t _{HI}	SCLK high time ⁽³⁾	40		ns
t _{LO}	SCLK low time ⁽³⁾	40		ns
t _{SCCS}	SCLK last edge to \overline{CS} rise setup time ⁽¹⁾	10		ns
t _{CS1}	CS rise to SCLK edge setup time ⁽¹⁾	10		ns
t _{SU}	DIN setup time	10		ns
t _{HD}	DIN hold time	10		ns
t _{DO}	SCLK to DOUT valid propagation delay ⁽¹⁾		25	ns
t _{SOZ}	CS rise to DOUT forced to Hi-Z ⁽¹⁾		20	ns

(1) Ensured by design; not production tested.

(2) When using devices in daisy-chain mode, the maximum clock frequency for SCLK is limited by SCLK rise and fall time, DIN setup time, and DOUT propagation delay. See Figure 61. Based on this limitation, the maximum SCLK frequency for daisy-chain mode is 9.09 MHz.

(3) t_{HI} and t_{LO} must not be less than 1/SCLK (maximum).



Figure 1. SPI Mode 0, 0









7.7 Typical Characteristics

at $T_A = 25^{\circ}C$, $AV_{DD} = DV_{DD} = 5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $DV_{DD}/2$, $V_{REF} = GND$, and $C_L = 100 \text{ pF}$, unless otherwise noted.



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Typical Characteristics (continued)



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Typical Characteristics (continued)



Figure 20. CAL3 Gain Error Drift (-40°C to 125°C)

Figure 19. CAL2 Gain Error Drift (-40°C to 125°C)

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Typical Characteristics (continued)



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8 Detailed Description

8.1 Overview

The PGA112 and PGA113 devices (binary and scope gains) offer two analog inputs, a three-pin SPI interface, and software shutdown in an 10-pin VSSOP package. The PGA116 and PGA117 (binary and scope gains) offer 10 analog inputs, and hardware and software shutdown in a 20-pin TSSOP package.

All versions provide internal calibration channels for system-level calibration. The channels are tied to GND, 0.9 V_{CAL} , 0.1 V_{CAL} , and V_{REF} , respectively. V_{CAL} , an external voltage connected to Channel 0, is used as the system calibration reference. Binary gains are: 1, 2, 4, 8, 16, 32, 64, and 128; scope gains are: 1, 2, 5, 10, 20, 50, 100, and 200.

The PGA uses a SPI interface with daisy-chain capability, a standard serial peripheral interface (SPI). Both SPI Mode 0,0 and Mode 1,1 are supported, as shown in Figure 56 and described in Table 2.

8.2 Functional Block Diagram



8.3 Feature Description

Featuring low offset, low offset drift and low noise, the PGA11x series provides a flexible analog building block for a variety of applications. The PGA112 and PGA116 offer binary gains of 1, 2, 4, 8, 16, 32, 64, 128 and a 2 channel MUX while the PGA113 and PGA117 offer scope gains of 1, 2, 5, 10, 20, 50, 100, 200 and a 10 channel MUX.

8.4 Device Functional Modes

The PGA112 and PGA113 devices have a software shutdown mode, and the PGA116 and PGA117 devices offer both a hardware and software shutdown mode, see *Shutdown and Power-On-Reset (POR)* for additional information. The PGA uses a standard serial peripheral interface (SPI). Both SPI Mode 0,0 and Mode 1,1 are supported. More information regarding serial communications, including daisy chaining can be found in *Serial Interface Information*.



8.5 Programming

BINARY GAIN (V/V)	TYPICAL -3-dB FREQUENCY (MHz)	SLEW RATE- FALL (V/µs)	SLEW RATE- RISE (V/µs)	0.1% SETTLING TIME: 4 V _{PP} (μs)	0.01% SETTLING TIME: 4 V _{PP} (µs)	SCOPE GAIN (V/V)	TYPICAL 3-dB FREQUENCY (MHz)	SLEW RATE- FALL (V/µs)	SLEW RATE- RISE (V/µs)	0.1% SETTLING TIME: 4 V _{PP} (μs)	0.01% SETTLING TIME: 4 V _{PP} (μs)
1	10	8	3	2	2.55	1	10	8	3	2	2.55
2	3.8	9	6.4	2	2.6	2	3.8	9	6.4	2	2.6
4	2	12.8	10.6	2	2.6	5	1.8	12.8	10.6	2	2.6
8	1.8	12.8	10.6	2	2.6	10	1.8	12.8	10.6	2.2	2.6
16	1.6	12.8	12.8	2.3	2.6	20	1.3	12.8	9.1	2.3	2.8
32	1.8	12.8	13.3	2.3	3	50	0.9	9.1	7.1	2.4	3.8
64	0.6	4	3.5	3	6	100	0.38	4	3.5	4.4	7
128	0.35	2.5	2.5	4.8	8	200	0.23	2.3	2	6.9	10

Table 1. Frequency Response Versus Gain (C_L = 100 pf, R_L= 10 kw)



Figure 55. Equivalent Input Circuit

8.6 Serial Interface Information



Figure 56. SPI Mode 0,0 And Mode 1,1

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Serial Interface Information (continued)

MODE	CPOL	CPHA	CPOL DESCRIPTION	CPHA DESCRIPTION
0, 0	0	0 ⁽¹⁾	Clock idles low	Data are read on the rising edge of clock. Data change on the falling edge of clock.
1, 1	1	1 ⁽²⁾	Clock idles high	Data are read on the rising edge of clock. Data change on the falling edge of clock.

(1) CPHA = 0 means sample on first clock edge (rising or falling) after a valid \overline{CS} .

(2) CPHA = 1 means sample on second clock edge (rising or falling) after a valid \overline{CS} .

8.6.1 Serial Digital Interface: SPI Modes

The PGA uses a standard serial peripheral interface (SPI). Both SPI Mode 0,0 and Mode 1,1 are supported, as shown in Figure 56 and described in Table 2.

If there are not even-numbered increments of 16 clocks (that is, 16, 32, 64, and so forth) between \overline{CS} going low (falling edge) and \overline{CS} going high (rising edge), the device takes no action. This condition provides reliable serial communication. Furthermore, this condition also provides a way to quickly reset the SPI interface to a known starting condition for data synchronization. Transmitted data are latched internally on the rising edge of \overline{CS} .

On the PGA116 and PGA117 devices, \overline{CS} , DIN, and SCLK are Schmitt-triggered CMOS logic inputs. DIN has a weak internal pulldown to support daisy-chain communications on the PGA116 and PGA117 devices. DOUT is a CMOS logic output. When \overline{CS} is high, the state of DOUT is high-impedance. When \overline{CS} is low, DOUT is driven as illustrated in Figure 57.



Figure 57. Digital I/O Structure—PGA116 and PGA117

On the PGA112 and PGA113 devices, there are digital output and digital input gates both internally connected to the DIO pin. DIN is an input-only gate and DOUT is a digital output that can give a 3-state output. The DIO pin has a weak 10-µA pulldown current source to prevent the pin from floating in systems with a high-impedance SPI DOUT line. When CS is high, the state of the internal DOUT gate is high-impedance. When CS is low, the state of DIO depends on the previous valid SPI communication; either DIO becomes an output to clock out data or it remains an input to receive data. This structure is shown in Figure 58.



Figure 58. Digital I/O Structure—PGA112 and PGA113



8.6.2 Serial Digital Interface: SPI Daisy-Chain Communications

To reduce the number of I/O port pins used on a microcontroller, the PGA116 and PGA117 support SPI daisychain communications with full read and write capability. A two-device daisy-chain configuration is shown in Figure 59, although any number of devices can be daisy-chained. The SPI daisy-chain communication uses a common SCLK and \overline{CS} line for all devices in the daisy chain, rather than each device requiring a separate \overline{CS} line. The daisy-chain mode of communication routes data serially through each device in the chain by using its respective DIN and DOUT pins as shown. Special commands are used (see Table 4) to ensure that data are written or read in the proper sequence. There is a special daisy-chain NOP command (No OPeration) which, when presented to the desired device in the daisy-chain, causes no changes in that respective device. Detailed timing diagrams for daisy-chain operation are shown in Figure 63 through Figure 65.



Figure 59. Daisy-Chain Read and Write Configuration

The PGA112 and PGA113 devices can be used as the last device in a daisy-chain as shown in Figure 60 if *write-only* communication is acceptable, because the PGA112 and PGA113 devices have no separate DOUT pin to connect back to the microcontroller DIN pin to read back data in this configuration.



Figure 60. Daisy-Chain Write-Only Configuration

The maximum SCLK frequency that can be used in daisy-chain operation is directly related to SCLK rise and fall times, DIN setup time, and DOUT propagation delay. Any number of two or more devices have the same limitations because it is the timing considerations between adjacent devices that limit the clock speed.

Figure 61 analyzes the maximum SCLK frequency for daisy-chain mode based on the circuit of Figure 59. A clock rise and fall time of 10 ns is assumed to allow for extra bus capacitance that could occur as a result of multiple devices in the daisy-chain.





Figure 61. Daisy-Chain Maximum SCLK Frequency

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Figure 62. SPI Serial Interface Timing Diagrams

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Daisy-Chain SPI Write, Mode = 0,0 CS 12 10 11 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 SCLK DOUT D4 D3 D2 D1 D0 D15 D14 D13 D12 D11 D10 D9 D8 X D7 X D6 D4 D3 D15 XD14 XD13 XD12 XD11 XD10 D9 D8 D7 D6 D5 (D5) D2 (D1) D0 DIN1 Command U1 Command U2 DOUT1 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 $\sqrt{D5}$ $\sqrt{D4}$ $\sqrt{D3}$ $\sqrt{D2}$ < D1) (D0 DIN2 DOUT Hi-Z Pulled Low by DIN Weak Pull-Down Command U2 Daisy-Chain SPI Write, Mode = 1,1 CS 15 16 10 11 12 13 20 21 22 23 32 17 19 25 SCLK DOUT





DO

D4) D3 D2 D1 DO





Figure 64. SPI Daisy-Chain Read Timing Diagram (Mode 0,0)

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Figure 65. SPI Daisy-Chain Read Timing Diagram (Mode 1,1)



0

0

0

1

SDN_EN WRITE

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D1

0 0 1

1

8.6.4 SPI Commands

0

1

0

0

0

1

5	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	THREE-WIRE SPI COMMAND
	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	READ
	0	1	0	1	0	1	0	G3	G2	G1	G0	СНЗ	CH2	CH1	CH0	WRITE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NOP WRITE
	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	SDN_DIS WRITE

Table 3. SPI Commands (PGA112 and PGA113)⁽¹⁾⁽²⁾

(1) SDN = Shutdown mode. Enter Shutdown mode by issuing an SDN_EN command. Shutdown mode is cleared (returned to the last valid write configuration) by a SDN_DIS command or by any valid Write command.

(2) POR (Power-on-Reset) value of internal Gain/Channel Select Register is all 0s; this value sets Gain = 1, and Channel = V_{CAL}/CH0.

1

Table 4. S	SPI Dais	v-Chain	Commands	(1)(2)
------------	----------	---------	----------	--------

1

1

1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DAISY-CHAIN COMMAND
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	NOP
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	SDN_DIS
1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	SDN_EN
0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	READ
0	0	1	1	1	0	1	0	G3	G2	G1	G0	CH3	CH2	CH1	CH0	WRITE

(1) SDN = Shutdown Mode. Shutdown Mode is entered by an SDN_EN command. Shutdown Mode is cleared (returned to the last valid write configuration) by a SDN_DIS command or by any valid Write command.

(2) POR (Power-on-Reset) value of internal Gain/Channel Register is all 0s; this value sets Gain = 1, V_{CAL}/CH0 selected.

Table 5. Gain Selection Bits (PGA112 and PGA113)

G3	G2	G1	G0	BINARY GAIN	SCOPE GAIN
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	4	5
0	0	1	1	8	10
0	1	0	0	16	20
0	1	0	1	32	50
0	1	1	0	64	100
0	1	1	1	128	200

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Table 6. MUX Channel Selection Bits

СНЗ	CH2	CH1	CH0	PGA112, PGA113	PGA116, PGA117
0	0	0	0	VCAL/CH0	VCAL/CH0
0	0	0	1	CH1	CH1
0	0	1	0	X ⁽¹⁾	CH2
0	0	1	1	X	CH3
0	1	0	0	X	CH4
0	1	0	1	X	CH5
0	1	1	0	X	CH6
0	1	1	1	X	CH7
1	0	0	0	X	CH8
1	0	0	1	X	CH9
1	0	1	0	X	X ⁽¹⁾
1	0	1	1	Factory Reserved	Factory Reserved
1	1	0	0	CAL1 ⁽²⁾	CAL1 ⁽²⁾
1	1	0	1	CAL2 ⁽³⁾	CAL2 ⁽³⁾
1	1	1	0	CAL3 ⁽⁴⁾	CAL3 ⁽⁴⁾
1	1	1	1	CAL4 ⁽⁵⁾	CAL4 ⁽⁵⁾

X = channel is not used. (1)

CAL1: connects to GND. (2)

(3) CAL2: connects to 0.9 V_{CAL} . (4) CAL3: connects to 0.1 V_{CAL} .

(5) CAL4: connects to V_{REF}.

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The PGA11x family of devices are single-ended input, single-supply, programmable gain amplifiers (PGAs) with an input multiplexer. Multiplexer channel selection and gain selection are done through a standard SPI interface. The PGA112 and PGA113 have a two-channel input MUX and the PGA116 and PGA117 devices have a 10channel input MUX. The PGA112 and PGA116 devices provide binary gain selections (1, 2, 4, 8, 16, 32, 64, 128) and the PGA113 and PGA117 devices provide scope gain selections (1, 2, 5, 10, 20, 50, 100, 200). All models use a split-supply architecture with an analog supply, AV_{DD}, and a digital supply, DV_{DD}. This split-supply architecture allows for ease of interface to analog-to-digital converters (ADCs) and microcontrollers in mixedsupply voltage systems, such as where the analog supply is 5 V and the digital supply is 3 V. Four internal calibration channels are provided for system-level calibration. The channels are tied to GND, 0.9 V_{CAL}, 0.1 V_{CAL}, and V_{REF} , respectively. V_{CAL} , an external voltage connected to V_{CAL} /CH0, acts as the system calibration reference. If V_{CAL} is the system ADC reference, then gain and offset calibration on the ADC are easily accomplished through the PGA11x devices using only one MUX input. If calibration is not used, then V_{CAL}/CH0 can be used as a standard MUX input. All four versions provide a V_{RFF} pin that can be tied to ground or, for ease of scaling, to midsupply in single-supply systems where midsupply is used as a virtual ground. The PGA112 and PGA113 devices offer a software-controlled shutdown feature for low standby power. The PGA116 and PGA117 devices offer both hardware- and software-controlled shutdown for low standby power. The PGA112 and PGA113 devices have a 3-wire SPI digital interface; the PGA116 and PGA117 devices have a four-wire SPI digital interface. The PGA116 and PGA117 devices also have daisy-chain capability.

9.1.1 Op Amp: Input Stage

The PGA op amp is a rail-to-rail input and output (RRIO) single-supply op amp. The input topology uses two separate input stages in parallel to achieve rail-to-rail input. As Figure 66 shows, there is a PMOS transistor on each input for operation down to ground; there is also an NMOS transistor on each input in parallel for operation to the positive supply rail. When the common-mode input voltage (that is, the single-ended input, because this PGA is configured internally for noninverting gain) crosses a level that is typically about 1.5 V less than the positive supply, there is a transition between the NMOS and PMOS transistors. The result of this transition appears as a small input offset voltage transition that is reflected to the output by the selected PGA gain. This transition may be either increasing or decreasing, and differs from part to part as described in Figure 67 and Figure 68. These figures illustrate possible differences in input offset voltage between two different devices when used with $AV_{DD} = 5$ V. Because the exact transition region varies from device to device, the *Electrical Characteristics:* $V_S = AV_{DD} = DV_{DD} = 5$ V table specifies an input offset voltage above and below this input transition region.

Application Information (continued)







Figure 67. V_{OS} Versus Input Voltage—Case 1



Figure 68. V_{os} Versus Input Voltage—Case 2

9.1.2 Op Amp: General Gain Equations

Figure 69 shows the basic configuration for using the PGA as a gain block. V_{OUT} / V_{IN} is the selected noninverting gain, depending on the model selected, for either binary or scope gains.



Application Information (continued)



Figure 69. PGA Used as a Gain Block

$$V_{OUT} = G \times V_{IN}$$

where

- G = 1, 2, 4, 8, 16, 32, 64, and 128 (binary gains)
- G = 1, 2, 5, 10, 20, 50, 100, and 200 (scope gains)

(1)

Figure 70 shows the PGA configuration and gain equations for $V_{REF} = AV_{DD}/2$. V_{OUT0} is V_{OUT} when CH0 is selected and V_{OUT1} is V_{OUT} when CH1 is selected. Notice the V_{REF} pin has no effect for G = 1 because the internal feedback resistor, R_F , is shorted out. This configuration allows for positive and negative voltage excursions around a midsupply virtual ground.



Figure 70. PGA112 and PGA113 Configuration for Positive and Negative Excursions Around Midsupply Virtual Ground

$$V_{OUT0} = G \times V_{IN0} - AV_{DD}/2 \times (G - 1)$$

(2)

(3)

When: G = 1

Then: $V_{OUT0} = G \times V_{IN0}$

$$\begin{aligned} V_{\text{OUT1}} &= G \times (V_{\text{IN1}} + AV_{\text{DD}}/2) - AV_{\text{DD}}/2 \times (G-1) \\ V_{\text{OUT1}} &= G \times V_{\text{IN1}} + AV_{\text{DD}}/2, \text{ where: } -AV_{\text{DD}}/2 < G \times V_{\text{IN1}} < +AV_{\text{DD}}/2 \end{aligned}$$

where

- G = 1, 2, 4, 8, 16, 32, 64, and 128 (binary gains)
- G = 1, 2, 5, 10, 20, 50, 100, and 200 (scope gains)

Table 7 details the internal typical values for the op amp internal feedback resistor (R_F) and op amp internal input resistor (R_I) for both binary and scope gains.

3.25 k

3.25 k

(4)

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Application Information (continued)

BINARY GAIN (V/V)	R _F (Ω)	R _I (Ω)	SCOPE GAIN (V/V)	R _F (Ω)	R _I (Ω)								
1	0	3.25 k	1	0	3.25 k								
2	3.25 k	3.25 k	2	3.25 k	3.25 k								
4	9.75 k	3.25 k	5	13 k	3.25 k								
8	22.75 k	3.25 k	10	29.25 k	3.25 k								
16	48.75 k	3.25 k	20	61.75 k	3.25 k								
32	100.75 k	3.25 k	50	159.25 k	3.25 k								

Table 7. Typical R_F and R₁ Versus Gain

9.1.3 Op Amp: Frequency Response Versus Gain

204.75 k

412.75 k

Table 8 documents how small-signal bandwidth and slew rate change correspond to changes in PGA gain.

3.25 k

3.25 k

Full power bandwidth (that is, the highest frequency that a sine wave can pass through the PGA for a given gain) is related to slew rate by Equation 4:

100

200

321.75 k

646.75 k

SR (V/ μ s) = 2 π f × V_{OP} (1 × 10⁻⁶)

where

64

128

- SR = Slew rate in V/µs
- f = Frequency in Hz
- V_{OP} = Output peak voltage in volts

9.1.3.1 Example:

For G = 8, then SR = 10.6 V/ μ s (slew rate rise is minimum slew rate).

For a 5-V system, choose 0.1 V < V_{OUT} < 4.9 V or V_{OUTPP} = 4.8 V or V_{OUTP} = 2.4 V.

SR (V/ μ s) = 2 π f × V_{OP} (1 × 10⁻⁶).

 $10.6 = 2\pi f (2.4) (1 \times 10^{-6}) \rightarrow f = 702.9 \text{ kHz}$

This example shows that a G = 8 configuration can produce a $4.8-V_{PP}$ sine wave with frequency up to 702.9 kHz. This computation only shows the theoretical upper limit of frequency for this example, but does not indicate the distortion of the sine wave. The acceptable distortion depends on the specific application. As a general guideline, maintain two to three times the calculated slew rate to minimize distortion on the sine wave. For this example, the application should only use G = 8, 4.8 V_{PP}, up to a frequency range of 234 kHz to 351 kHz, depending upon the acceptable distortion. For a given gain and slew rate requirement, check for adequate small-signal bandwidth (typical –3-dB frequency) to assure that the frequency of the signal can be passed without attenuation.

9.1.4 Analog MUX

The analog input MUX provides two input channels for the PGA112 and PGA113 devices and 10 input channels for the PGA116 and PGA117 devices. The MUX switches are designed to be break-before-make and thereby eliminate any concerns about shorting the two input signal sources together.

Four internal MUX CAL channels are included in the analog MUX for ease of system calibration. These CAL channels allow ADC gain and offset errors to be calibrated out. This calibration does not remove the offset and gain errors of the PGA for gains greater than 1, but most systems should see a significant increase in the ADC accuracy. In addition, these CAL channels can be used by the ADC to read the minimum and maximum possible voltages from the PGA. With these minimum and maximum levels known, the system architecture can be designed to indicate an out-of-range condition on the measured analog input signals if these levels are ever measured.



To use the CAL channels, V_{CAL} /CH0 must be permanently connected to the system ADC reference. There is a typical 100-k Ω load from V_{CAL} /CH0 to ground. Table 9 illustrates how to use the CAL channels with V_{REF} = ground. Table 10 describes how to use the CAL channels with V_{REF} = AV_{DD}/2. The V_{REF} pin must be connected to a source that is low-impedance for both DC and AC to maintain gain and nonlinearity accuracy. Worst-case current demand on the V_{REF} pin occurs when G = 1 because there is a 3.25-k Ω resistor between V_{OUT} and V_{REF}. For a 5-V system with AV_{DD}/2 = 2.5 V, the V_{REF} pin buffer must source and sink 2.5 V/3.25 k Ω = 0.7 mA minimum for a V_{OUT} that can swing from ground to 5 V.

BINARY GAIN (V/V)	TYPICAL –3dB FREQUENCY (MHz)	SLEW RATE- FALL (V/µs)	SLEW RATE- RISE (V/µs)	0.1% SETTLING TIME: 4V _{PP} (μs)	0.01% SETTLING TIME: 4V _{PP} (μs)	SCOPE GAIN (V/V)	TYPICAL –3dB FREQUENCY (MHz)	SLEW RATE- FALL (V/µs)	SLEW RATE- RISE (V/µs)	0.1% SETTLING TIME: 4V _{PP} (μs)	0.01% SETTLING TIME: 4V _{PP} (μs)
1	10	8	3	2	2.55	1	10	8	3	2	2.55
2	3.8	9	6.4	2	2.6	2	3.8	9	6.4	2	2.6
4	2	12.8	10.6	2	2.6	5	1.8	12.8	10.6	2	2.6
8	1.8	12.8	10.6	2	2.6	10	1.8	12.8	10.6	2.2	2.6
16	1.6	12.8	12.8	2.3	2.6	20	1.3	12.8	9.1	2.3	2.8
32	1.8	12.8	13.3	2.3	3	50	0.9	9.1	7.1	2.4	3.8
64	0.6	4	3.5	3	6	100	0.38	4	3.5	4.4	7
128	0.35	2.5	2.5	4.8	8	200	0.23	2.3	2	6.9	10

Table 8. Frequency Response versus Gain (C_L = 100 pf, R_L= 10 k ω)



Figure 71. Using CAL Channels With V_{REF} = Ground

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Table 9. Using the MUX CAL Channels With $V_{REF} = GND$ (AV_{DD} = 3 V, DV_{DD} = 3 V, ADC Ref = 2.5 V, and $V_{REF} = GND$)

FUNCTION	MUX SELECT	GAIN SELECT	MUX INPUT	OP AMP (+ln)	ОР АМР (V _{OUT})	DESCRIPTION
Minimum Signal	CAL1	1	GND	GND	50 mV	Minimum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by negative saturation.
Gain Calibration	CAL2	1	0.9 × (V _{CAL} /CH0)	2.25 V	2.25 V	90% ADC Ref for system full- scale or gain calibration of the ADC.
Maximum Signal	CAL2	2	0.9 × (V _{CAL} /CH0)	2.25 V	2.95 V	Maximum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by positive saturation. System is limited by ADC max input of 2.5 V (ADC Ref = 2.5 V).
Offset Calibration	CAL3	1	0.1 × (V _{CAL} /CH0)	0.25 V	0.25 V	10% ADC Ref for system offset calibration of the ADC.
Minimum Signal	CAL4	1	V _{REF}	GND	50 mV	Minimum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by negative saturation.







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Table 10. Using the MUX CAL Channels With $V_{REF} = AV_{DD}/2$ (Av_{DD} = 3 V, DV_{DD} = 3 V, ADC Ref = 3 V, and $V_{REF} = 1.5$ V) (continued)

FUNCTION	MUX SELECT	GAIN SELECT	MUX INPUT	OP AMP (+ln)	ОР АМР (V _{оит})	DESCRIPTION					
Minimum Signal	CAL1	1	GND	GND	50 mV	Minimum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by negative saturation.					
Gain Calibration	CAL2	1	0.9 × (V _{CAL} /CH0)	2.7 V	2.7 V	90% ADC Ref for system full-scale or gain calibration of the ADC.					
Maximum Signal	CAL2	4 or 5	0.9 × (V _{CAL} /CH0)	2.25 V	2.95 V	Maximum signal level that the MUX, op amp, and ADC can read. Op amp $V_{\rm OUT}$ is limited by positive saturation.					
Offset Calibration	CAL3	1	0.1 × (V _{CAL} /CH0)	0.3 V	0.3 V	10% ADC Ref for system offset calibration of the ADC.					
V _{REF} Check	CAL4	1	V _{REF}	1.5 V	1.5 V	Midsupply voltage used as V _{REF} .					

 $(Av_{DD} = 3 V, DV_{DD} = 3 V, ADC Ref = 3 V, and V_{REF} = 1.5 V)$

9.1.5 System Calibration Using The PGA

Analog-to-digital converters (ADCs) contain two major errors that can be easily removed by calibration at a system level. These errors are gain error and offset error, as shown in Figure 73. Figure 73 shows a typical transfer function for a 12-bit ADC. The analog input is on the x-axis with a range from 0 V to ($V_{REF_ADC} - 1LSB$), where V_{REF_ADC} is the ADC reference voltage. The y-axis is the hexadecimal equivalent of the digital codes that result from ADC conversions. The dotted red line represents an ideal transfer function with *0000h* representing 0 V analog input and *0FFFh* representing an analog input of ($V_{REF_ADC} - 1LSB$). The solid blue line illustrates the offset error. Although the solid blue line includes both offset error and gain error, at an analog input of 0 V the offset error voltage, V_{Z_ACTUAL} , can be measured. The dashed black line represents the transfer function with gain error. The dashed black line is equivalent to the solid blue line without the offset error, and can be measured and computed using V_{Z_ACTUAL} and V_{Z_IDEAL} . The difference between the dashed black line and the dotted red line is the gain error. Gain and offset error can be computed by taking zero input and full-scale input readings. Using these error calculations, compute a calibrated ADC reading to remove the ADC gain and offset error.





Figure 73. ADC Offset and Gain Error

In practice, the zero input (0 V) or full-scale input ($V_{REF_ADC} - 1LSB$) of ADCs cannot always be measured because of internal offset error and gain error. However, if measurements are made very close to the full-scale input and the zero input, both zero and full-scale can be calibrated very accurately with the assumption of linearity from the calibration points to the desired end points of the ADC ideal transfer function. For the zero calibration, choose $10\%V_{REF_ADC}$; this value should be above the internal offset error and sufficiently out of the noise floor range of the ADC. For the gain calibration, choose $90\%V_{REF_ADC}$; this value should be less than the internal gain error and sufficiently below the tolerance of V_{REF} . These key points can be summarized in this way:

For zero calibration:

- The ADC cannot read the ideal zero because of offset error
- Must be far enough above ground to be above noise floor and ADC offset error
- Therefore, choose 10%V_{REF_ADC} for zero calibration

For gain calibration:

- The ADC cannot read the ideal full-scale because of gain error
- Must be far enough below full-scale to be below the V_{REF} tolerance and ADC gain error
- Therefore, choose 90%V_{REF_ADC} for gain calibration

The 12-bit ADC example in Figure 74 illustrates the technique for calibrating an ADC using a $10\%V_{REF_ADC}$ and $90\%V_{REF_ADC}$ reading where V_{REF_ADC} is the ADC reference voltage. The $10\%V_{REF}$ reading also contains a gain error because it is not a $V_{IN} = 0$ calibration point. First, use the $90\%V_{REF}$ and $10\%V_{REF}$ points to compute the measured gain error. The measured gain error is then used to remove the gain error from the $10\%V_{REF}$ reading, giving a measured $10\%V_{REF}$ number. The measured $10\%V_{REF}$ number is used to compute the measured offset error.

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Figure 74. 12-Bit Example of ADC Calibration for Gain and Offset Error

The gain error and offset error in ADC readings can be calibrated by using $10\% V_{REF_ADC}$ and $90\% V_{REF_ADC}$ calibration points. Because the calibration is ratiometric to V_{REF_ADC} , the exact value of V_{REF_ADC} does not need to be known in the end application.

Follow these steps to compute a calibrated ADC reading:

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1. Take the ADC reading at $V_{IN} = 90\% \times V_{REF}$ and $V_{IN} = 10\% \times V_{REF}$. The ADC readings for $10\% V_{REF}$ and $90\% V_{REF}$ are taken.

$V_{\text{REF}}90 = 0.9(V_{\text{REF}_ADC})$	(5)
$V_{\text{REF}}10 = 0.1(V_{\text{REF}_\text{ADC}})$	(6)
$V_{\text{MEAS}}90 = \text{ADC}_{\text{MEASUREMENT}} \text{ at } V_{\text{REF}}90$	(7)
$V_{MEAS}10 = ADC_{MEASUBEMENT}$ at $V_{BEE}10$	(8)

2. Compute the ADC measured gain. The slope of the curve connecting the measured $10\% V_{REF}$ and measured $90\% V_{REF}$ point is computed and compared to the slope between the ideal $10\% V_{REF}$ and ideal $90\% V_{REF}$. This result is the measured gain.

$$G_{MEAS} = \frac{V_{MEAS}90 - V_{MEAS}10}{V_{REF}90 - V_{REF}10}$$
(9)

3. Compute the ADC measured offset. The measured offset is computed by taking the difference between the measured $10\% V_{REF}$ and the (ideal $10\% V_{REF}$) × (measured gain).

$$O_{\text{MEAS}} = V_{\text{MEAS}} 10 - (V_{\text{REF}} 10 \times G_{\text{MEAS}})$$
(10)

4. Compute the calibrated ADC readings.

 $V_{AD MEAS} = Any V_{IN} ADC_{MEASUREMENT}$

$$V_{ADC_CAL} = \frac{V_{AD_MEAS} - O_{MEAS}}{G_{MEAS}}$$
(12)

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(11)

PGA112, PGA113, PGA116, PGA117

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Any ADC reading can therefore be calibrated by removing the gain error and offset error. The measured offset is subtracted from the ADC reading and then divided by the measured gain to give a corrected reading. If this calibration is performed on a timed basis, relative to the specific application, gain and offset error over temperature are also removed from the ADC reading by calibration.

For example; given:

- 12-Bit ADC
- ADC Gain Error = 6 LSB
- ADC Offset Error = 4 LSB
- ADC Reference (V_{REF ADC}) = 5 V
- Temperature = 25°C

Table 11 shows the resulting system accuracy.

Table 11. Bits of System Accuracy⁽¹⁾ (To 0.5 LSB)

V _{IN}	ADC ACCURACY WITHOUT CALIBRATION	ADC ACCURACY WITH PGA112 CALIBRATION
10%V _{REF_ADC}	8.80 Bits	12.80 Bits
90%V _{REF_ADC}	7.77 Bits	11.06 Bits

(1) Difference in maximum input offset voltage for $V_{IN} = 10\% V_{REF_ADC}$ and $V_{IN} = 90\% V_{REF_ADC}$ is the reason for different accuracies.

9.1.6 Driving and Interfacing to ADCs

CDAC SAR ADCs contain an input sampling capacitor, C_{SH} , to sample the input signal during a sample period as shown in Figure 75. After the sample period, C_{SH} is removed from the input signal. Subsequent comparisons of the charge stored on C_{SH} are performed during the ADC conversion process. To achieve optimal op amp stability, input signal settling, and the demands for charge from the input signal conditioning circuitry, most ADC applications are optimized by the use of a resistor (R_{FILT}) and capacitor (C_{FILT}) filter placed between the op amp output and ADC input. For the PGA112 and PGA113 devices, or the PGA116 and PGA117 devices, setting C_{FILT} = 1 nF and R_{FILT} = 100 Ω yields optimum system performance for sampling converters operating at speeds up to 500 kHz, depending upon the application settling time and accuracy requirements.







9.1.7 Power Supplies

Figure 76 shows a typical mixed-supply voltage system where the analog supply, AV_{DD} , is 5 V and the digital supply voltage, DV_{DD} , is 3 V. The analog output stage of the PGA and the SPI interface digital circuitry are both powered from DV_{DD} . When considering the power required for DV_{DD} , use the *Electrical Characteristics:* $V_S = AV_{DD} = DV_{DD} = 5 V$ table and add any load current anticipated on V_{OUT} ; this load current must be provided by DV_{DD} . This split-supply architecture ensures compatible logic levels with the microcontroller. It also ensures that the PGA output cannot run the input for the onboard ADC into an overvoltage condition; this condition could cause device latch-up and system lock-up, and require power-supply sequencing. Each supply pin should be individually bypassed with a 0.1 µF ceramic capacitor directly at the device to ground. If there is only one power supply in the system, AV_{DD} and DV_{DD} can both be connected to the same supply; however, TI recommends using individual bypass capacitors directly at each respective supply pin to a single point ground. V_{OUT} is diodeclamped to AV_{DD} (as shown in Figure 76); therefore, set DV_{DD} less than or equal to $AV_{DD} + 0.3 V$. DV_{DD} and AV_{DD} must be within the operating voltage range of 2.2 V to 5.5 V.

At initial power-on, the state of the PGA is G = 1 and Channel 0 active.

NOTE

For most applications, set $AV_{DD} \ge DV_{DD}$ to prevent V_{OUT} from driving current into AV_{DD} and raising the voltage level of AV_{DD}

9.1.8 Shutdown and Power-On-Reset (POR)

The PGA112 and PGA113 devices have a software shutdown mode, and the PGA116 and PGA117 devices offer both a hardware and software shutdown mode. When the PGA11x is shut down, it goes into a low-power standby mode. The *Electrical Characteristics:* $V_S = AV_{DD} = DV_{DD} = 5$ V table details the current draw in shutdown mode with and without the SPI interface being clocked. In shutdown mode, R_F and R_I remain connected between V_{OUT} and V_{REF}.

When DV_{DD} is less than 1.6 V, the digital interface is disabled and the channel and gain selections are held to the respective POR states of Gain = 1 and Channel = V_{CAL} /CH0. When DV_{DD} is above 1.8 V, the digital interface is enabled and the POR gain and channel states remain unchanged until a valid SPI communication is received.



Figure 76. Split Power-Supply Architecture: $AV_{DD} \neq Dv_{DD}$





Figure 77. PGA112, PGA113 (VSSOP-10) Typical Application Schematic

9.1.9 Typical Connections: PGA116, PGA117 (TSSOP-20)







9.2 Typical Applications

9.2.1 Bipolar Input to Single-Supply Scaling



Figure 79. Bipolar to Single-Ended Input Algorithm

9.2.1.1 Design Requirements

V _{REF ADC} (V)	V _{IN1} (V)	CH1 INPUT	R _A (kΩ)	R _X (Ω)	R _B (kΩ)
2.5	-5	0.047613	9.2	4.81 k	10
	0	1.247613			
	5	2.447613			
2.5	-10	0.050317	3.16	2.4 k	10
	0	1.250317			
	10	2.450317			
3	-5	0.058003	13.5	5.76 k	10
	0	1.498003			
	5	2.938003			
3	-10	0.059303	4.02	2.87 k	10
	0	1.499303			
	10	2.939303			
4.096	-5	0.082224	37	7.87 k	10
	0	2.048304			
	5	4.014384			
4.096	-10	0.086018	6.49	3.92 k	10
	0	2.052098			
	10	4.018178			
5	-5	0.093506	24	965	10
	0	2.493506			
	5	4.893506			
5	-10	0.095227	9.2	4.81 k	10
	0	2.495227			
	10	4.895227			

Table 12. Bipolar to Single-Ended Input Scaling⁽¹⁾⁽²⁾

Scaling is based on 0.02(V_{REF_ADC}) to 0.98(V_{REF_ADC}), using standard 0.1% resistor values. Assumes symmetrical V_{IN} and symmetrical scaling for CH1 input minimum and maximum. (1)

(2)

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This process assumes a symmetrical VIN1 and that symmetrical scaling is used for CH1 input minimum and maximum values. The following steps give the algorithm to compute resistor values for references not listed in Table 12.

Step 1: Choose the following:

- a. $V_{REF ADC} = 2.5 V$ (ADC reference voltage)
- b. $|V_{IN1}| = 5$

(magnitude of V_{IN} , assuming scaling is for $\pm V_{IN1}$)

c. Choose R_B as a standard resistor value. The input on-channel current multiplied by R_B should be less than the input offset voltage, such that R_B is not a major source of inaccuracy.

 $R_{\rm B} = 10 \ \rm k\Omega$ (select as a starting value for resistors)

d. For the most negative V_{IN1}, choose the percentage (in decimal format) of V_{REF_ADC} desired at the ADC input.

 $k_{VO-} = 0.02$

(CH1 input = $k_{VO-} \times V_{REF_ADC}$ when $V_{IN1} = -V_{IN1}$)

e. For the most positive V_{IN1}, choose the percentage (in decimal format) of V_{REF ADC} desired at the ADC input. Because this scaling is based on symmetry, k_{VO+} must be the same percentage away from V_{REF_ADC} at the upper limit as at the lower limit where k_{VO-} is computed.

 $k_{VO+} = 1 - k_{VO-}$

 $k_{VO+} = 1 - 0.02 = 0.98$

(CH1 input = $k_{VO+} \times V_{REF ADC}$ when $V_{IN1} = +V_{IN1}$)

Step 2: Compute the following:

a. To simplify analysis, create one constant called k_{VO}.

$$k_{VO} = k_{VO+} - k_{VO-}$$

$$0.96 = 0.98 - 0.02$$
(13)

b. A constant, g, is created to simplify resistor value computations.

$$g = \frac{k_{VO} \times v_{REF_ADC}}{2 \times |V_{IN1}| - k_{VO} \times V_{REF_ADC}}$$

$$0.315789474 = \frac{0.96 \times 2.5}{2 \times 5 - 0.96 \times 2.5} \tag{14}$$

c. R_A is now selected from the starting value of R_B and the g constant.

$$R_{A} = \frac{2 \times R_{B} \times g}{1 - g}$$

$$9.23077k\Omega = \frac{2 \times 10k\Omega \times 0.315789474}{1 - 0.315789474}$$
(15)

d. R_x can now be computed from the starting value of R_B and the computed value for R_A .

$$R_{X} = \frac{R_{B} \times R_{A}}{R_{B} + R_{A}}$$

44

$$4.81k\Omega = \frac{10k\Omega \times 9.23077k\Omega}{10k\Omega + 9.23077k\Omega}$$
(16)

Product Folder Links: PGA112 PGA113 PGA116 PGA117





9.2.1.3 Application Curve



Figure 80. Voltage (V) vs Time (s)

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9.2.2 Typical Application: General-Purpose Input Scaling

Figure 81 is an example application that demonstrates the flexibility of the PGA for general-purpose input scaling. V_{IN0} is a ±100-mV input that is ac-coupled into CH0. The PGA112 and PGA113 are powered from a 5-V supply voltage, V_S , and configured with the V_{REF} pin connected to $V_S/2$ (2.5 V). V_{CH0} is the ±100-mV input, level-shifted and centered on $V_S/2$ (2.5 V). A gain of 20 is applied to CH0, and because of the PGA113 configuration, the output voltage at V_{OUT} is ±2 V centered on $V_S/2$ (2.5 V).

CH1 is set to G = 1; through a resistive divider and scalar network, we can read ± 5 V or 0 V. This setting provides bipolar to single-ended input scaling. Table 12 summarizes the scaling resistor values for R_A, R_X, and R_B for different ADC Ref voltages. V_{REF_ADC} is the reference voltage used for the ADC connected to the PGA112 and PGA113 output. It is assumed the ADC input range is 0 V to V_{REF_ADC}. The *Table 12* section gives the algorithm to compute resistor values for references not listed in Table 12. As a general guideline, R_B should be chosen such that the input on-channel current multiplied by R_B is less than or equal to the input offset voltage. This value ensures that the scaling network contributes no more error than the input offset voltage. Individual applications may require other design trade-offs.



Figure 81. General-Purpose Input Scaling

10 Power Supply Recommendations

Power-supply bypass: Bypass each power-supply pin separately. Use a ceramic capacitor connected directly from the power-supply pin to the ground pin of the IC on the same PCB plane. Vias can then be used to connect to ground and voltage planes. This configuration keeps parasitic inductive paths out of the local bypass for the PGA. Good analog design practice dictates the use of a large value tantalum bypass capacitor on the PCB for each respective voltage.



11 Layout

11.1 Layout Guidelines

11.1.1 High Gain and Wide Bandwidth Considerations

As a result of the combination of wide bandwidth and high gain capability of the PGA112 and PGA113 devices and PGA116 and PGA117 devices, there are several printed-circuit-board (PCB) design and system recommendations to consider for optimum application performance.

- 1. Power-supply bypass: Refer to Power Supply Recommendations.
- 2. **Signal trace routing:** Keep V_{OUT} and other low impedance traces away from MUX channel inputs that are high impedance. Poor signal routing can cause positive feedback, unwanted oscillations, or excessive overshoot and ringing on step-changing signals. If the input signals are particularly noisy, separate MUX input channels with guard traces on either side of the signal traces. Connect the guard traces to ground near the PGA and at the signal entry point into the PCB. On multilayer PCBs, ensure that there are no parallel traces near MUX input traces on adjacent layers; capacitive coupling from other layers can be a problem. Use ground planes to isolate MUX input signal traces from signal traces on other layers.

Additionally, group and route the digital signals into the PGA as far away as possible from the analog MUX input signals. Most digital signals are fast rise and fall time signals with low-impedance drive capability that can easily couple into the high-impedance inputs of the input MUX channels. This coupling can create unwanted noise that gains up to V_{OUT} .

3. Input MUX channels and source impedance: Input MUX channels are high-impedance; when combined with high gain, the channels can pick up unwanted noise. Keep the input signal sources low-impedance (< 10 k Ω). Also, consider bypassing input MUX channels with a ceramic bypass capacitor directly at the MUX input pin. Bypass capacitors greater than 100 pF are recommended. Lower impedances and a bypass capacitor placed directly at the input MUX channels keep crosstalk between channels to a minimum as a result of parasitic capacitive coupling from adjacent PCB traces and pin-to-pin capacitance.



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11.2 Layout Example









12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Shelf-Life Evaluation of Lead-Free Component Finishes, SZZA046.
- PGA112/113EVM Users Guide, SBOU073.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
PGA112	Click here	Click here	Click here	Click here	Click here
PGA113	Click here	Click here	Click here	Click here	Click here
PGA116	Click here	Click here	Click here	Click here	Click here
PGA117	Click here	Click here	Click here	Click here	Click here

Table 13. Related Links

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments. SPI is a trademark of Motorola. All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
				_			(6)				
PGA112AIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA112AIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA112AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA113AIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA113AIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA113AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA116AIPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA116AIPWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA116AIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA117AIPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA117	Samples
PGA117AIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA117	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



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⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA112AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA112AIDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PGA112AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA113AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA113AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA116AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PGA117AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

5-Jan-2022



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA112AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
PGA112AIDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
PGA112AIDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
PGA113AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
PGA113AIDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
PGA116AIPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
PGA117AIPWR	TSSOP	PW	20	2000	853.0	449.0	35.0



5-Jan-2022

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
PGA116AIPW	PW	TSSOP	20	70	530	10.2	3600	3.5
PGA116AIPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
PGA117AIPW	PW	TSSOP	20	70	530	10.2	3600	3.5

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0020A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0020A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



LAND PATTERN DATA



NOTES: Α. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
 C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



DGS0010A

EXAMPLE BOARD LAYOUT

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DGS0010A

EXAMPLE STENCIL DESIGN

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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