

PESD5V0L2UU; PESD6V0L2UU

Low capacitance unidirectional ESD protection diodes

Rev. 01 — 11 March 2009

Product data sheet

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1. Product profile

1.1 General description

Low capacitance unidirectional double ElectroStatic Discharge (ESD) protection diodes in a very small Surface-Mounted Device (SMD) plastic package designed to protect up to two signal lines from the damage caused by ESD and other transients.

Table 1. Product overview

Type number	Package		Package configuration
	NXP	JEITA	
PESD5V0L2UU	SOT323	SC-70	very small
PESD6V0L2UU			

1.2 Features

- Unidirectional ESD protection of up to two lines
- Low diode capacitance: $C_d = 34$ pF
- Max. peak pulse power: $P_{PP} = 70$ W
- Low clamping voltage: $V_{CL} = 13$ V
- Ultra low leakage current
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{PP} = 6.5$ A
- AEC-Q101 qualified

1.3 Applications

- Audio and video equipment
- Computers and peripherals
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection

1.4 Quick reference data

Table 2. Quick reference data

$T_{amb} = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage					
	PESD5V0L2UU		-	-	5.0	V
	PESD6V0L2UU		-	-	6.0	V

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Table 2. Quick reference data ...continued $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified.

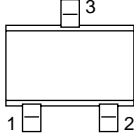
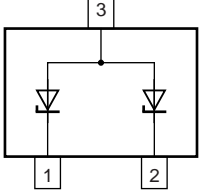
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _d	diode capacitance	f = 1 MHz; V _R = 0 V				
	PESD5V0L2UU		[1] -	19	23	pF
			[2] -	38	46	pF
	PESD6V0L2UU		[1] -	17	20	pF
			[2] -	34	40	pF

[1] Bidirectional configuration: measured from pin 1 to 2 or pin 2 to 1.

[2] Unidirectional configuration: measured from pin 1 to 3 or pin 2 to 3.

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode (diode 1)		
2	cathode (diode 2)		
3	common anode		

006aaa154

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0L2UU	SC-70	plastic surface-mounted package; 3 leads	SOT323
PESD6V0L2UU			

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PESD5V0L2UU	H1*
PESD6V0L2UU	H2*

[1] * = -: made in Hong Kong

* = p: made in Hong Kong

* = t: made in Malaysia

* = W: made in China

5. Limiting values

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Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
P _{PP}	peak pulse power	t _p = 8/20 μs	[1][2]		
	PESD5V0L2UU		-	70	W
	PESD6V0L2UU		-	60	W
I _{PP}	peak pulse current	t _p = 8/20 μs	[1][2]		
	PESD5V0L2UU		-	6.5	A
	PESD6V0L2UU		-	5.5	A
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	+150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

Table 7. ESD maximum ratings

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1] -	30	kV
		MIL-STD-883 (human body model)	[2] -	16	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 or 2 to pin 3.

Table 8. ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

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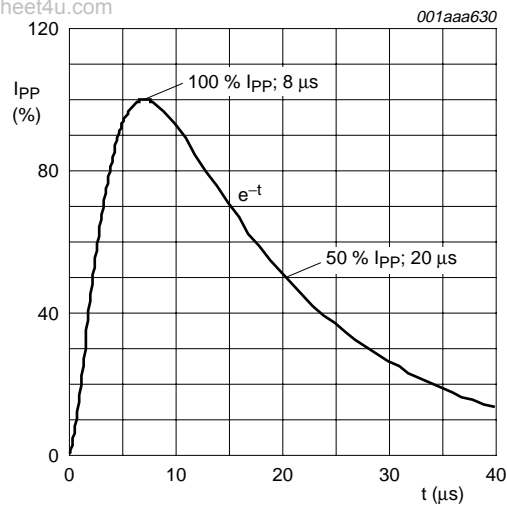


Fig 1. 8/20 μs pulse waveform according to IEC 61000-4-5

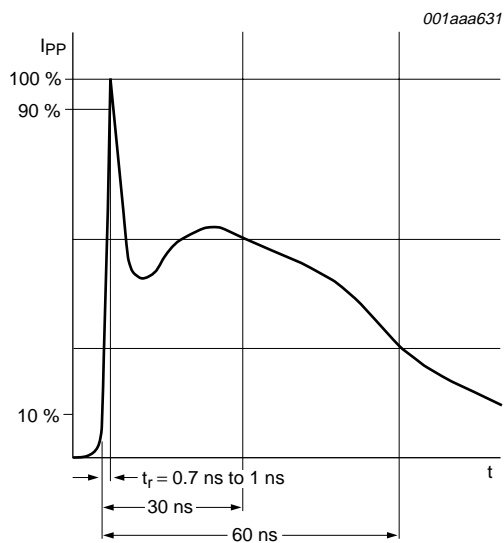


Fig 2. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

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Table 9. Characteristics

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified.

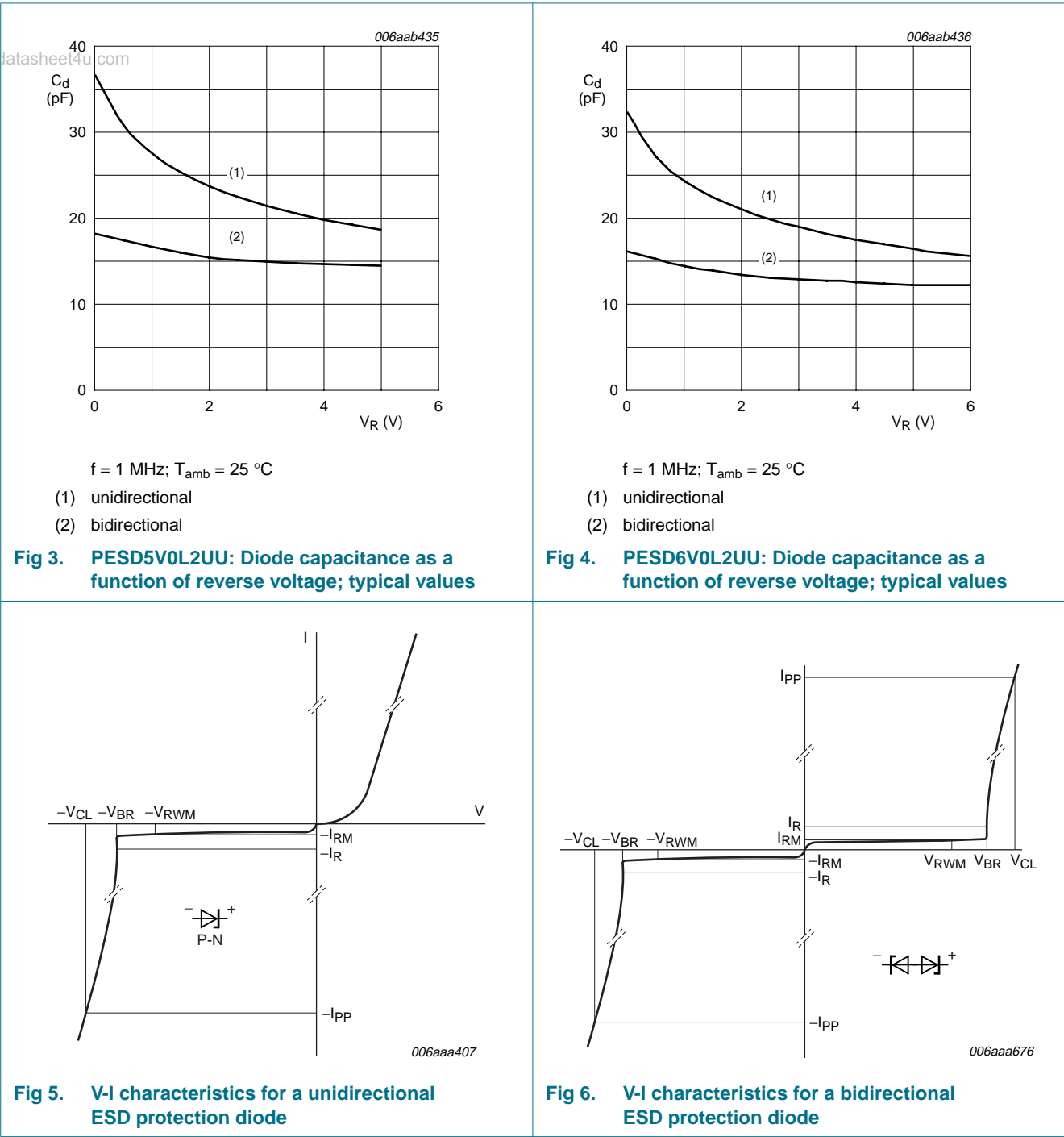
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage					
	PESD5V0L2UU		-	-	5.0	V
	PESD6V0L2UU		-	-	6.0	V
I_{RM}	reverse leakage current					
	PESD5V0L2UU	$V_{RWM} = 4.0\text{ V}$	-	20	90	nA
	PESD6V0L2UU	$V_{RWM} = 4.3\text{ V}$	-	1.5	18	nA
	PESD5V0L2UU	$V_{RWM} = 5.0\text{ V}$	-	430	-	nA
	PESD6V0L2UU	$V_{RWM} = 6.0\text{ V}$	-	310	-	nA
V_{BR}	breakdown voltage	$I_R = 5\text{ mA}$				
	PESD5V0L2UU		5.8	6.2	6.6	V
	PESD6V0L2UU		6.4	6.8	7.2	V
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$				
	PESD5V0L2UU	[1]	-	19	23	pF
		[2]	-	38	46	pF
	PESD6V0L2UU	[1]	-	17	20	pF
		[2]	-	34	40	pF
V_{CL}	clamping voltage	$I_{PP} = 5.5\text{ A}$	[3][4]			
	PESD5V0L2UU		-	-	13	V
	PESD6V0L2UU		-	-	13.5	V
r_{dif}	differential resistance	$I_R = 5\text{ mA}$				
	PESD5V0L2UU		-	-	25	Ω
	PESD6V0L2UU		-	-	30	Ω

[1] Bidirectional configuration: measured from pin 1 to 2 or pin 2 to 1.

[2] Unidirectional configuration: measured from pin 1 to 3 or pin 2 to 3.

[3] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[4] Measured from pin 1 or 2 to pin 3.



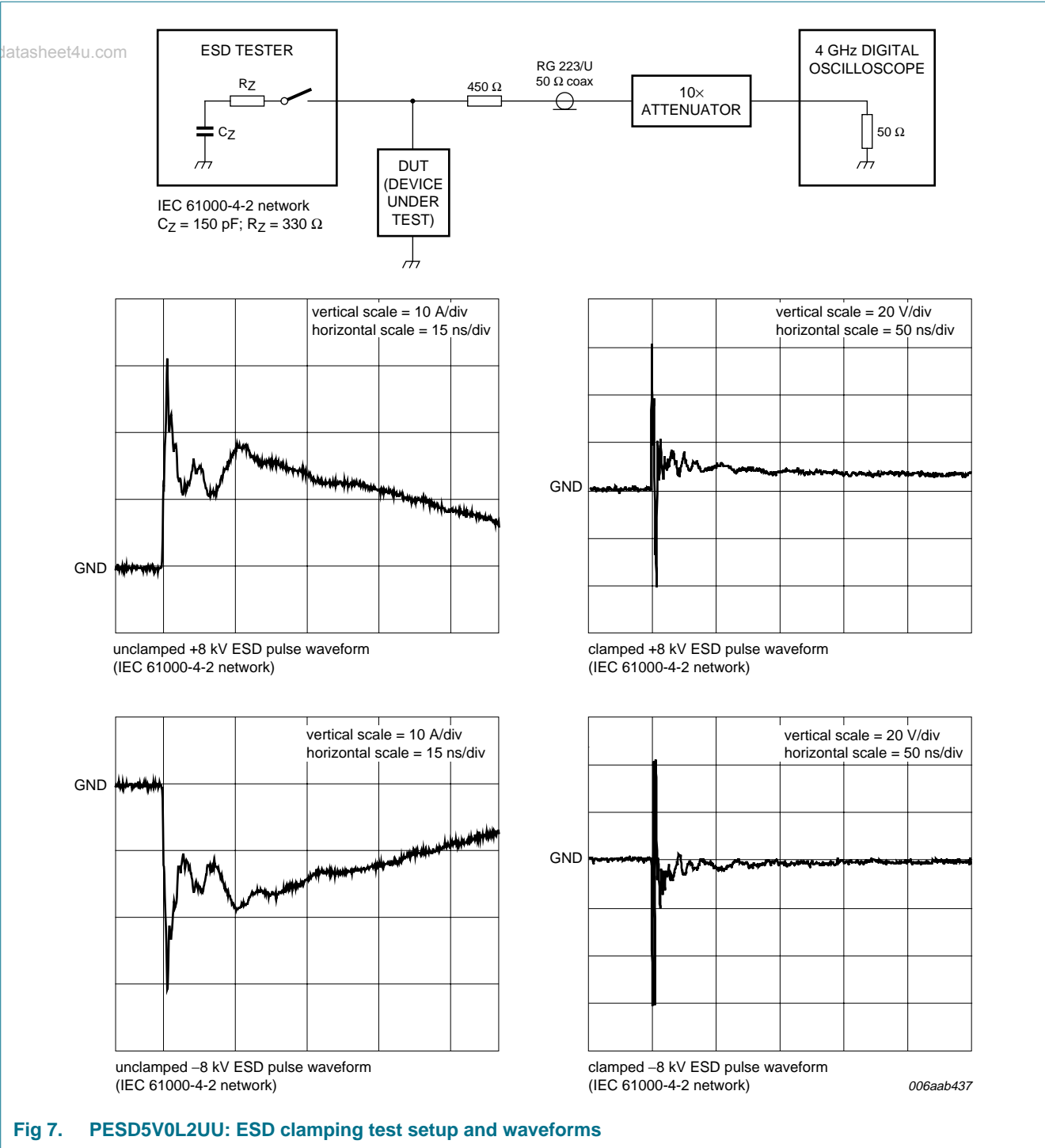


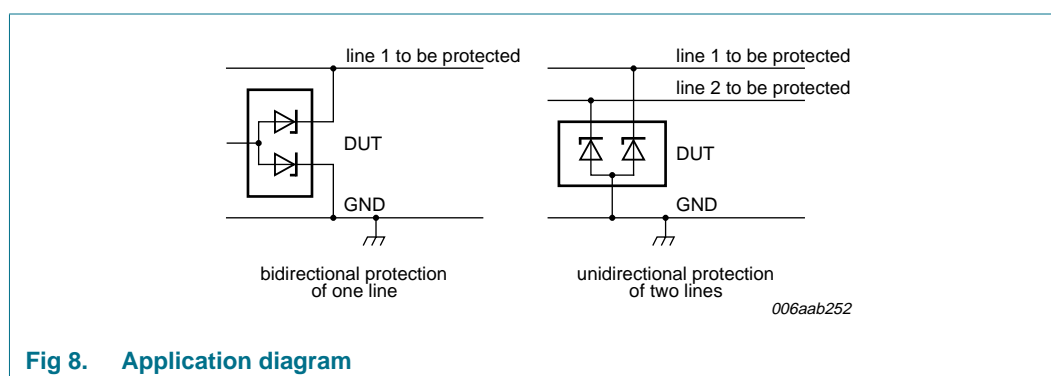
Fig 7. PESD5V0L2UU: ESD clamping test setup and waveforms

7. Application information

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PESD5V0L2UU and PESD6V0L2UU are designed for the protection of up to two unidirectional data or signal lines, or for the protection of one bidirectional data or signal line, from the damage caused by ESD. For unidirectional protection, the devices may be used on lines where the signal polarities are positive with respect to ground, and for bidirectional protection, the devices may be used on lines where the signal polarities are both, positive and negative with respect to ground.

For an 8/20 μ s waveform, the PESD5V0L2UU provides a surge capability of up to 70 W per line, and the PESD6V0L2UU provides a surge capability of up to 60 W per line.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD and Electrical Fast Transient (EFT). The following guidelines are recommended:

1. Place the devices as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

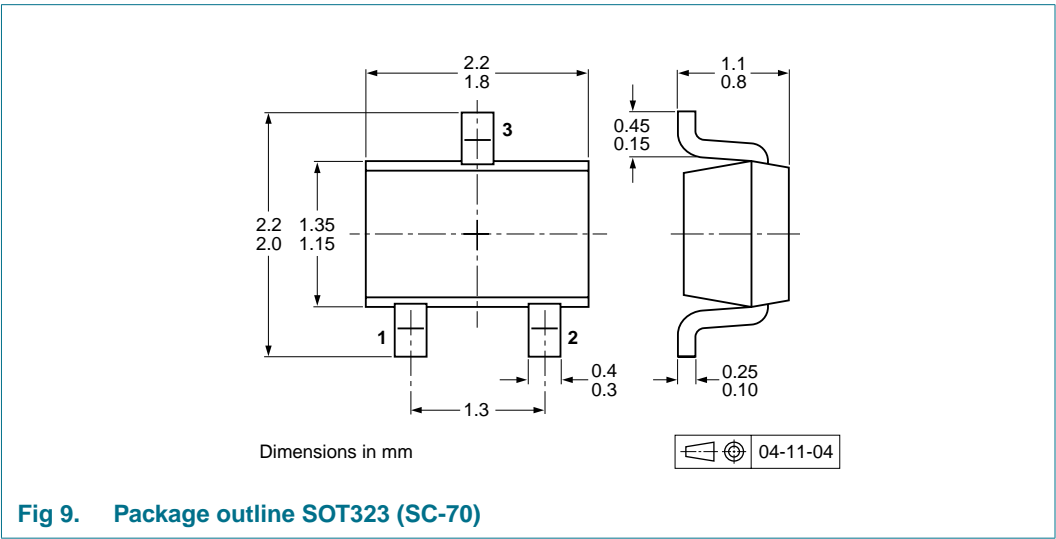
8. Test information

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8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

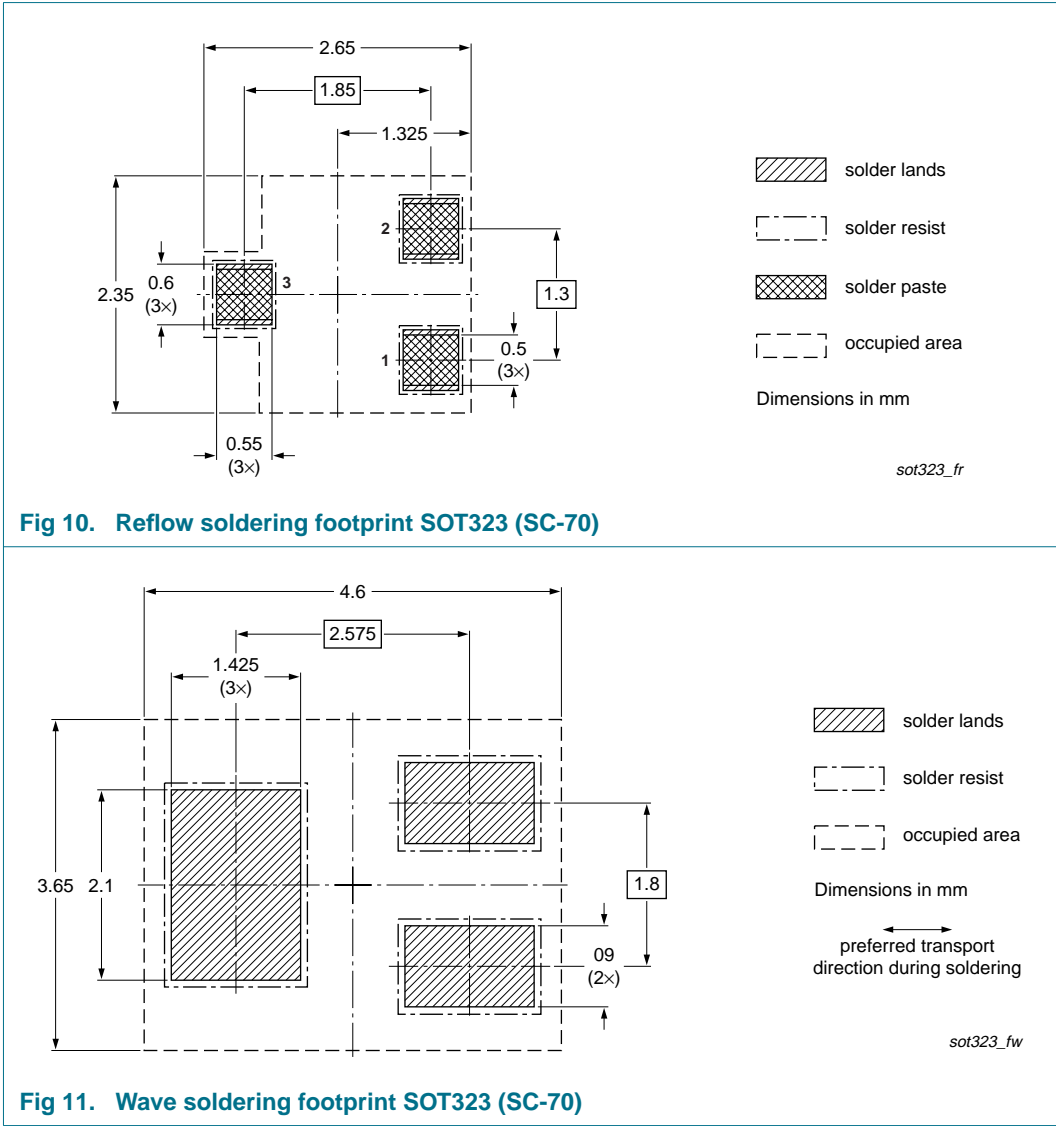
Table 10. Packing methods
The indicated -xxx are the last three digits of the 12NC ordering code.[\[1\]](#)

Type number	Package	Description	Packing quantity	
			3000	10000
PESD5V0L2UU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-135
PESD6V0L2UU				

[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering

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12. Revision history

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Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0L2UU_PESD6V0L2UU_1	20090311	Product data sheet	-	-

13. Legal information

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13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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