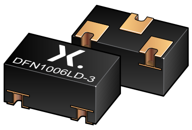

PESD5V0H2BFG-Q

Extremely low clamping bidirectional ESD protection diode

3 February 2025 Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode array, part of the TrEOS Protection family. This device is housed in a small leadless DFN1006LD-3 (SOT8079LD) Surface-Mounted Device (SMD) laminate package with side-wettable flanks. The device is designed to protect two automotive in-vehicle network bus lines from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra low capacitance: C_d < 0.25 pF
- ESD protection starting from 15 kV (IEC 61000-4-2)
- Deep snap-back combined with dynamic resistance of 0.35 Ω
- DFN1006LD-3 package with side-wettable flanks, performance optimized for high-speed networks
- Qualified according to AEC-Q101 / Automotive grade

3. Applications

ESD protection for in-vehicle network lines in automotive environments

- Ultra high-speed data lines such as USB 3.2 or HDMI 2.0
- Low-Voltage Differential Signaling (LVDS) automotive
- Automotive Multi-Gigabit Ethernet
- Automotive A/V monitors, displays and cameras

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	-	6.25	A
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[2]	-	-	0.25	pF

[1] According to IEC 61000-4-5.
[2] Measured from pin 1 or 2 to pin 3.

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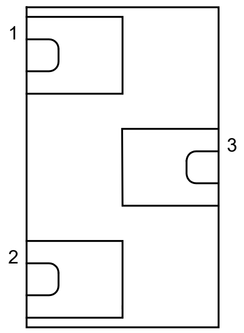
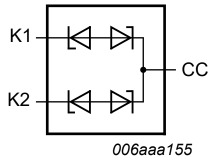
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DFN1006LD-3 (SOT8079LD-1)**	
2	K2	cathode (diode 2)		
3	CC	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0H2BFG-Q	DFN1006LD-3	Leadless ultra small plastic package with side-wettable flanks (SWF); 3 terminals; 0.7 mm pitch; 1 mm × 0.6 mm × 0.45 mm body	SOT8079LD-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0H2BFG-Q	A2

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	6.25	A
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	15	-	kV

[1] According to IEC 61000-4-5.
[2] Measured from pin 1 to pin 2.
[3] Device stressed with ten non-repetitive ESD pulses.

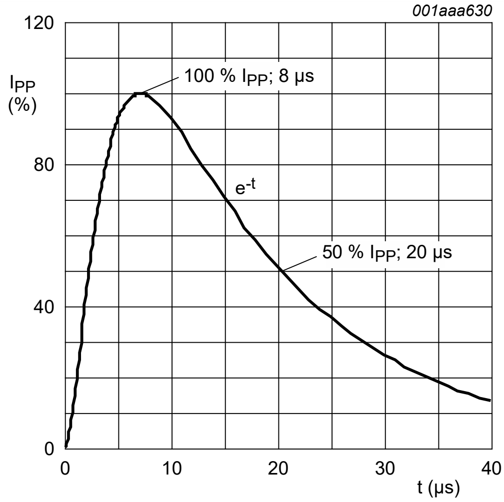


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

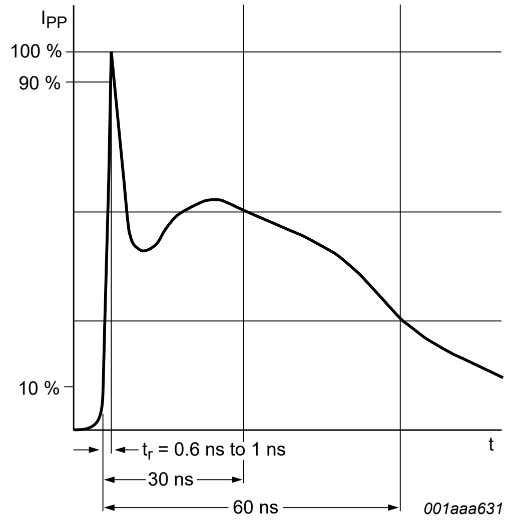


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
V_{BR}	breakdown voltage		[1]	6	10	-	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V; T_{amb} = 25 °C	[1]	-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	-	0.25	pF
V_{CL}	clamping voltage	I_{PPM} = 6.25 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1] [2]	-	5	-	V
		I_{PP} = 8 A; t_p = 100 ns; T_{amb} = 25 °C	[1] [3]	-	5	-	V
		I_{PP} = 16 A; t_p = 100 ns; T_{amb} = 25 °C	[1] [3]	-	7	-	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[1] [3]	-	0.35	-	Ω

[1] Measured from pin 1 or 2 to pin 3.
[2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

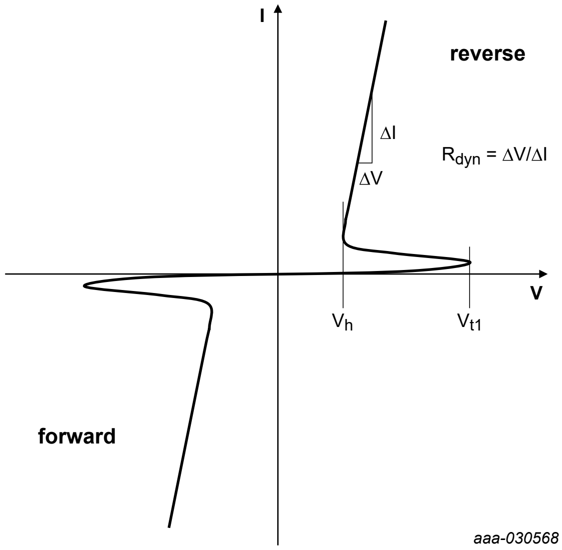


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

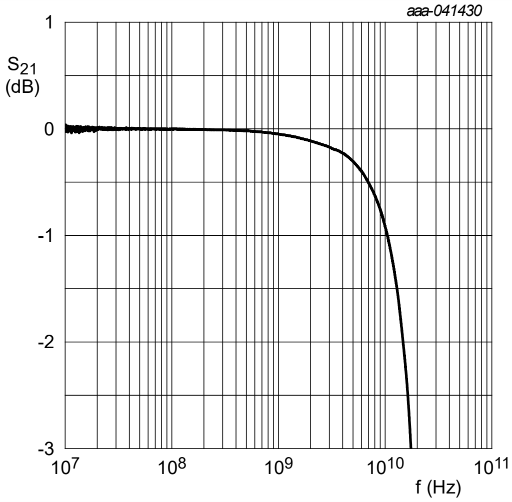


Fig. 4. Insertion loss; typical values

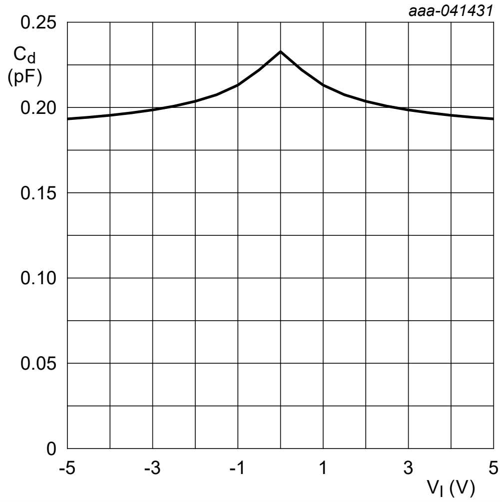
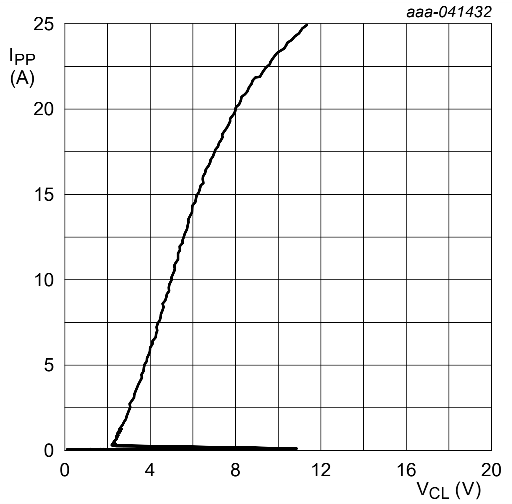
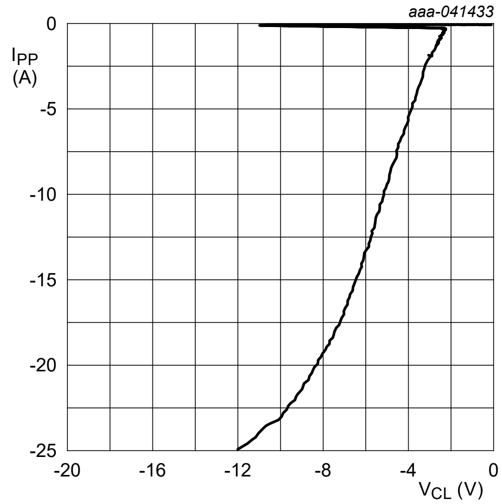


Fig. 5. Capacitance as a function of reverse voltage; typical values



Transmission Line Pulse (TLP);
t_p = 100 ns; t_r = 1 ns

Fig. 6. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP);
t_p = 100 ns; t_r = 1 ns

Fig. 7. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of two data or signal lines from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground. The device uses an advanced clamping structure showing a negative dynamic resistance.

This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

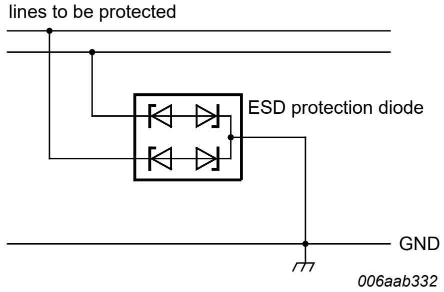


Fig. 8. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

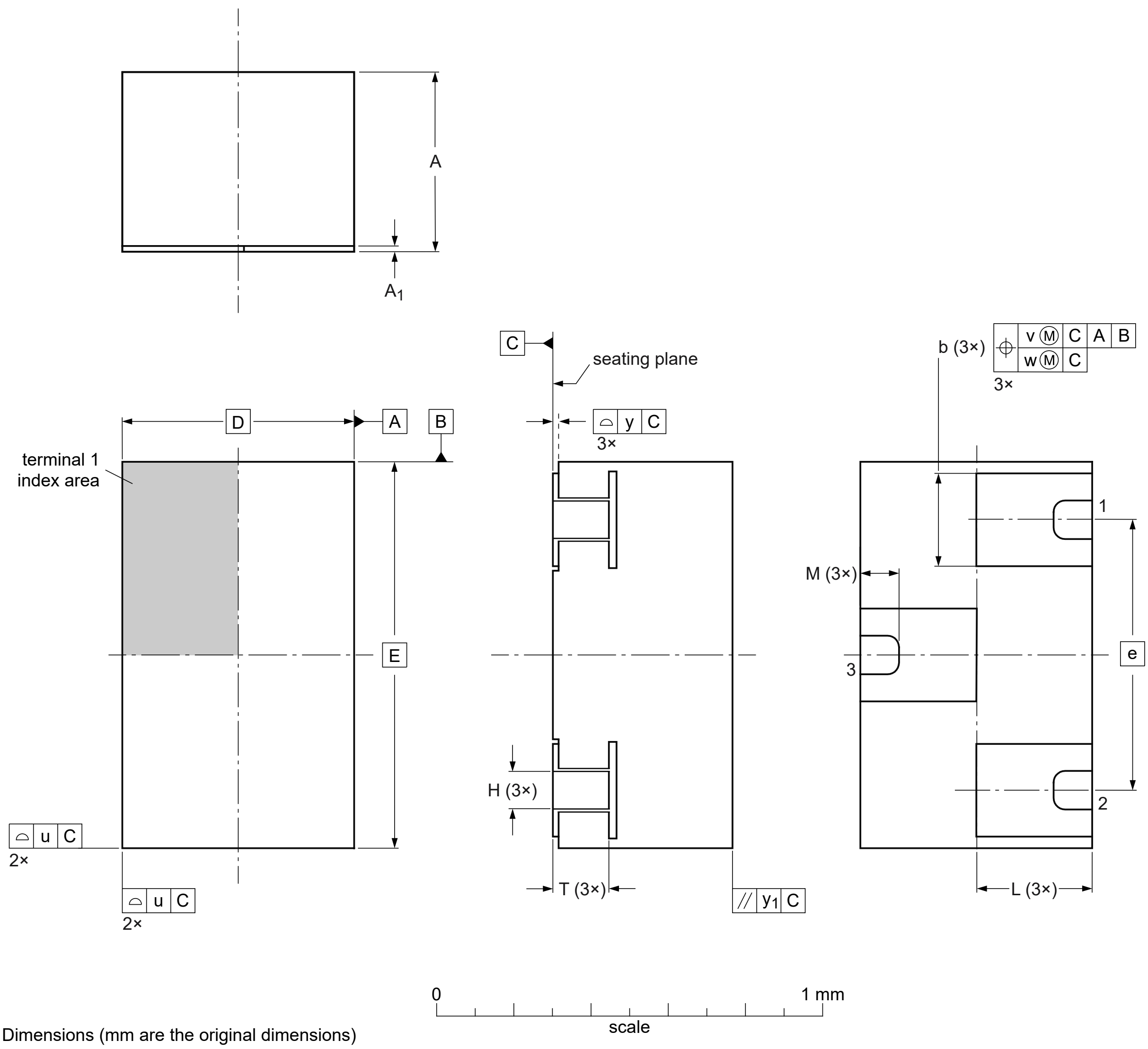
11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1006LD-3: Leadless ultra small plastic package with side-wettable flanks (SWF); 3 terminals; 0.7 mm pitch; 1 mm × 0.6 mm × 0.45 mm body **SOT8079LD-1**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	b	D	E	e	H	L	M	T	u	v	w	y	y_1
mm	max	0.50	0.05	0.29				0.1 REF	0.35	0.1 REF						
	nom	0.45		0.24	0.6	1.0	0.7		0.30			0.01	0.1	0.05	0.05	0.05
	min	0.40		0.19					0.25		0.1					

Note
1. Dimension A includes plating thickness

sot8079ld-1_po

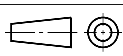
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8079LD-1						~~23-03-06~~ 24-08-05

Fig. 9. Package outline DFN1006LD-3 (SOT8079LD-1)

13. Soldering

Footprint information for reflow soldering of DFN1006LD-3 package **SOT8079LD-1**

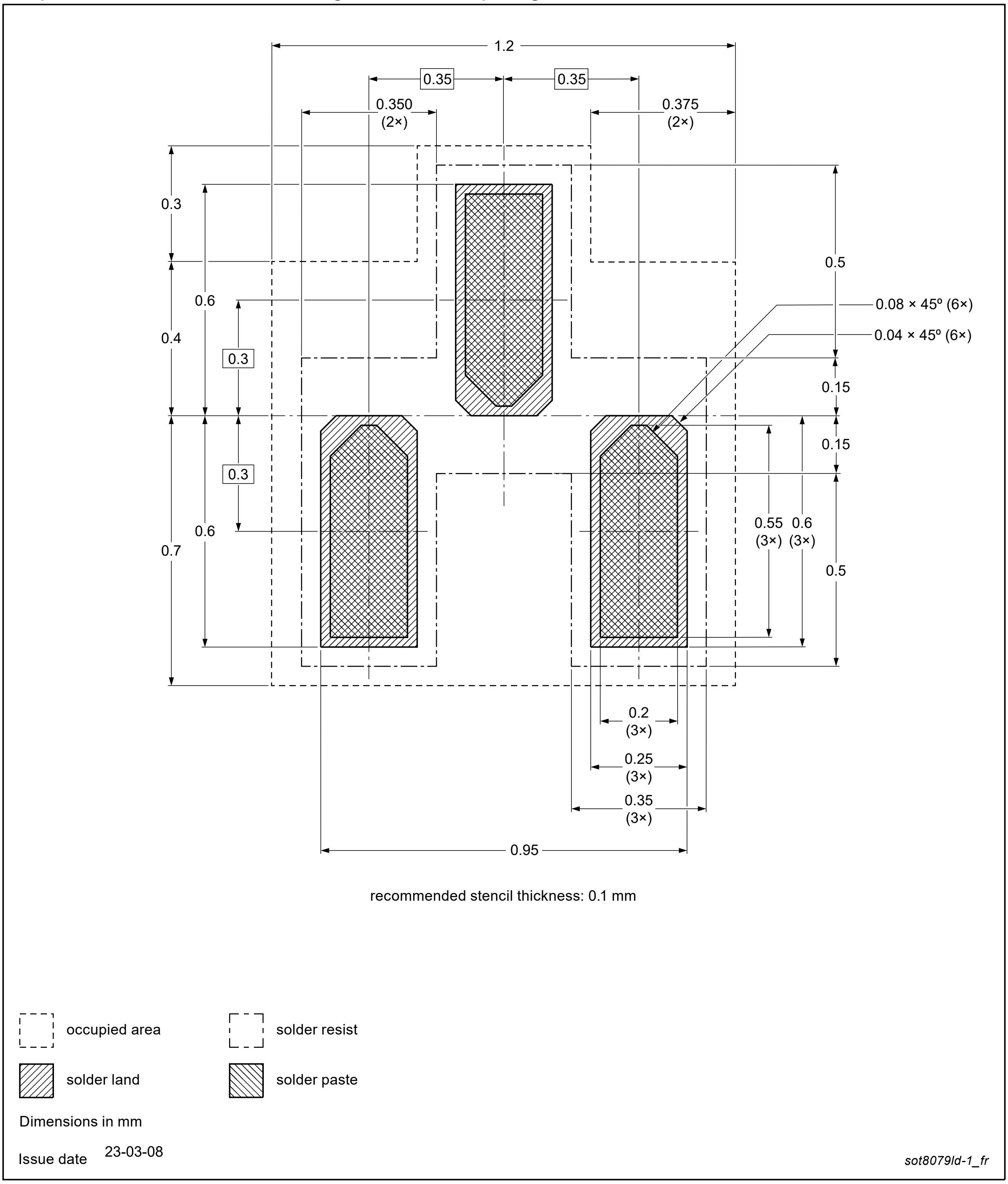


Fig. 10. Reflow soldering footprint for DFN1006LD-3 (SOT8079LD-1)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0H2BFG-Q v.1	20250203	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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