



PESD5V0G1BL

Very low capacitance bidirectional ESD protection diode

4 May 2018

Product data sheet

1. General description

Very low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006-2 (SOD882) leadless ultra small Surface-Mounted Device (SMD) plastic package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra small SMD plastic package
- Low clamping voltage $V_{CL} = 13\text{ V}$
- Ultra low leakage current $I_{RM} < 1\text{ nA}$
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{PPM} = 5.5\text{ A}$

3. Applications

- Portable electronics
- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems

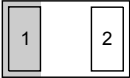
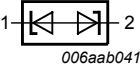
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$	-	-	5	V
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$	-	11	18	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view DFN1006-2 (SOD882)	 006aab041
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0G1BL	DFN1006-2	plastic, leadless ultra small package; 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOD882

7. Marking

Table 4. Marking codes

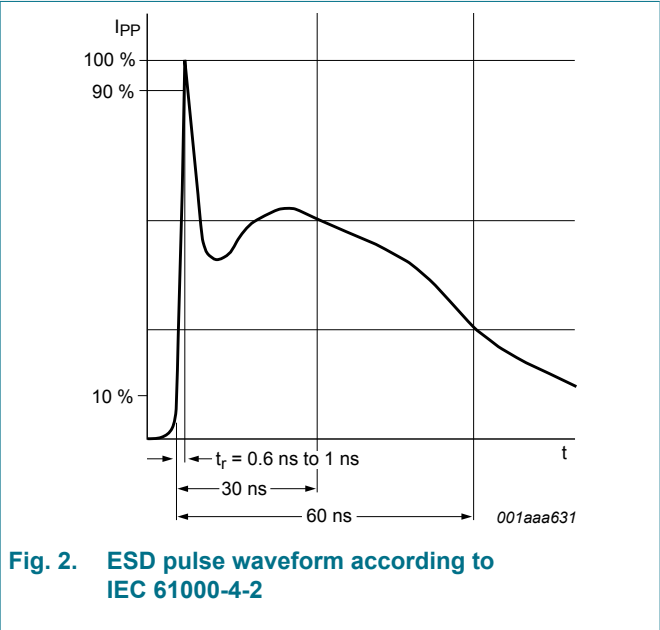
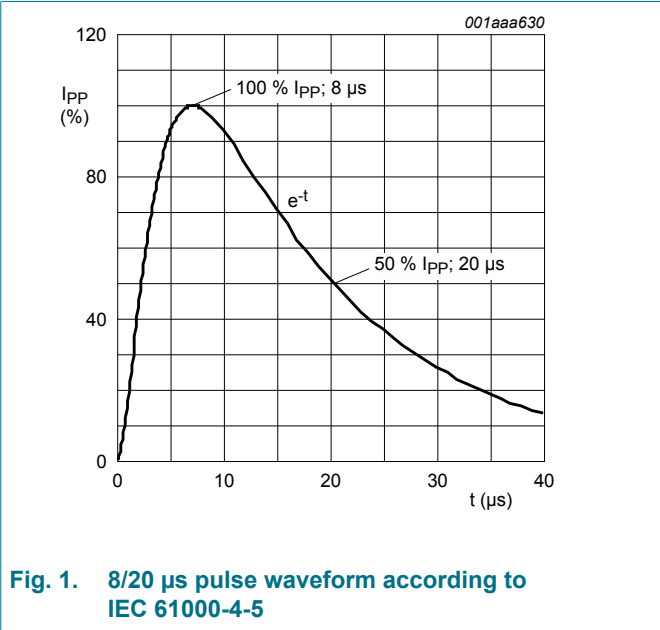
Type number	Marking code
PESD5V0G1BL	X1

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1]	-	5.5	A
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	contact discharge		-	30	kV
		MM		-	2	kV
		HBM (MIL-STD)		-	16	kV

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

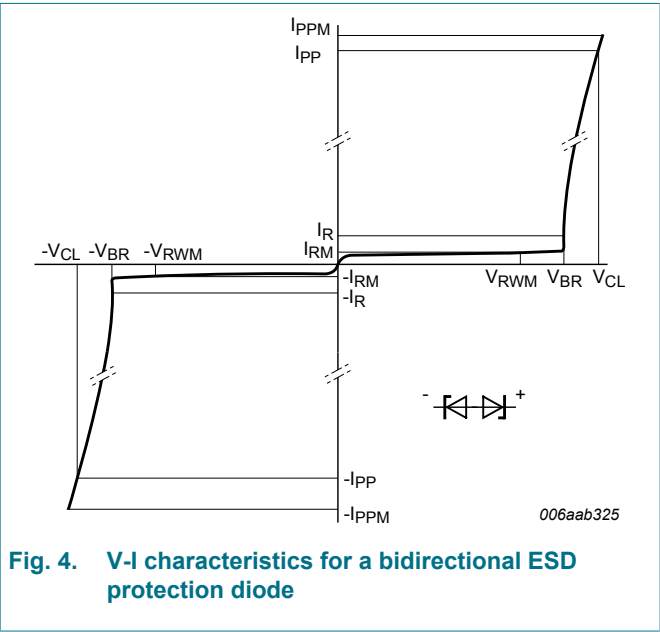
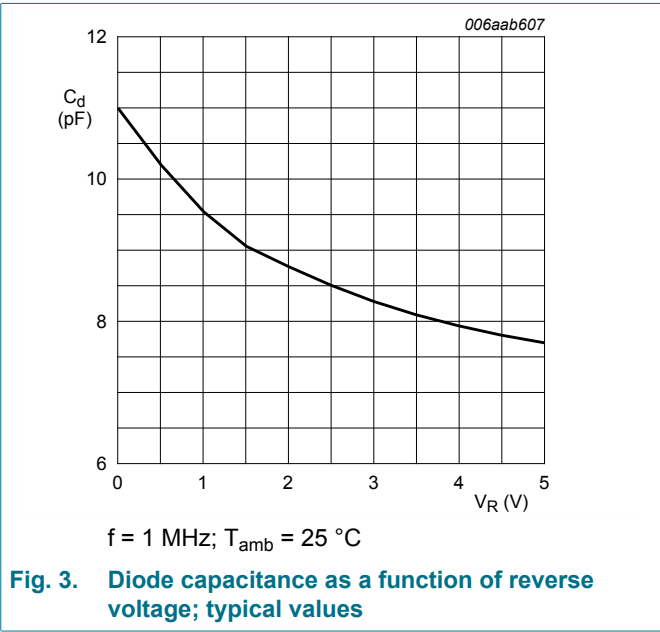


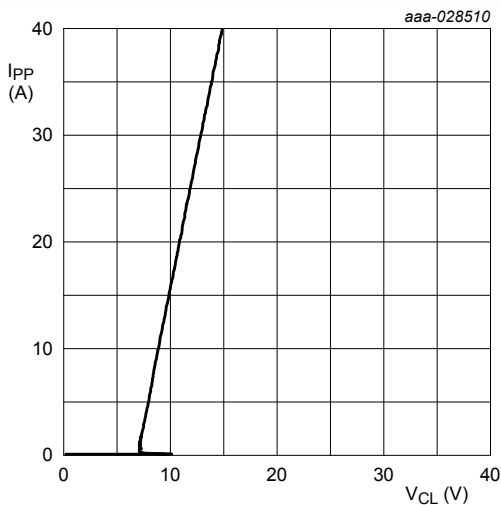
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	5	V
V_{BR}	breakdown voltage	$I_R = 5\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		5.8	6.8	7.8	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	1	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}$; $V_R = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	11	18	pF
V_{CL}	clamping voltage	$I_{PPM} = 5.5\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	13	V
R_{dyn}	dynamic resistance	$I_R = 10\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	0.2	-	Ω

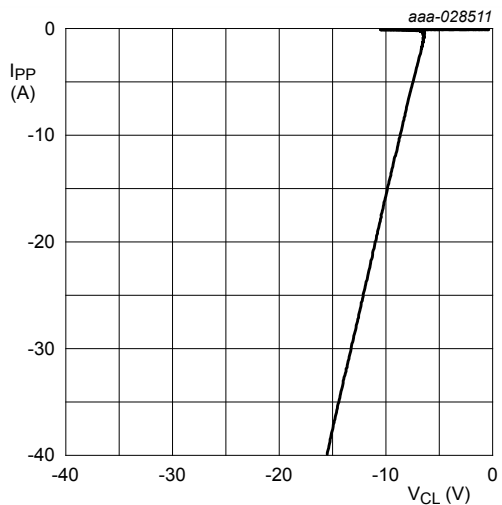
[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANSI / ESD STM5.1.1-2008.





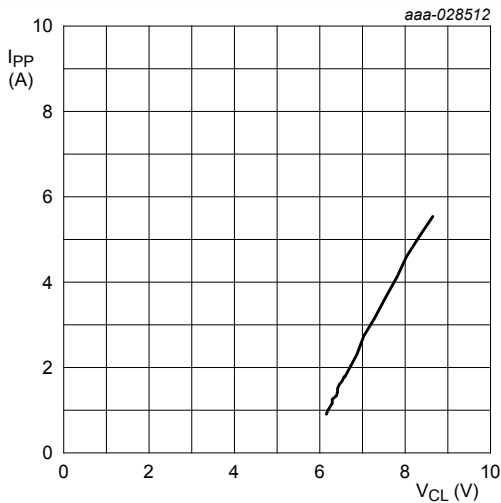
Transmission Line Pulse (TLP) = 100 ns;
rise time = 1 ns

Fig. 5. Dynamic resistance with positive clamping; typical values



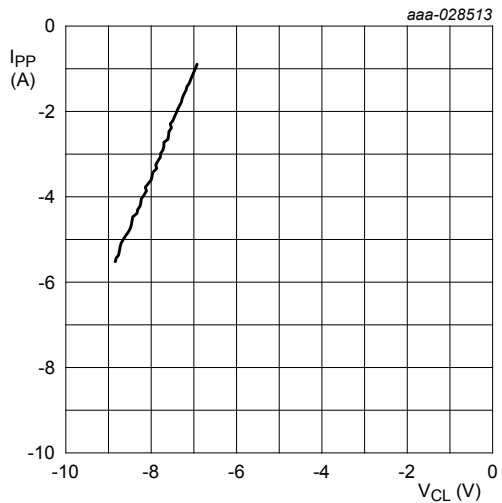
Transmission Line Pulse (TLP) = 100 ns;
rise time = 1 ns

Fig. 6. Dynamic resistance with negative clamping; typical values



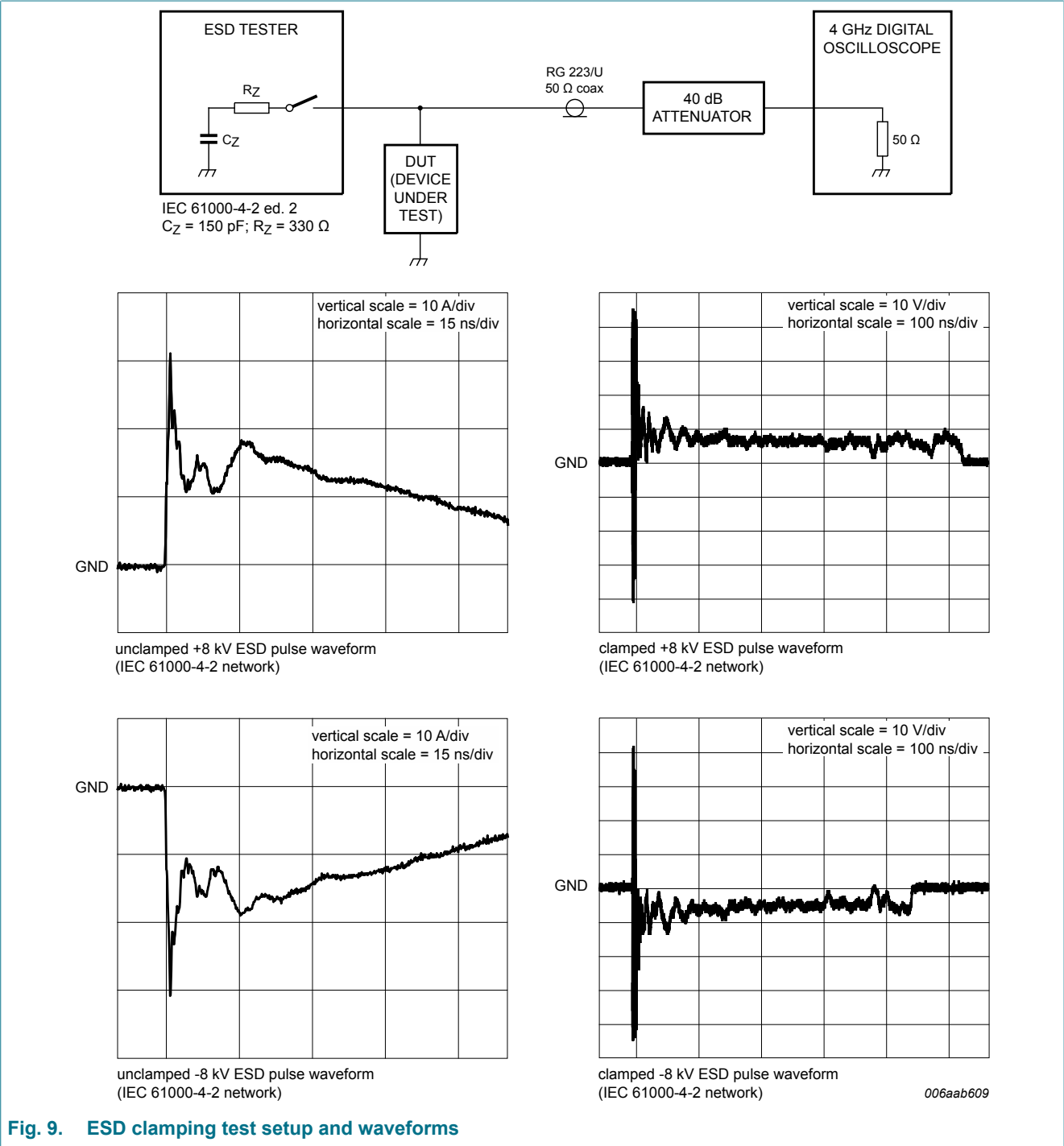
IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig. 7. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig. 8. Dynamic resistance with negative clamping; typical values



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

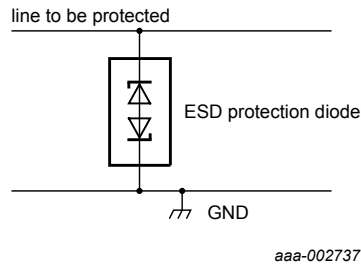


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

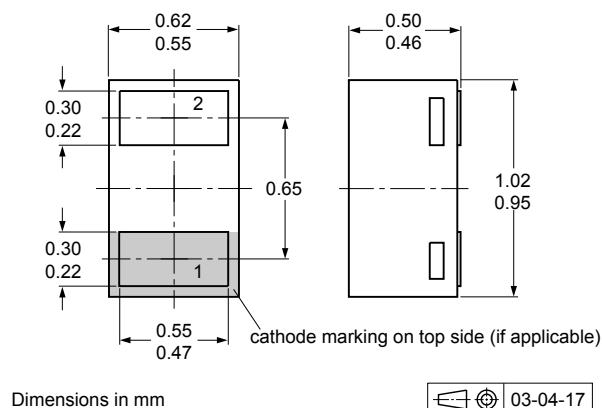


Fig. 11. Package outline DFN1006-2 (SOD882)

12. Soldering

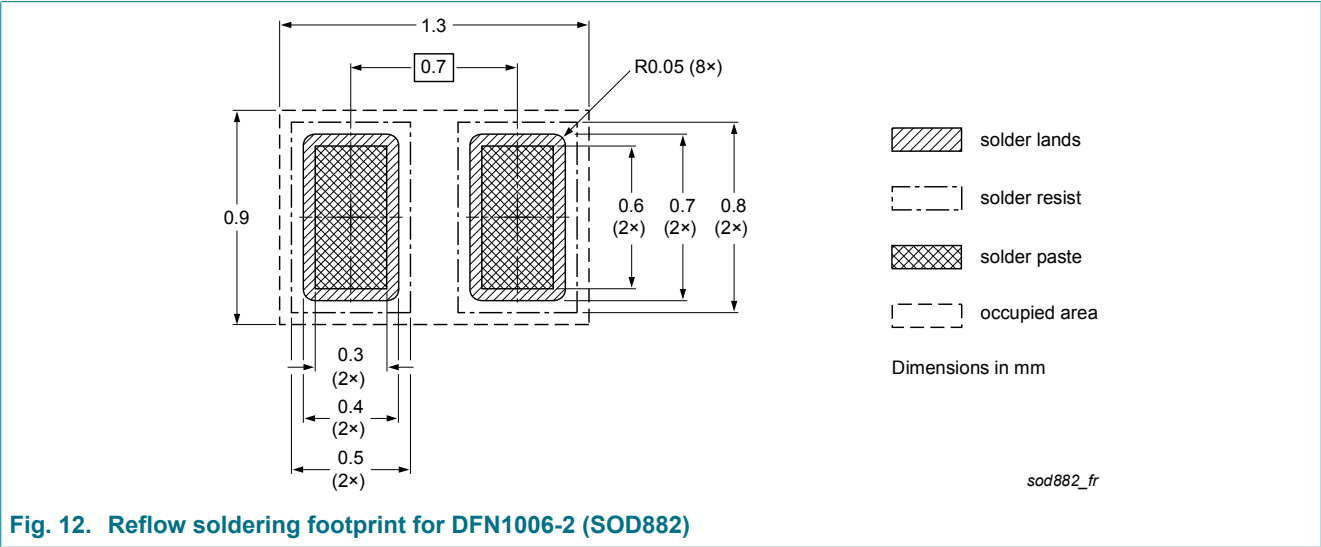


Fig. 12. Reflow soldering footprint for DFN1006-2 (SOD882)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0G1BL v.3	20180504	Product data sheet	-	PESD5V0G1BL v.2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Updated rated peak pulse current I_{PPM} to 5.5 A.Added figures 5 to 8.			
PESD5V0G1BL v.2	20151204	Product data sheet	-	PESD5V0G1BL v.1
PESD5V0G1BL v.1	20130523	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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