P-Channel Enhancement Mode Power MOSFET

DESCRIPTION

The PED705 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switching application and a wide variety of other applications

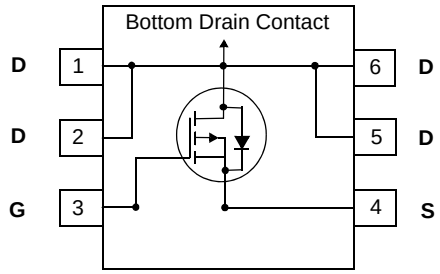
GENERAL FEATURES

- V_{DS} = -12V,I_D = -8A
  $R_{DS(ON)}$ <30mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ <40mΩ @ V_{GS}=-2.5V
  $R_{DS(ON)}$ <60mΩ @ V_{GS}=-1.8V

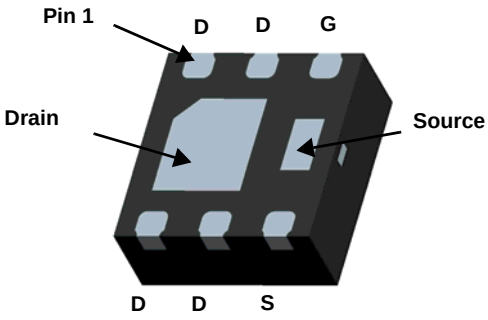
- Asvanced trench MOSFET process technology
- Ultra low on-resistance with low gate charge
- New Thermally Enhanced DFN2X2-6L Package

Application

- PWM applications
- Load switch
- battery charge in cellular handset



Pin Assignment



DFN2X2-6L bottom review

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	±8	V
Drain Current -Continuous	I_D	-8	A
Drain Current -Pulsed (Note 1)	I_{DM}	-35	A
Maximum Power Dissipation	P_D	2.4	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	℃/W
Thermal Resistance,Junction-to-case(Note 2)	$R_{\theta JC}$	6.9	℃/W

Electrical Characteristics (TC=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-12	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-12V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±8V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.4	-0.7	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-6A	-	19	30	mΩ
		V_{GS}=-2.5V, I_D=-5A	-	26	40	
		V_{GS}=-1.8V, I_D=-2.5A	-	42	60	
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-6A	25	45	-	S
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-8A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-15	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Characteristics T_J = 25 °C unless otherwise noted

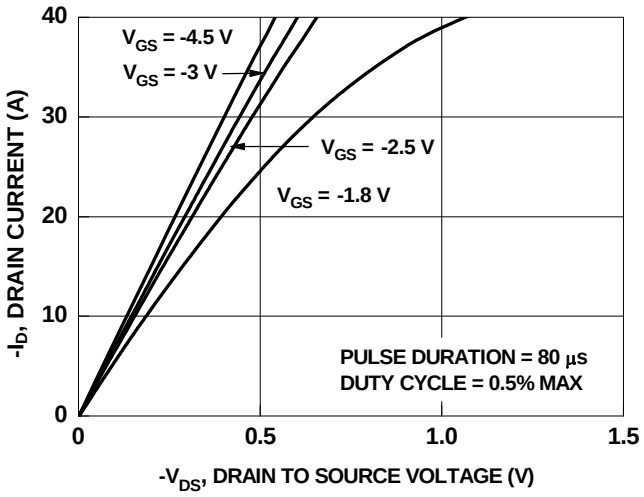


Figure 1. On-Region Characteristics

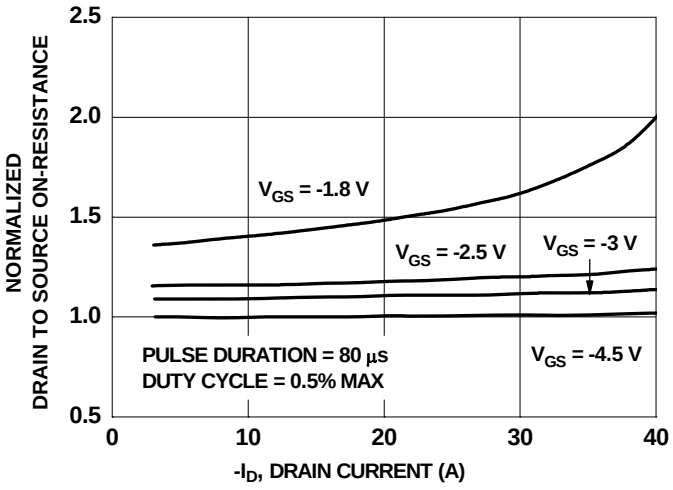


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

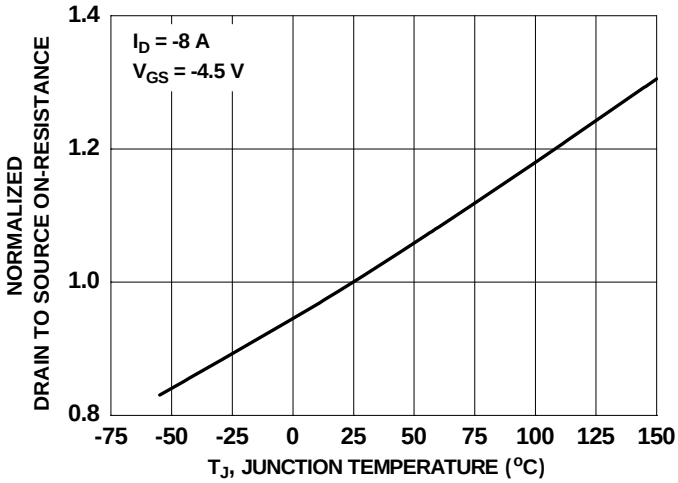


Figure 3. Normalized On-Resistance vs Junction Temperature

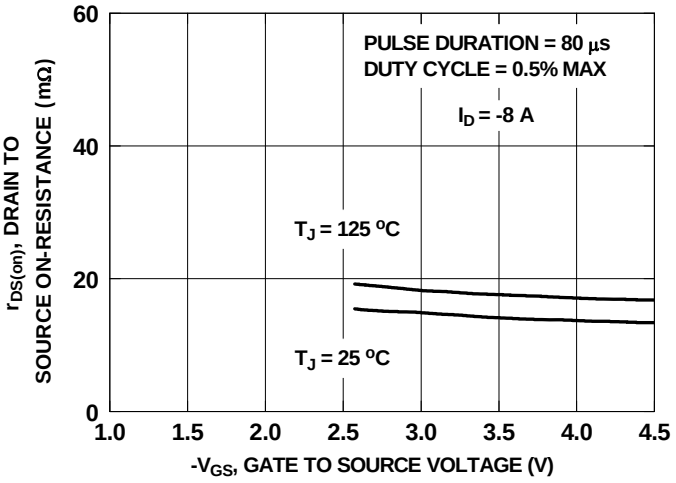


Figure 4. On-Resistance vs Gate to Source Voltage

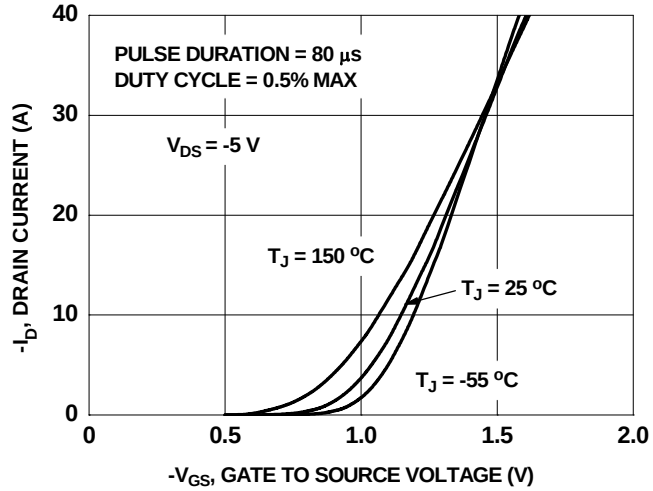


Figure 5. Transfer Characteristics

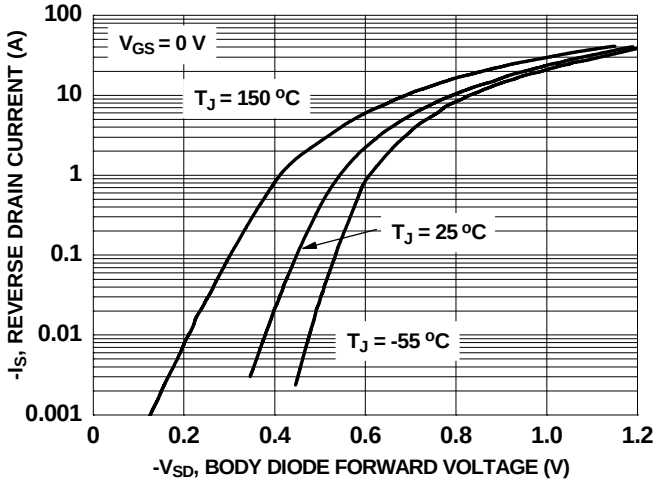


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

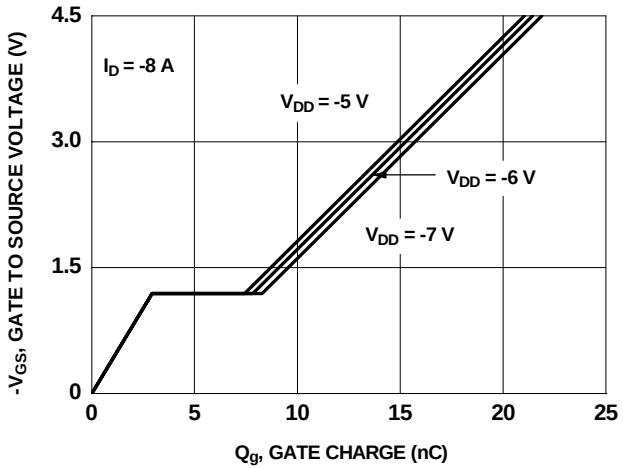


Figure 7. Gate Charge Characteristics

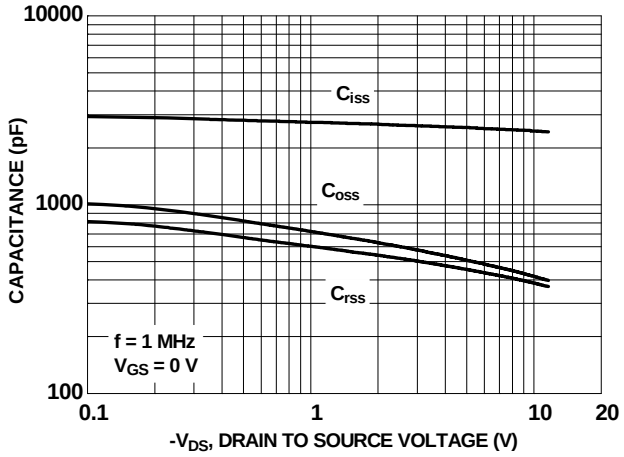


Figure 8. Capacitance vs Drain to Source Voltage

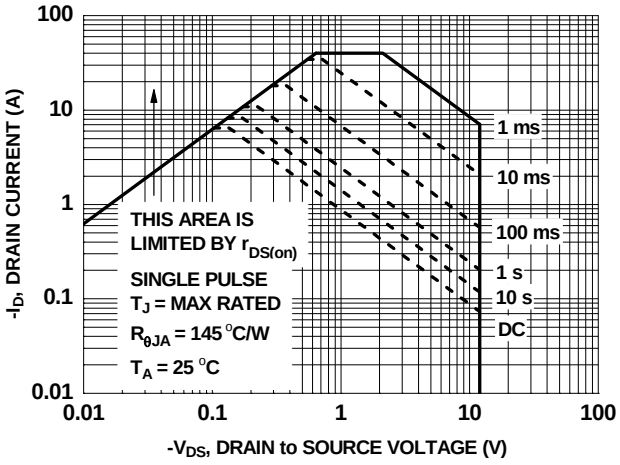


Figure 9. Forward Bias Safe Operating Area

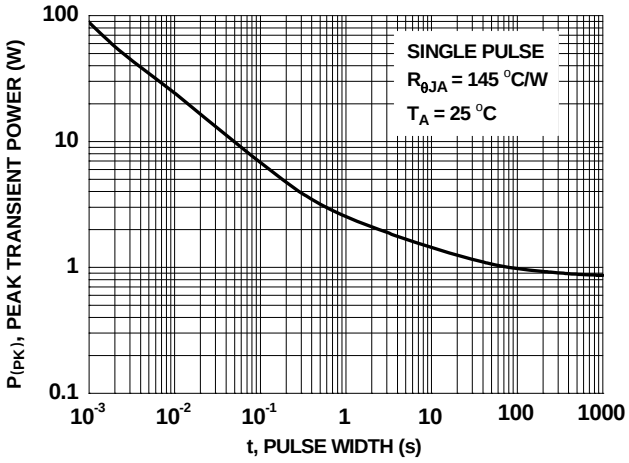


Figure 10. Single Pluse Maximum Power Dissipation

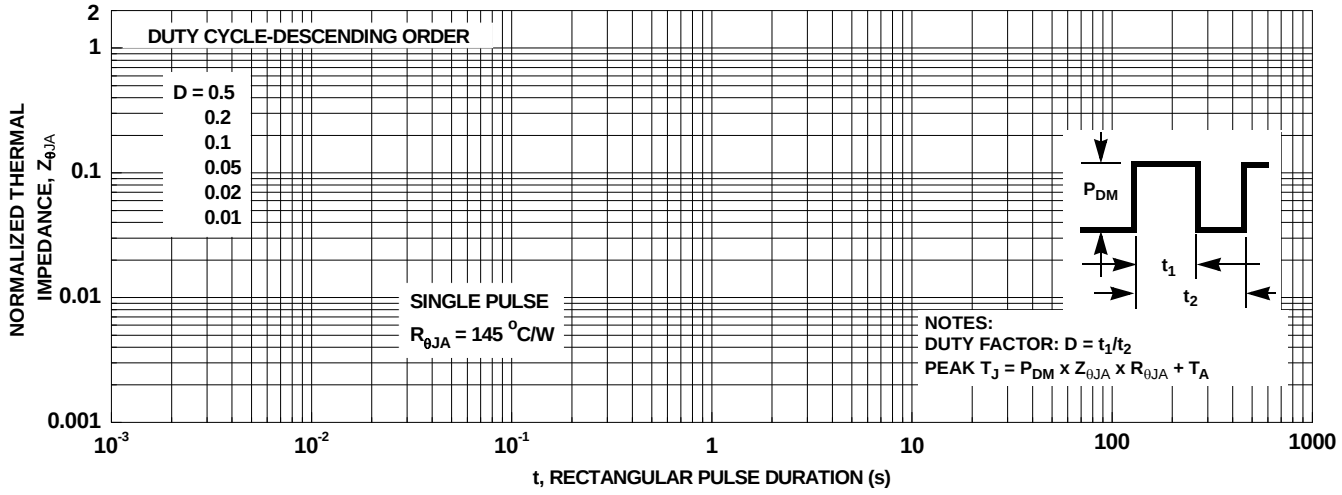
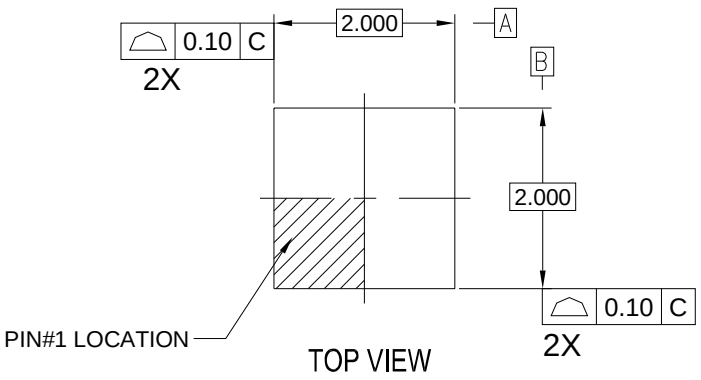
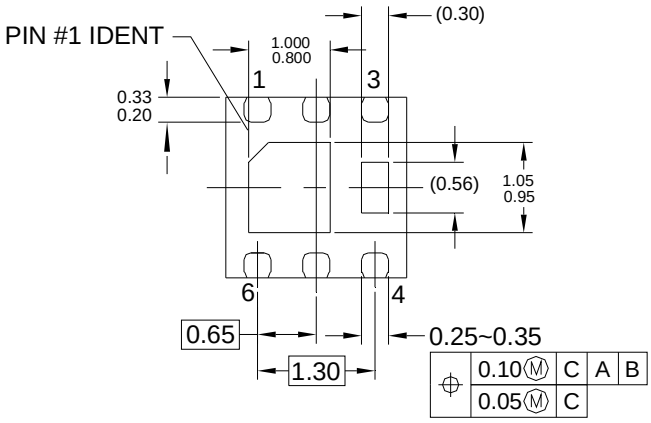
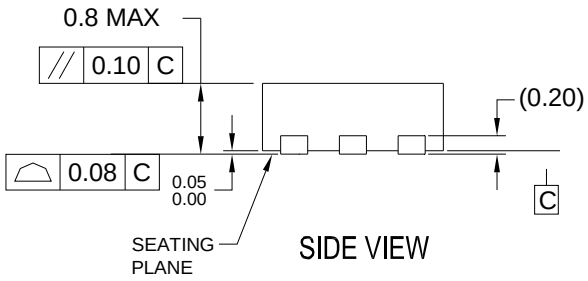


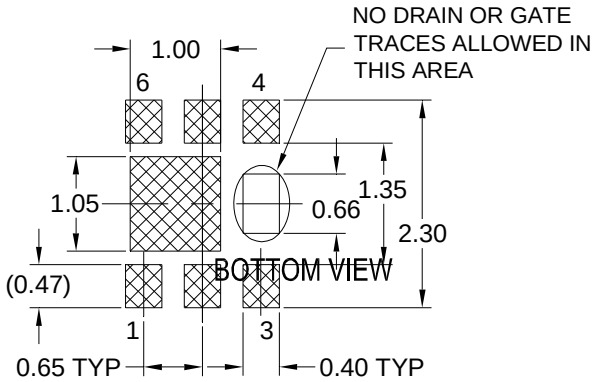
Figure 11. Junction-to-Ambient Transient Thermal Response Curve

DFN2X2-6L PACKAGE INFORMATION

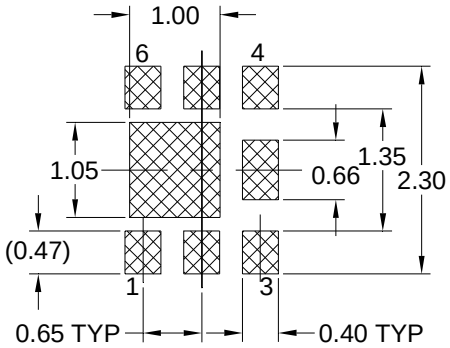








RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.