P-Channel Enhancement Mode Power MOSFET

DESCRIPTION

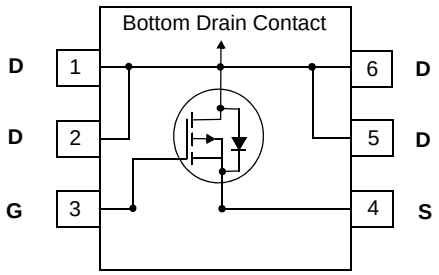
The PED305 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

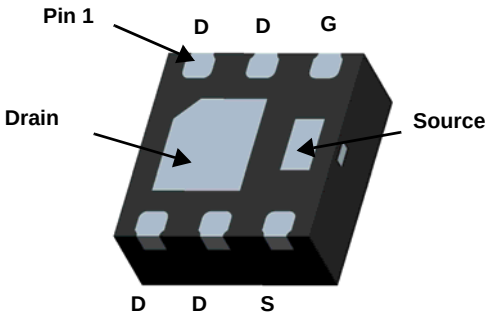
- V_{DS} = -16V,I_D = -3.5A
  $R_{DS(ON)}$ < 65mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ <75mΩ @ V_{GS}=-2.5V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management



Pin Assignment



DFN2X2-6L bottom review

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-16	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_C =25℃	I_D	-3.5	A
	T_C =70℃		-2.2	
	T_A =25℃		-2.0	
	T_A =70℃		-1.8	
Drain Current -Pulsed (Note 1)		I_{DM}	-8	A
Maximum Power Dissipation		P_D	1.7	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	68	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-16	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±8V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.45	-0.7	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-3.0A	-	48	65	mΩ
		V_{GS}=-2.5V, I_D=-2.2A	-	65	75	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-2.0A	-	8.5	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-4V,V_{GS}=0V, F=1.0MHz	-	405	-	PF
Output Capacitance	C_{oss}		-	75	-	PF
Reverse Transfer Capacitance	C_{rss}		-	55	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-4V,I_D=-1A , R_L=-1.2Ω,V_{GEN}=-4.5V,R_g=1Ω	-	11	-	nS
Turn-on Rise Time	t_r		-	35	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=-4V,I_D=-1A,V_{GS}=-4.5V	-	7.8	-	nC
Gate-Source Charge	Q_{gs}		-	1.2	-	nC
Gate-Drain Charge	Q_{gd}		-	1.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-1.6A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	1.6	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

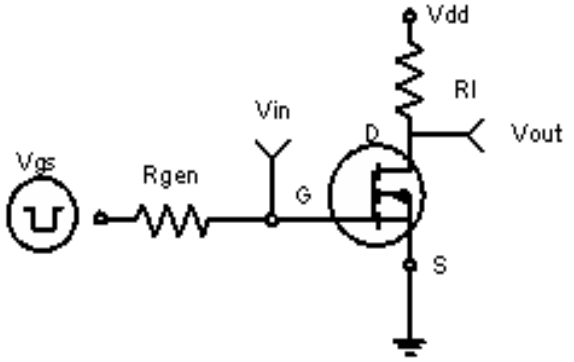


Figure 1:Switching Test Circuit

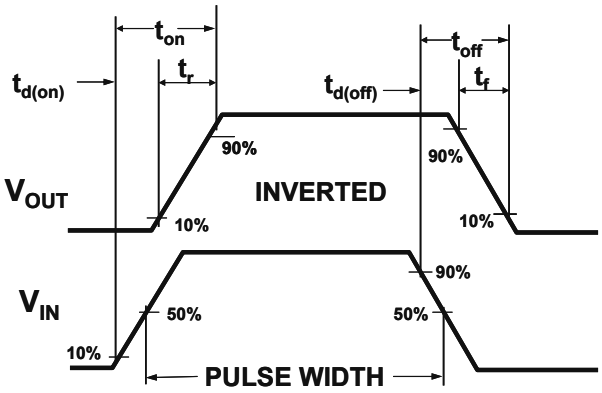


Figure 2:Switching Waveforms

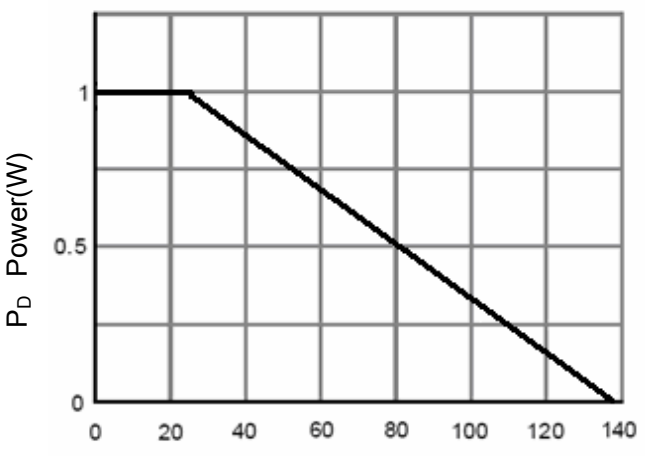


Figure 3 Power Dissipation

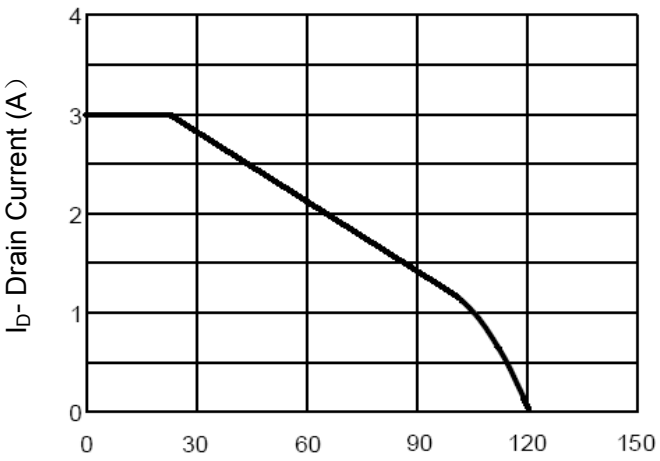


Figure 4 Drain Current

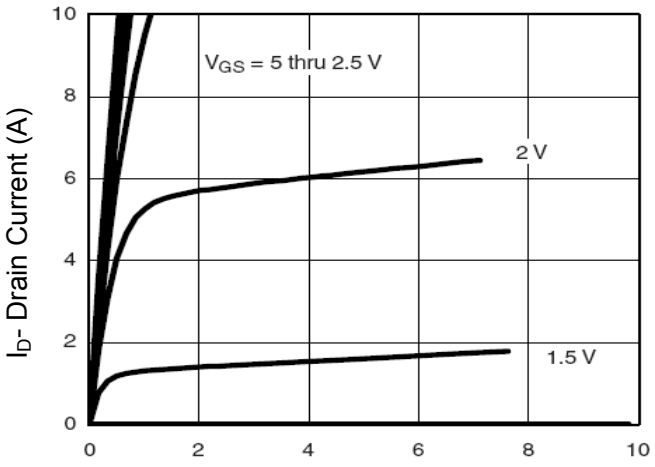


Figure 5 Output CHARACTERISTICS

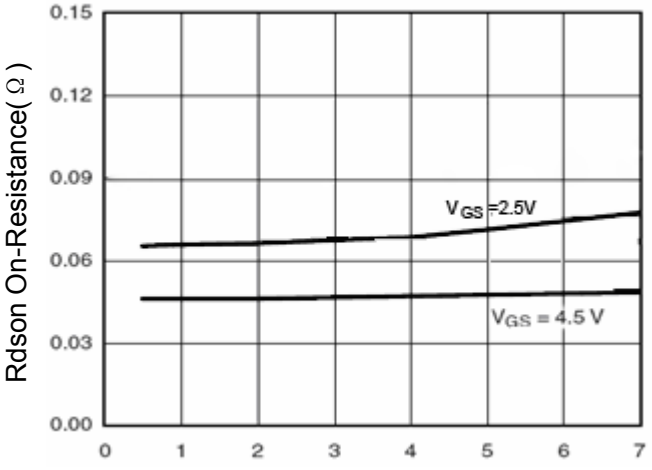


Figure 6 Drain-Source On-Resistance

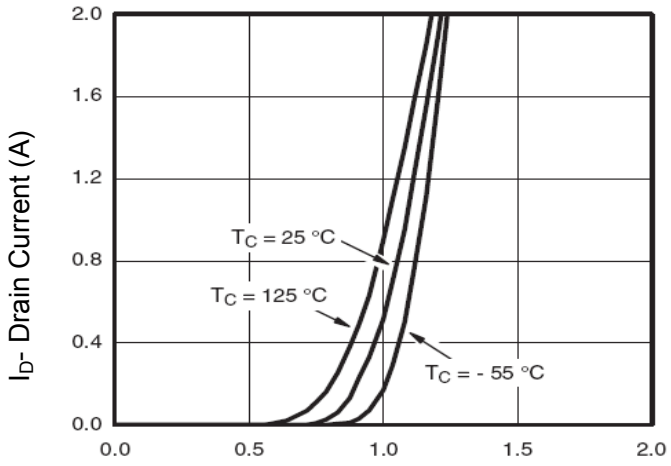


Figure 7 Transfer Characteristics

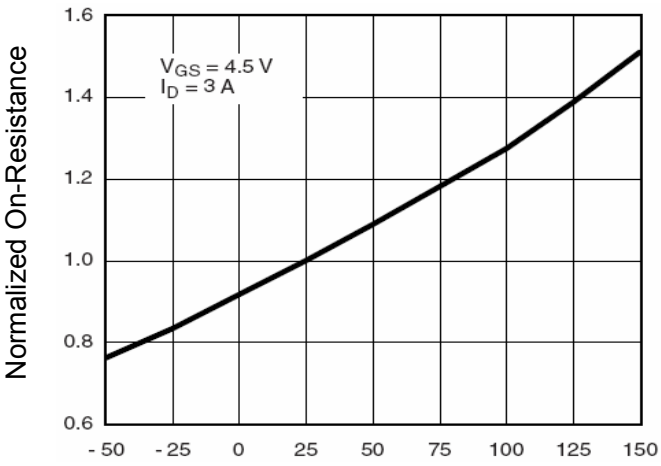


Figure 8 Drain-Source On-Resistance

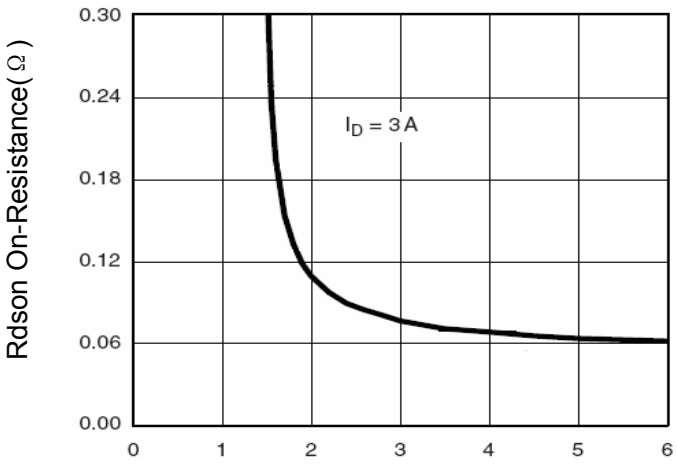


Figure 9 Rdson vs Vgs

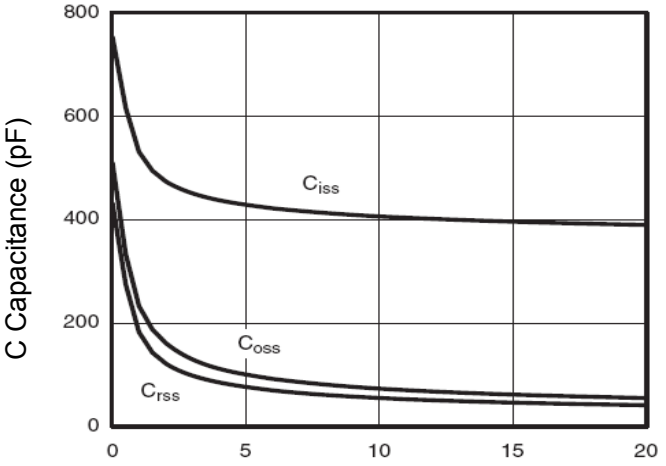


Figure 10 Capacitance vs Vds

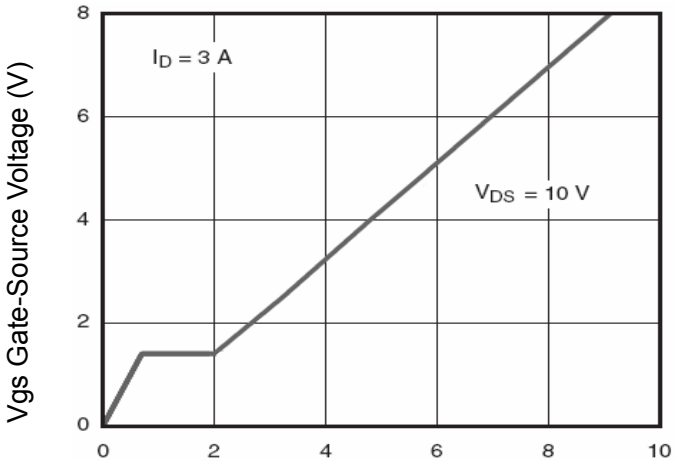


Figure 11 Gate Charge

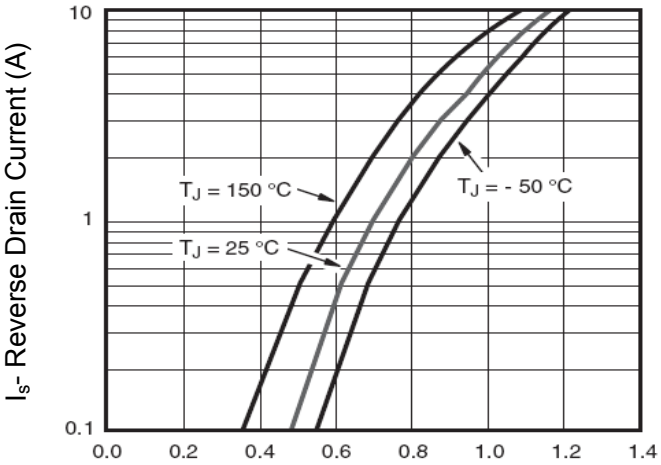


Figure 12 Source- Drain Diode Forward

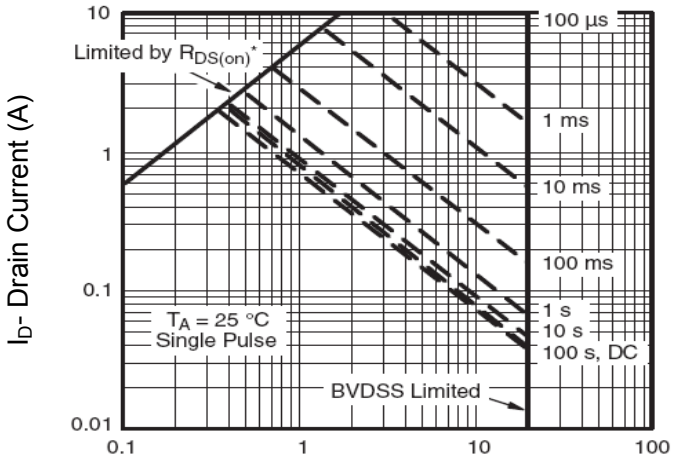


Figure 13 Safe Operation Area

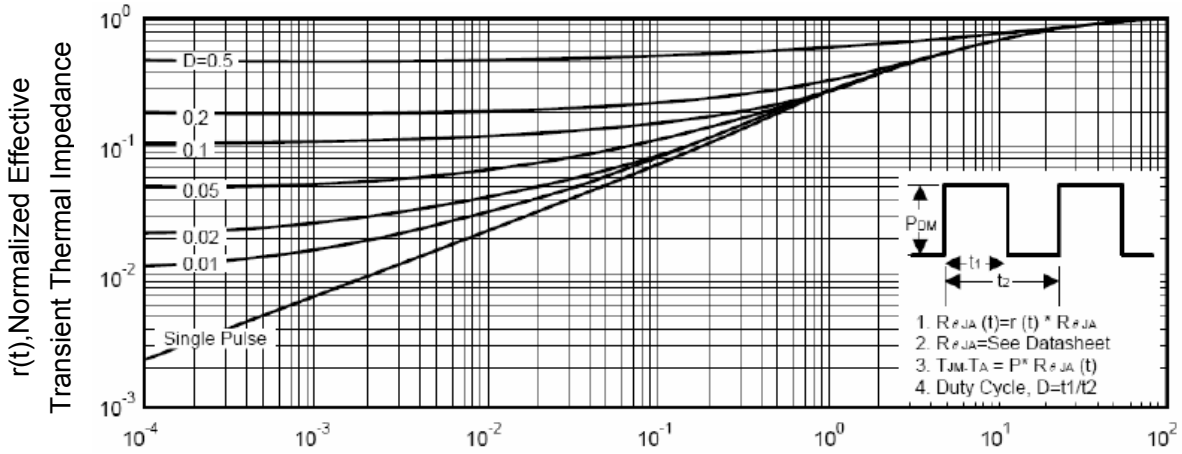
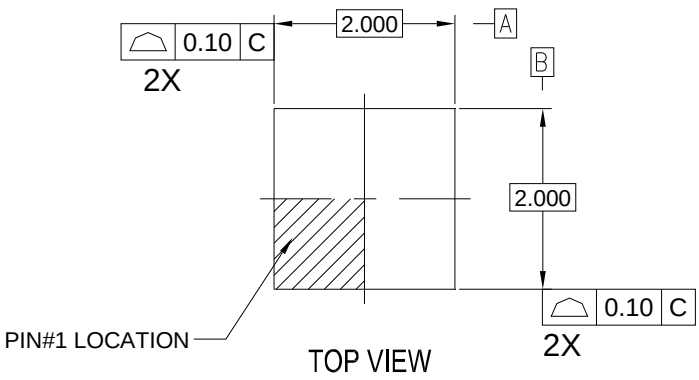
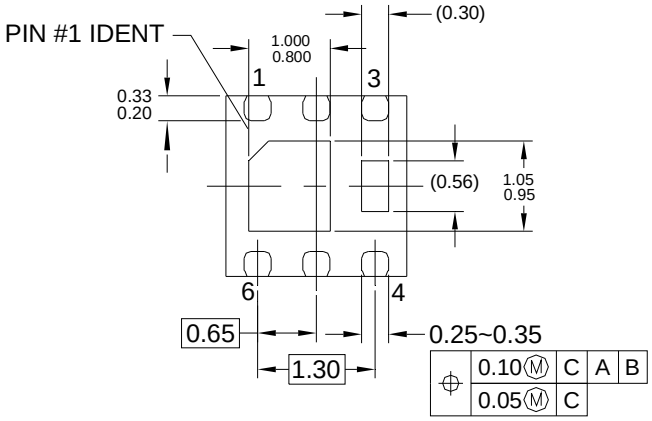
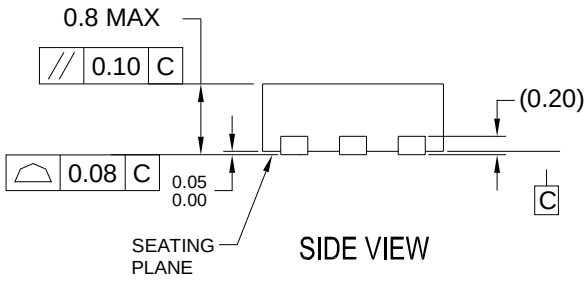


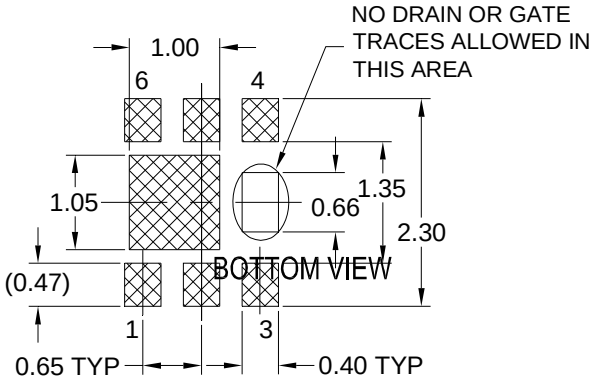
Figure 14 Normalized Maximum Transient Thermal Impedance

DFN2X2-6L PACKAGE INFORMATION

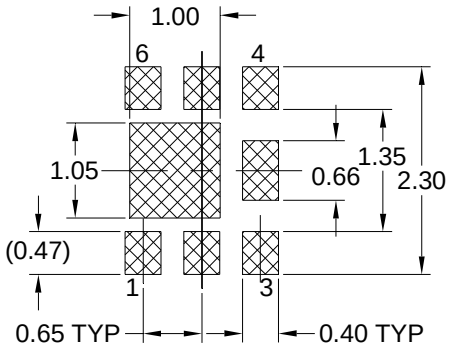








RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.