N-Channel Enhancement Mode Power MOSFET

Description

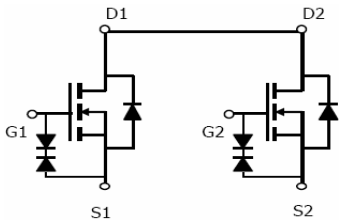
The PED2310L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.It is ESD protested.

General Features

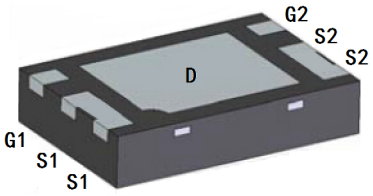
- V_{DS} = 20V,I_D =8A
  $R_{DS(ON)}$ =11.5mΩ @ V_{GS}=4.5V
  $R_{DS(ON)}$ =12mΩ @ V_{GS}=4.2V
  $R_{DS(ON)}$ =12.8mΩ @ V_{GS}=3.8V
  $R_{DS(ON)}$ =15.5mΩ @ V_{GS}=2.5V
  ESD Rating: 2000V HBM
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM application
- Load switch



Schematic diagram



DFN2x3-6L bottom view

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current-Continuous	I_D	8	A
Drain Current-Pulsed (Note 1)	I_{DM}	30	A
Maximum Power Dissipation	P_D	0.98	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	126	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V,V_{GS}=0V	-	-	1	μA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.45	0.7	0.95	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=6A	7.5	11.5	17	mΩ
		V_{GS}=4.2V, I_D=6A	8	12	17.5	mΩ
		V_{GS}=3.8V, I_D=5.5A	9.5	12.8	18	mΩ
		V_{GS}=2.5V, I_D=5.5A	11.5	15.5	20	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=7A	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=10V,V_{GS}=0V, F=1.0MHz	-	1150	-	PF
Output Capacitance	C_{oss}		-	185	-	PF
Reverse Transfer Capacitance	C_{rss}		-	145	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,R_L=1.35Ω V_{GS}=5V,R_{GEN}=3Ω	-	6		nS
Turn-on Rise Time	t_r		-	13		nS
Turn-Off Delay Time	$t_{d(off)}$		-	52		nS
Turn-Off Fall Time	t_f		-	16		nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=7A, V_{GS}=4.5V	-	15		nC
Gate-Source Charge	Q_{gs}		-	0.8	-	nC
Gate-Drain Charge	Q_{gd}		-	3.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=1A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	7	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

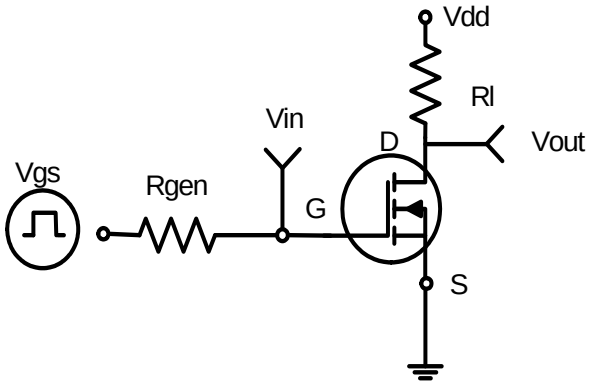


Figure 1:Switching Test Circuit

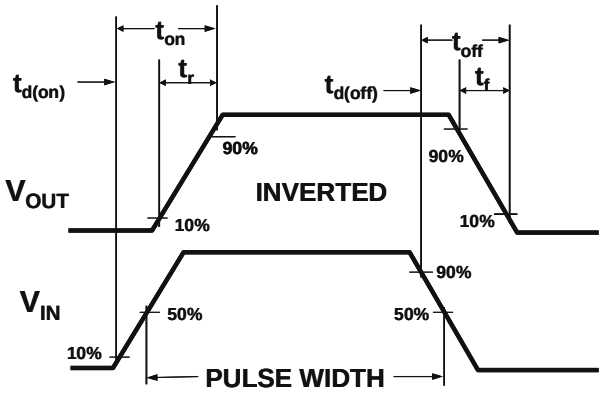


Figure 2:Switching Waveforms

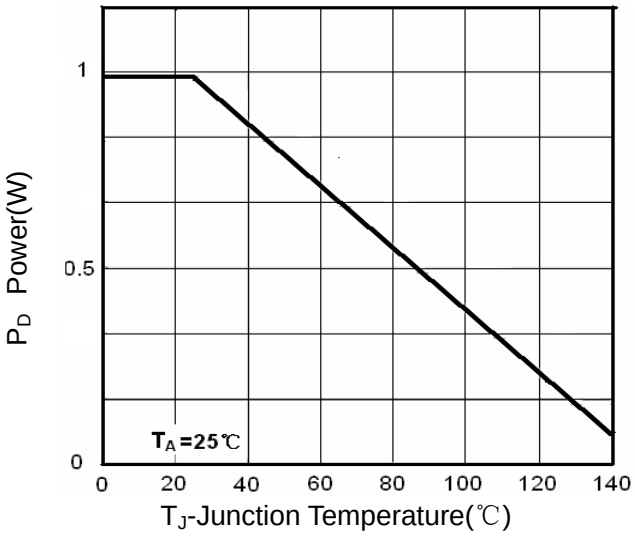


Figure 3 Power Dissipation

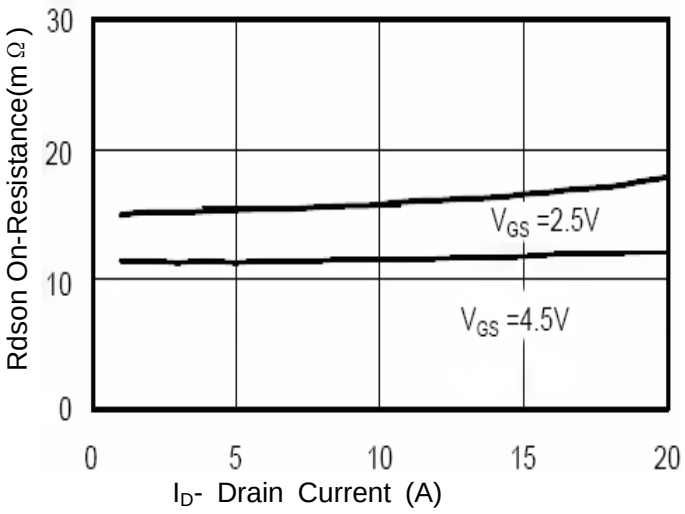


Figure 4 Drain-Source On-Resistance

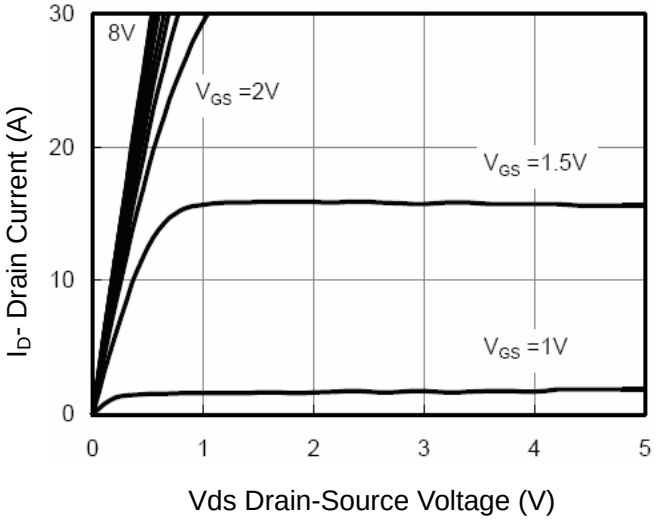


Figure 5 Output CHARACTERISTICS

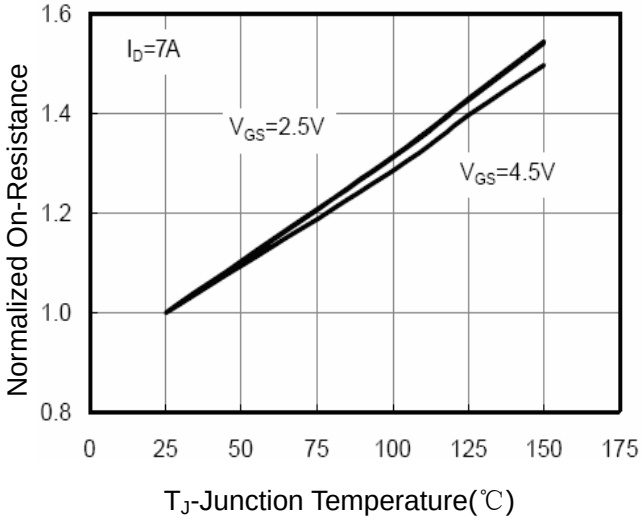


Figure 6 Drain-Source On-Resistance

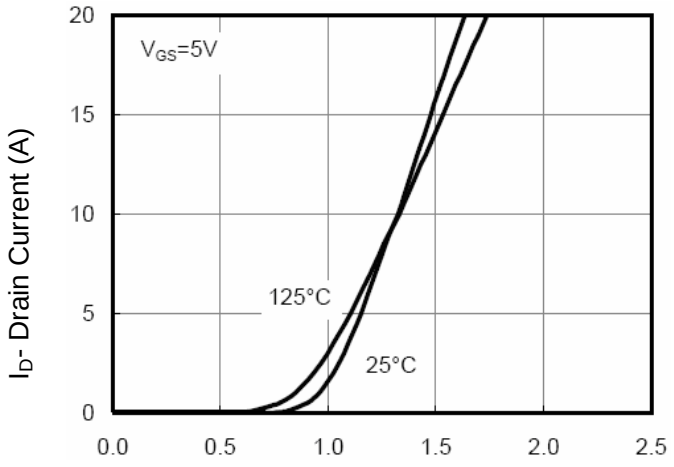


Figure 7 Transfer Characteristics

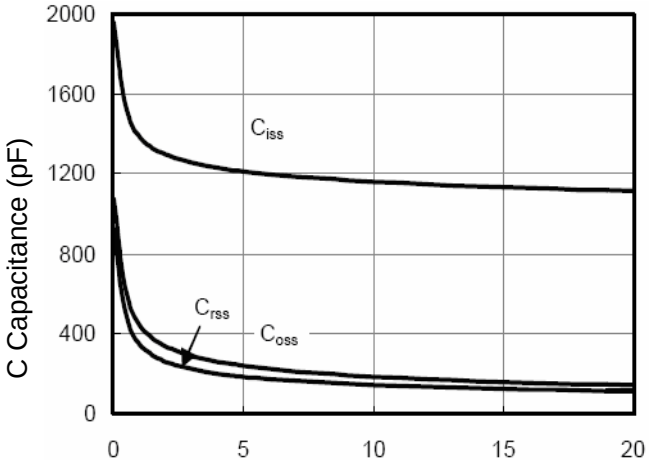


Figure 8 Capacitance vs Vds

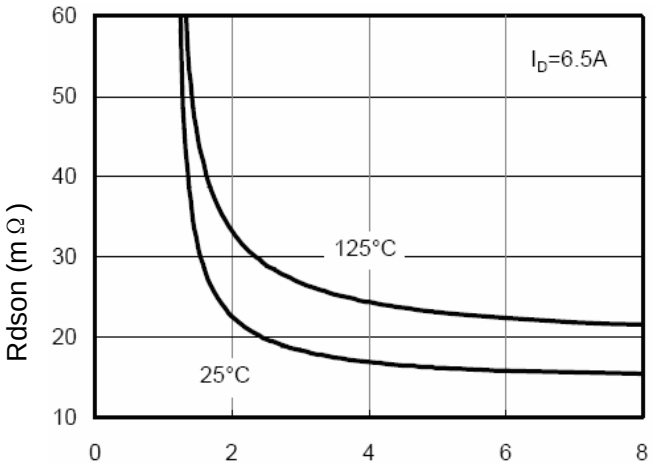


Figure 9 Rdson vs Vgs

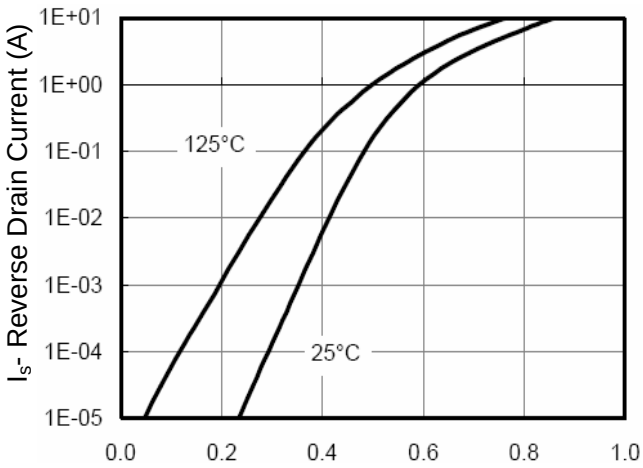


Figure 10 Capacitance vs Vds

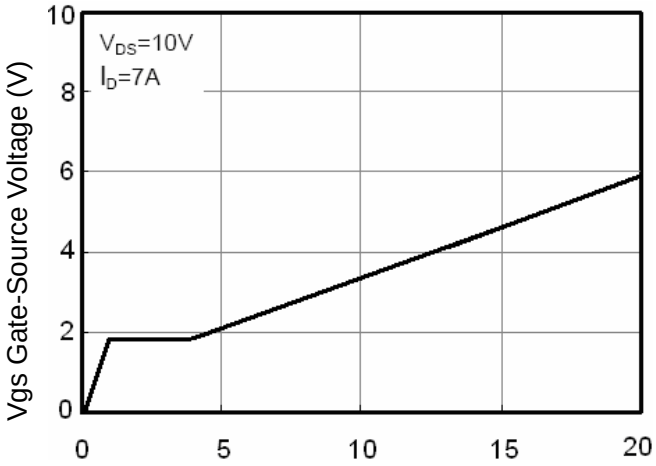


Figure 11 Gate Charge

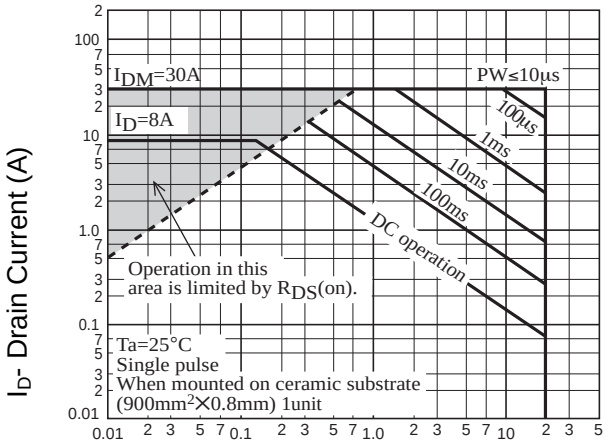


Figure 12 Safe Operation Area

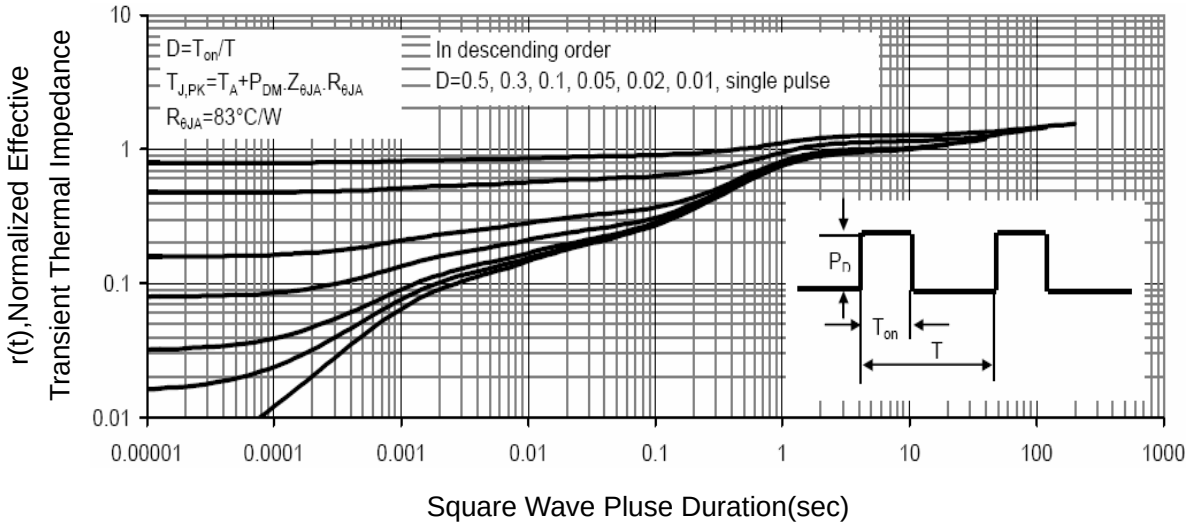
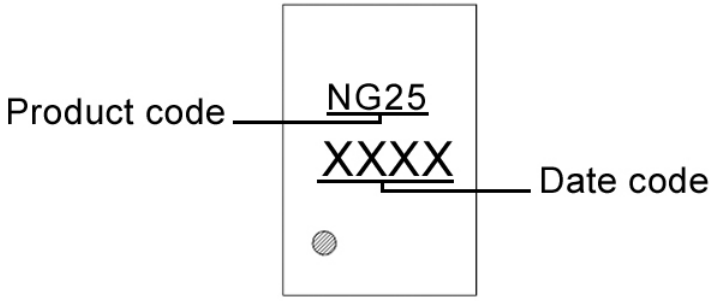
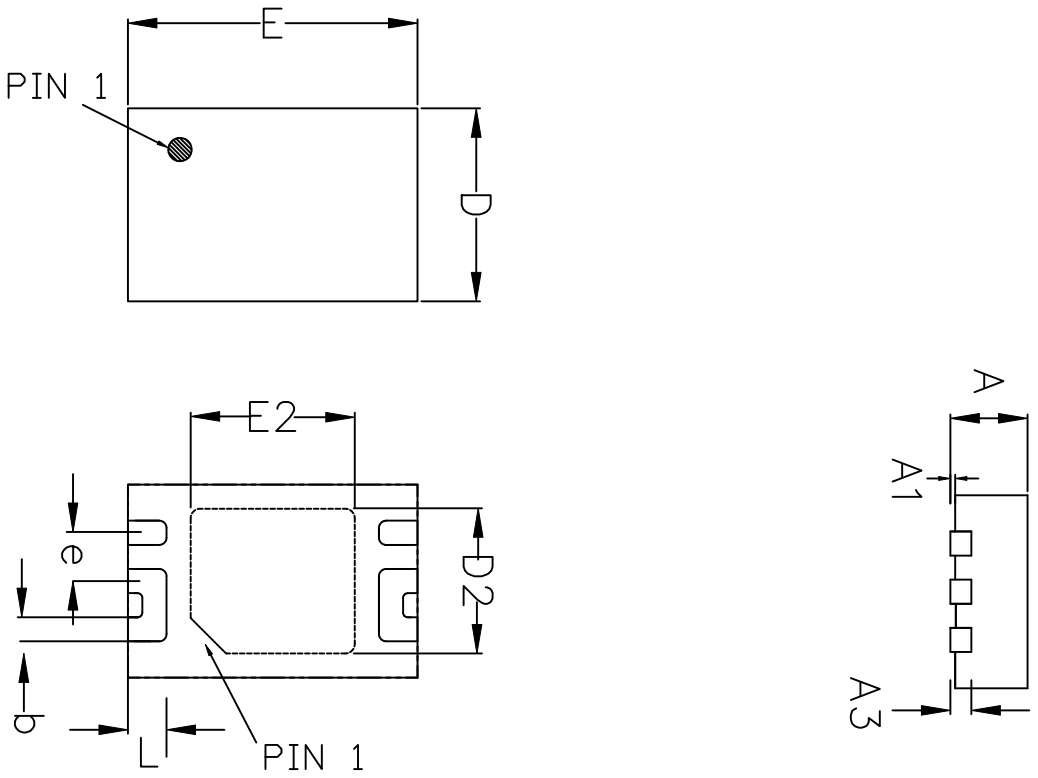


Figure 13 Normalized Maximum Transient Thermal Impedance

Marking Description



DFNWB2×3-6L(P0.50T0.75) PACKAGEOUTLINEDIMENSIONS



COMMON DIMENSIONS(MM)			
PKG.	W:VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.195	0.203	0.211
D	1.95	2.00	2.05
E	2.95	3.00	3.05
b	0.20	0.25	0.30
L	0.35	0.40	0.45
D2	1.45	1.50	1.55
E2	1.65	1.70	1.75
e	0.50 BSC		