

PE521BA

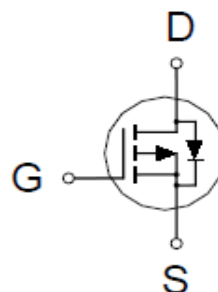
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	20m Ω @ $V_{GS} = -4.5V$	-23A



PDFN 3X3P



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ³	$T_c = 25\text{ }^{\circ}\text{C}$	I_D	-23	A
	$T_c = 100\text{ }^{\circ}\text{C}$		-18	
	$T_A = 25\text{ }^{\circ}\text{C}$		-7	
	$T_A = 70\text{ }^{\circ}\text{C}$		-6	
Pulsed Drain Current ¹		I_{DM}	-60	
Avalanche Current		I_{AS}	-20	mJ
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	20	
Power Dissipation	$T_c = 25\text{ }^{\circ}\text{C}$	P_D	17.8	W
	$T_c = 100\text{ }^{\circ}\text{C}$		11.4	
	$T_A = 25\text{ }^{\circ}\text{C}$		1.8	
	$T_A = 70\text{ }^{\circ}\text{C}$		1.2	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		68	$^{\circ}\text{C} / \text{W}$
Junction-to-Case	$R_{\theta JC}$		7	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design.

³Package limitation current is -11A.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.3	-0.6	-1	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	uA
		V _{DS} = -10V, V _{GS} = 0V, T _J = 125 °C			-10	
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -2.5A		14	20	mΩ
		V _{GS} = -2.5V, I _D = -2A		17	25	
		V _{GS} = -1.8V , I _D = -1A		22	35	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -2.5A		21		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		1801		pF
Output Capacitance	C _{oss}			179		
Reverse Transfer Capacitance	C _{rss}			160		
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		10		Ω
Total Gate Charge ²	Q _g (V _{GS} =-4.5V)	V _{DS} = -10V ,I _D = -2.5A		22.7		nC
	Q _g (V _{GS} =-2.5V)			13.3		
Gate-Source Charge ²	Q _{gs}			1.9		
Gate-Drain Charge ²	Q _{gd}			5.4		
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = -10V, I _D ≅ -2.5A, V _{GS} = -4.5V, R _{GS} = 6Ω		19		nS
Rise Time ²	t _r			34		
Turn-Off Delay Time ²	t _{d(off)}			216		
Fall Time ²	t _f			165		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _J = 25 °C)						
Continuous Current ³	I _S				-16	A
Forward Voltage ¹	V _{SD}	I _F = -2.5A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = -2.5A, dI _F /dt = 100A / μS		35		nS
Reverse Recovery Charge	Q _{rr}			18		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

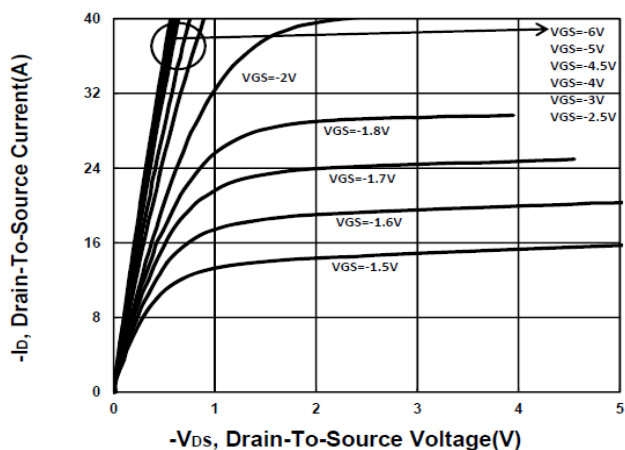
²Independent of operating temperature.

³Package limitation current is -11A.

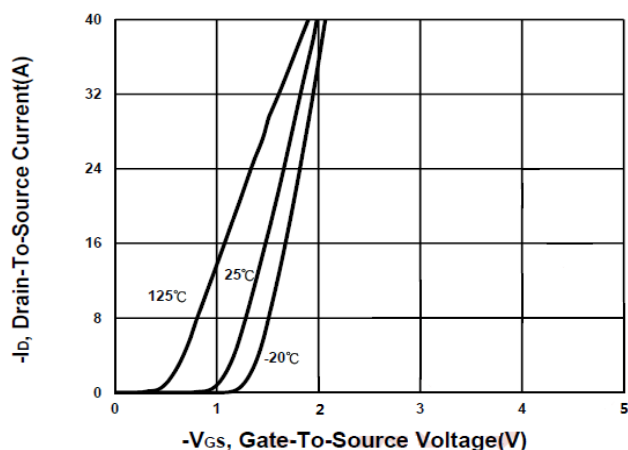
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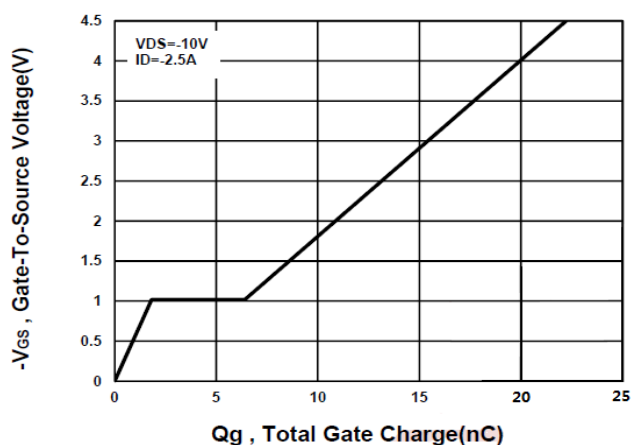
Output Characteristics



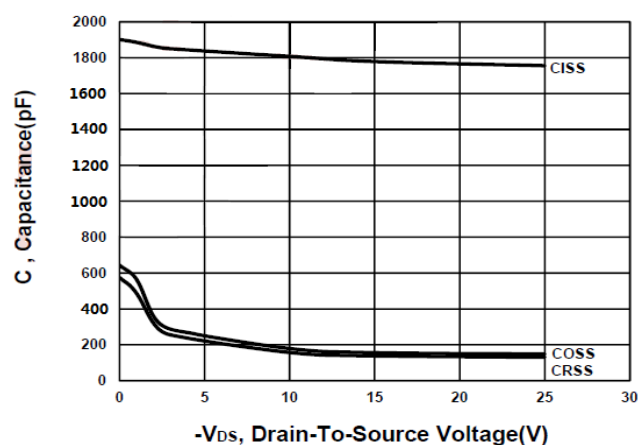
Transfer Characteristics



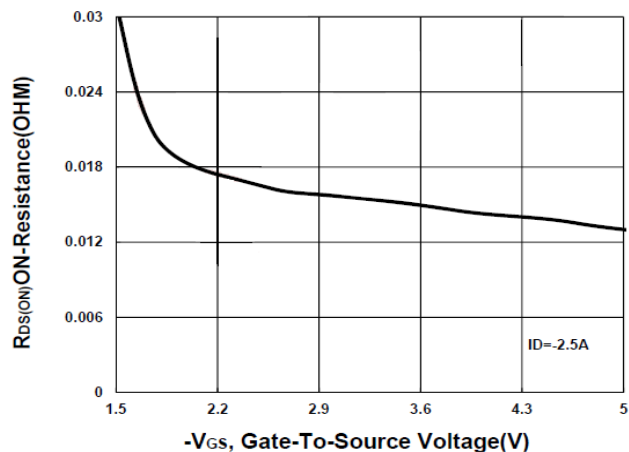
Gate charge Characteristics



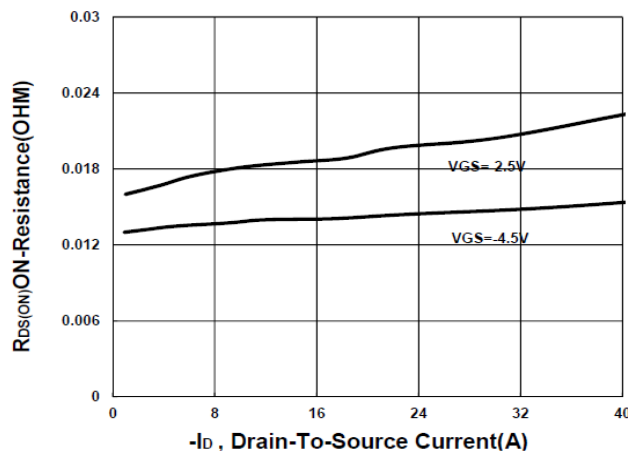
Capacitance Characteristic



On-Resistance VS Gate-To-Source



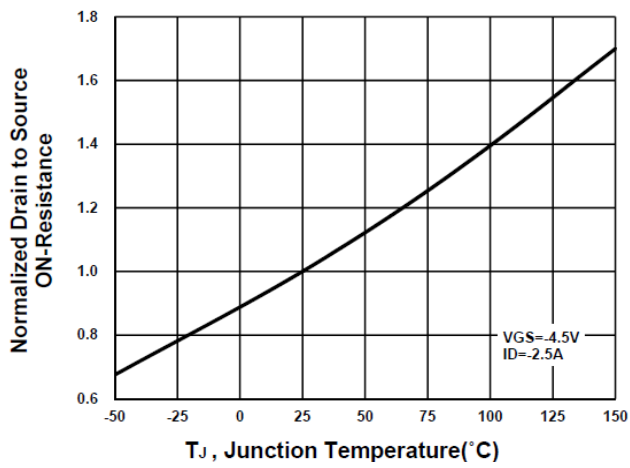
On-Resistance VS Drain Current



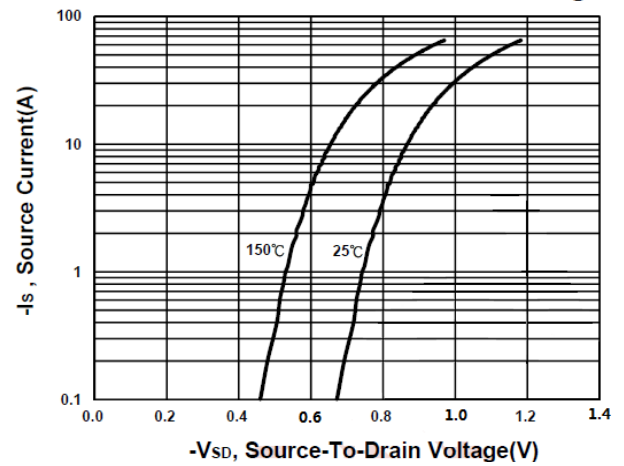
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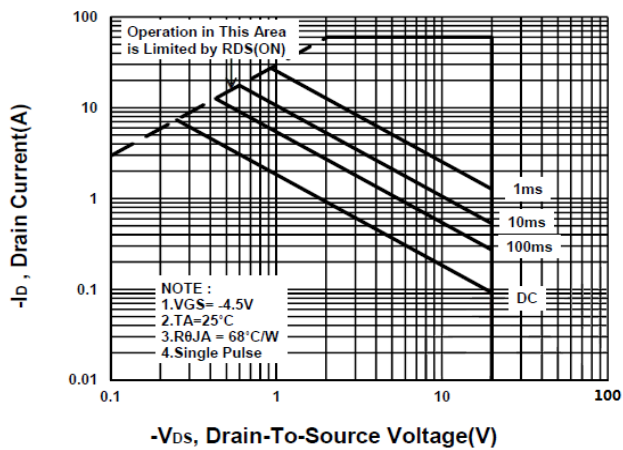
On-Resistance VS Temperature



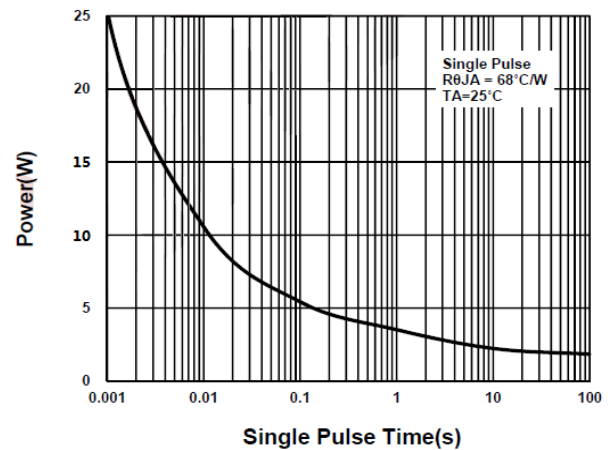
Source-Drain Diode Forward Voltage



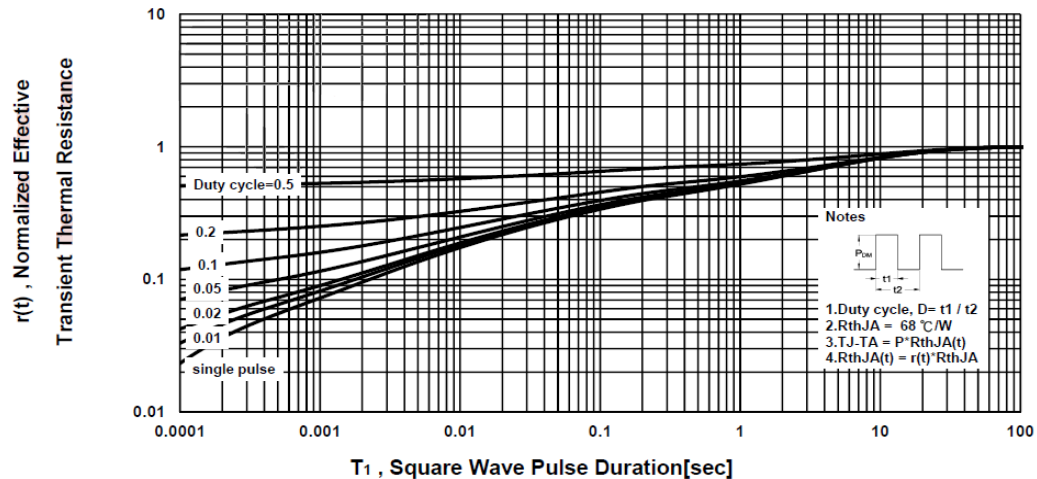
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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Package Dimension

PDFN 3x3P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	3		3.6	I	0.7		1.12
B	2.88		3.2	J	0.1		0.33
C	2.9		3.2	K	0.6		
D	1.98		2.69	L	0°	10°	12°
E	3		3.6	M	0.14		0.41
F	0		0.455	N	0.6		0.7
G	1.47		2.2	O	0.12		0.36
H	0.15		0.56	P	0		0.2

